Background ADC Calibration in Digital Domain

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***Abstract*— A 100MS/s pipelined ADC is digitally calibrated by a slow ΣΔ ADC using a least-mean-square (LMS) algorithm. Both linear and nonlinear memoryless residue gain errors of the pipeline stages are adaptively corrected. With a 411kHz sinusoidal input, the peak SNDR improves from 28dB to 59dB and the SFDR improves from 29dB to 68dB. The complete 0.13μm ADC SoC occupies a die size of 3.7mm×4.7mm, and consumes a total power of 448mW.**

I. Introduction

Recent digital CMOS technology advancement has spurred a flurry of research activities in seeking digital adaptive techniques to address the inherent problem of analog impairments in a genre of mixed-mode and RF integrated circuits. In the context of pipelined ADCs, such approaches often result in relaxed matching and gain requirements of the switched-capacitor residue gain stages [1]–[4]; and in return, power efficiency and/or conversion speed can be improved. The latest effort in this regime seems to have been focusing on various nonlinear calibration schemes, as revealed by the recently reported works in the literature [5]–[7].

The general approaches of the reported calibration techniques thus far can be categorized into mainly three types: the statistics-based approach [5], the correlation-based approach [1]–[3], and the equalization-based ones [8], [9]. The former two share a common drawback of long calibration times, and thus are not suitable for time-variant operations [10]. In this work, we present a fast adaptive digital nonlinear calibration technique that is an extension of the work reported in [9]. We show that, with the aid of a slow ΣΔ ADC, the nonlinear residue transfer function of a pipeline stage can be fully reversed in a backend digital filter, enabling the use of simple cascode inverters as the residue amplifiers in the ADC. The resulting simplicity of the analog circuits potentially leads to a much relaxed design tradeoff between the circuit speed and accuracy, one of the most difficult aspects of analog design.

II. Code Domain Filtering Approach

A detailed mathematical formulation of the proposed calibration technique is described in this section. First, we express the nonlinear transfer function of a 1.5-b/stage residue amplifier in the (digital) code domain as an FIR filter. It follows that the digital equivalence of the input analog voltage can be represented as a function of the output code from each pipeline stage and some circuit parameters related to matching, op-amp gain, and offset. We will then demonstrate that a properly designed nonlinear digital filter is sufficient to correct the analog errors using a known reference signal (obtained from the ΣΔ ADC).

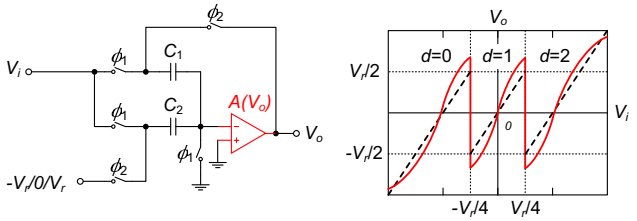

Fig. 1. Residue amplifier of a 1.5-b/stage pipelined ADC and its ideal (dashed line) and nonideal (solid line) voltage transfer function.

A. Code Domain Formulation of 1.5-b Pipeline Stage

Fig. 1 shows the residue amplifier of a typical switched-capacitor 1.5-b pipeline ADC stage and its voltage transfer curve. The residue voltage can be expressed as [9]

$$V_o = \frac{V_i(C_1+C_2)-(d-1)V_rC_2+V_{os}(C_1+C_2+C_x)}{C_1(1+\frac{C_1+C_2+C_x}{A(V_o)C_1})}, \tag{1}$$

where, V_r is the reference voltage, C_x is the summing-node parasitic capacitance, V_{os} is the lumped offset voltage, $A(V_o)$ is the signal-dependent op-amp gain, and d is the digital decision of the current stage that assumes a value of 0, 1, or 2. The term $\frac{A(V_o)C_1}{C_1+C_2+C_x}$ is the loop gain of the residue amplifier. After dividing both sides of (1) by V_r, a digital representation is obtained,

$$\begin{aligned} D_i(\frac{C_1+C_2}{C_1}) = D_o(1+\frac{C_1+C_2+C_x}{C_1}\frac{1}{A(D_o)}) \\ +(d-1)(\frac{C_2}{C_1})-D_{os}(\frac{C_1+C_2+C_x}{C_1}), \end{aligned} \tag{2}$$

where, $D_i=\frac{V_i}{V_r}$, $D_o=\frac{V_o}{V_r}$, and $D_{os}=\frac{V_{os}}{V_r}$. Equivalently, (2) can be approximated by a power series expansion [11]:

$$\begin{aligned} D_i = D_o\alpha_1 + {D_o}^2\alpha_2 + {D_o}^3\alpha_3 + {D_o}^4\alpha_4 + ... \\ +(d-1)\beta - D_{os}\gamma, \end{aligned} \tag{3}$$

where, $\alpha_k = f_k(C_1,C_2,C_x,A(D_o))$, $\beta=(\frac{C_2}{C_1+C_2})$, $\gamma=(\frac{C_1+C_2+C_x}{C_1+C_2})$. Note that the truncated version of (3) resembles

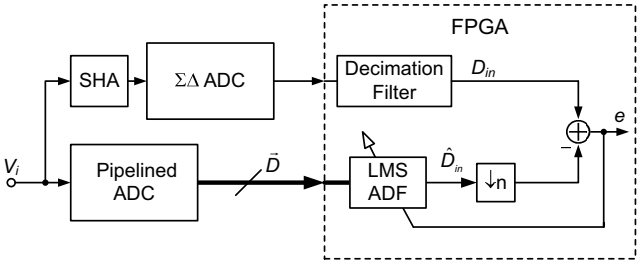

Fig. 2. Nonlinear adaptive digital calibration of pipelined ADC.

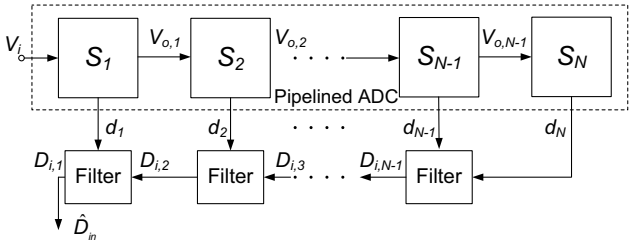

Fig. 3. Reverse pipelining of the multistage adaptive digital filter.

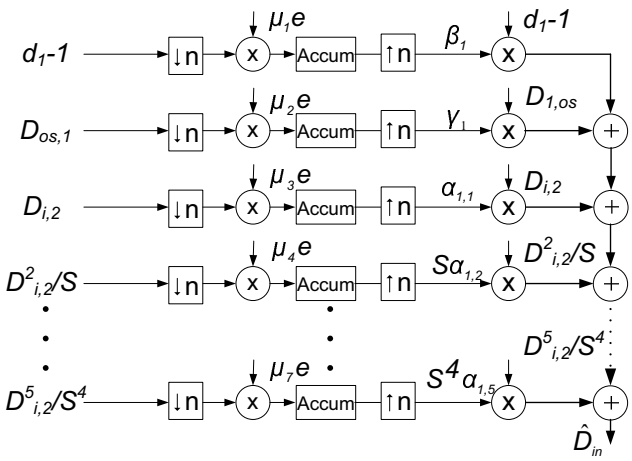

Fig. 4. Simplified coefficient update diagram for the first pipeline stage. Parameter S is a constant scaling factor.

an FIR filter with coefficients α_k, β, and γ. For an ideal pipeline stage, the values of α_1 and β are 0.5, the values of $\alpha_2 - \alpha_k$ are 0, and the value of γ is 1. In practice, these coefficients are generally unknown due to PVT (process, voltage, and temperature) variations.

B. Code Domain Multistage Formulation

After deriving the input-output (D_i-D_o) relationship of a single-stage residue amplifier, we now extend this treatment to a complete multistage pipelined ADC. Using (3) and again assuming a 1.5-b/stage architecture, we arrive at the following expressions for D_i's from all stages [9]:

$$\begin{aligned} D_{i,1} =& D_{o,1}\alpha_{1,1} + D_{o,1}^2\alpha_{1,2} + D_{o,1}^3\alpha_{1,3} + ... \\ &+ (d_1 - 1)\beta_1 - D_{os,1}\gamma_1 \\ D_{i,2} =& D_{o,2}\alpha_{2,1} + D_{o,2}^2\alpha_{2,2} + D_{o,2}^3\alpha_{2,3} + ... \\ &+ (d_2 - 1)\beta_2 - D_{os,2}\gamma_2 \\ D_{i,3} =& D_{o,3}\alpha_{3,1} + D_{o,3}^2\alpha_{3,2} + D_{o,3}^3\alpha_{3,3} + ... \\ &+ (d_3 - 1)\beta_3 - D_{os,3}\gamma_3 \\ &\vdots \\ D_{i,N} =& D_{o,N}\alpha_{N,1} + D_{o,N}^3\alpha_{N,2} + D_{o,N}^3\alpha_{N,3} \\ & (d_N - 1)\beta_N - D_{os,N}\gamma_N. \end{aligned} \tag{4}$$

Since $D_{o,N}$ = $D_{i,N+1}$, a digital representation of the input signal (D_{in}) can be obtained from the above equations (recursively):

$$\begin{aligned} D_{in} = D_{i,1} =& D_{i,2}\alpha_{1,1} + D_{i,2}^2\alpha_{1,2} + D_{i,2}^3\alpha_{1,3} + ... \\ &+ (d_1 - 1)\beta_1 - D_{os,1}\gamma_1. \end{aligned} \tag{5}$$

Eq. (5) formulates a nonlinear FIR filter in the code domain. In order to obtain D_{in}, we need to find the coefficients β_i, γ_i, and $\alpha_{i,k}$. Note that the treatment in (5) can be generalized to an x.5-b/stage pipeline architecture.

C. Calibration Algorithm and System Architecture

As the filter tap values of (5) are unknown a priori, adaptive learning can be applied to obtain them on the fly. This leads to a background calibration approach using a gradient-descent algorithm. As shown in Fig. 2, the output digital codes ($\vec{D}$) from all pipeline stages of an inaccurate, high-speed pipelined ADC is decimated and applied to an LMS adaptive digital filter (ADF); while a slow-and-accurate ΣΔ converter is used to obtain an accurate version of D_{in} to compare with those procured from the pipeline. An LMS algorithm is used to update the filter coefficients at the sample rate of the ΣΔ converter. The recursive formulation of the adaptive digital filter as explained before is implemented as a reverse pipeline (Fig. 3). The detailed coefficient adaptation scheme is shown in Fig. 4 for the first stage. Note that a sampling clock skew may exist at the front-end between the SHA of the ΣΔ ADC and the pipelined ADC. As long as the resulting sampling error exhibits a symmetrical probability distribution in the long term, the effect is removed by the accumulator of the LMS loop.

III. CMOS Prototype Design

In the prototype, the reference ADC consists of a SHA followed by a 2-1 MASH ΣΔ ADC [12]. A traditional flip-over switched-capacitor S/H architecture with a two-stage amplifier is used. As the calibration performance tends to be limited by the linearity of the reference path instead of noise, extra attention was paid in the SHA and ΣΔ design to ensure an almost 14-bit accuracy. The clock frequencies of the SHA and the ΣΔ ADC are $1/2^{14}$ and $1/2^4$ of that of the pipelined ADC, respectively. The sample rate of the SHA determines the update frequency of the ADF and its convergence time.

The pipelined ADC uses a SHA-less 1.5-b front-end stage, followed by 2.5-b stages from stage 2 to 6, and ending in a 3-

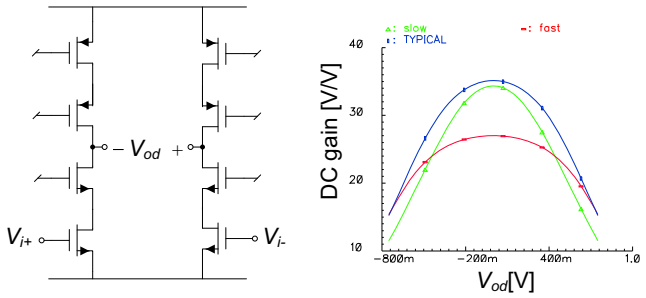

Fig. 5. Second-stage residue amplifier and its gain curves.

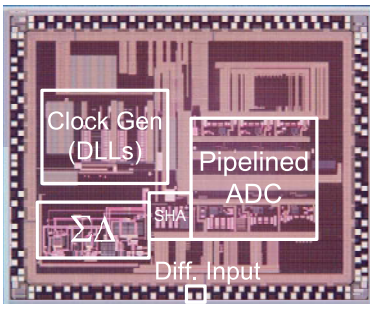

Fig. 6. Die photo of the prototype ADC (3.7mm×4.7mm).

b flash stage. Altogether 14 raw bits are collected. Simple cascode pseudo-differential inverters (Fig. 5) are used as residue amplifiers to enable high conversion speed and power efficiency. A similar common-mode feedback/feed-forward circuit as in [13] is devised to set the common-mode levels along the pipeline. The (simulated) open-loop gain curves of the 2nd-stage amplifier are shown in Fig. 5. Relative sizes of the amplifiers are 7:4:1 in stage 1, 2, and 3, respectively. The sampling capacitors of the pipelined ADC and the SHA are 2pF and 0.5pF, respectively. To ensure good matching between the reference and the main signal paths, a replica switched-capacitor S/H structure was used by the SHA to mimic that of the pipeline. This also minimizes the systematic sampling clock skew existent in between the paths. They further share the same analog supply.

Clock generation/distribution of the ADC SoC is facilitated by two DLLs producing synchronized multi-phase clocks for the SHA, the ΣΔ and the pipelined ADCs. The analog portion of the prototype was fabricated in a triple-well 0.13μm digital CMOS process without analog options. Capacitors are implemented using fingered metal capacitor (MOM). A micrograph of the 3.7mm×4.7mm chip is shown in Fig. 6. The LMS ADF is implemented in FPGA.

IV. Measured Results

In experiments, the LMS ADF converges within a few seconds after power-up. Nonlinear residue gain errors up to the 5th-order in stage 1 and 2 are calibrated, while only linear gain errors are filtered for the remaining stages. Fig. 7 shows the power spectral density (PSD) of the ADC before (a) and after (b) calibration. The input frequency is 411kHz and the sample rate of the pipelined ADC is 100.12MS/s. Before calibration, the SFDR is limited by HD_3 at 29.8dB; after calibration, the HD_3 drops to -72.2dB, and the SFDR is limited to 67.8dB by a spur at $f_s/2$. The SNDR improves from 28.1dB to 59.4dB before and after calibration, respectively. The results of a similar experiment performed on a 49MHz input are plotted in Fig. 8, wherein the SNDR improves from 29.4dB to 54.8dB and the SFDR improves from 31.7dB to 63.4dB. Fig. 9 plots the measured SNDR vs. the sampling frequency with a 10MHz input. Fig. 10 shows the measured SNDR and SFDR vs. the input frequency. Table I summarizes the measured performance of the prototype.

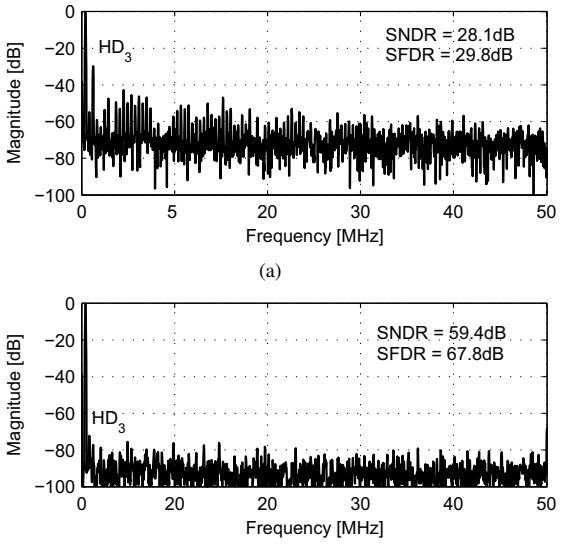

Fig. 7. Measured ADC spectra for f_s=100MHz, V_{in}=0dBFS, f_{in}=411kHz: (a) before calibration, (b) after calibration.

TABLE I
Experimental Results

	Before cal.	After cal.
Process	0.13μm digital CMOS	
Supplies: Analog/Digital	1.35V/1.2V	
Full-scale Input(pk-pk)	±0.5V	
Sampling Rate	100MHz	
Chip Area	3.7mm×4.7mm	
ΣΔ Power	10mW	
SHA + Pip. ADC Power	332mW	
Clock Gen. Power (DLLs+Buffer)	106mW	
Total Power	448mW	
SNDR(411kHz)	28.1dB	59.4dB
SNDR(49MHz)	29.4dB	54.8dB
SFDR(411kHz)	29.8dB	67.8dB
SFDR(49MHz)	31.7dB	63.4dB
HD_3(411kHz)	-29.8dB	-72.2dB
HD_3(49MHz)	-31.7dB	-68.0dB

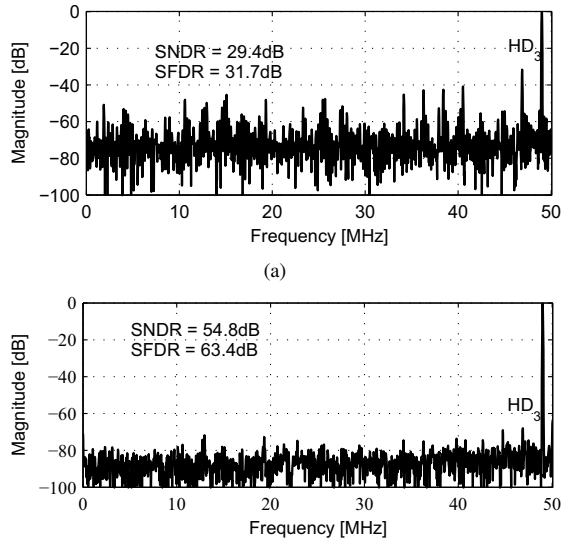

Fig. 8. Measured ADC spectra for f_s=100MHz, V_{in}=0dBFS, f_{in}=49MHz: (a) before calibration, (b) after calibration.

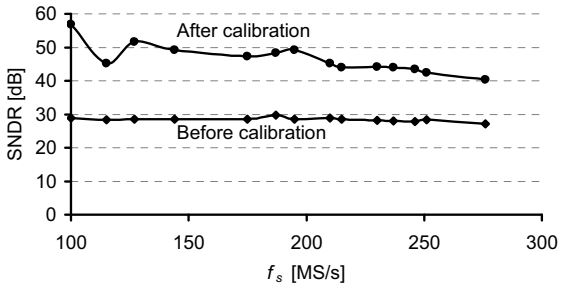

Fig. 9. Measured SNDR versus f_s with 10MHz input.

V. Conclusion

A fully digital, adaptive, background calibration algorithm, capable of correcting linear as well as nonlinear residue gain errors in pipelined ADCs, has been reported. The technique allows the use of power-efficient, broadband, and low-gain cascode inverters as precision residue amplifiers. Experimental results show that the calibration improves the SNDR and SFDR of the prototype ADC by >25dB across the Nyquist band at a sample rate of 100MS/s.

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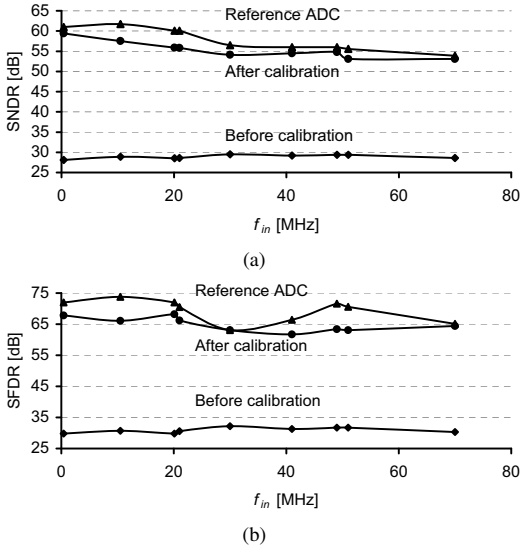

Fig. 10. Measured performance at 100MS/s: (a) SNDR, (b) SFDR.

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