The RISC-V Instruction Set

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www.riscv.org

Why a new ISA?

- Provide a realistic but simple ISA that captures important details of commercial general-purpose ISA designs and is suitable for hardware implementation.
- Provide a completely open ISA around which a community can grow.
- Avoid “over-architecting” for a particular microarchitectural style or implementation technology, but which allows efficient implementation in any of these.

Additional RISC-V Goals

- Support 64-bit address spaces for desktops and servers.
- Support 32-bit address spaces for small, low-power implementations.
- Implement the revised 2008 IEEE 754 floating-point standard.
- Easy to add ISA extensions and specialized variants.
- Fully virtualizable to ease hypervisor development.
- Support highly-parallel multicore or manycore implementations.
- Simple to subset for educational purposes and to reduce complexity of bringing up new implementations.

RISC-V Software Ecosystem

- GCC 4.6.1 with newlib and glibc C libraries
- “Proxy Kernel” to support POSIX calls by forwarding to a Linux host machine
- Akaros cloud research operating system
- Linux operating system
- python 3
- LLVM support in the near future

RISC-V Base User-Level ISA

- 45 instructions in the RV32I base ISA
- Additional 12 instructions for the RV64I base ISA
- Load-store architecture
- Multiprocessor synchronization via fetch-and-op and load-reserved/store-conditional
- Efficient position-independent code support
- No architecturally-visible delay slots

45nm RISC-V Processor

Fabricated in IBM 45nm SOI
Runs at > 1GHz

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Rocket: A single-issue in-order RISC-V Implementation

- Simple 6-stage fixed-point pipeline
- Full supervisor support
- Comparable to a Cortex A5; 1.6 DMIPS/MHz (better than A5)
- 64-bit fixed-point datapath, double-precision FPU

A RISC-V Supervisor ISA

- User and supervisor ISAs defined separately to facilitate different supervisor implementations (e.g. for µcontrollers)
- Current RV64 supervisor ISA:
  - 3-level page table; page sizes 8KB/8MB/8GB
  - Interprocessor interrupts
  - Timers
  - Tethered to host machine for disk, frame buffer

DEMO

- Rocket core mapped to a ZedBoard running Linux

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