The Maven Vector-Thread Architecture

1 Motivation
Future manycore processors will be energy-constrained, and thus the primary metric for evaluating these architectures will be their energy-efficiency. In this work, we investigate new architectural and microarchitectural mechanisms which enable a wider array of applications to be mapped to energy-efficient vector units.

2 Architectural Patterns
Three different architectural patterns (excluding subword-SIMD and SIMT) were evaluated in terms of their performance, energy efficiency and area. Maven is a new vector-thread architecture, which is based on a vector-SIMD architecture, adds minimal hardware to support irregular DLP well, and is considerably simpler to implement than previous vector-thread designs.

3 Maven Programming Methodology

4 Maven Tile Microarchitecture
We focus on comparing the various architectural design patterns with respect to a single data-parallel tile. Example tiles are a MIMD tile, a vector tile with four single-lane cores, or one four-lane core. To manage complexity of many design points, we developed a library of parameterized synthesizable RTL components.

5 Evaluation Framework
We first compare tile configurations based on their cycle time and area before exploring the impact of various microarchitectural optimizations. We then compare implementation efficiency and performance of the Maven VT pattern against the MIMD, and vector-SIMD patterns for the six application kernel.

6 Evaluation Results

7 Conclusions
1. The Maven vector-thread architecture is more area and energy efficient than MIMD architectures on regular DLP and (surprisingly) on irregular DLP
2. The Maven vector-thread architecture is a promising alternative to traditional vector-SIMD architectures, providing greater efficiency and easier programmability
3. Using real RTL implementations and a standard ASIC toolset is necessary to compare energy-optimized future architectures.

For more details, see our ISCA '11 paper below or use the QR code on the right with a barcode reader.

“Exploring the Tradeoffs between Programmability and Efficiency in Data-Parallel Accelerators”

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