UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE105 Lab Experiments

Prelab 4: Single Stage BJT Amplifiers: Common Emitter

Solutions

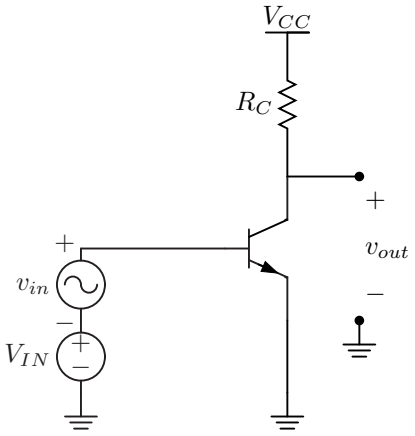


Figure 1: Common emitter amplifier

1. Let's analyze this common emitter amplifier! See Figure 1. Let $V_{CC} = 5$ V, $V_T = 26$ mV, $I_S = 26.03$ fA, $V_A = 90.7$ V, $R_C = 1$ kΩ, and $\beta = 270$.

   (a) For this transistor draw a graph (found on the next page) of I_C vs. V_{CE} for $V_{BE} = 600$ mV, 620 mV, 640 mV, 660 mV, 680 mV, and 700 mV. Take care drawing this graph as it will be used in answering some of the following questions. Assume the boundary between deep saturation and forward active occurs at $V_{CE} = 400$ mV. You can use a piecewise linear model for this graph.

   (b) On this graph, draw the load line for R_C in this circuit.

   (c) Using the intersection points, draw a graph (also found on the next page) of V_{OUT} vs. V_{IN}. What is this graph useful for?

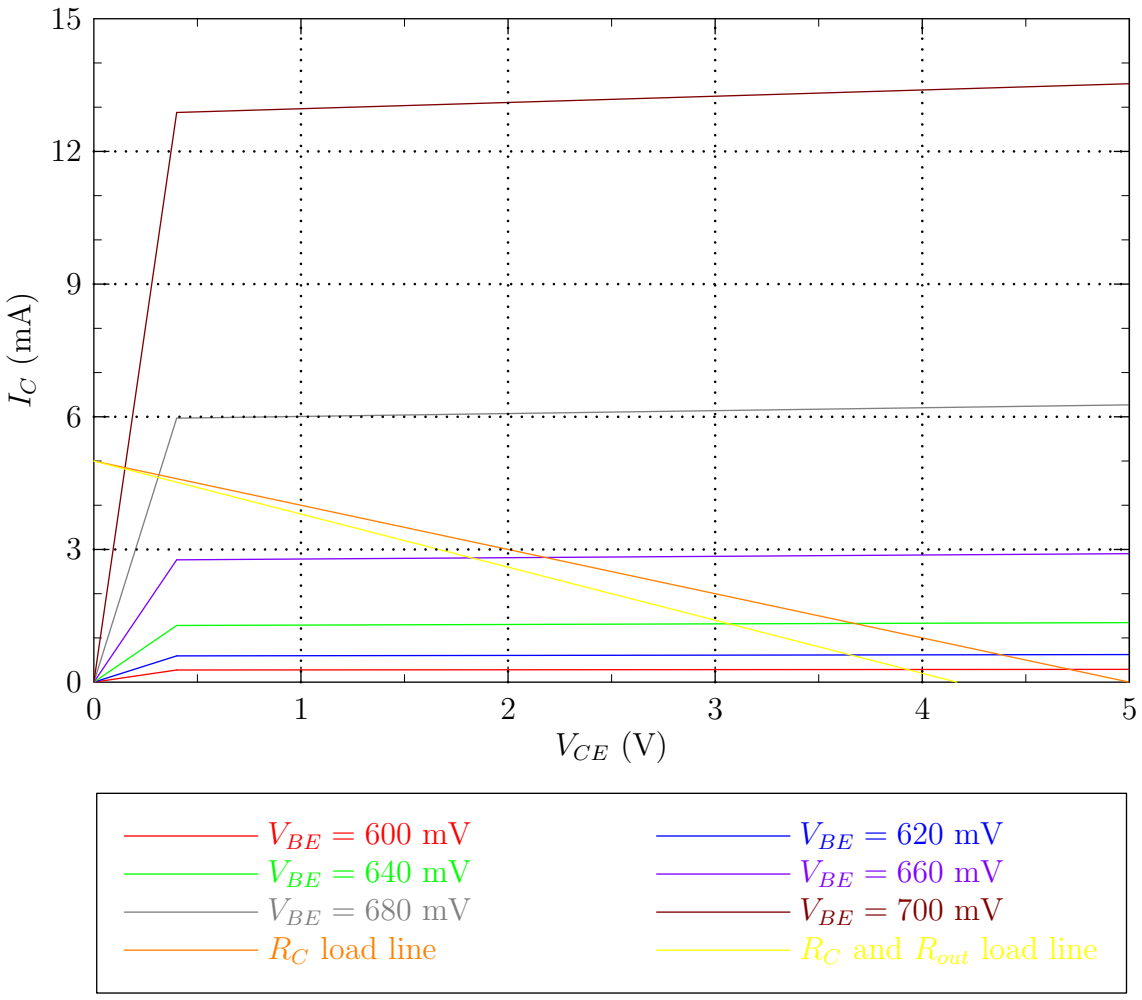
   This graph is useful for determining the maximum gain bias point.

   (d) What is the gain for $V_{IN} = 650$ mV ? What is the region of operation of the transistor?

$$A_v = \frac{2.180 - 3.672}{0.020} = \boxed{-74.6}$$

The BJT is operating in the **forward active** region.

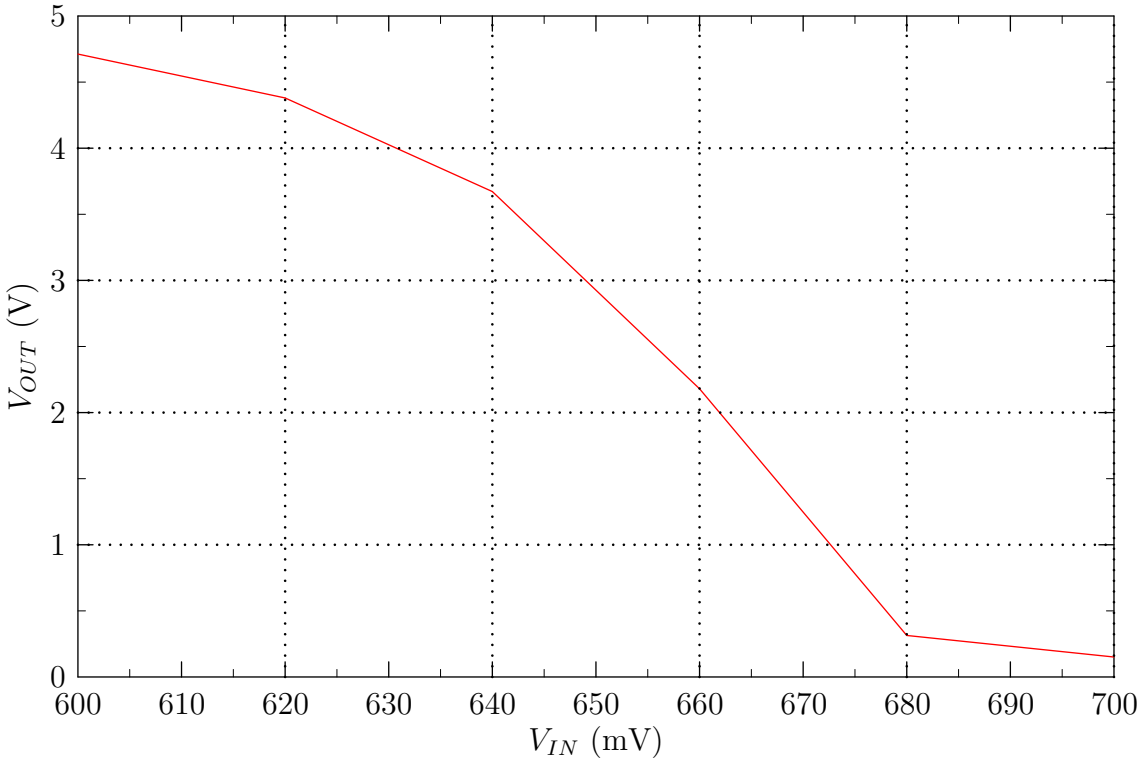
2. Now that we've analyzed the large-signal properties of the amplifier, let's analyze some of its small-signal properties. Assume $V_{IN} = 650$ mV for the rest of the prelab.

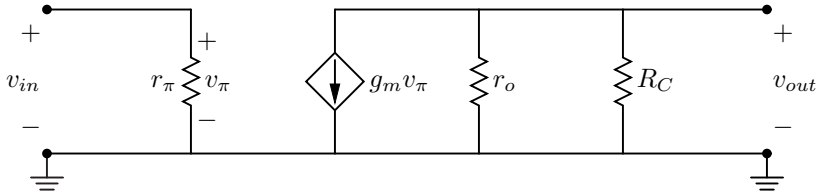


(a) Draw the small signal model of the amplifier (answer space provided on next page).

(b) Calculate the following (be sure to include the Early effect):

- Output voltage V_{OUT}
- Collector current I_C
- Transconductance g_m
- Output impedance R_{out}
- Input impedance R_{in}
- Gain A_v. Does this gain match your answer to question 1(d)?





$$V_{OUT} = V_{CC} - R_C I_s \left(e^{V_{BE}/V_T} - 1\right)\left(1 + \frac{V_{OUT}}{V_A}\right)$$

$$V_{OUT} = \boxed{3.06 \text{ V}}$$

$$I_C = I_s \left(e^{V_{BE}/V_T} - 1\right)\left(1 + \frac{V_{OUT}}{V_A}\right)$$

$$I_C = \boxed{1.938 \text{ mA}}$$

$$g_m = \frac{I_C}{V_T} = \boxed{0.0745 \text{ mS}}$$

$$r_o = \frac{V_A}{I_c} = 46.812 \text{ k}\Omega$$

$$R_{out} = r_o \parallel R_C = \boxed{979\ \Omega}$$

$$R_{in} = r_\pi = \frac{\beta}{g_m} = \boxed{3.623 \text{ k}\Omega}$$

$$A_v = -g_m(r_o \parallel R_C) = \boxed{-73}$$

The gain is nearly identical to the value computed in 1(d).

(c) If we change the bias point, which of the above properties change?

They all change!

3. Let's explore what happens when we change the bias point by adding a load resistor.

(a) Add a load of 5 kΩ to the output of the circuit. Intuitively, how do you think this will affect the gain and why?

Intuitively we can guess that adding a load resistor will decrease the gain. We know a load resistor will have two effects: in large signal, it will change the bias point and in small signal, it will lower the output impedance. We know that lowering the output impedance will decrease the gain, so we only have to consider the effect on the bias point. If we assume $r_o >> R_C$ and $r_o >> 5\,\text{k}\Omega$, then the change in I_C will be minimal, meaning g_m and r_o will remain relatively unchanged. Thus, the change in R_{out} will dominate and cause the gain to decrease.

(b) Draw the new load line on the graph you made for question 1(a) (be sure to label which load line goes with which question).

(c) If we keep the same bias point (i.e., the same V_{BE} value), is the transistor still in forward active mode?

Yes, we can see that from the graph.

(d) What happens to the gain? How about the output voltage swing? *Note: The output voltage swing is the maximum and minimum values of V_{OUT} for which all transistors stay in forward active.*

The gain decreases, and the output voltage swing decreases as well. This can be seen from the graph.

(e) What is the load resistance value for which the amplifier's BJT begins to transition between forward active mode and deep saturation (i.e., where $V_{CE} = 400\,\text{mV}$)?

Looking at the graph, we can see that this event will occur when the load resistance becomes small enough so that the load line causes V_{OUT} to become less than 400 mV. The load line is given by the following:

$$\begin{aligned} I_C &= \frac{V_{CC} - V_{CE}}{R_C} - \frac{V_{CE}}{R_L} \\ &= \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} - \frac{V_{CE}}{R_L} \\ &= \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C \parallel R_L} \end{aligned}$$

For $V_{IN} = 650\,\text{mV}$ and $V_{OUT} = 400\,\text{mV}$, $I_C = I_S\left(e^{0.65/0.026} - 1\right)(1 + 0.4/90.7) = 1.883\,\text{mA}$. Thus, we need to find R_L such that $I_C = 1.883\,\text{mA}$ and $V_{CE} = 400\,\text{mV}$ satisfies the above equation.

$$\begin{aligned} 1.883\,\text{mA} &= \frac{V_{CC}}{R_C} - \frac{0.4}{R_C \parallel R_L} \\ R_L &= \boxed{147\,\Omega} \end{aligned}$$