Nano-Electro-Mechanical Memory Technology for Future Compact and Ultra-Low-Power Integrated Systems

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A Vision of the Future

Infrastructural core

Sensory swarm (trillions of devices)

Mobile access

More than Moore's Law

- **<u>Energy efficiency</u> and functional capabilities beyond the limits of CMOS devices will be needed for electronics to expand into new applications.**

Mobile Internet Devices:
- high speed (>2 GHz)
- low operating voltage
- low standby power

Micro/Nano Electronics

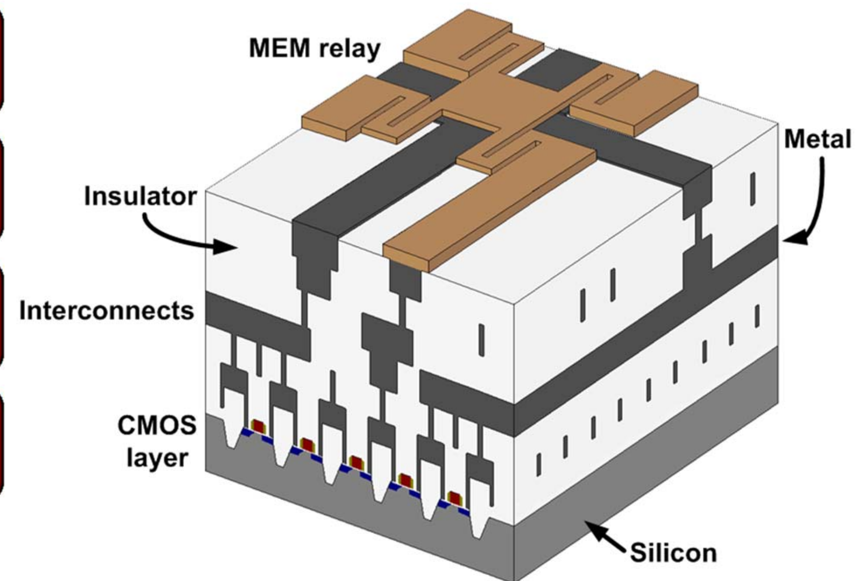
RF

MEMS

Photonics

Sensors

Monolithic integration can provide for compact, high-performance systems



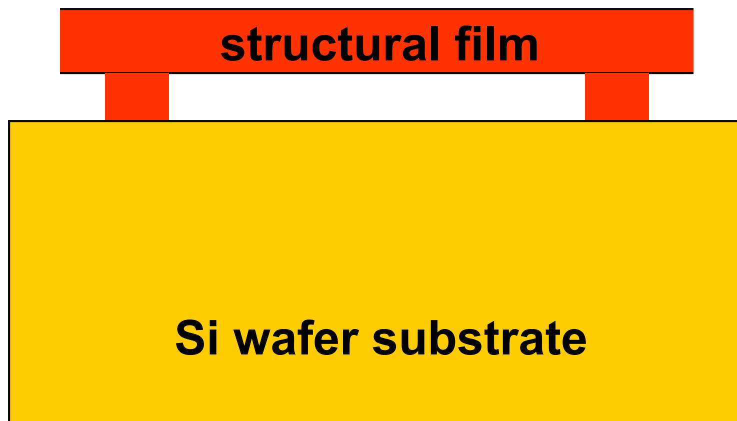
Outline

- **Introduction**
  - MEMS technology
  - Non-volatile memory (NVM) technology
- **MEMs-based NVM technologies**
- **Conclusion**

MEMS Technology

Surface Micromachining

(cross-sectional view)



- **Mechanical structures can be made using conventional microfabrication techniques**
- **Structures are freed by selective removal of sacrificial layer(s)**

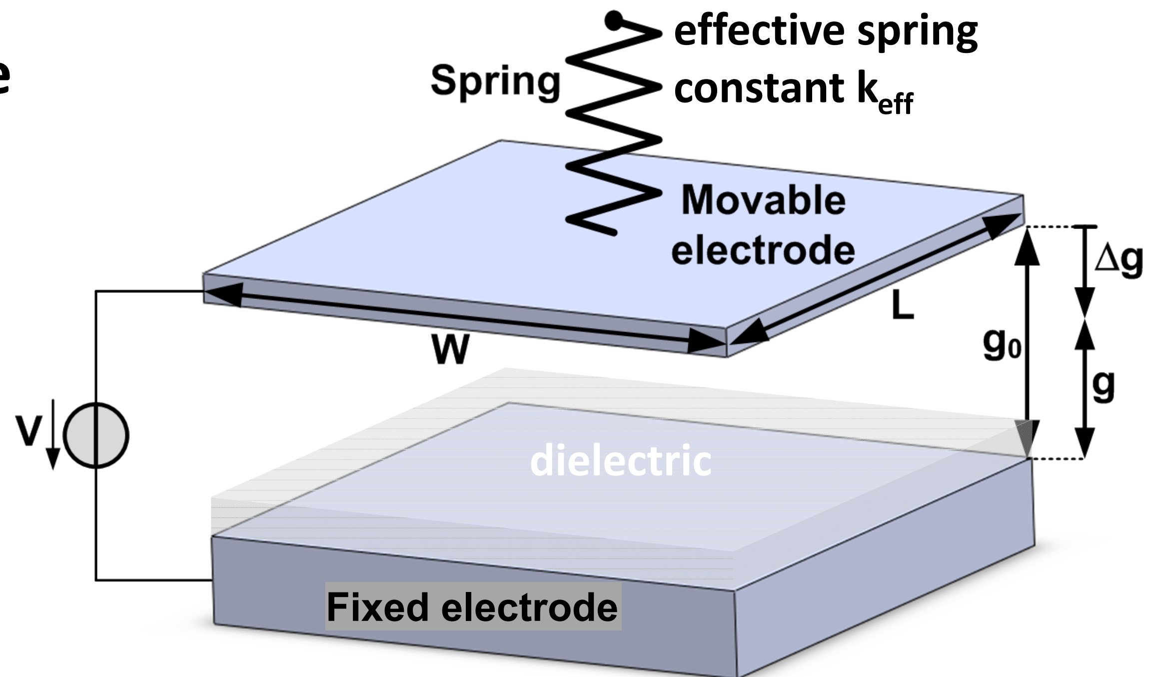
Electrostatic Gap-Closing Actuator

Spring restoring force

$F_{spring} = k_{eff}\Delta g$

Electrostatic force

$$F_{elec} = -\frac{\varepsilon_0 WLV^2}{2g^2}$$



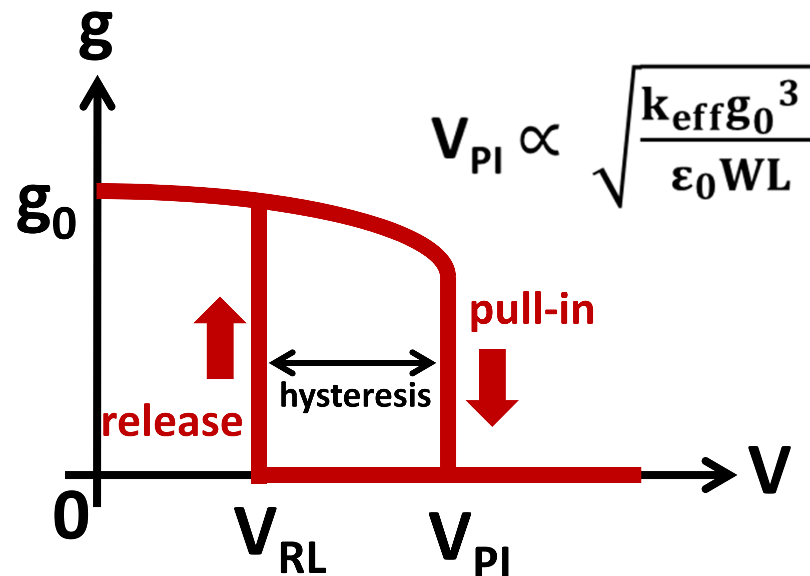
- F_{spring} increases linearly with displacement Δg, whereas F_{elec} increases super-linearly with Δg.

→ As the applied voltage difference (V) is increased beyond a critical "pull-in voltage" (V_{PI}), the beam snaps down.

Hysteretic Switching Behavior

- When the beam is pulled in, F_{elec} is larger than F_{spring}.

→ V must be reduced below the "release voltage" ($V_{RL} < V_{PI}$) to release the beam.

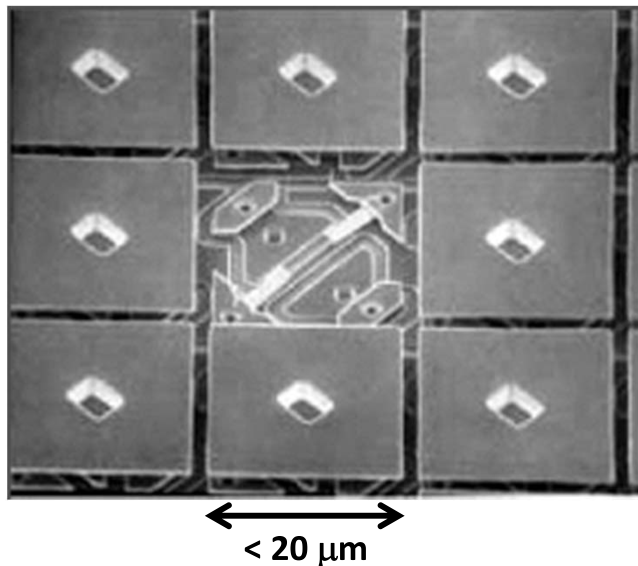


DMD^{TM} Projection Display Chip

Texas Instruments Inc.

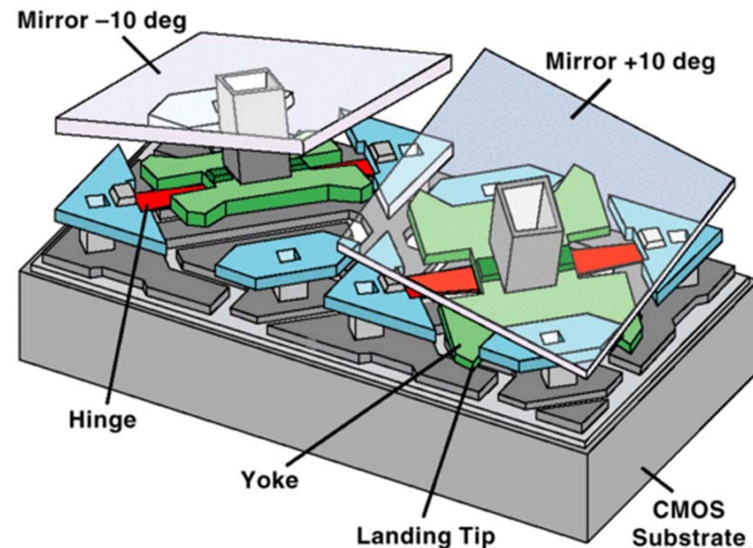
- **Electrostatically actuated mirrors are made using metal structural layers (Al alloys)**
  - sacrificial material is photoresist

SEM image of pixel array



< 20 μm

Schematic of 2 pixels



Each mirror corresponds to a single pixel, programmed by an underlying memory cell to deflect light either into a projection lens or a light absorber.

Non-Volatile Memory Technologies

ITRS (Table ERD3), 2011 Edition

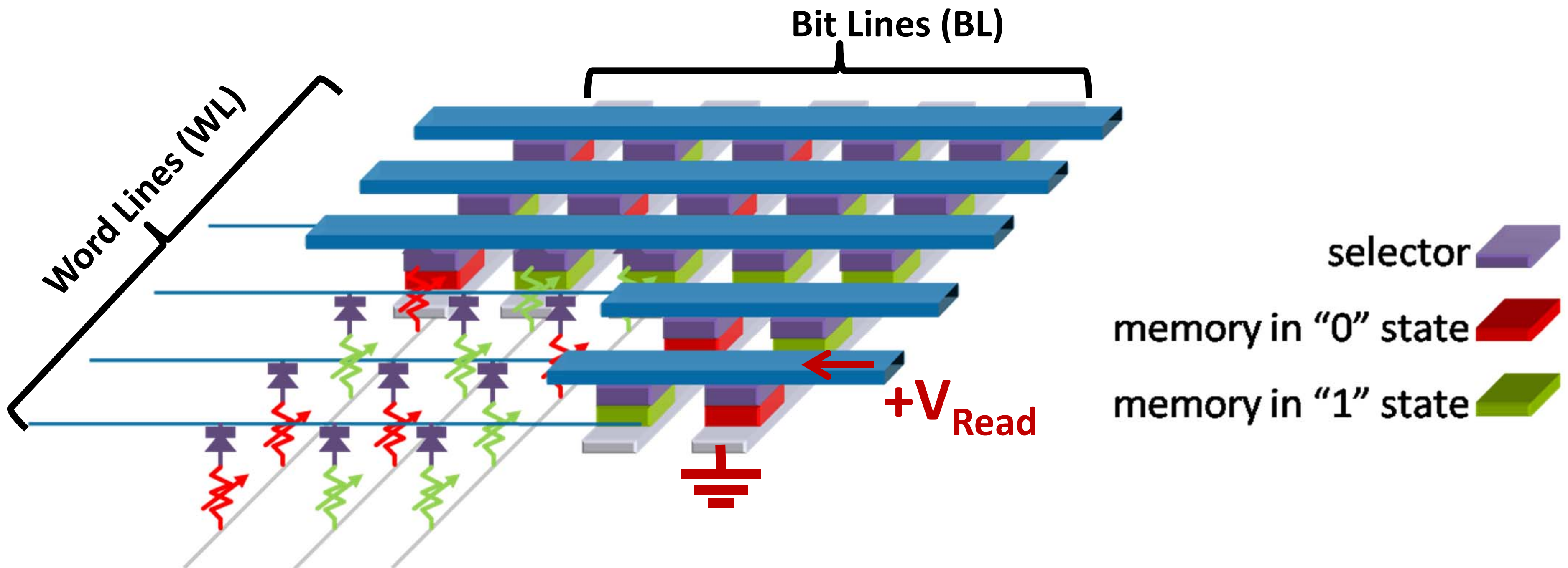
		Baseline Technologies		Prototypical technologies		
		Flash				
		NOR Embedded	NAND Stand-alone	FeRAM	STT-MRAM	PCM
Storage Mechanism		Charge trapped in floating gate or in gate insulator		Remnant polarization on a ferroelectric capacitor	Magnetization of ferromagnetic layer	Reversibly changing amorphous and crystalline phases
Cell Elements		1T		1T1C	1(2)T1R	1T(D)1R
Feature size F, nm	**2011**	90	22	180	65	45
	2024	25	8	65	16	8
Cell Area	**2011**	10 F^2	4 F^2	22F^2	20F^2	4F^2
	2024	10 F^2	4 F^2	12F^2	8F^2	4F^2
Read Time	**2011**	15 ns	0.1ms	40 ns	35 ns	12 ns
	2024	8 ns	0.1ms	<20 ns	<10 ns	< 10 ns
W/E Time	**2011**	1μs/10ms	1/0.1 ms	65 ns	35 ns	100 ns
	2024	1μs/10ms	1/0.1 ms	<10 ns	<1 ns	<50 ns
Retention Time	**2011**	10 y	10 y	10 y	>10 y	>10 y
	2024	10 y	10 y	10 y	>10 y	>10 y
Write Cycles	**2011**	1E5	1E4	1E14	>1E12	1E9
	2024	1E5	5E3	>1E15	>1E15	1E9
Write Operating Voltage (V)	**2011**	10	15	1.3-3.3	1.8	3
	2024	9	15	0.7–1.5	<1	<3
Read Operating Voltage (V)	**2011**	1.8	1.8	1.3–3.3	1.8	1.2
	2024	1	1	0.7–1.5	<1	<1
Write Energy (J/bit)	**2011**	1E-10	>2E-16	3E-14	2.5E-12	6E-12
	2024	1E-11	>2E-17	7E-15	1.5E-13	~1E-15

In contrast to logic switches, NVM devices can have:

- **Long write/erase times (>1 us)**
- **Modest endurance (< 10^6 cycles)**
- **Large operating voltages (>1 V)**

Cross-Point Array Architecture

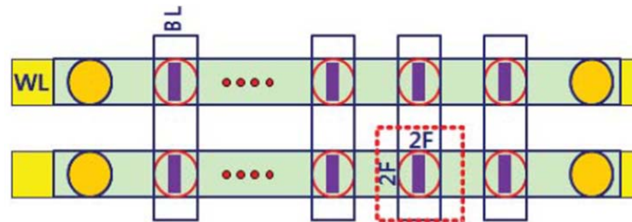
- **Most compact architecture ($4F^2$ cell size)**
- **Requires selector device at each cross-point to reduce "sneak" leakage current during a read operation**
  - *e.g.* 2-terminal diode



http://www.smartplanet.com/blog/thinking-tech/what-might-replace-flash-memory/943

20 nm Phase Change Memory

Schematic Plan View of Array



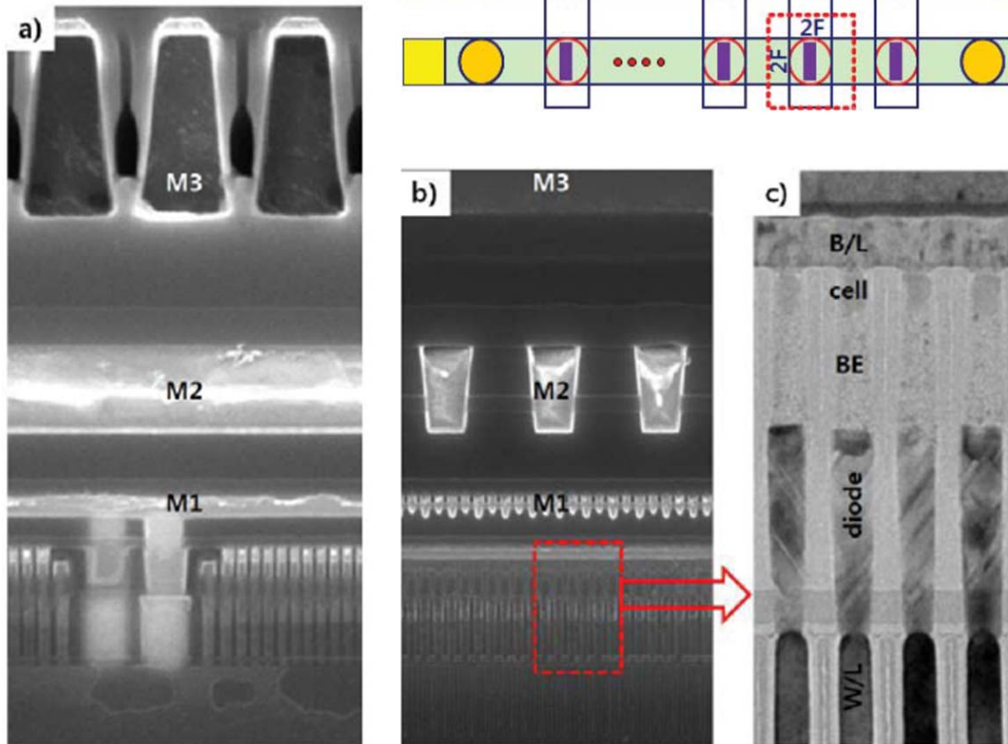
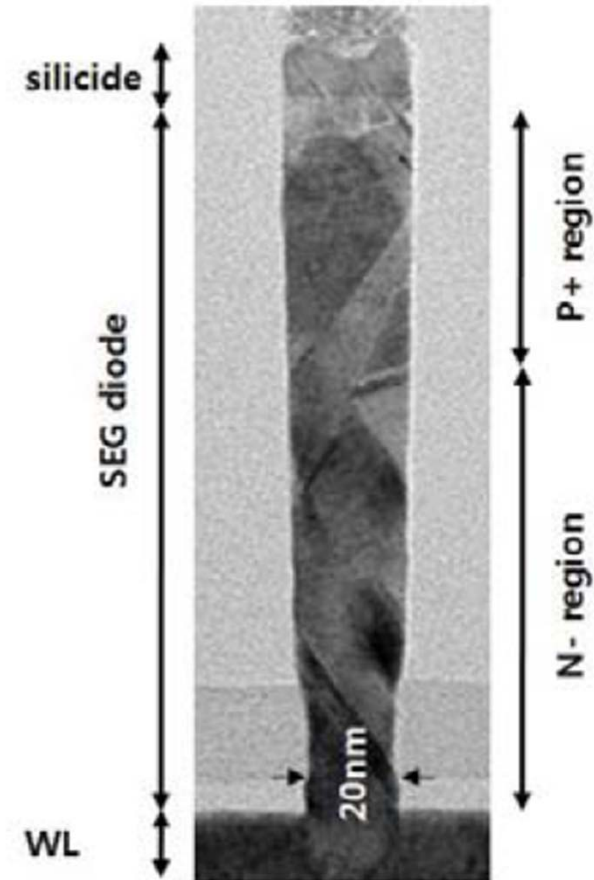


Fig. 12 Cross sectional SEM images along (a) BL direction and (b) WL direction, respectively. (c) TEM image of cell module along BL direction.

TEM Image of Diode



M. J. Kang *et al*. (Samsung Electronics), *IEDM* 2011

Outline

- Introduction
- **MEMs-based memory technologies**
  - Early designs
  - Recent design for cross-point array architecture
- Conclusion

First MEMS NVM Cell

B. Halg, *IEEE Trans. Electron Devices*, Vol. 37, pp. 2230-2236, 1990

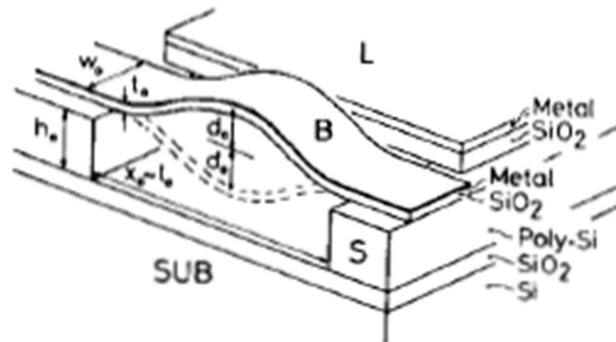


Fig. 1. Schematic drawing of a micro-electro-mechanical nonvolatile memory cell based on a bistable bridge (*B*) on a spacer (*S*) on the substrate (*SUB*) with lateral electrodes (*L*). The materials used are indicated, and the symbols for the dimensions are defined.

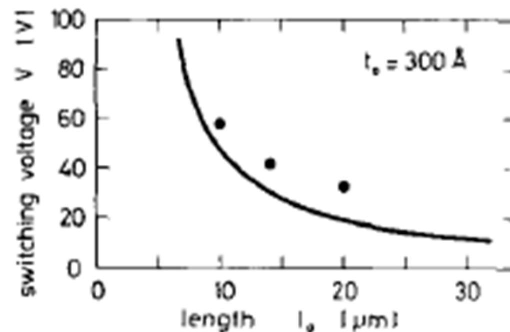


Fig. 6. Experimentally observed and calculated switching voltages *V* as a function of the length l_0 of a 300-Å-thick bridge.

- **Bistable buckled beam**
  - Switched with electrostatic force
  - Immune to radiation, shock
- **Too large (>100um^2) for reasonable storage capacities…**

Nanomech^{TM} NVM Technology

M. A. Beunder *et al*. (Cavendish Kinetics Ltd.), *Non-Volatile Memory Technology Symposium*, 2005

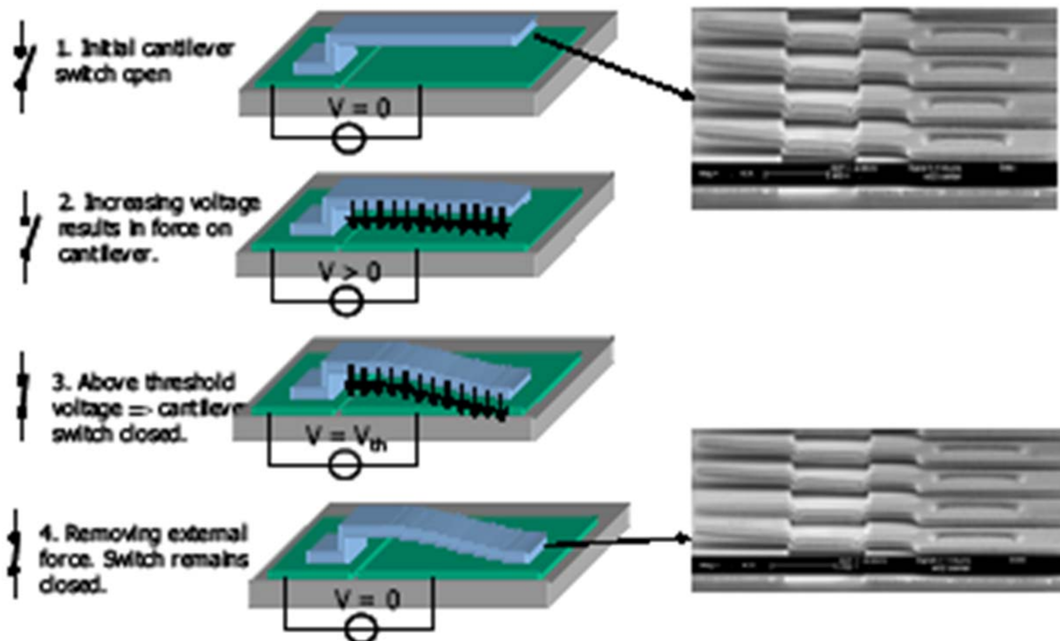


Fig. 2. Nanomech cantilever programming event

Characteristics	Value	Value – Example: 0.18µm CMOS
Bit Cell Size (inc. programming transistor)	18F^2	2.2 µm
Programming Voltage	native	1.8 V
Write time	1-5 µs	3 µs
Write current	1-5 mA	2 mA
Read Voltage	100mV	100 mV
Leakage current	0 mA	0 mA
Endurance	∞	∞

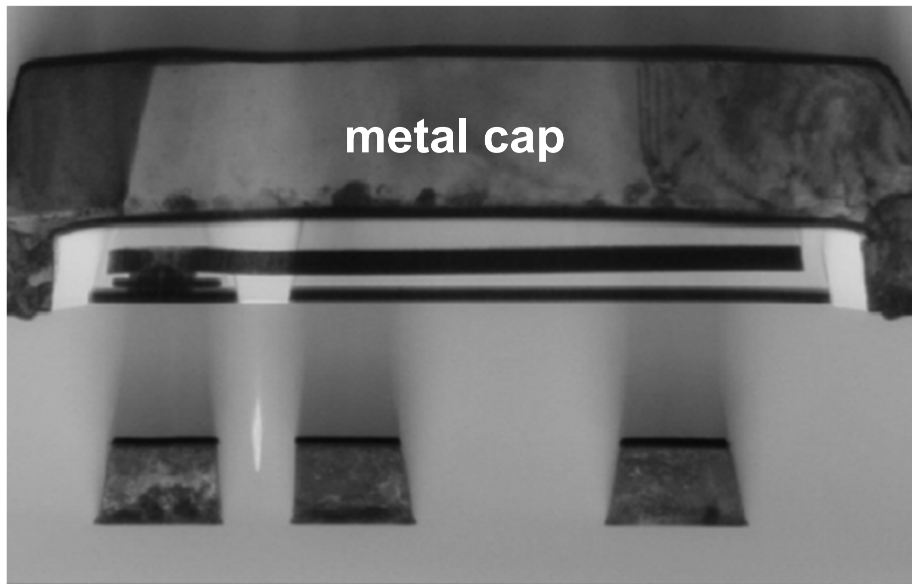
Table 1. Nanomech eFuse Device Characteristics (nominal process values)

- **Cantilever beam**
  - Programmed with electrostatic force
  - Surface forces hold beam down
  - Immune to radiation, extreme temperatures
- **MTP operation is a challenge…**

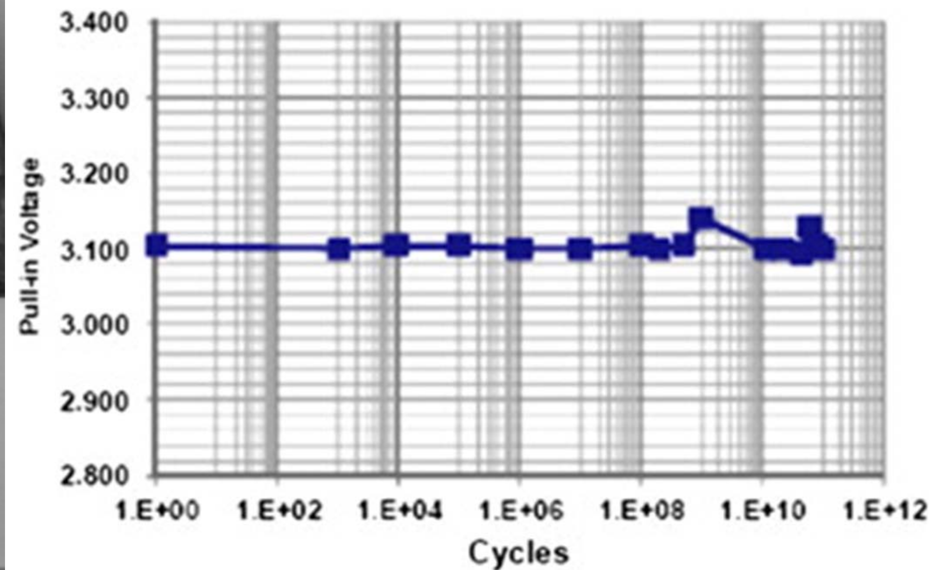
Improved Nanomech^{TM} Technology

R. Gaddi *et al*. (Cavendish Kinetics), *Microelectronics Reliability* Vol. 50, pp. 1593-1598, 2010

TEM cross-section



Endurance test results

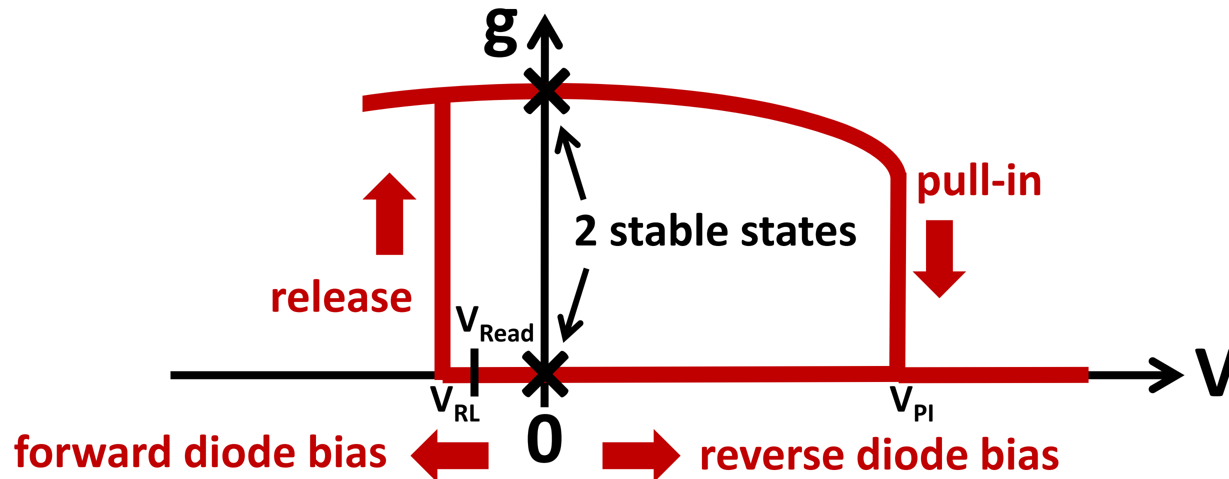


- **The beam can be pulled out of contact by biasing the cap.**
- **A select device (*e.g.* a transistor) is needed for each MEM switch in the memory array.**

Electro-Mechanical Diode NVM Cell

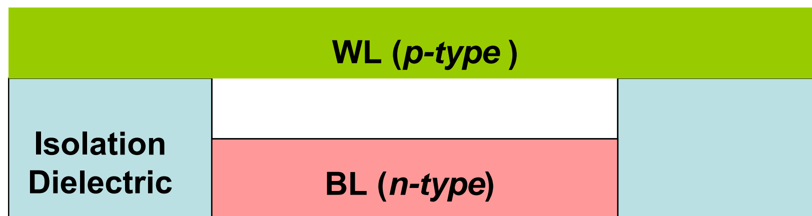
W. Kwon *et al.* (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012

- Achieve bi-stable operation of an electrostatic gap-closing actuator by leveraging the built-in electric field of a diode:

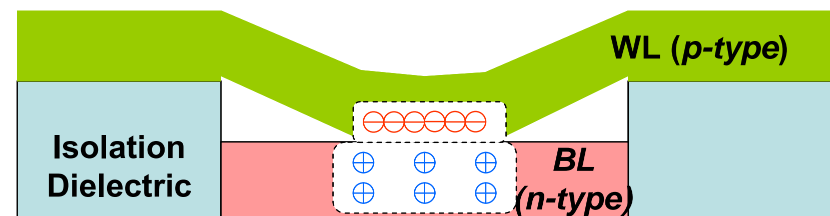


CROSS-SECTIONAL ILLUSTRATIONS

Reset State



Set State



$F_{adhesion} + F_{elec} > F_{spring}$

Memory Cell/Array Operation

	SET	RESET	READ
Selected WL P-type	0 Volts	$V_{Reset} > V_{RL}$	$V_{Read} > 0$ V
Selected BL N-type	$V_{Set} > V_{PI}$	0 Volts	sense amp.
Unselected WL P-type	$V_{Set}/2 < V_{PI}$	0 Volts	0 Volts
Unselected BL N-type	$V_{Set}/2 < V_{PI}$	0 Volts	(floating)

SET Operation: Cells along the same WL can be written together.

RESET Operation: Cells along the same WL are Reset together.

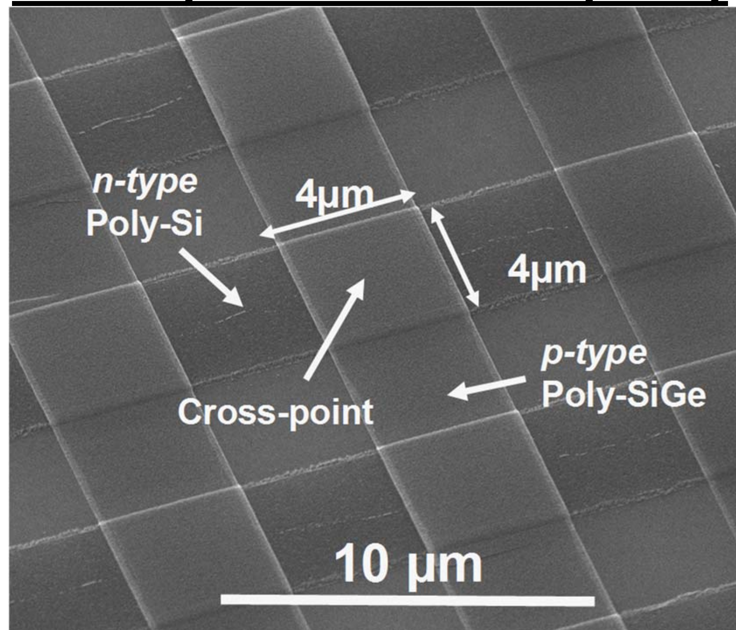
READ Operation: Reverse diode leakage of all other cells along the same BL should be less than Forward diode current of Set cell.

First Prototype Devices

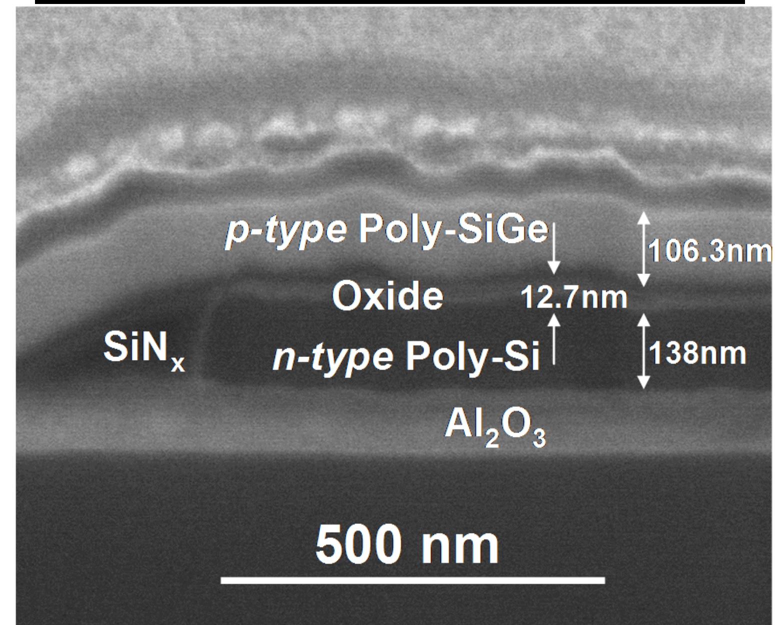
W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012

- **Cross-point arrays of MEM diodes were fabricated using conventional planar processing techniques.**
  - The WL (100-nm p-type poly-$Si_{0.4}Ge_{0.6}$) is supported by SiN_x spacers formed along the sidewalls of the BL (100 nm n-type poly-Si).
  - The air-gap (~13 nm thick) between the WL and BL is formed by selectively removing a sacrificial layer of LTO using HF vapor.

Bird's-eye view of memory array

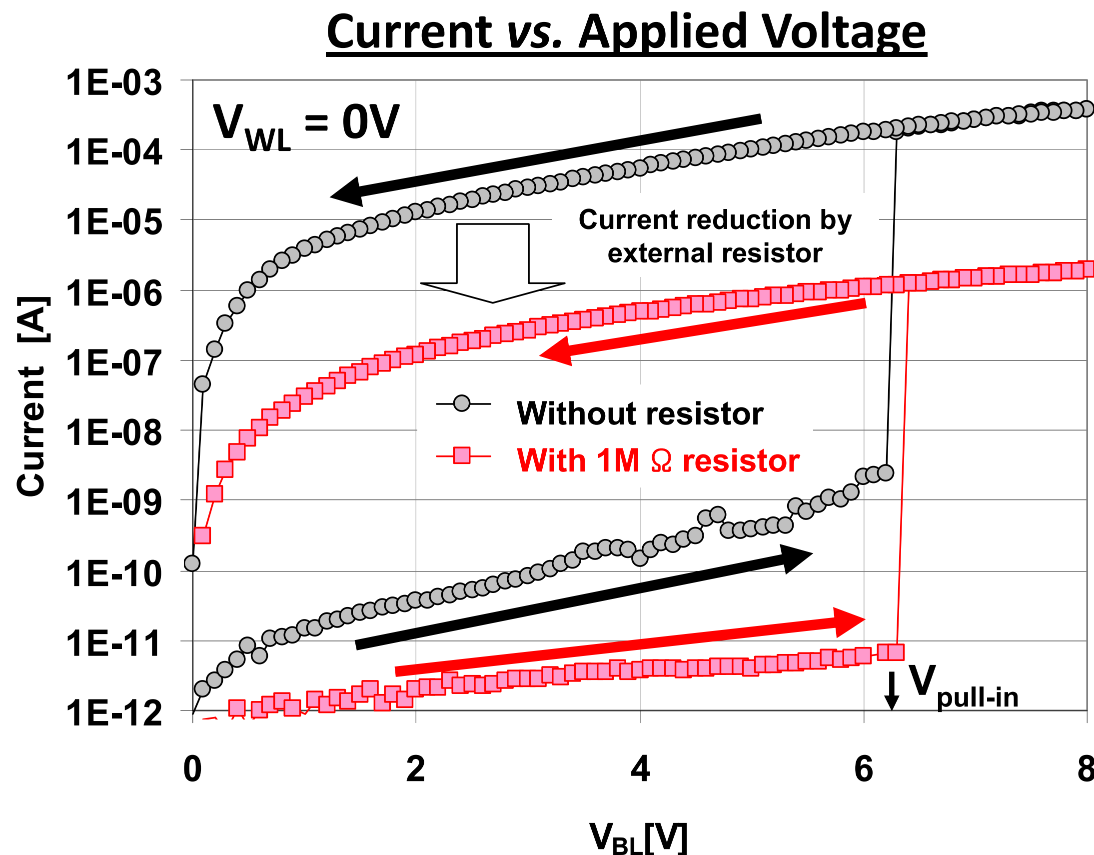


Cross-sectional view of a bit-cell



MEM Diode Set Operation

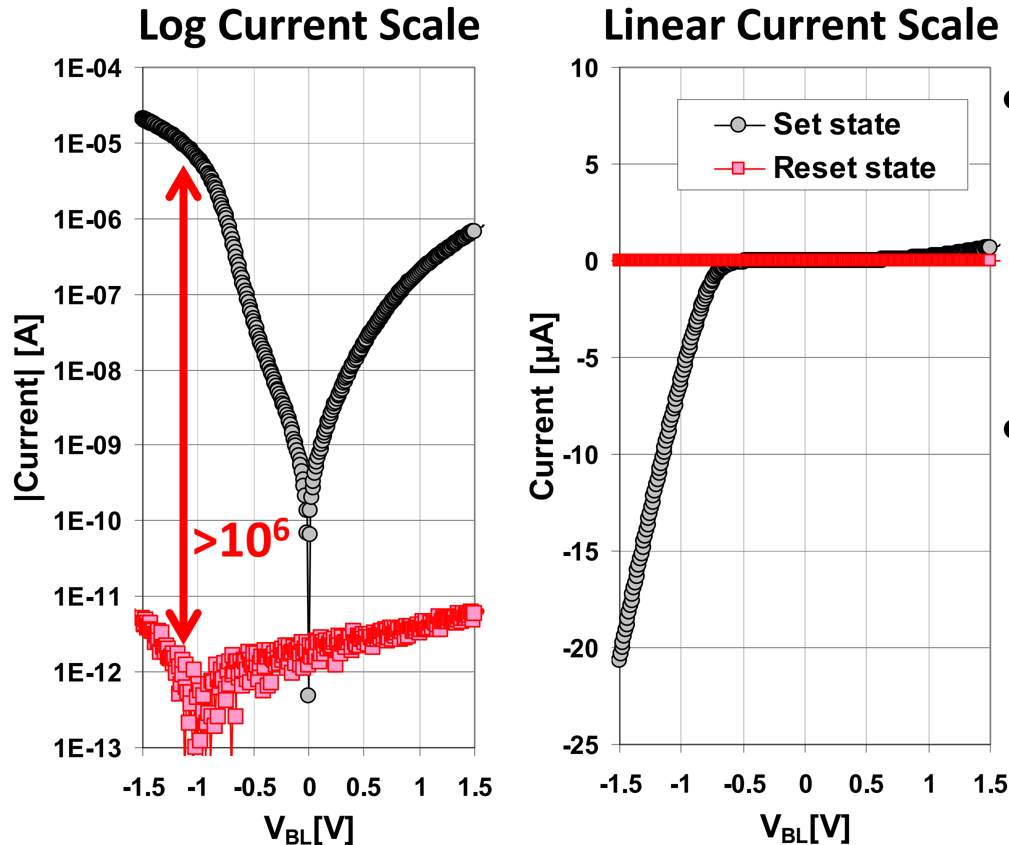
W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012



- **A sudden increase in current is seen at the voltage when the WL is pulled in to the BL.**
  - $V_{Set} \cong 6$ V, $t_{Set} \cong 2$ us
- **Since it is an applied voltage (not current) that is required to actuate the WL, the Set current can be lowered by inserting a current-limiting resistor.**

Measured *I-V* Characteristics

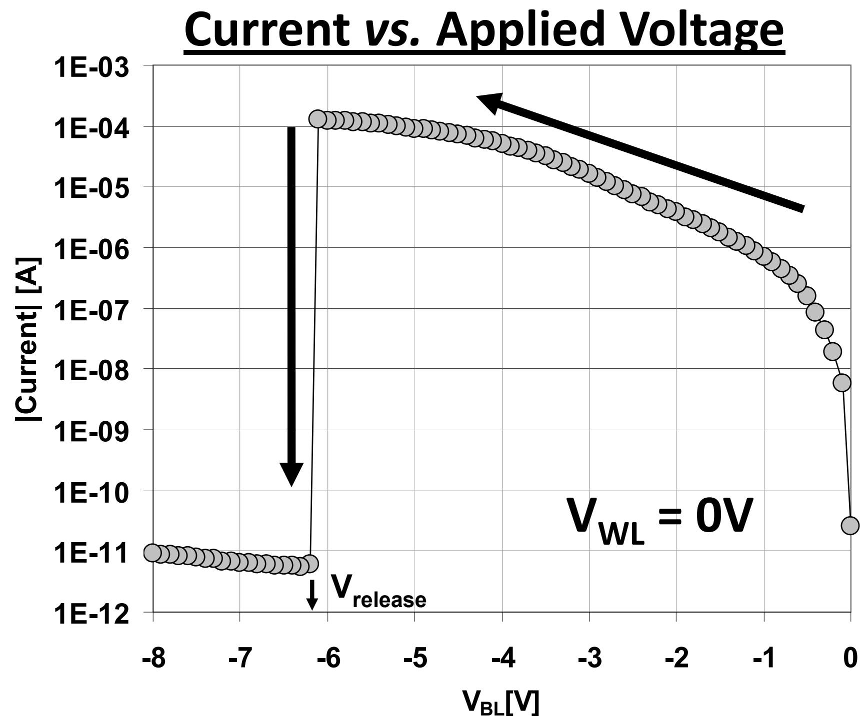
W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012



- **Set/Reset current ratio > 10^6**
  - Leakage through SiN_x spacers can be reduced with process improvements.
- **For V_{Read} = 1.2 V, the ratio of Set cell current to sneak path leakage current is ~100 for the prototype device**
  - This rectification ratio can be increased with process improvements.

MEM Diode Reset Operation

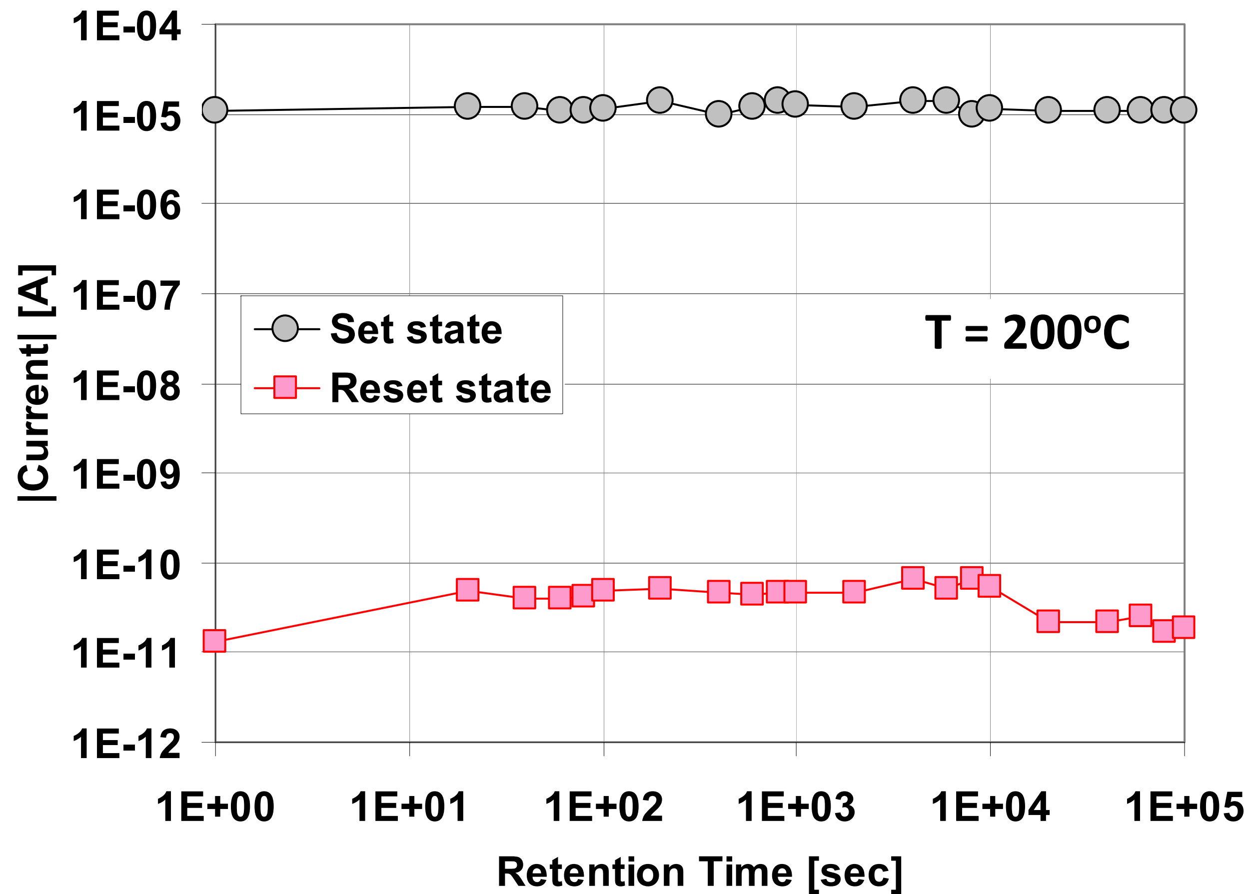
W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012



- **To Reset a memory cell, a voltage pulse is applied to counteract the built-in field of the p-n diode.**
  - forward bias → current flow
- **A sudden decrease in current is seen at the voltage when the WL comes out of contact with the BL.**
  - $V_{Reset} \cong$ -6 V, $t_{Reset} \cong$ 100 ms

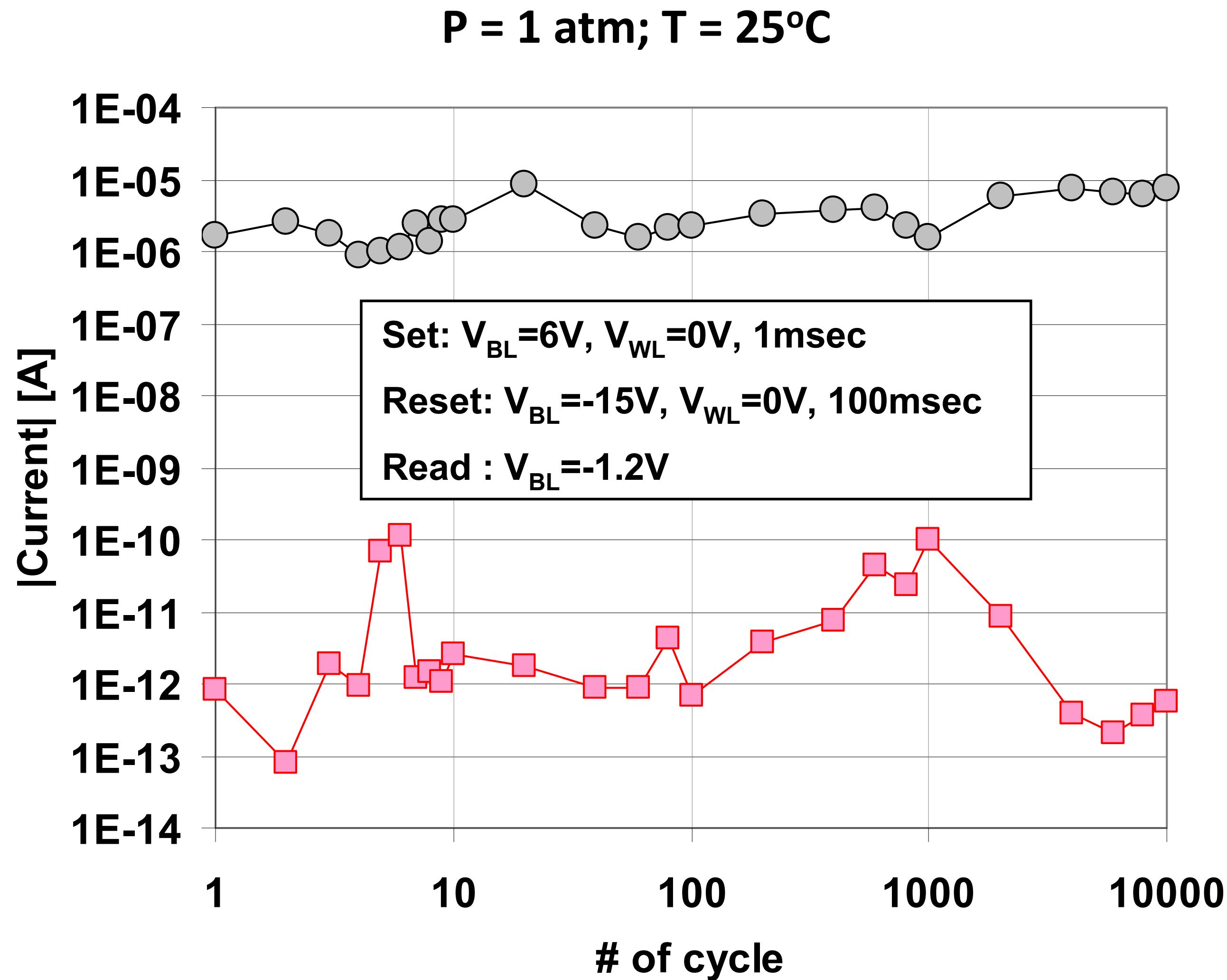
Measured Retention Behavior

W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012



Measured Endurance Characteristics

W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012



Cell Scaling Methodology

- **In the Set state, the built-in electrostatic force must be larger than the spring restoring force. The ratio of these forces is given by the equation**

$$\frac{F_{spring}}{F_{elec}} \propto \left(\frac{t}{l}\right)^3 \frac{g}{l} \frac{E}{E_{\max}}$$

t **= beam thickness**

l **= beam length**

g **= gap thickness**

E **= Young's modulus**

E_{max} **= peak electric field at the junction**

→ *t* and *g* should be scaled down together with the beam length

Beam Scaling Theory

Pull-in Voltage: $V_{\mathrm{PI}} \propto \sqrt{\dfrac{k_{\mathrm{eff}}\, g^3}{\varepsilon_0 A}}$

Pull-in Delay: $t_{\mathrm{PI}} \propto \sqrt{\dfrac{m}{k_{\mathrm{eff}}}}\left(\dfrac{V_{\mathrm{PI}}}{V_{\mathrm{DD}}}\right)$

$$k_{\mathrm{eff}} \propto \frac{EWt^3}{l^3}$$

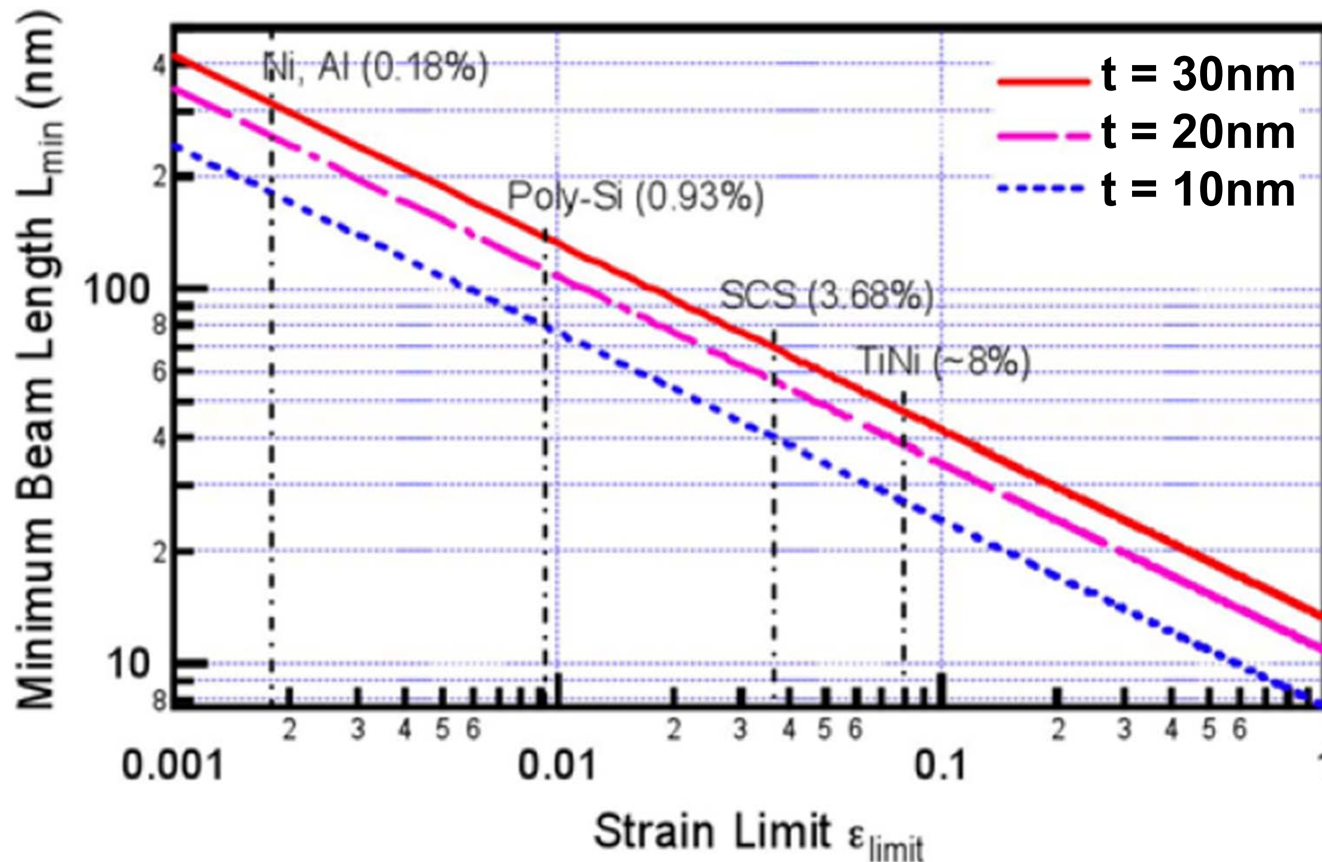
W = beam width
A = actuation area

Beam Parameter	Scaling Factor
Spring constant, k_{eff}	$1 / \kappa$
Mass, *m*	$1 / \kappa^3$
Pull-in voltage, V_{PI}	$1 / \kappa$
Pull-in delay, t_{PI}	$1 / \kappa$
Switching energy	$1 / \kappa^3$
Device density	κ^2
Power density	1

Beam Length Scaling Limitations

D. T. Lee *et al.* , *IEEE Trans. Electron Devices*, Vol. 56, p. 688-691, 2009

- **Structural materials with high yield strain will be needed to scale beam lengths to below 100 nm, for 5 nm actuation gap**



Projected Performance

W. Kwon *et al*. (UC Berkeley), to be presented at the *2012 International Memory Workshop*

Technology	4um	90 nm	20 nm	10 nm
Cell size	64 μm^2	0.0324 μm^2	0.002 μm^2	0.0008 μm^2
F^2	4 F^2	4 F^2	6 F^2	8 F^2
Structural material	Poly-SiGe	Al	TiNi	CNT
Young's Modulus	140GPa	77 GPa	14 GPa	5 GPa
Beam thickness	100nm	5 nm	4 nm	3 nm
Actual Gap thickness	36nm	3 nm	2 nm	2 nm
Set Voltage	7.0 V	2.8 V	2.4 V	2.1 V
Set Time	21 ns	0.3 ns	0.27 ns	0.12 ns

NVM Technology Comparison

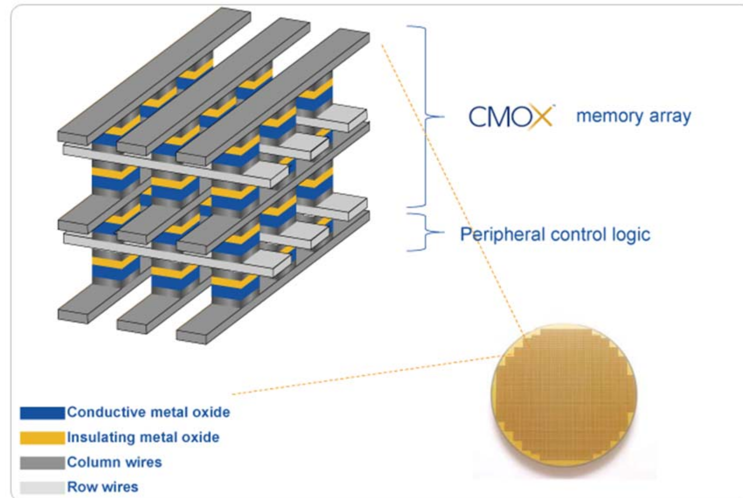
W. Kwon *et al.* (UC Berkeley), to be presented at the *2012 International Memory Workshop*

Technology	NAND Flash	PCM	STT-MRAM	Redox RRAM	Electro-mechanical diode
Cell Size	2.5 F^2	6 F^2	20-40 F^2	5-8 F^2	4-6 F^2
Scaling Limit	16 nm	5-10 nm	7-10 nm	5-10 nm	5 nm W x 20 nm L
Storage Mechanism	F-N Tunneling	Phase change by Joule heating	Electron spin torque transfer	Ion transport and redox reaction	Mechanical gap closing actuation
Write/Erase Voltage	18-20 V	< 3 V	< 1.8 V	< 0.5 V	< 3 V
Write time	>10 us	50-120 ns	< 100 ns	< 5 ns	< 1 ns
Endurance	10^4 - 10^5	10^{15}	10^{12}	10^{16}	>10^{10}
Retention	10 yrs	10 yrs	10 yrs	10 yrs	> 10 yrs @ 200 ℃
Ease of Integration	10 Masks	2-3 Masks to BEOL	3-4 Masks to BEOL	2-3 Masks to BEOL	2 Masks
Write Energy per Bit	> 1 fJ	< 2 pJ	< 4 pJ	1 fJ	< 0.1 fJ

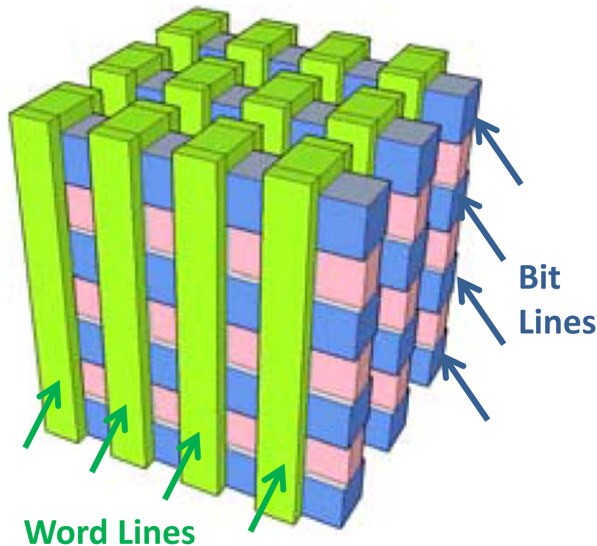
http://www.itrs.net/Links/2010ITRS/2010Update/ToPost/ERD_ERM_2010FINALReportMemoryAssessment_ITRS.pdf

- **NEMory technology potentially offers the best performance and lowest energy consumption.**

3-Dimensional Integration



Unity Semiconductor Corp.



W. Kwon *et al*. (UC Berkeley), to be published

- **Conventional cross-point memory array technologies require 2 lithography steps per memory layer**

- **NEMory technology requires only 2 lithography steps to define the 3-D memory array**
  - built-in redundancy (2 WL/cell)
  - allows for longer beam length

Outline

- Introduction
- MEMs-based memory technologies
- **Conclusion**

Conclusion

- **Mechanical devices are attractive for NVM applications.**
  - Performance is adequate.
  - Operating voltage and energy can be low.
  - Immune to radiation, heat, and mechanical shock.
  - Potentially very low manufacturing cost.
- **The electro-mechanical diode cell design is well suited to a cross-point array architecture. The first prototypes show**
  - ✓ excellent retention behavior
  - ✓ good endurance

  indicating promise for embedded NVM applications.
- **Optimization of thin-film materials and processes is needed to maximize cell performance and scalability.**