Recent Progress and Challenges for Relay Logic Switch Technology

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Outline

• Introduction
  – Why relays?
  – Relay-based IC design

• Recent Progress

• Current Challenges

• Conclusion
• **Emergence of Ambient Intelligence**
  – Sense/monitor, communicate, and react to the environment
CMOS Voltage Scaling

- Scaling supply voltage ($V_{DD}$) reduces circuit speed
- Scaling threshold voltage ($V_T$) increases leakage

![Graph showing Drain Current ($I_d$) vs. Gate Voltage ($V_g$) and Normalized Energy/cycle vs. $V_{DD}(V)$]

- $S > 60\text{mV/dec}$

$E_{tot}$, $E_{dyn}$, $E_{leak}$

Slide 3
Why Relays?

- Zero OFF-state current ($I_{OFF}$); abrupt switching
  - Turns on by electrostatic actuation when $|V_{GS}| \geq V_{PI}$
  - Turns off by spring restoring force when $|V_{GS}| \leq V_{RL}$
Relay Endurance

- Endurance increases exponentially with decreasing $V_{DD}$, and linearly with decreasing $C_L$

- Endurance is projected to exceed $10^{15}$ cycles @ 1V
4-Terminal (4-T) Relay for Digital Logic

- Voltage applied between the gate and body brings the channel into contact with the source and drain.
  - Folded-flexure design relieves residual stress.
  - Gate oxide layer insulates the channel from the gate.

R. Nathanael et al., IEDM 2009
4-T Relay $I_D$-$V_G$ Characteristics

- Zero $I_{OFF}$ and abrupt switching behavior observed
- Hysteresis is due to pull-in mode operation ($t_{dimple} > t_{gap}/3$) and contact surface adhesion.

R. Nathanael et al., IEDM 2009; V. Pott et al., Proc. IEEE 2010
Digital IC Design with Relays

- **CMOS**: delay is set by electrical time constant
  - Quadratic delay penalty for stacking devices
  - \( \Rightarrow \) Buffer & distribute logical/electrical effort over many stages

- **Relays**: delay is dominated by mechanical movement
  - Can stack \( \sim 100 \) devices before \( t_{elec} \approx t_{mech} \)
  - \( \Rightarrow \) Implement relay logic as a single complex gate
Relay-Based VLSI Building Blocks

In collaboration with V. Stojanović (MIT) and D. Marković (UCLA)

F. Chen et al., ISSCC 2010
Relay Carry Generation Circuit

- Demonstrates propagate-generate-kill logic as a single complex gate
Energy-Delay Comparison with CMOS

- 90nm relay vs. CMOS adders and multipliers:
  >2-100× energy savings @ 3-100× higher delay

M. Spencer et al., JSSC 2011; H. Fariborzi et al., ESSCIRC 2011
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• Introduction
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  – Relay scaling
  – Multi-input/multi-output relay designs
• Current Challenges
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Structural Layer Requirements

• To reduce $V_{pi}$, the effective spring constant ($k_{eff}$) and actuation gap thickness ($t_{gap}$) must be reduced.

\[
V_{pi} \propto \sqrt{\frac{k_{eff} t_{gap}^3}{\varepsilon_0 A}} \text{ where } k_{eff} \propto \frac{E W h^3}{L^3}
\]

→ Need to reduce the structural layer thickness ($h$)

• Strain gradient causes out-of-plane bending

\[
\frac{1}{\rho} = \frac{2\Delta z}{L^2} \propto \frac{M}{E W h^3}
\]

$\Delta z$: tip deflection

$\rho$: radius of curvature

$M$: bending moment

→ Need very low strain gradient
Structural Film Development

- Thin TiN + poly-Si$_{0.4}$Ge$_{0.6}$ bi-layer stack:
  - Tensile TiN compensates strain gradient in Si$_{0.4}$Ge$_{0.6}$

- Interferometry topograph shows low strain gradient of $-7 \times 10^{-4}/\mu$m
  (~10x improvement)

I-R. Chen et al., ECS Spring Meeting 2012
Single-Gate, Dual-Source/Drain Relay

Circuit Symbol

Drain 1 || Drain 2
Gate || Body
Source 1 || Source 2

Temperature Dependence:

Measured I-V

Plan-View SEM

5 µm

(a)
Single-Gate Relay Inverter/Buffer

\[ V_{\text{IN}} \] \[ V_{\text{OUT}} \] (INV) \[ V_{\text{OUT}} \] (BUF) \[ V_{\text{B\_HIGH}} = 13V \] \[ V_{\text{B\_LOW}} = -12V \] \[ V_{\text{OUT}} \] \[ V_{\text{DD}} = 1V \] \[ V_{\text{GND}} = 0V \] 

(a) 

(b) 

R. Nathanael et al., VLSI-TSA 2012
Dual-Gate, Dual Source/Drain Relay

- Gate electrodes are interdigitated to ensure that each gate has equal influence on the movable body.
Measured $V_{PI}$ and $V_{RL}$ of a Dual-Gate Relay

- "1" $\equiv V_G$
- Each gate has equal influence
- Depending on $V_B$, relay can be actuated using one or two gate electrodes

R. Nathanael et al., VLSI-TSA 2012
Dual-Gate Relay Circuit: AND/NAND

- $V_{DD} = 8V$
- $V_{B_{LOW}} = -4V$
- $V_{B_{HIGH}} = 15V$
- $V_{OUT}^{(AND)}$
- $V_{OUT}^{(NAND)}$

Input voltages:

- $V_{IN1}$
- $V_{IN2}$

Output voltages:

- $V_{OUT}$

Time-domain behaviour:

- AND
- NAND

Graphs show input and output waveforms over time.
Dual-Gate Relay Circuit: OR/NOR

- $V_{DD} = 8V$
- $V_{B\_LOW} = -6V$
- $V_{B\_HIGH} = 12V$
- $GND = 0V$

Truth tables:

- OR:
  0 0 1 1 0

- NOR:
  0 1 0 1 0

Output voltages:

- OR: 0 0.1 0.2 0.3
- NOR: 0 0.1 0.2 0.3

R. Nathanael et al., VLSI-TSA 2012
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  – Contact resistance
  – Surface adhesion
• Conclusion
Tungsten Contact Resistance Evolution

- Joule heating occurs when the relay is on
- Contacting surfaces oxidize when the relay is turned off
- Surface oxide layers result in increased $R_{ON}$

Current

Y. Chen et al., IEEE/ASME J-MEMS 2012
Stiction: The Ultimate Relay Scaling Limiter

- Hysteresis voltage \( (V_{PI} - V_{RL}) \) scales with \( V_{PI} \):

\[
V_{PI} - V_{RL} = V_{PI} \left[ 1 - 2.6 \sqrt{\frac{t_{dimple}}{t_{gap}}} \left(1 - \frac{t_{dimple}}{t_{gap}}\right)\right]
\]

ignoring surface adhesion force

- Adhesive force reduces with contacting region area:

XSEM of Contact Dimple

- J. Yaung et al., to be published
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Conclusion

• Relays have zero $I_{\text{OFF}}$ and can incorporate multiple input/output electrodes
  → potentially can achieve lower energy per operation and greater functionality per device than CMOS for digital logic applications.

• Practical challenges remain to be solved:
  – Contact surface oxidation
  – Minimization of adhesion force within $R_{\text{ON}}$ limits
  – Development of ultra-thin structural films with very low strain gradient
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