Recent Progress and Challenges for Relay Logic Switch Technology

Tsu-Jae King Liu

Louis Hutin, I-Ru Chen, Rhesa Nathanael, Yenhao Chen, Matthew Spencer and Elad Alon

Electrical Engineering and Computer Sciences Department
University of California, Berkeley, CA USA

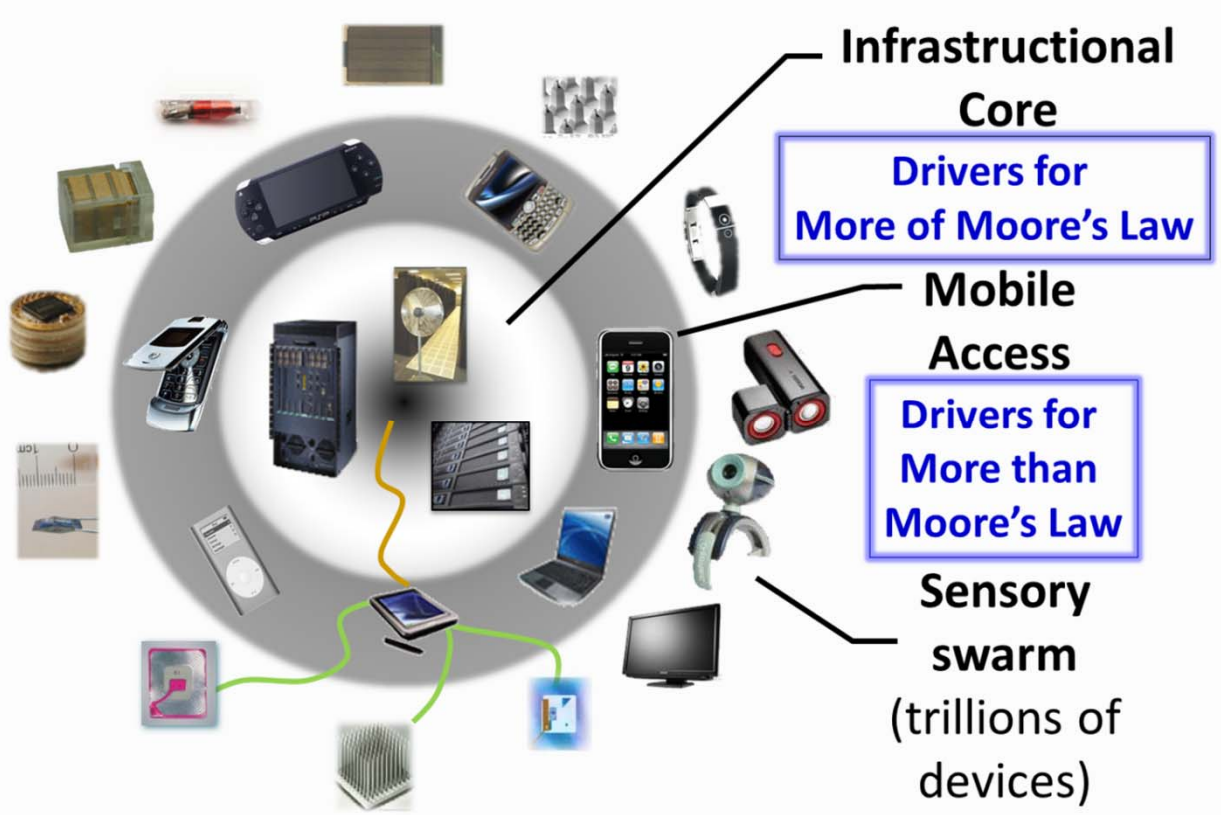
June 12, 2012

Symposia on VLSI Technology and Circuits

Outline

- **Introduction**
  - Why relays?
  - Relay-based IC design
- **Recent Progress**
- **Current Challenges**
- **Conclusion**

Vision of the Future: Swarms of Electronics



Smart Grid

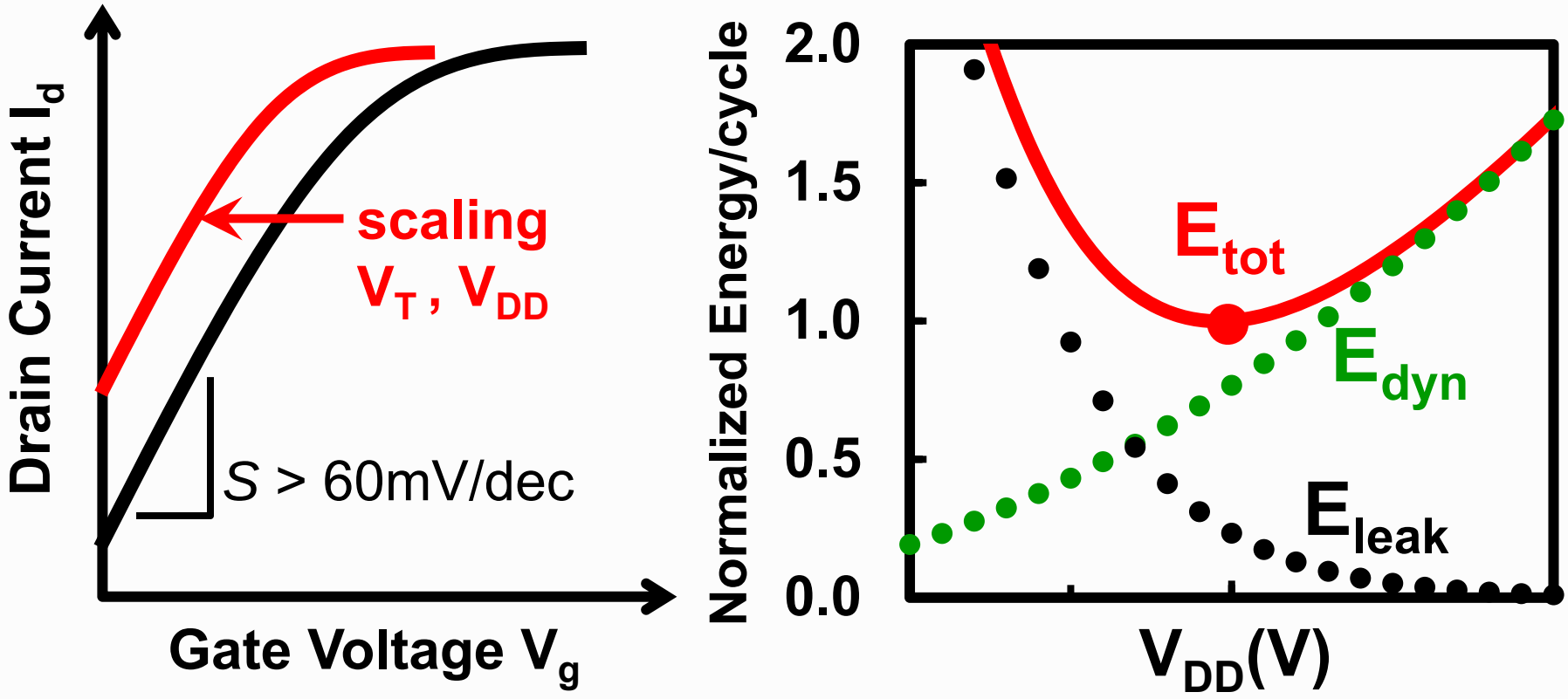
Traffic management

Smart Buildings

Infrastructure maintenance

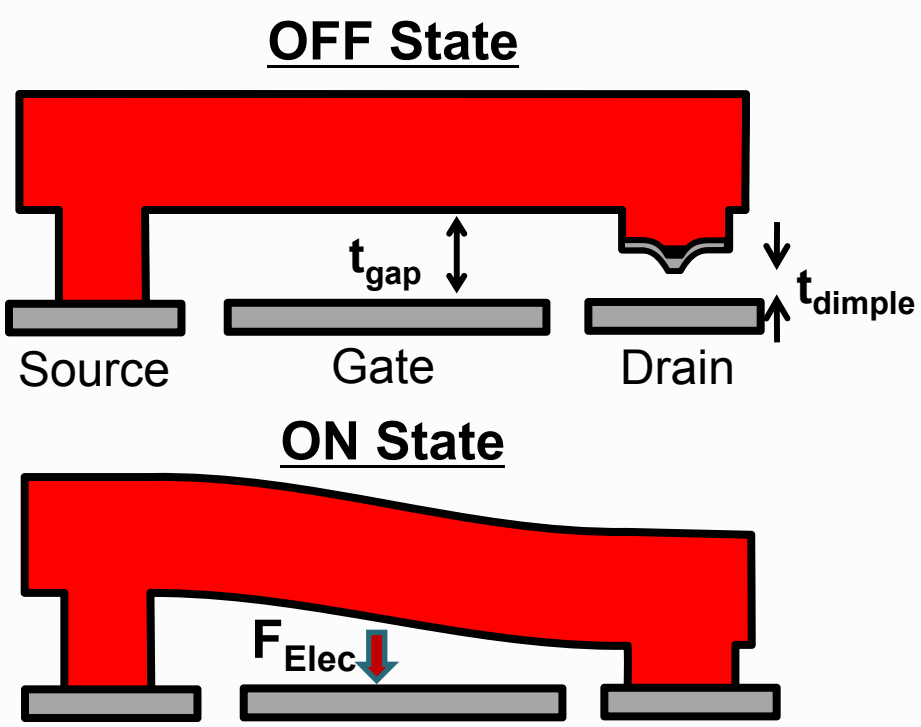
- **Emergence of Ambient Intelligence**
  - Sense/monitor, communicate, and react to the environment

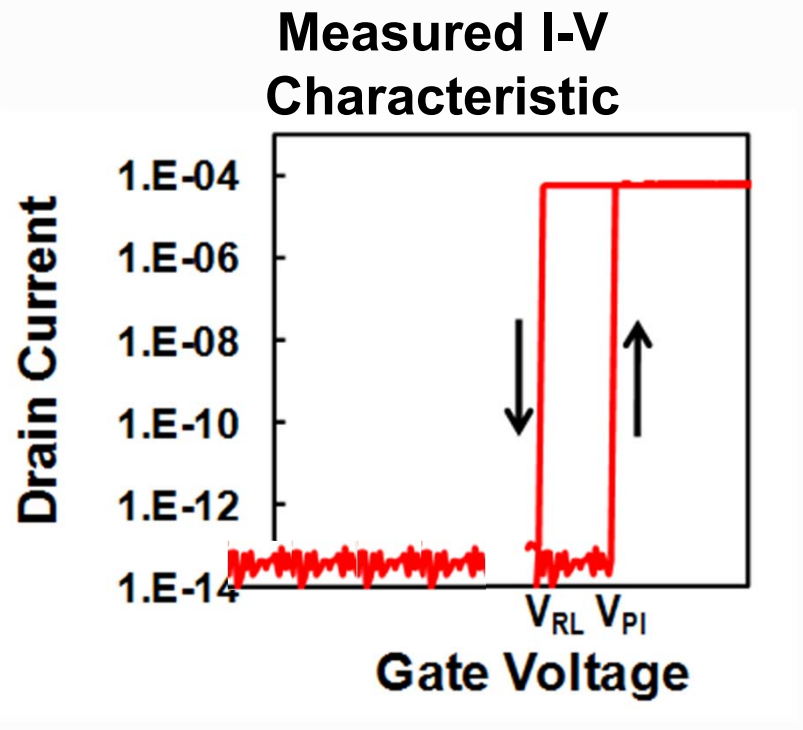
CMOS Voltage Scaling



- Scaling supply voltage (V_{DD}) reduces circuit speed
- Scaling threshold voltage (V_T) increases leakage

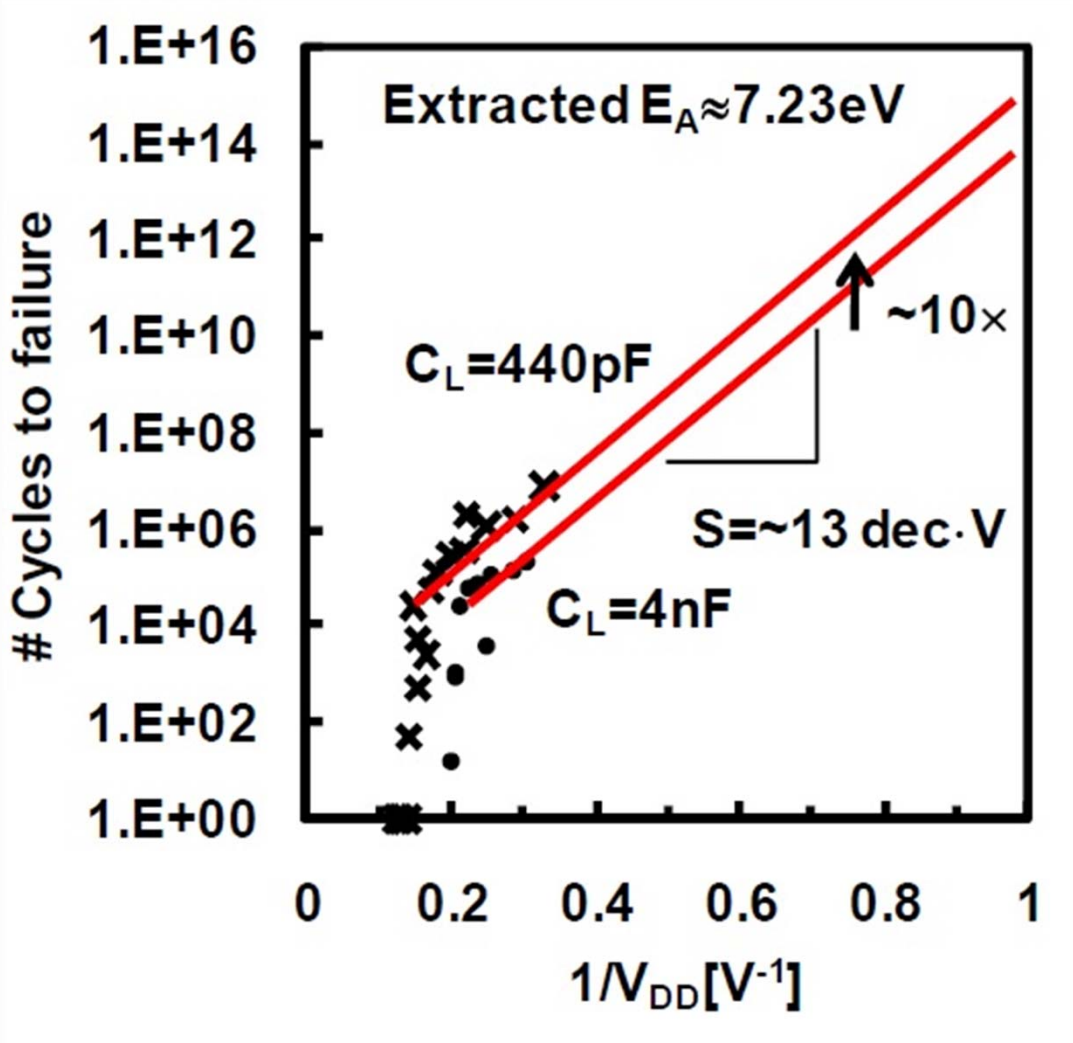
Why Relays?





- **Zero OFF-state current (I_{OFF}); abrupt switching**
  - Turns on by electrostatic actuation when $|V_{GS}| \geq V_{PI}$
  - Turns off by spring restoring force when $|V_{GS}| \leq V_{RL}$

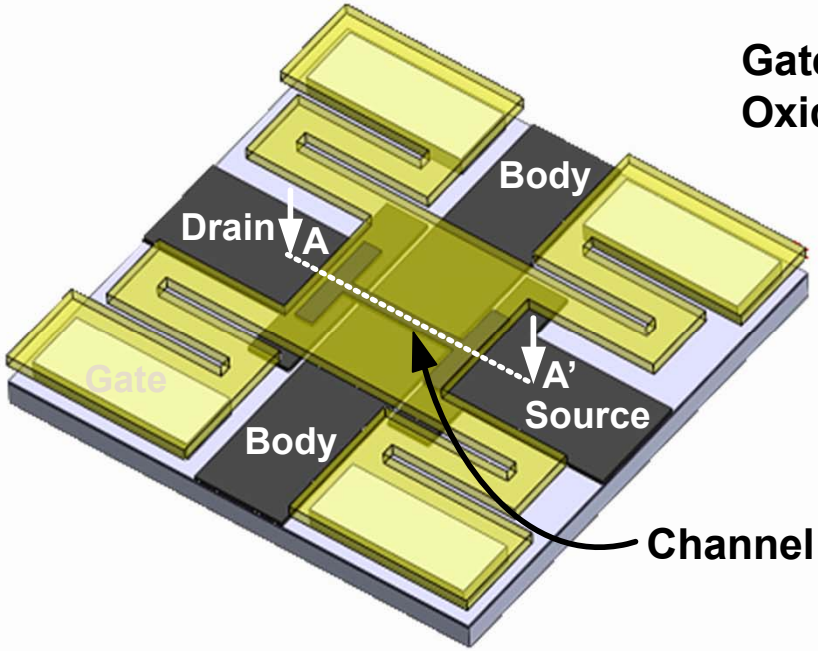
Relay Endurance



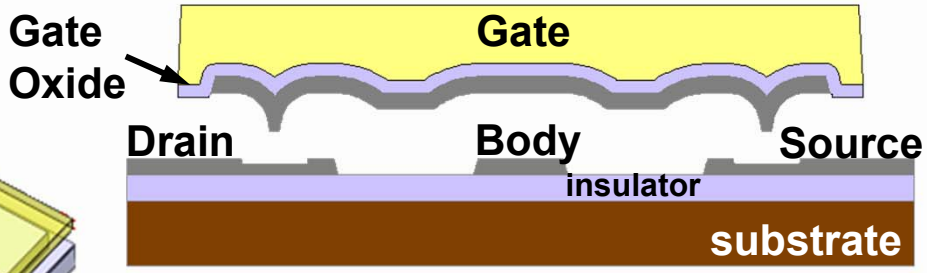
- Endurance increases exponentially with decreasing V_{DD}, and linearly with decreasing C_L
- Endurance is projected to exceed 10^{15} cycles @ 1V

4-Terminal (4-T) Relay for Digital Logic

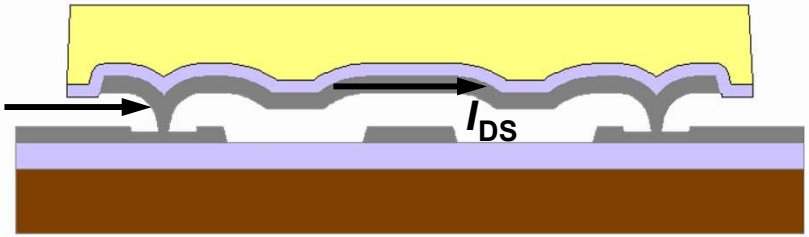
Isometric View:



AA' cross-section: OFF state



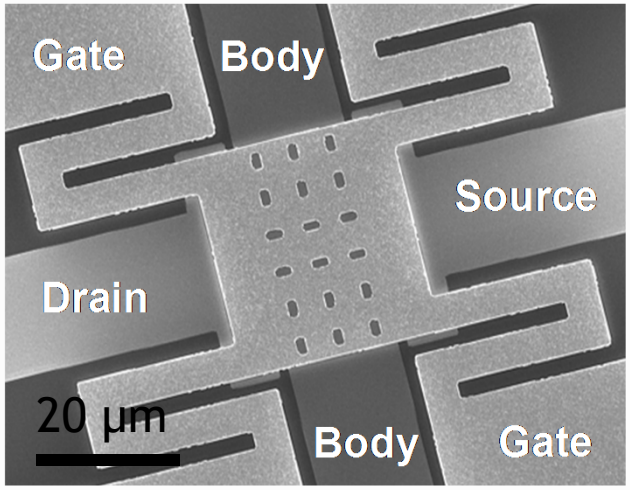
AA' cross-section: ON state

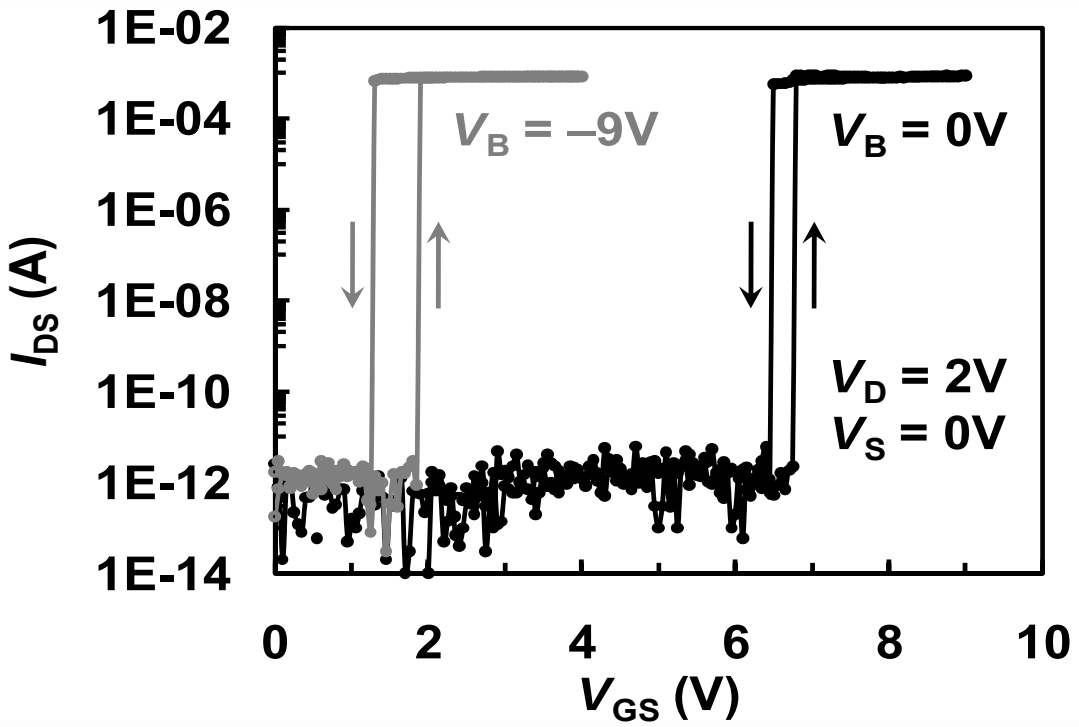


- **Voltage applied between the gate and body brings the channel into contact with the source and drain.**
  - Folded-flexure design relieves residual stress.
  - Gate oxide layer insulates the channel from the gate.

4-T Relay I_D-V_G Characteristics

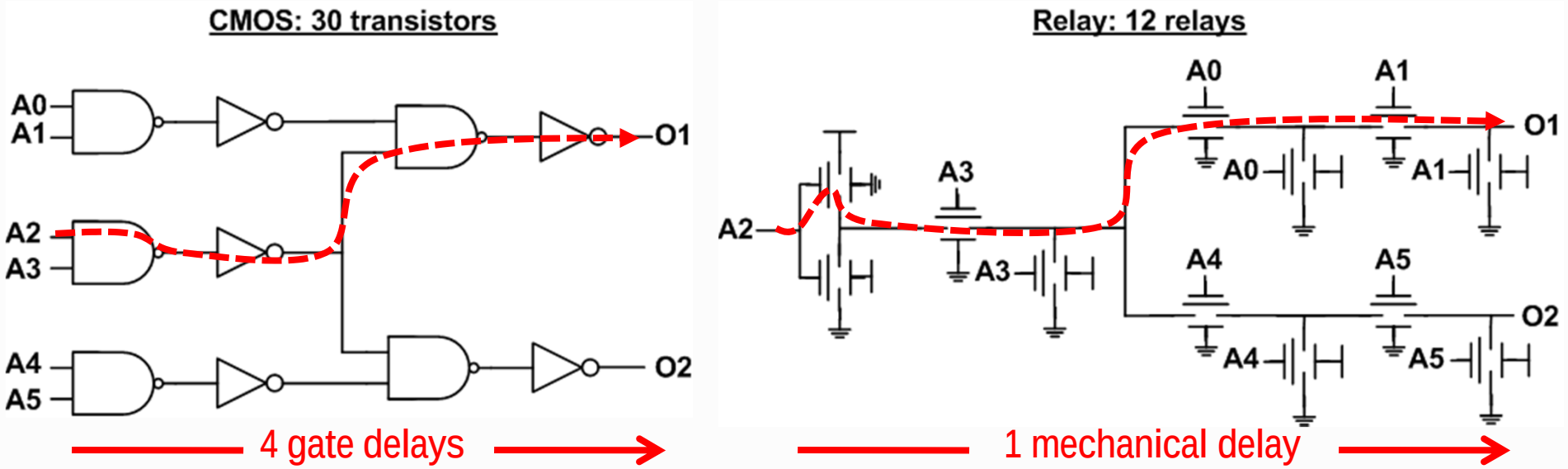
Plan View SEM of 4-T Relay





- Zero I_{OFF} and abrupt switching behavior observed
- Hysteresis is due to pull-in mode operation ($t_{dimple} > t_{gap}/3$) and contact surface adhesion.

Digital IC Design with Relays

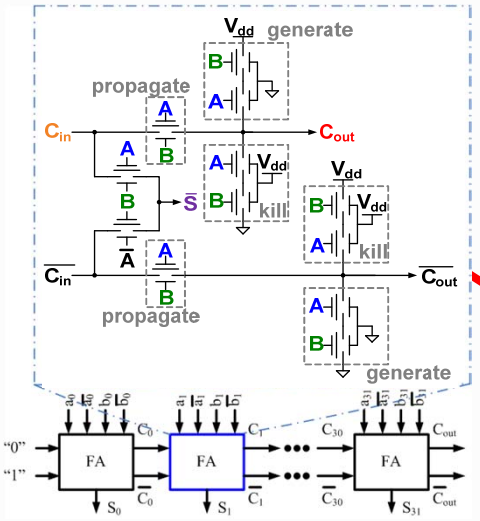


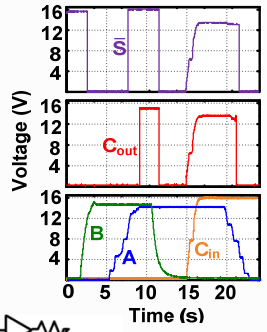
- **<u>CMOS</u>: delay is set by electrical time constant**
  - Quadratic delay penalty for stacking devices

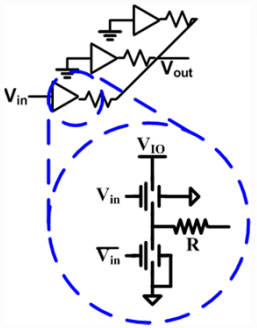
  → Buffer & distribute logical/electrical effort over many stages
- **<u>Relays</u>: delay is dominated by mechanical movement**
  - Can stack ~100 devices before $t_{elec} \approx t_{mech}$

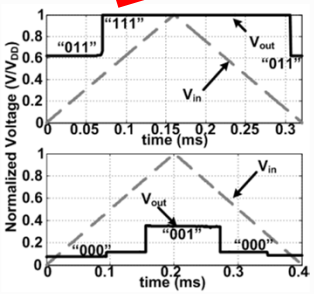
  → Implement relay logic as a single complex gate

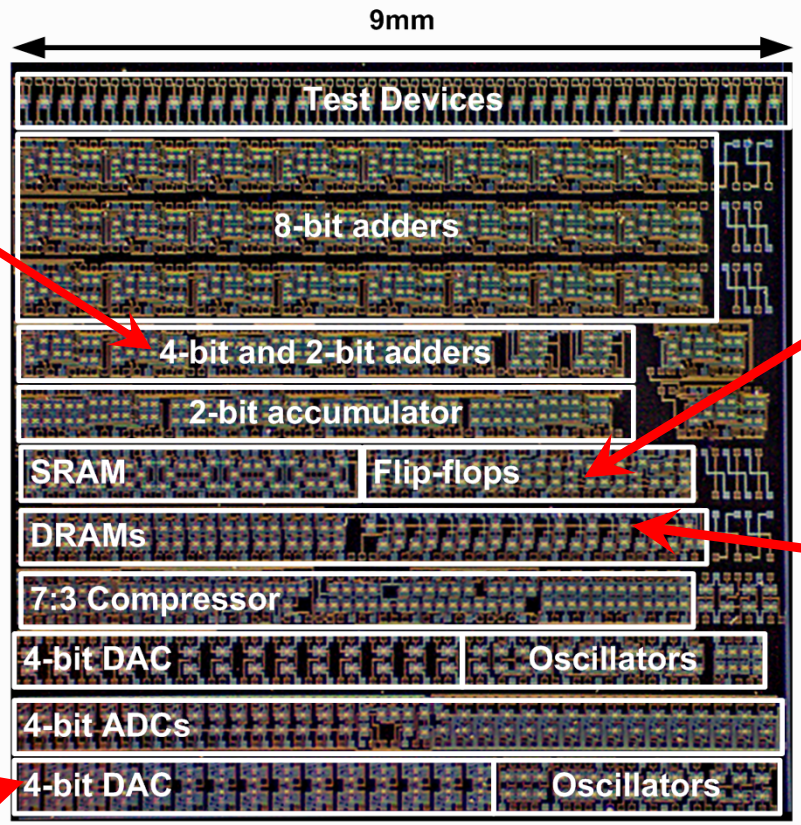
Relay-Based VLSI Building Blocks

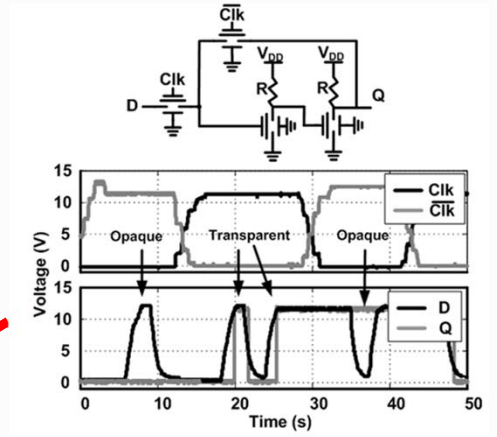


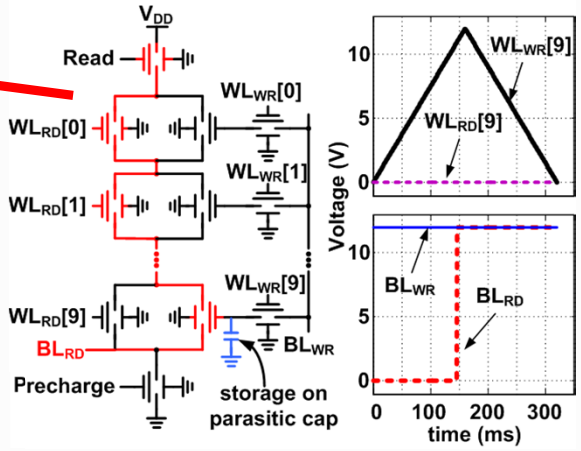






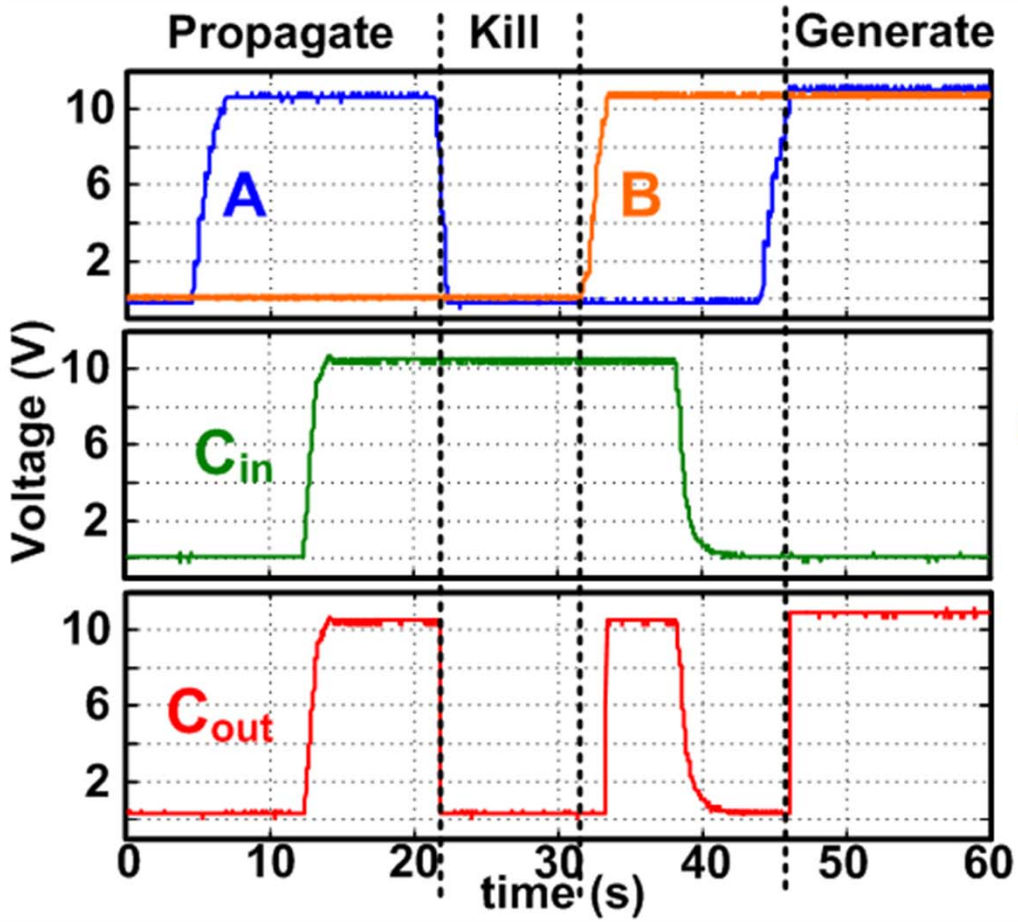


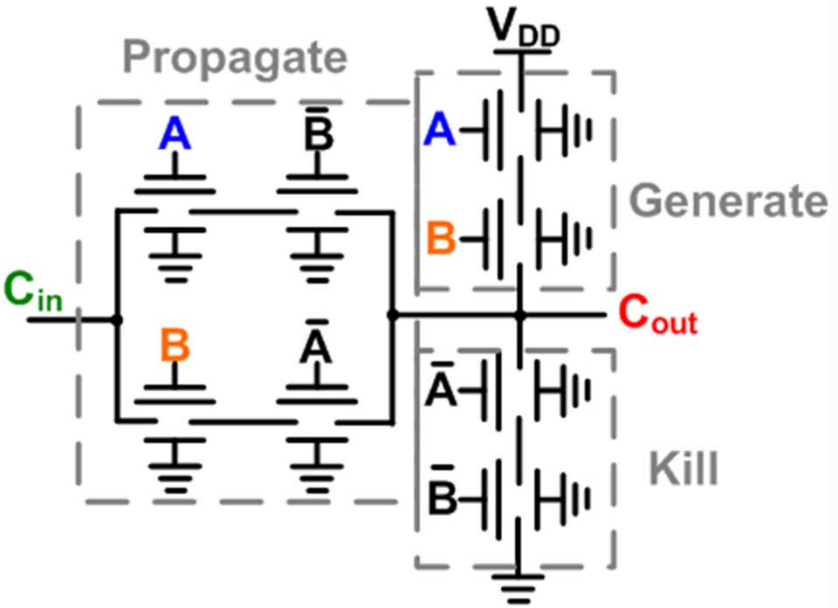




In collaboration with
V. Stojanović (MIT) and
D. Marković (UCLA)

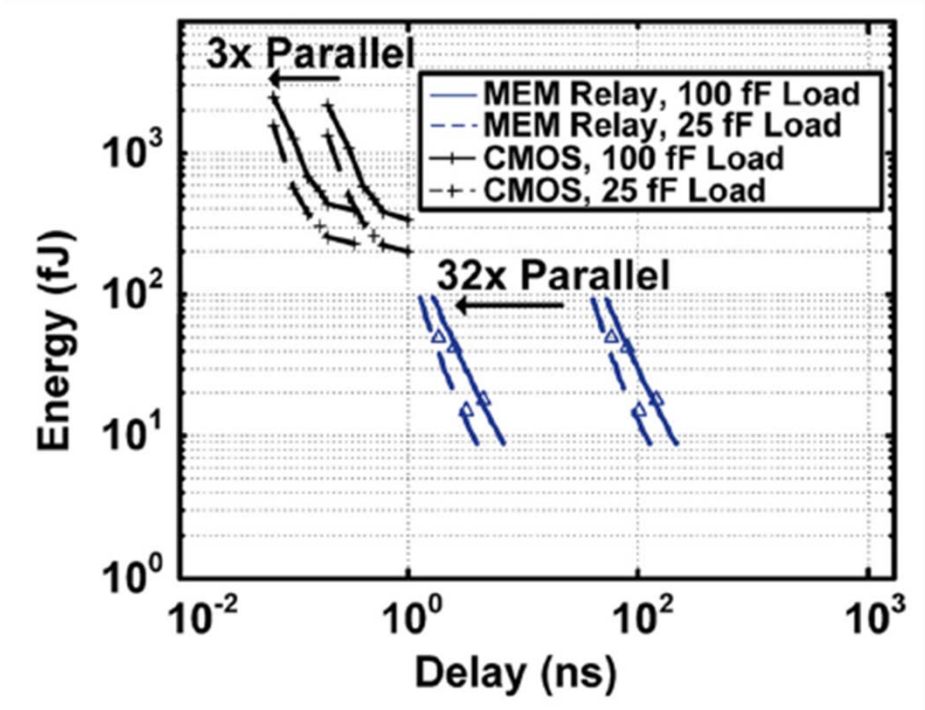
Relay Carry Generation Circuit

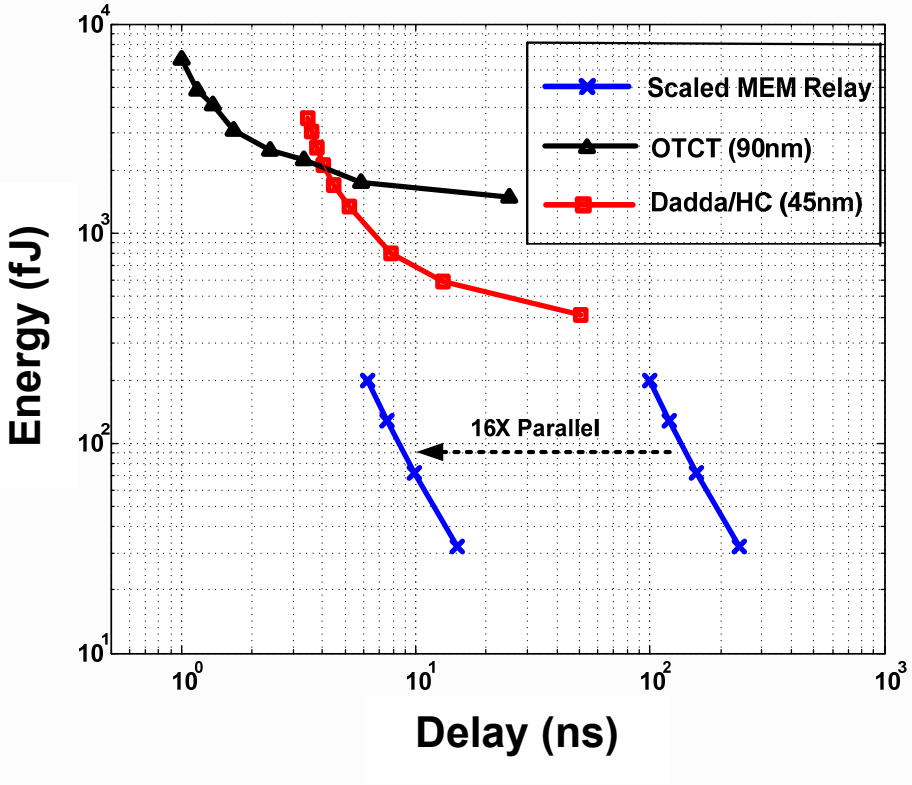




- **Demonstrates propagate-generate-kill logic as a single complex gate**

Energy-Delay Comparison with CMOS





- **90nm relay *vs.* CMOS adders and multipliers:**

  >2-100× energy savings @ 3-100× higher delay

Outline

- Introduction
- **Recent Progress**
  - Relay scaling
  - Multi-input/multi-output relay designs
- Current Challenges
- Conclusion

Structural Layer Requirements

- **To reduce V_{PI}, the effective spring constant (k_{eff}) and actuation gap thickness (t_{gap}) must be reduced.**

$$V_{PI} \propto \sqrt{\frac{k_{eff} {t_{gap}}^3}{\varepsilon_0 A}} \qquad \text{where} \qquad k_{eff} \propto \frac{EWh^3}{L^3}$$

→ **Need to reduce the structural layer thickness (h)**

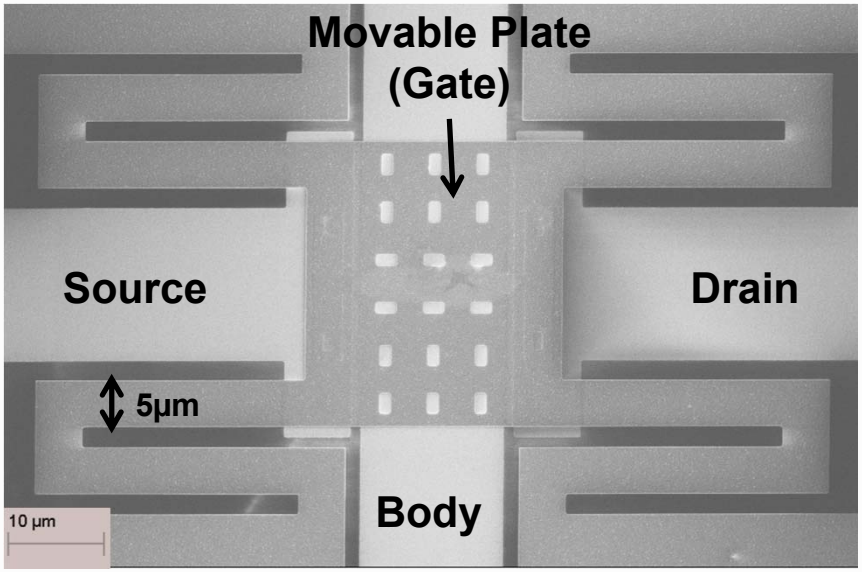
- **Strain gradient causes out-of-plane bending**

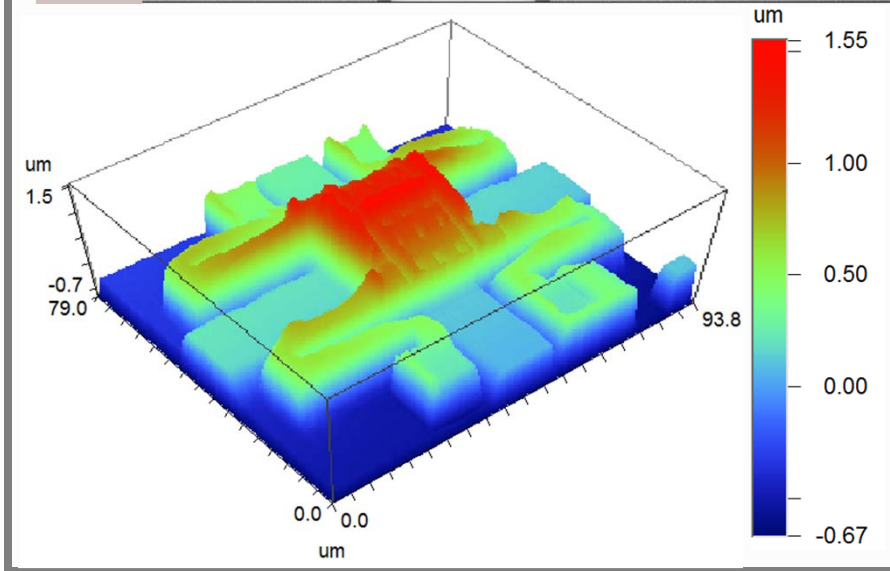
$$\frac{1}{\rho} = \frac{2\Delta z}{L^2} \propto \frac{M}{EWh^3}$$

Δz: tip deflection
ρ: radius of curvature
M: bending moment

→ **Need very low strain gradient**

Structural Film Development





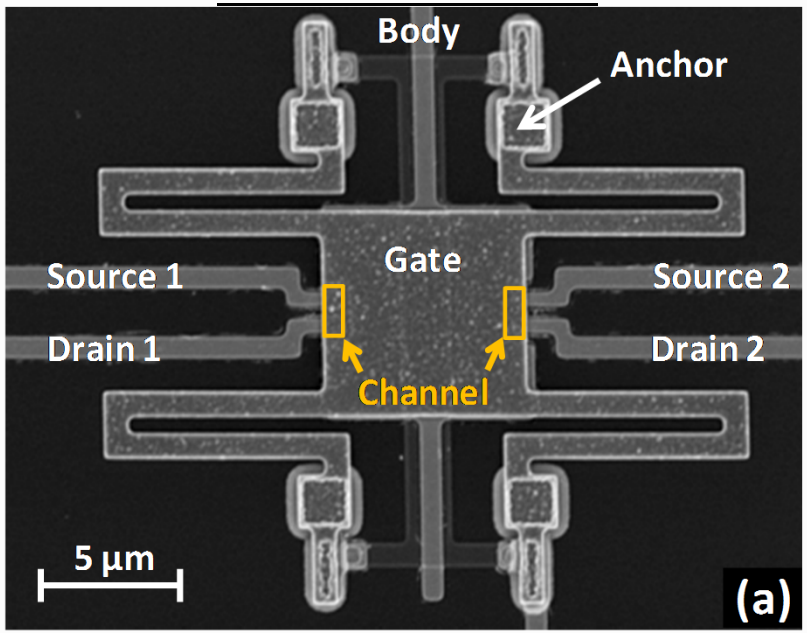
- **Thin TiN + poly-$Si_{0.4}Ge_{0.6}$ bi-layer stack:**
  - Tensile TiN compensates strain gradient in $Si_{0.4}Ge_{0.6}$

- **Interferometry topograph shows low strain gradient of -7×10^{-4}/μm**

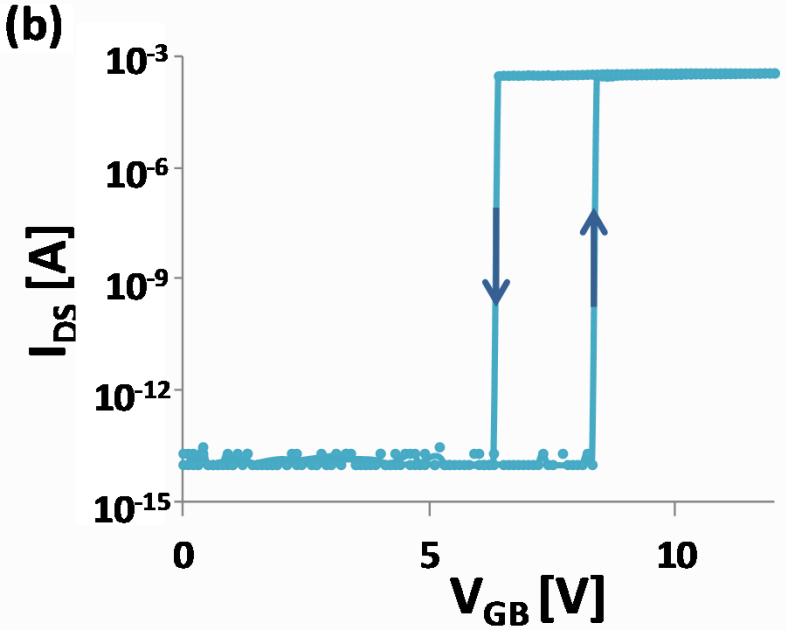
  (~10x improvement)

Single-Gate, Dual-Source/Drain Relay

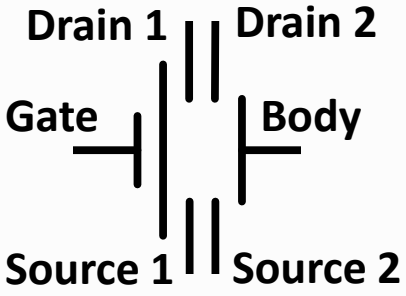
Plan-View SEM



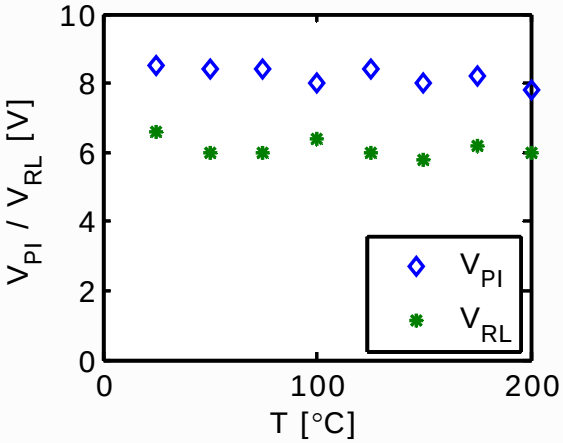
Measured I-V



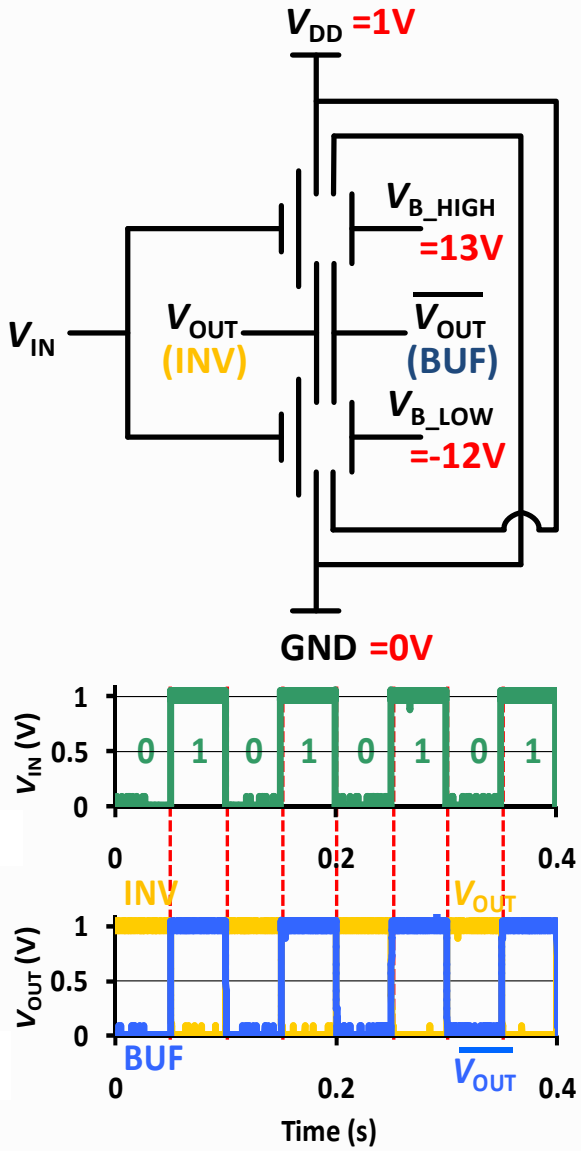
Circuit Symbol

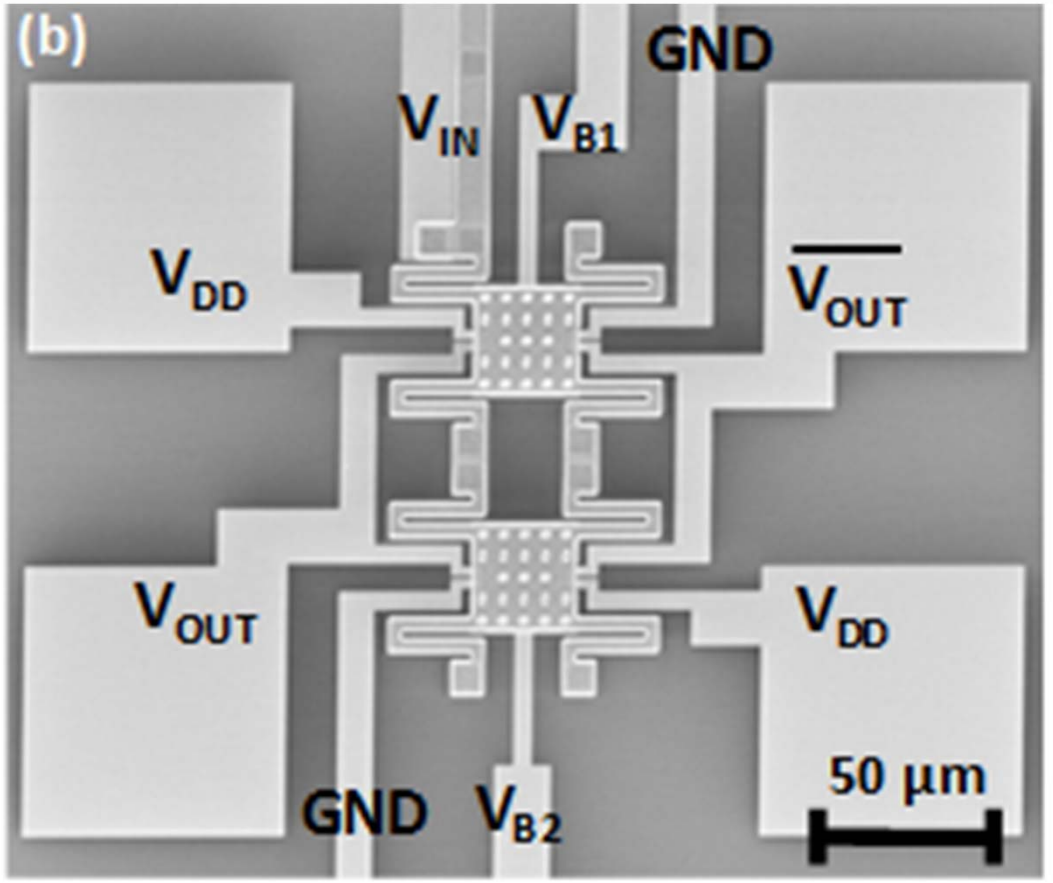


Temperature Dependence:

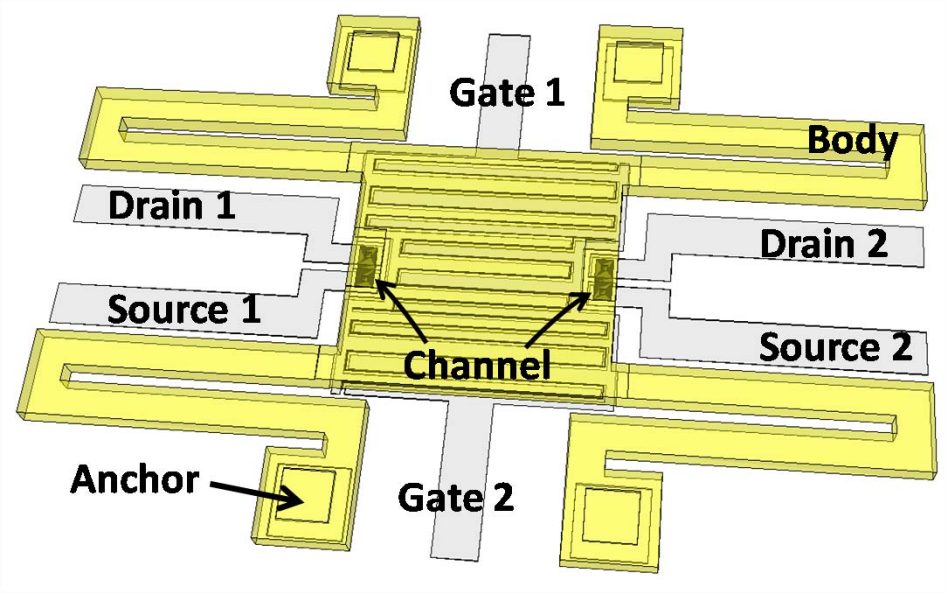


Single-Gate Relay Inverter/Buffer

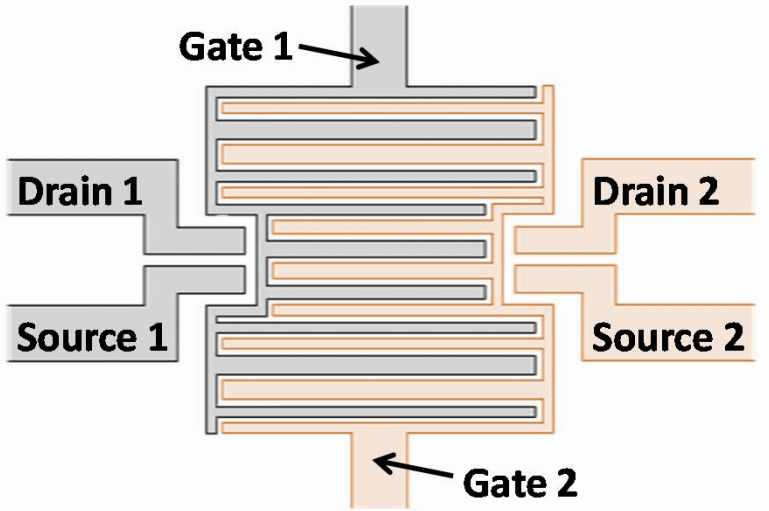




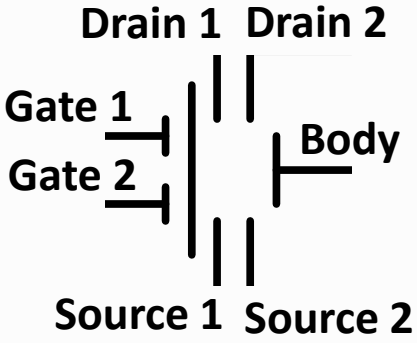
Dual-Gate, Dual Source/Drain Relay



Bottom (Gate) Electrode Layout

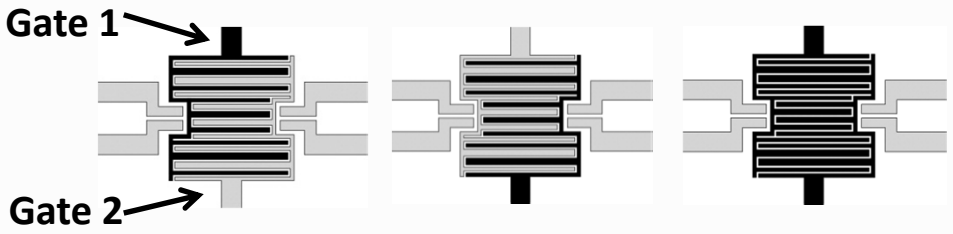


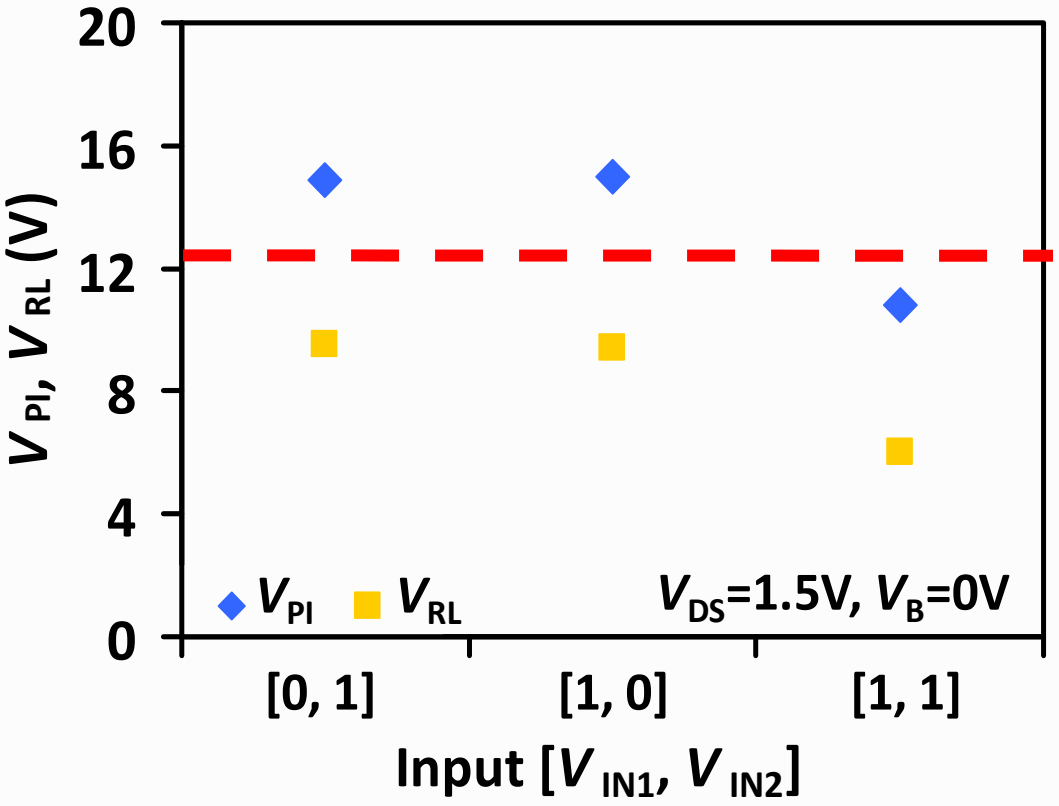
Circuit Symbol



- **Gate electrodes are interdigitated to ensure that each gate has equal influence on the movable body**

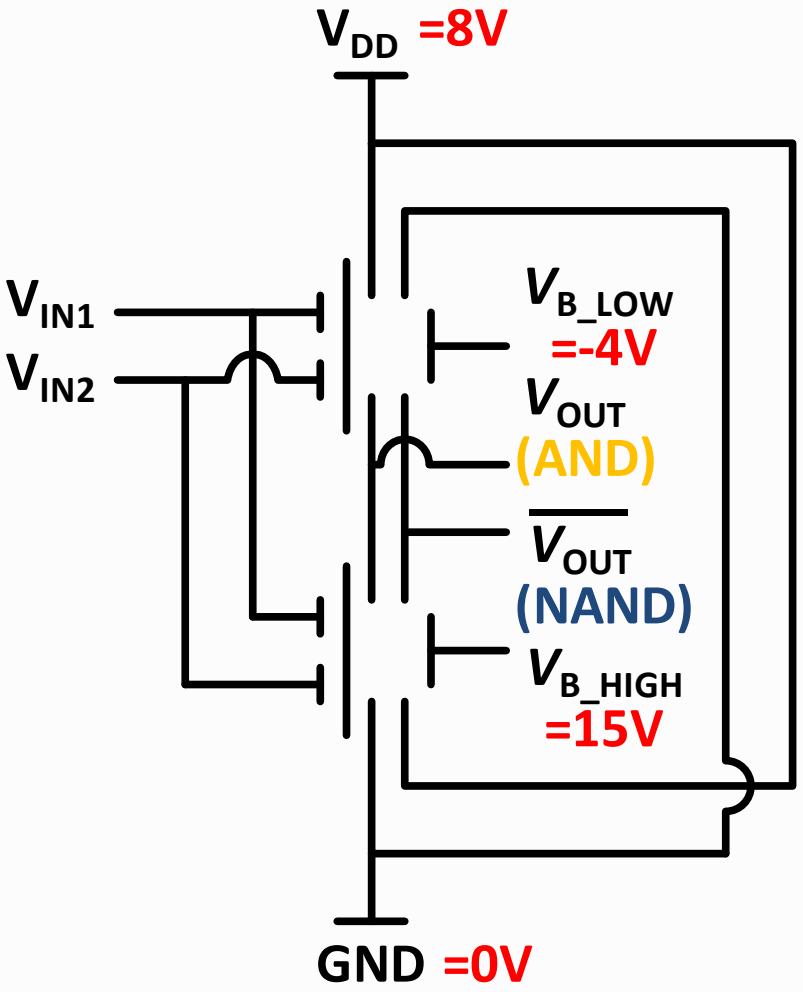
Measured V_{PI} and V_{RL} of a Dual-Gate Relay

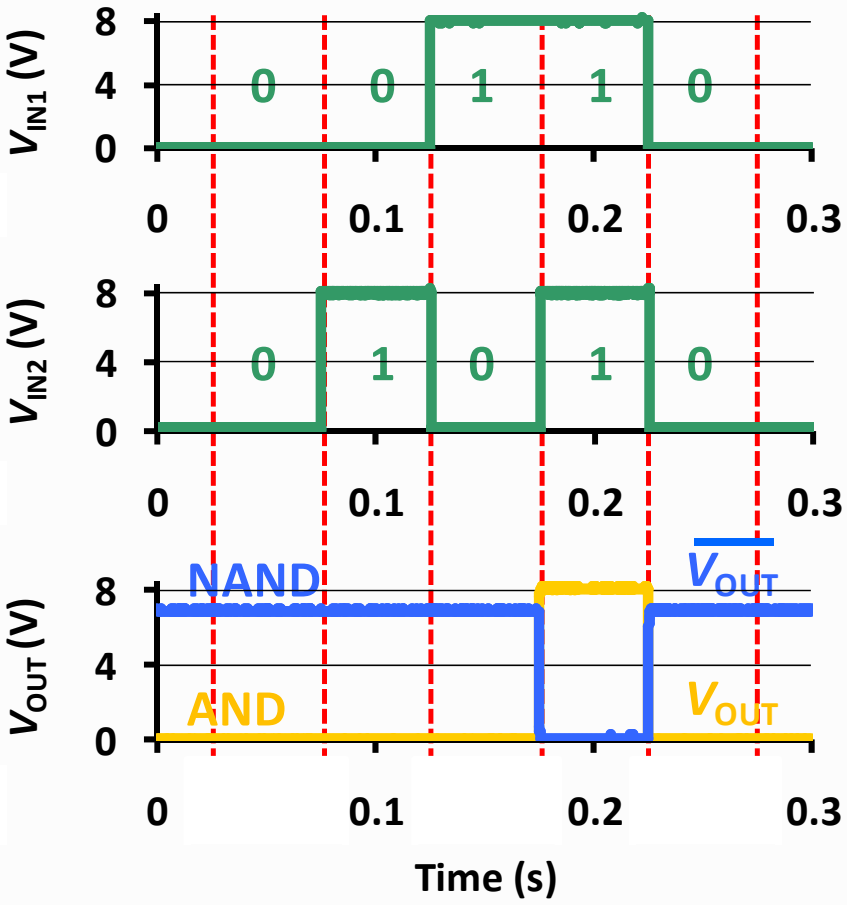




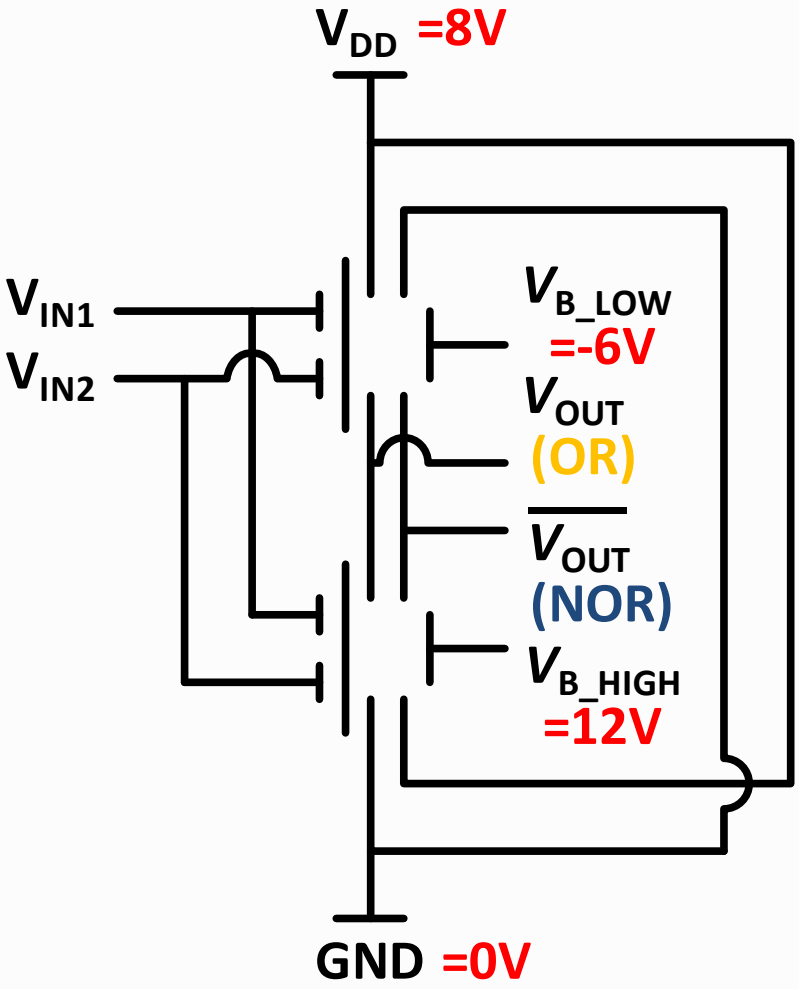
- "1"≡V_G
- Each gate has equal influence
- Depending on V_B, relay can be actuated using one or two gate electrodes

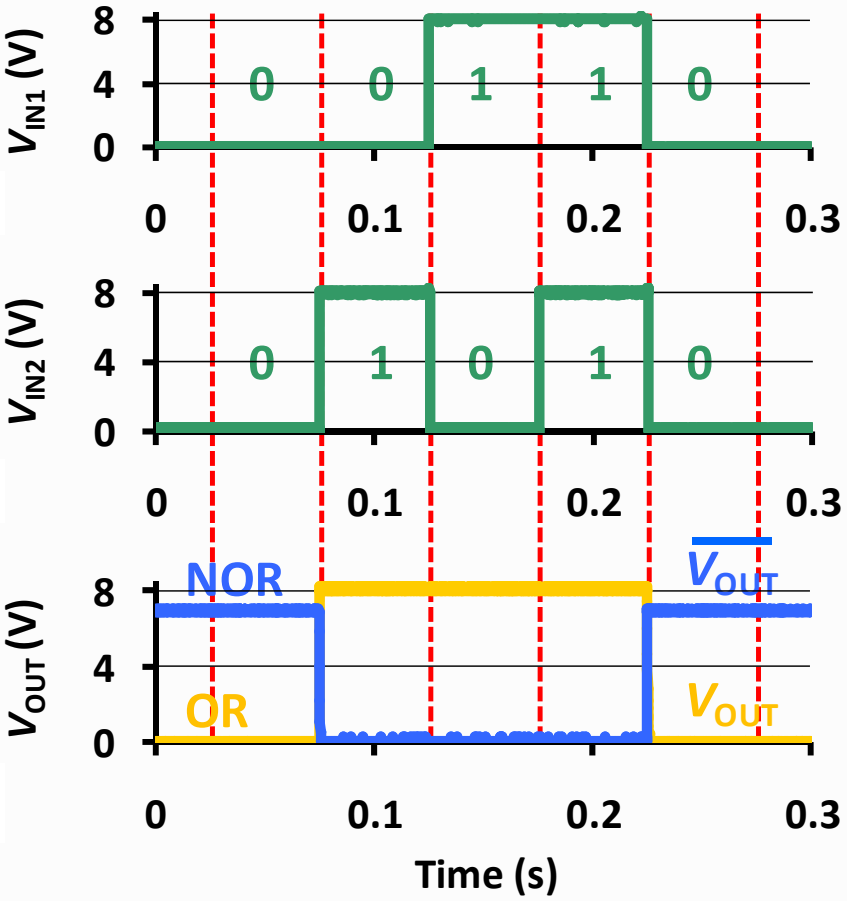
Dual-Gate Relay Circuit: AND/NAND





Dual-Gate Relay Circuit: OR/NOR

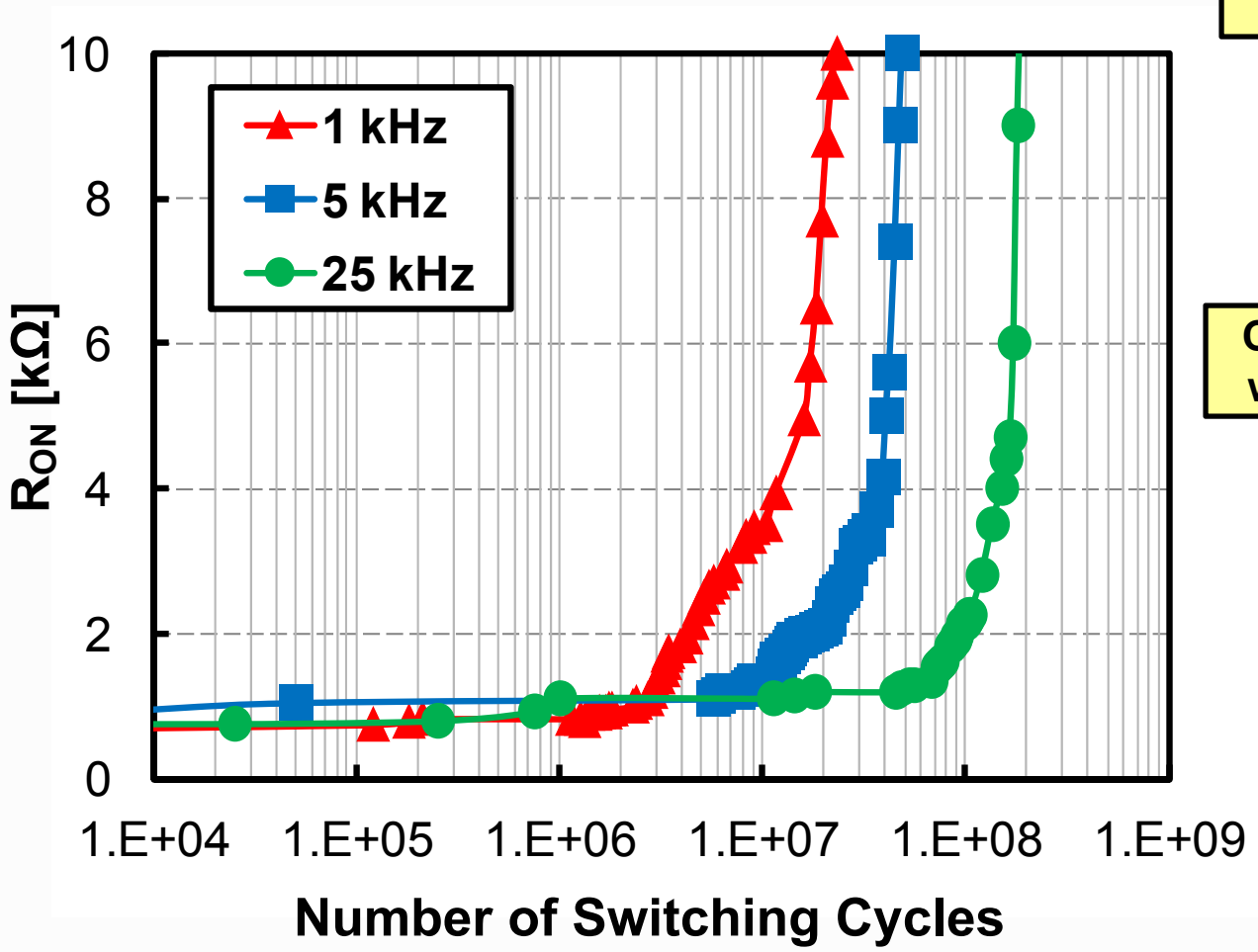




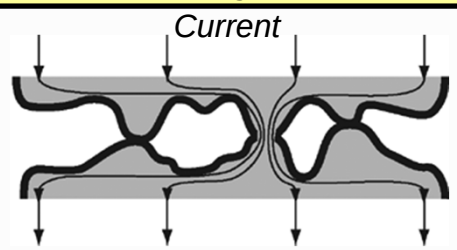
Outline

- Introduction
- Recent Progress
- **Current Challenges**
  - Contact resistance
  - Surface adhesion
- Conclusion

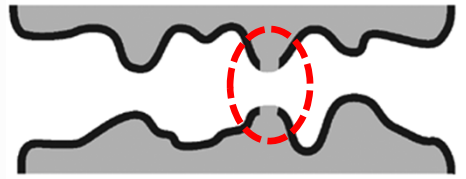
Tungsten Contact Resistance Evolution



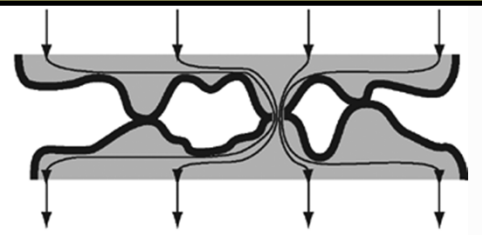
Joule heating occurs when the relay is on



Contacting surfaces oxidize when the relay is turned off



Surface oxide layers result in increased R_{ON}



Stiction: The Ultimate Relay Scaling Limiter

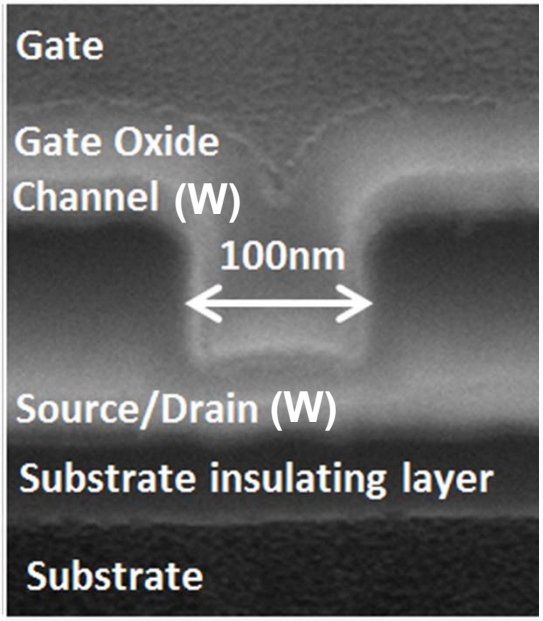
- **Hysteresis voltage (V_{PI}-V_{RL}) scales with V_{PI}:**

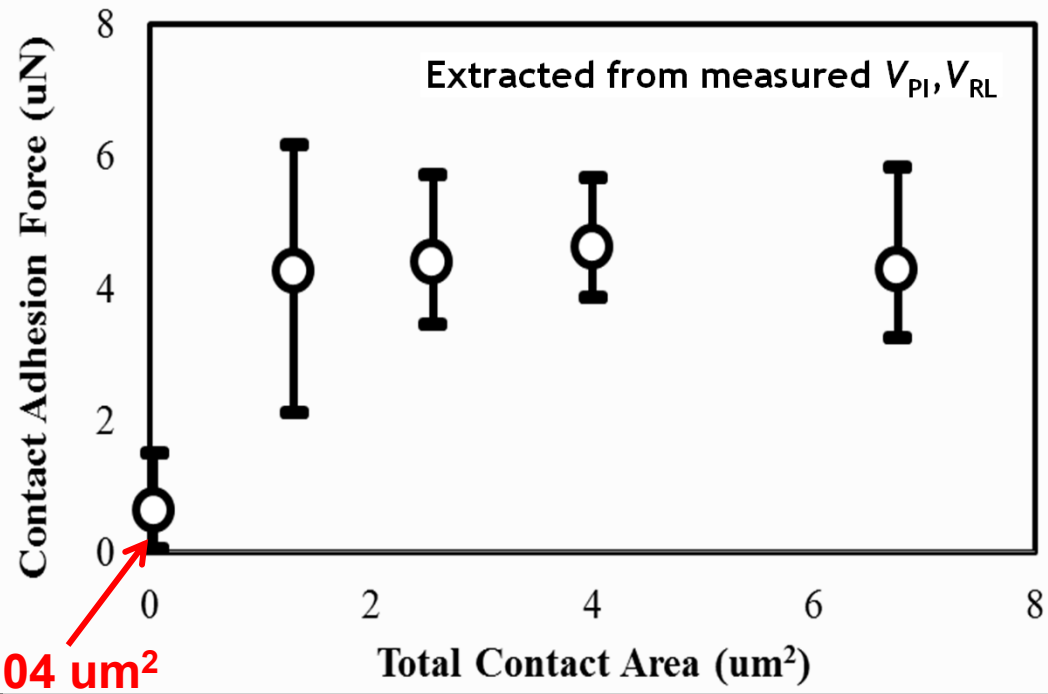
$$V_{PI} - V_{RL} = V_{PI}\left[1 - 2.6\sqrt{\frac{t_{dimple}}{t_{gap}}}\left(1 - \frac{t_{dimple}}{t_{gap}}\right)\right]$$

ignoring surface adhesion force

- **Adhesive force reduces with contacting region area:**

XSEM of Contact Dimple





Outline

- Introduction
- Recent Progress
- Current Challenges
- **Conclusion**

Conclusion

- **Relays have zero I_{OFF} and can incorporate multiple input/output electrodes**

→ **potentially can achieve lower energy per operation and greater functionality per device than CMOS for digital logic applications.**

- **Practical challenges remain to be solved:**
  - Contact surface oxidation
  - Minimization of adhesion force within R_{ON} limits
  - Development of ultra-thin structural films with very low strain gradient

Acknowledgments

- **Collaborators:**
  - Fred Chen, Hossein Fariborzi, Prof. Vladimir Stojanović (MIT)
  - Chengcheng Wang, Kevin Dwan, Prof. Dejan Marković (UCLA)
- **Funding sources:**
  - DARPA/MTO NEMS Program
  - SRC/DARPA Focus Center Research Program
  - NSF Center for Energy Efficient Electronics Science (E3S)
  - NSF Center of Integrated Nanomechanical Systems (COINS)
  - Berkeley Wireless Research Center
- **Device fabrication support:**
  - UC Berkeley Marvell Nanofabrication Laboratory
  - SVTC Technologies & SPTS Technologies