Electronics Proliferation through Diversification

of Solid-State Devices and Materials

Prof. Tsu-Jae King Liu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720

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The Information Age

The Semiconductor Market*:

Computers
42%

Industrial
8%

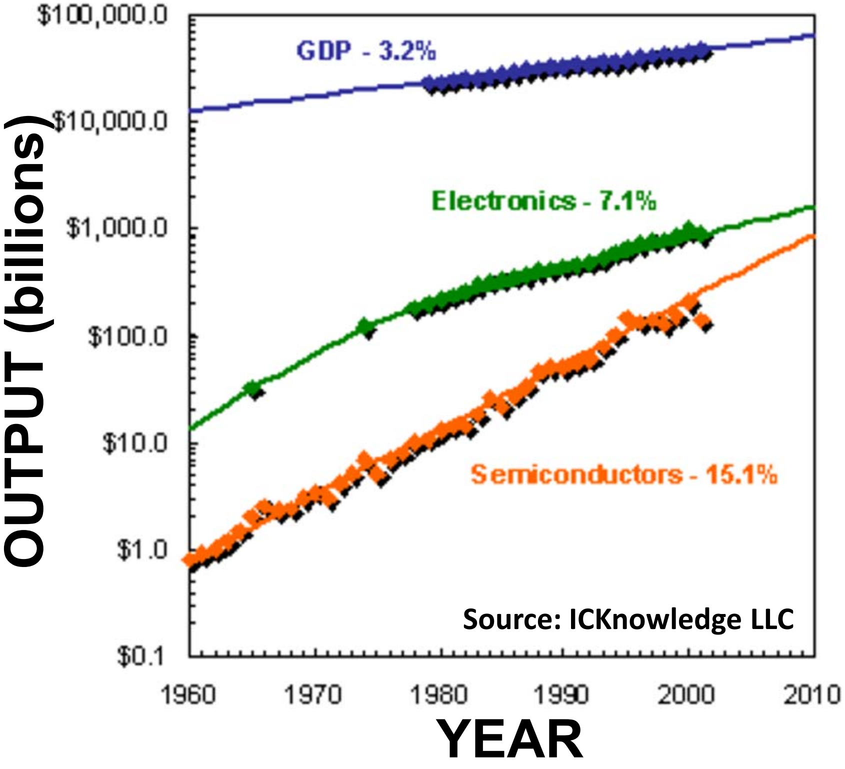
Communications
24%

Transportation
8%

Consumer Electronics
16%

Military
2%

- **IC technology advancement over the past 40+ years has had dramatic impact on the way we live, work, and play.**

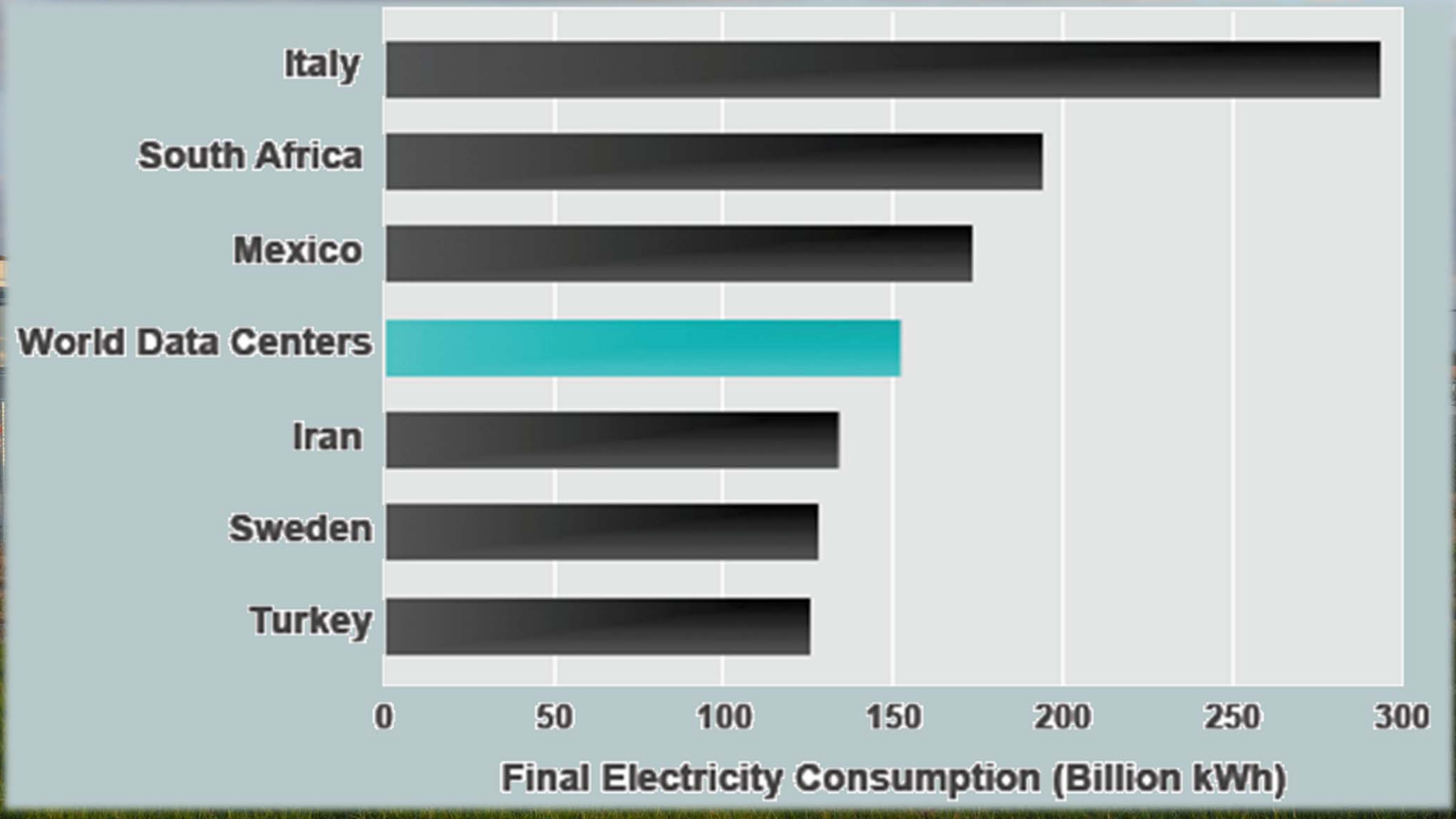


Source: ICKnowledge LLC

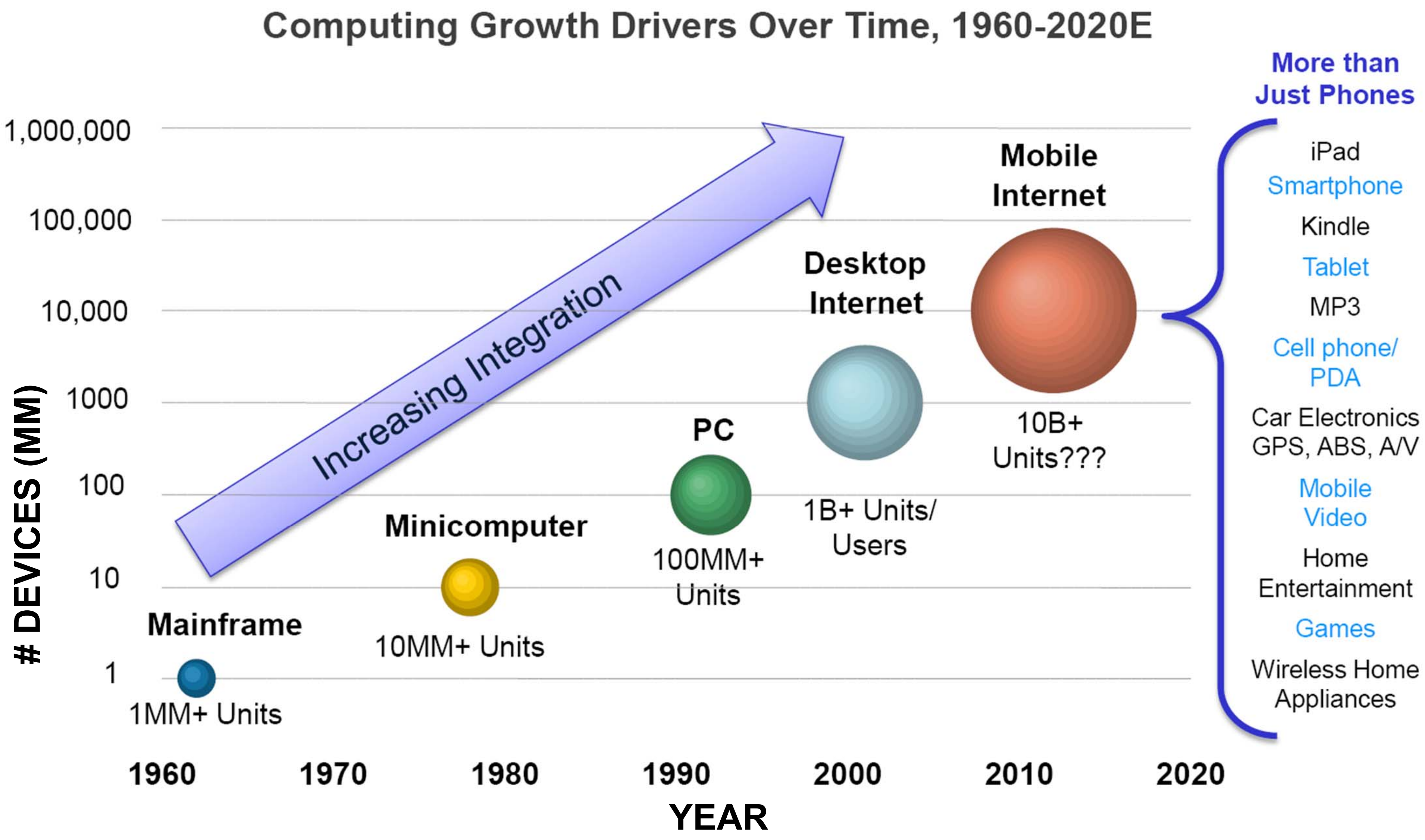
*Source: IC Insights – Market Drivers 2008

Data center electricity use increased from 0.5% of world total in 2000 to 1% of world total in 2005

Source: J. Koomey (LBNL), 2008



Better processing power + Smaller form factor + Lower prices → more units

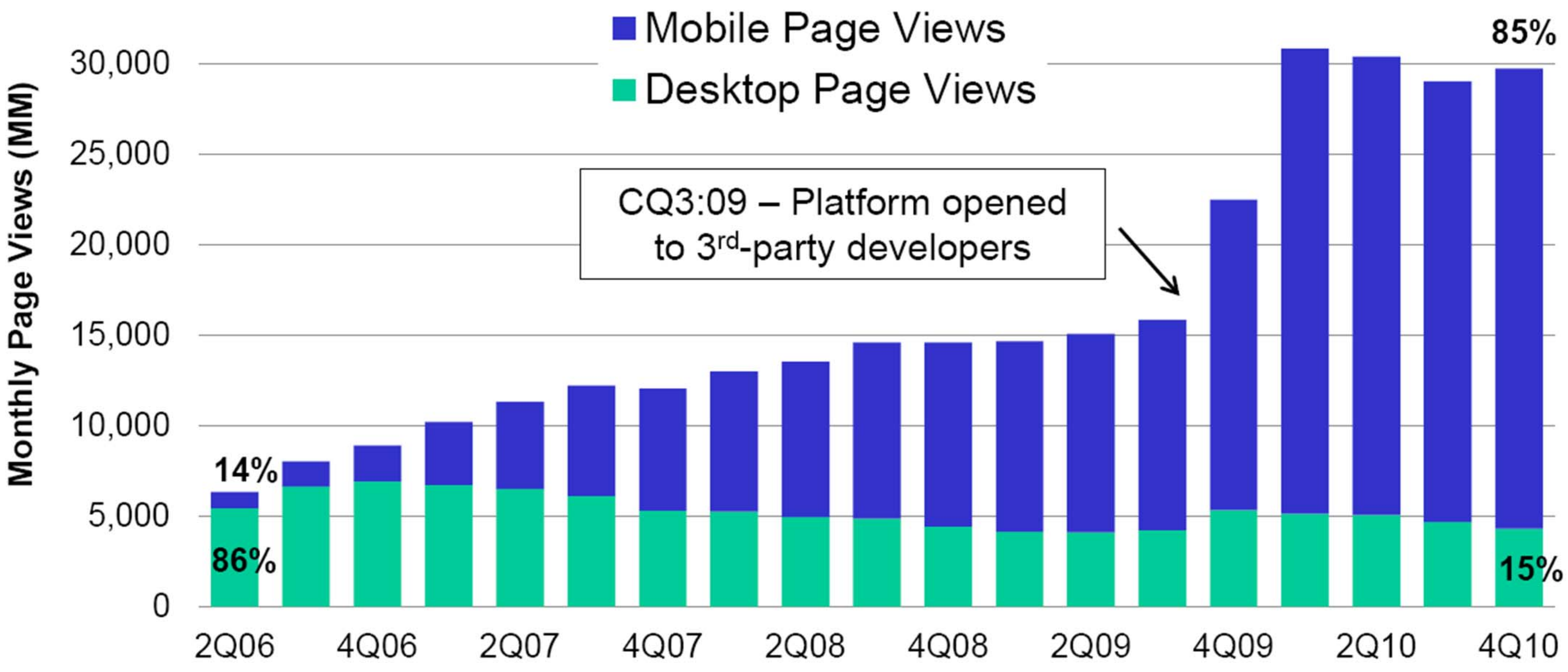


Source: ITU, Mark Lipacis, Morgan Stanley Research

http://www.morganstanley.com/institutional/techresearch/pdfs/2SETUP_12142009_RI.pdf

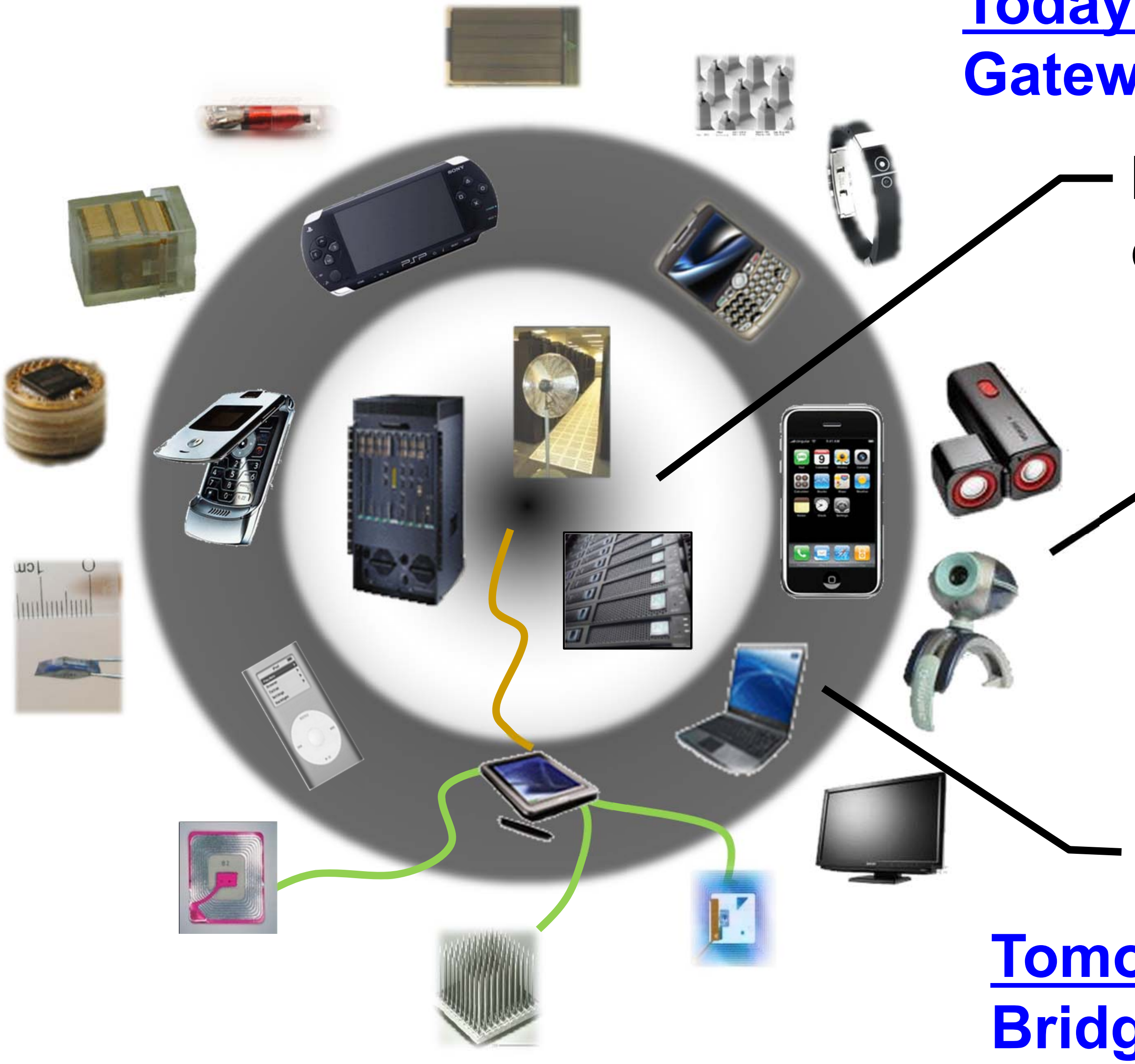
Shift to Mobile Usage

Mixi's (Japan's Leading Social Network) Monthly Page Views, Mobile vs. PC, CQ2:06-CQ4:10



Note: Mixi is one of Japan's leading social networking sites on PC and mobile with 20MM registered users as of 12/31/10. It monetizes mobile usage via sales of avatars, customized homepages and other premium services.
Source: Company reports, Naoshi Nema, Morgan Stanley Research

Vision for 2020: Swarms of Electronics



Today's Mobile:
Gateway to the Cloud

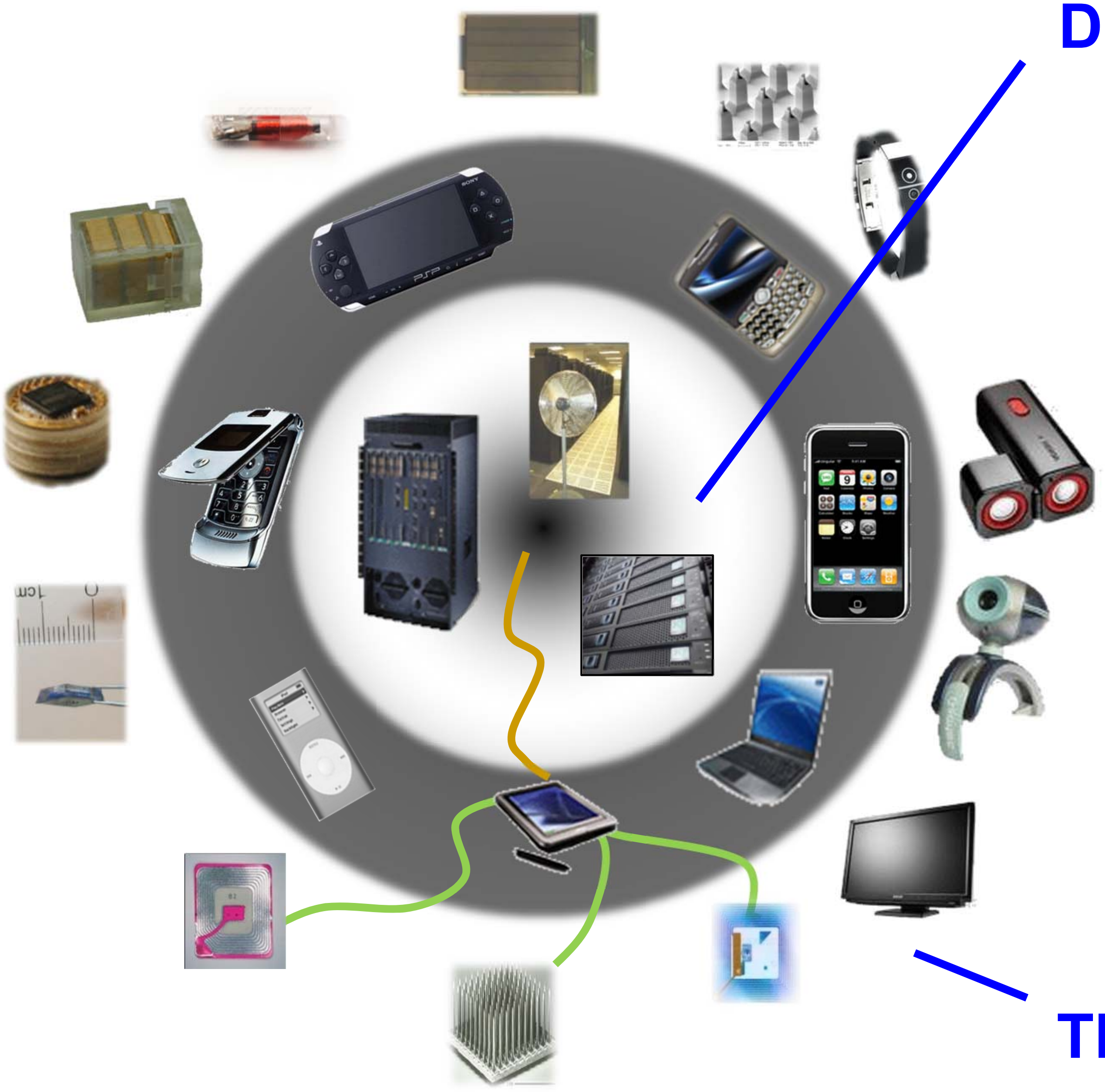
Infrastructructional core

Sensory swarm
(trillions of devices)

Mobile access

Tomorrow's Mobile:
Bridge to the Swarm

Technology Drivers



Driver for More of Moore's Law

Still need >10x reductions in energy, size, cost…

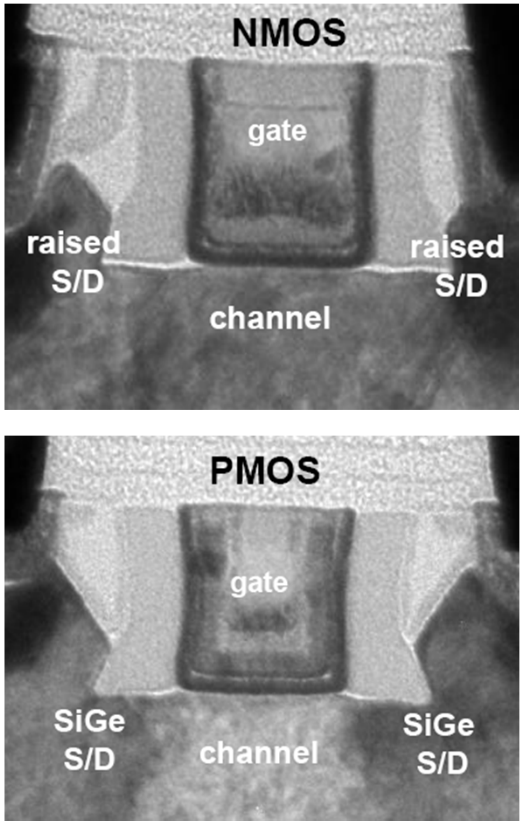
Driver for More Than Moore's Law"

Diversification for More of Moore's Law

- MOSFET structures
- MOSFET gate-stack materials
- Alternative switch designs
  - Tunnel FET
  - Mechanical switch
- III-V MOSFETs

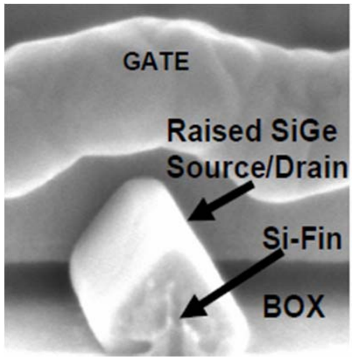
Improving MOSFET Scalability

32 nm
planar

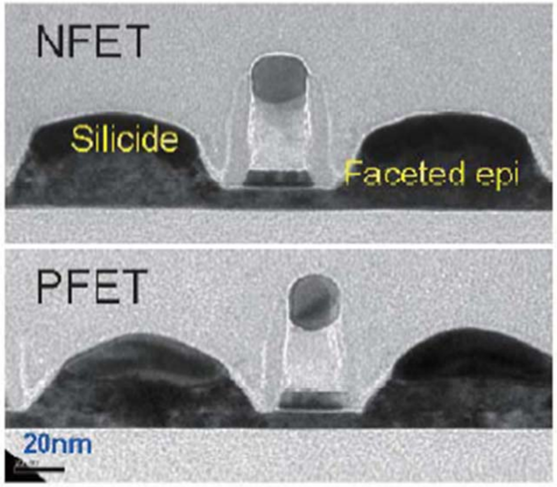


P. Packan *et al.*, *IEDM* 2009

22 nm
thin-body

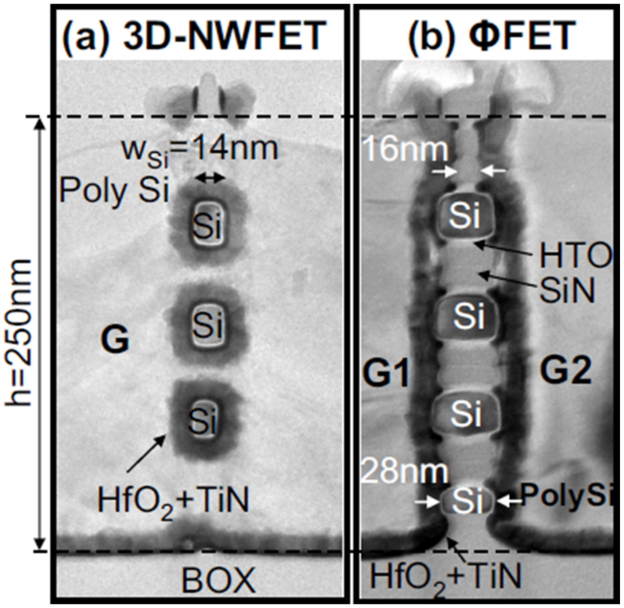


J. Kavalieros *et al.*, *VLSI* 2006



K. Cheng *et al.*, *VLSI* 2009

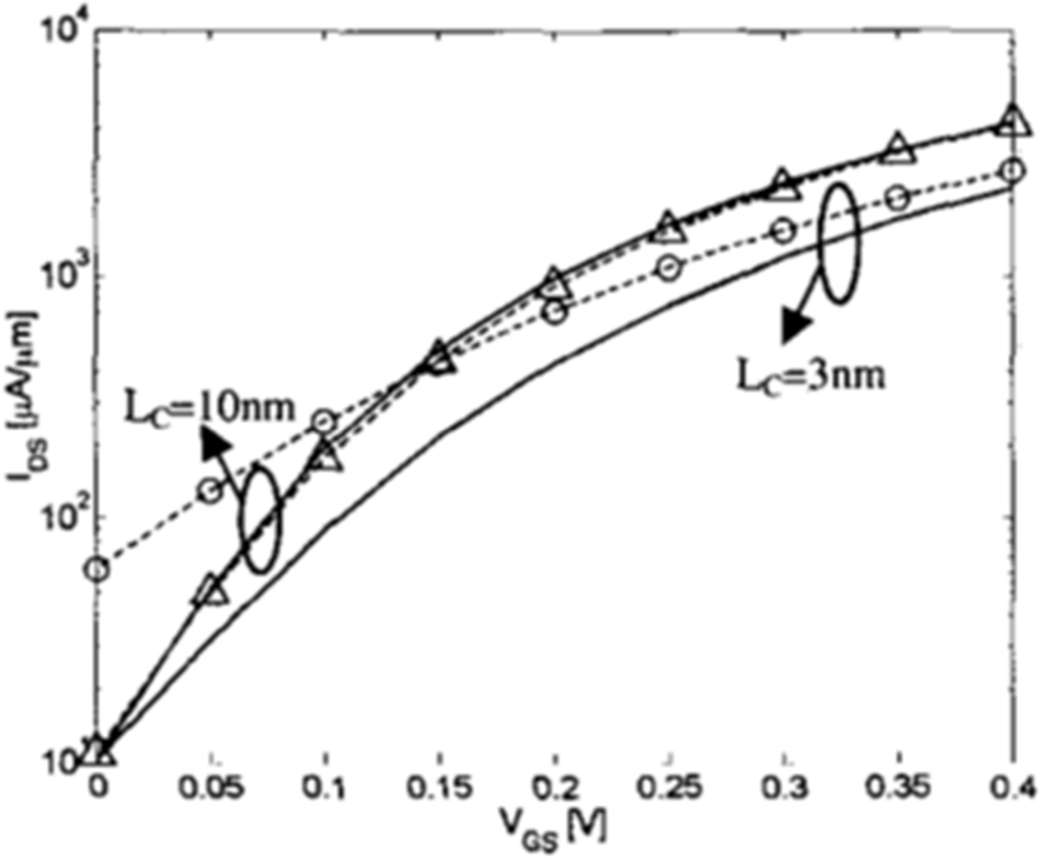
beyond 10 nm
nanowires?



C. Dupré *et al.*, *IEDM* 2008

Channel-Length Scaling Limit

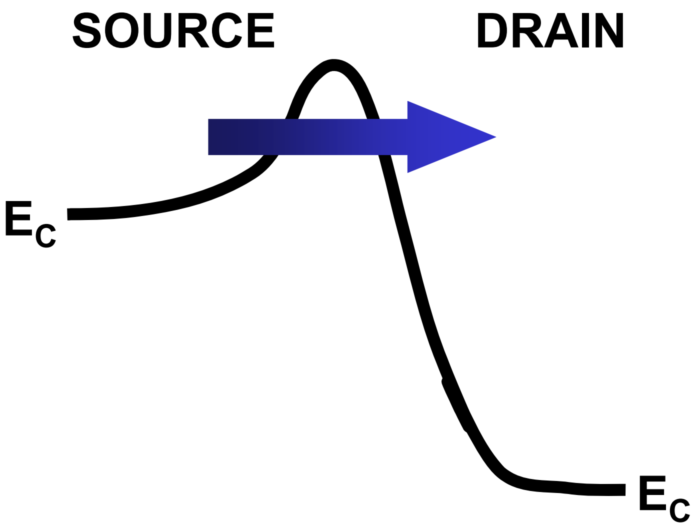
- **Quantum mechanical tunneling sets a fundamental scaling limit for the channel length (L_C).**



J. Wang *et al.*, *IEDM Technical Digest*, pp. 707-710, 2002

If electrons can easily tunnel through the source potential barrier, the gate cannot shut off the transistor.

<u>nMOSFET Energy Band Diagram</u>
(OFF state)

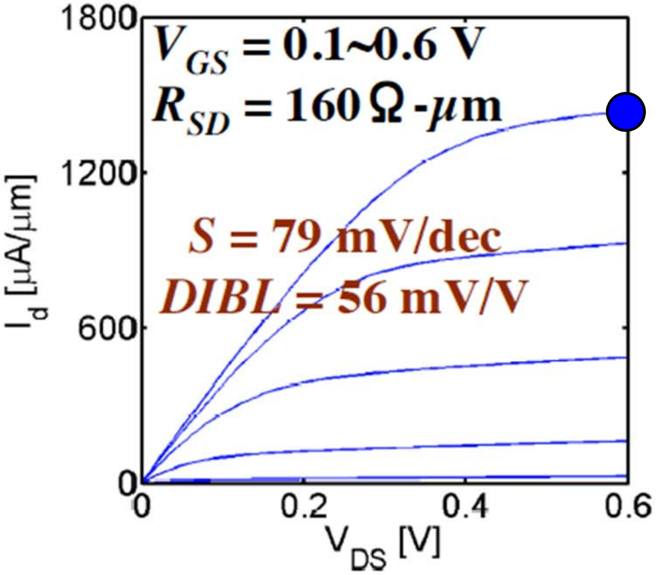


Ultimately Scaled MOSFET

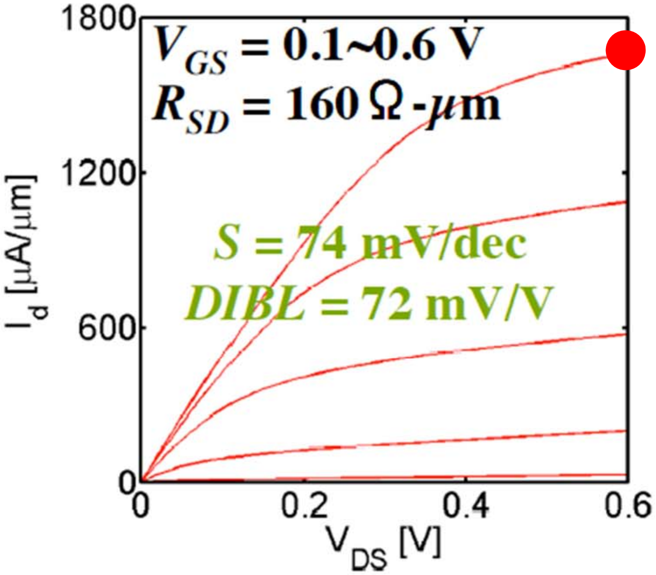
Double-Gate Ballistic MOSFETs

L_C = 8 nm, EOT = 0.45 nm

$In_{0.75}Ga_{0.25}As$



s-Si



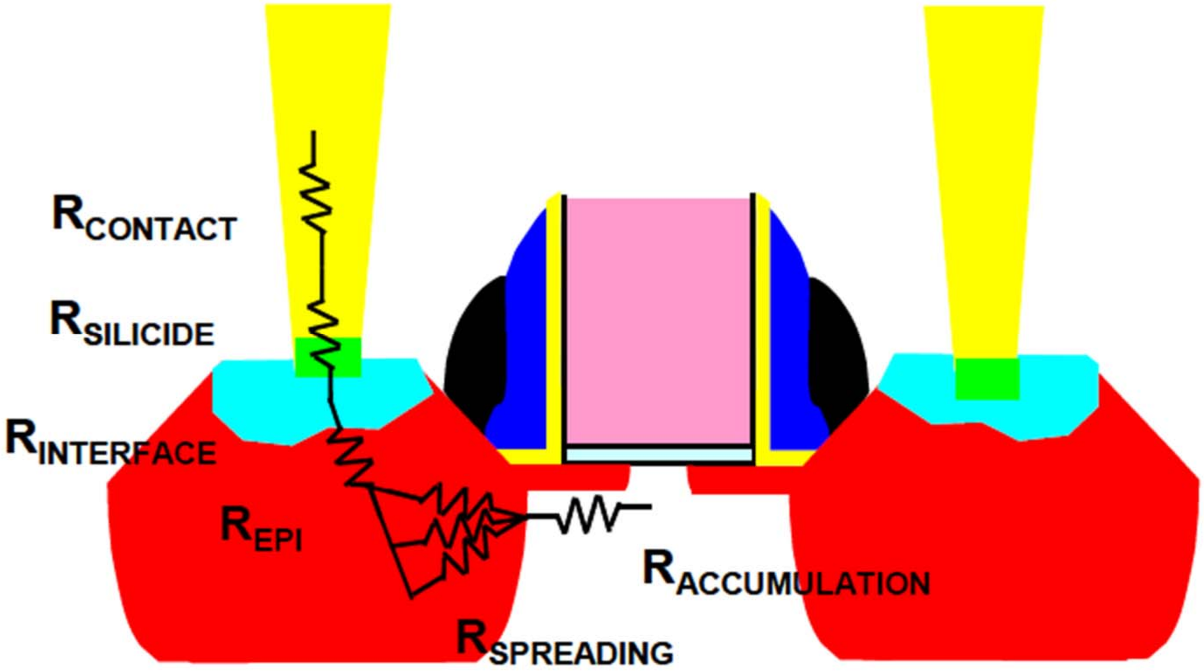
	τ_{unload} (ps)	τ_{load} (ps)
InGaAs	**0.05**	**0.93**
s-Si	**0.12**	**0.82**

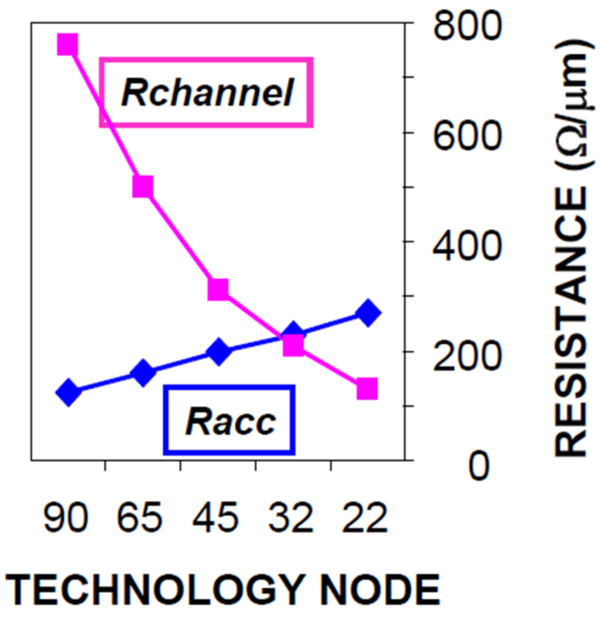
⇨ **Ballistic Si MOSFET**

(L_C < 10 nm)

K. Cantley *et al.*, *IEDM Technical Digest*, pp. 113-116, 2007

Reducing Parasitic Resistance

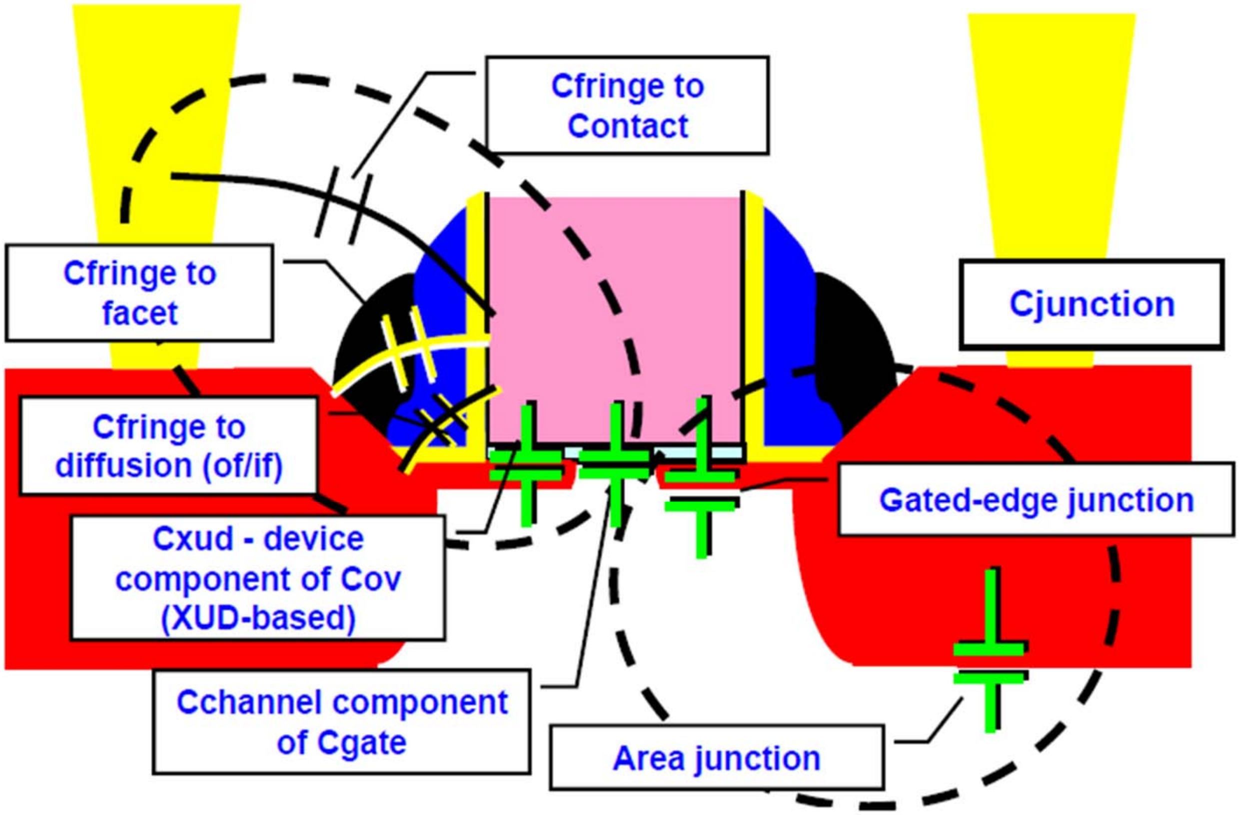




A. M. Noori *et al*.,
IEEE Trans. Electron Devices
pp. 1259-1264, 2008

- **Advanced anneal techniques**
- **Low Schottky barrier height contacts**
  - **alloy and implant approaches, dual silicide…**

Reducing Parasitic Capacitance



Cfringe to Contact

Cfringe to facet

Cfringe to diffusion (of/if)

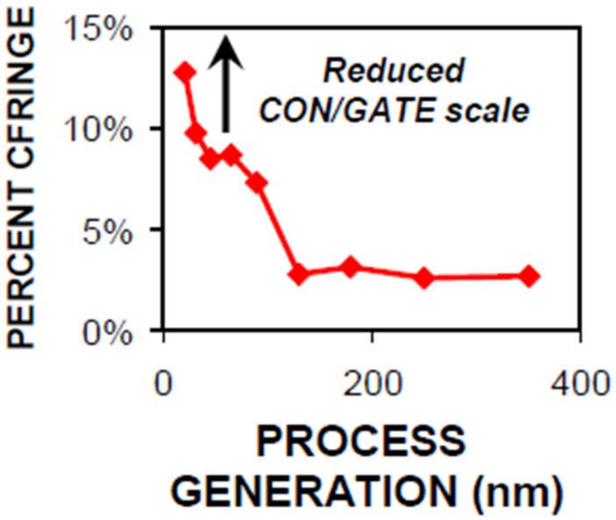
Cxud - device component of Cov (XUD-based)

Cchannel component of Cgate

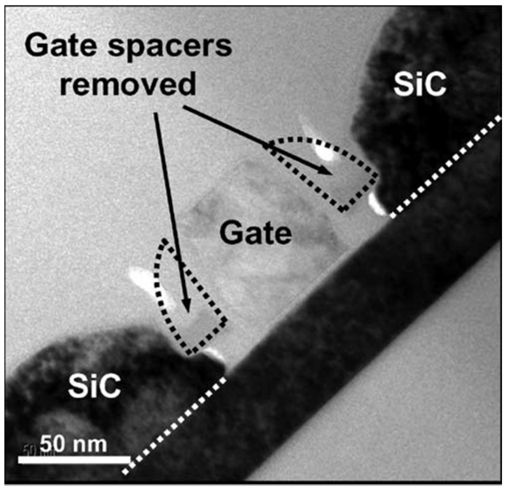
Area junction

Cjunction

Gated-edge junction

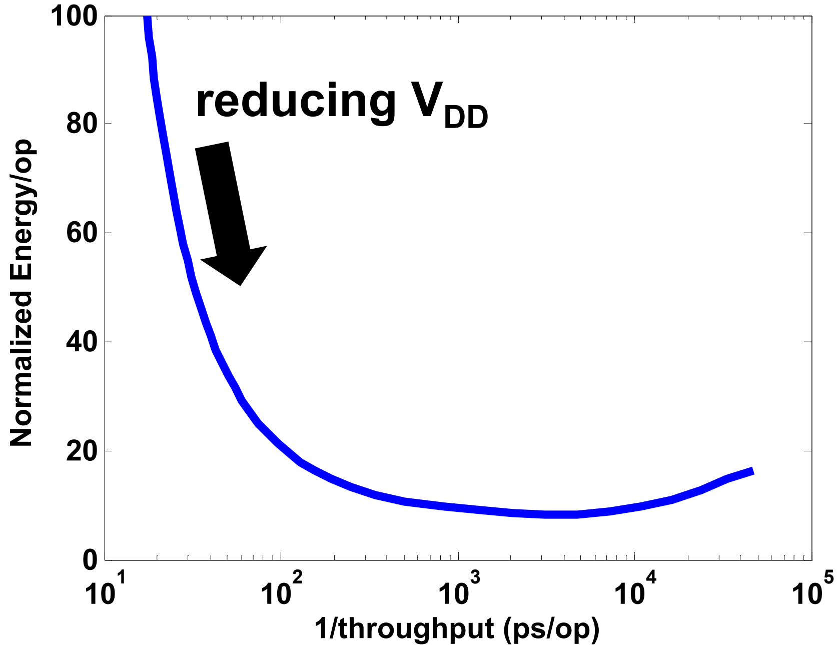


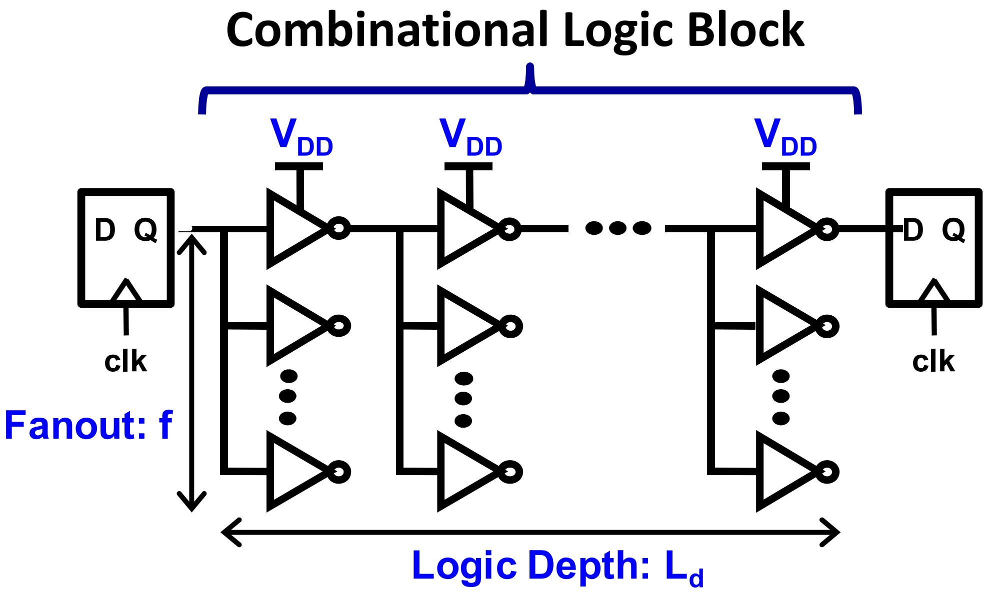
Low-k or air spacers



T.-Y. Liow *et al.*, *IEEE Electron Device Letters* pp. 80-82, 2008

CMOS Energy-Efficiency Limit





$$E_{total} = \overbrace{\alpha L_d f C V_{DD}^2}^{\text{Active Energy}}[1 + \overbrace{(L_d f/2\alpha)(I_{OFF}/I_{ON})}^{\text{Passive Energy}}]$$

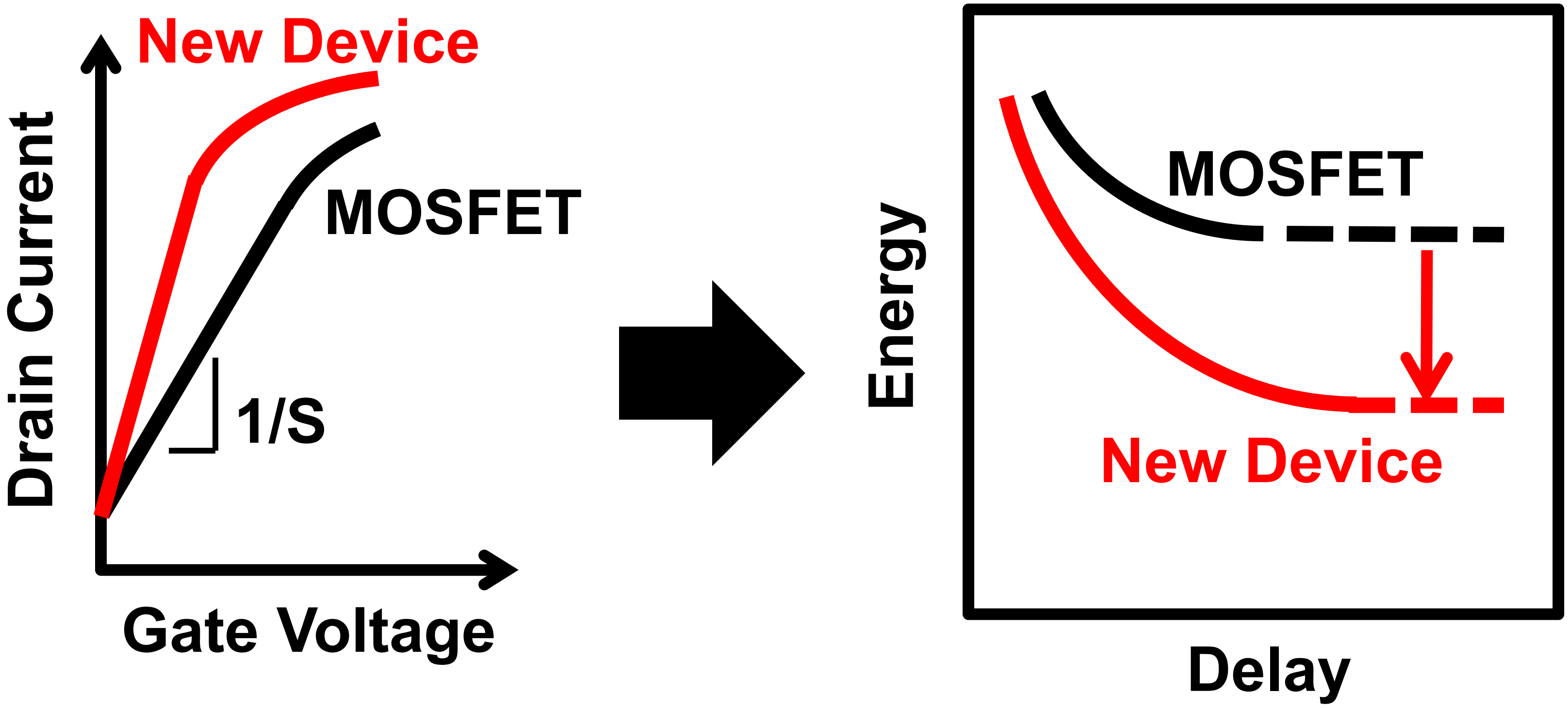
$$t_{delay} = L_d f C V_{DD} / (2I_{ON})$$

- A lower limit in E/op exists due to transistor OFF-state leakage.
  - optimal $I_{ON}/I_{OFF} \propto L_d f/\alpha$

α: Activity Factor L_d: Logic Depth f: Fanout C: Capacitance per Stage

B. Calhoun *et al.*, *IEEE J. Solid State Circuits*, Vol. 50, pp. 1778-1786, 2005

MOSFET-Replacement Devices



- Higher I_{ON}/I_{OFF} ratio → lower minimum Energy/op

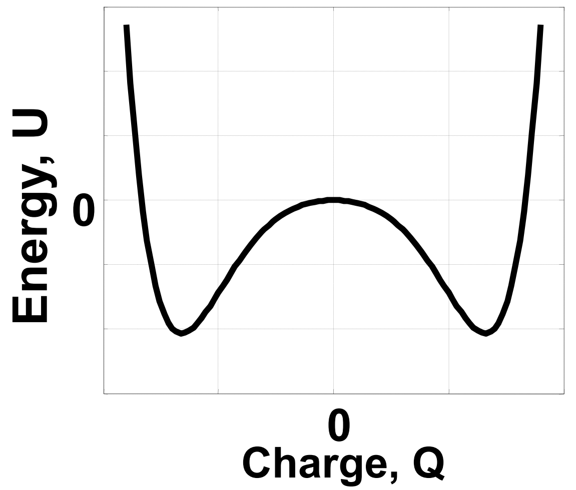
→ New device with steeper switching behavior needed (S < 60mV/dec)

Diversification for More of Moore's Law

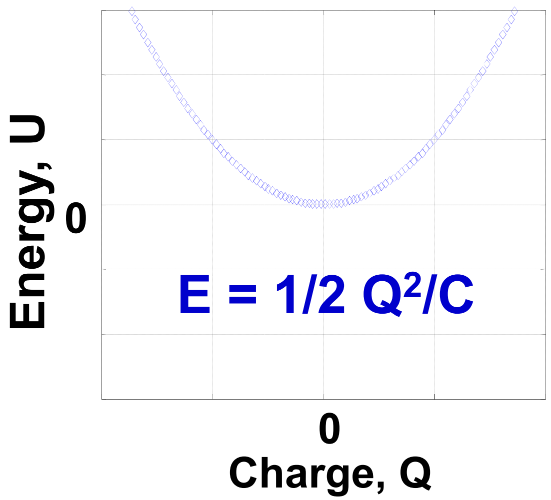
- MOSFET structures
- MOSFET gate-stack materials
- Alternative switch designs
  - Tunnel FET
  - Mechanical switch
- III-V MOSFETs

Advanced Gate Stack Materials for Giant Capacitance

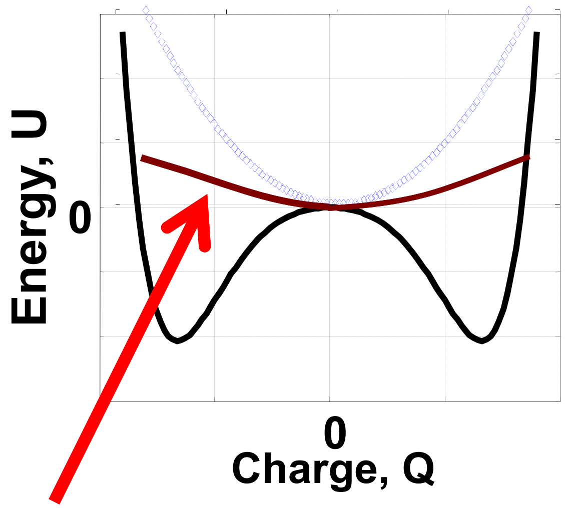
Ferroelectric



Dielectric



Ferroelectric + Dielectric



Resultant Capacitance > C

S. Salahuddin *et al.*, *Nanoletters* 2008 and *IEDM* 2008 17

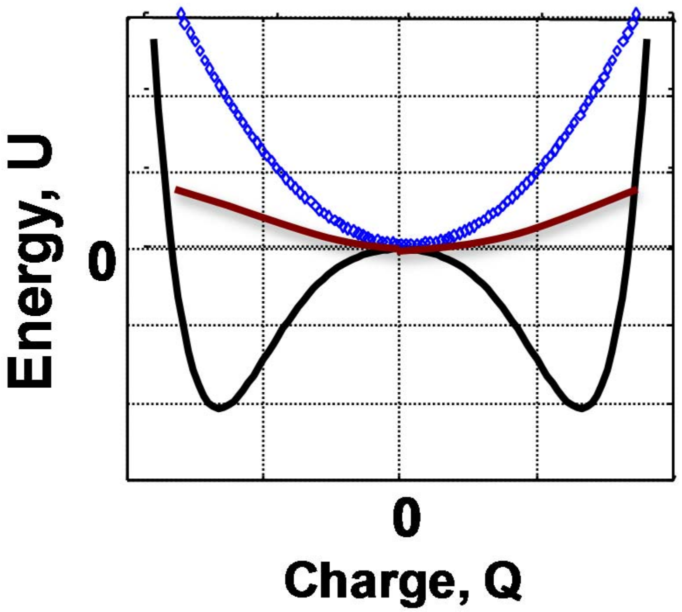
Sub-60 mV/dec MOSFET

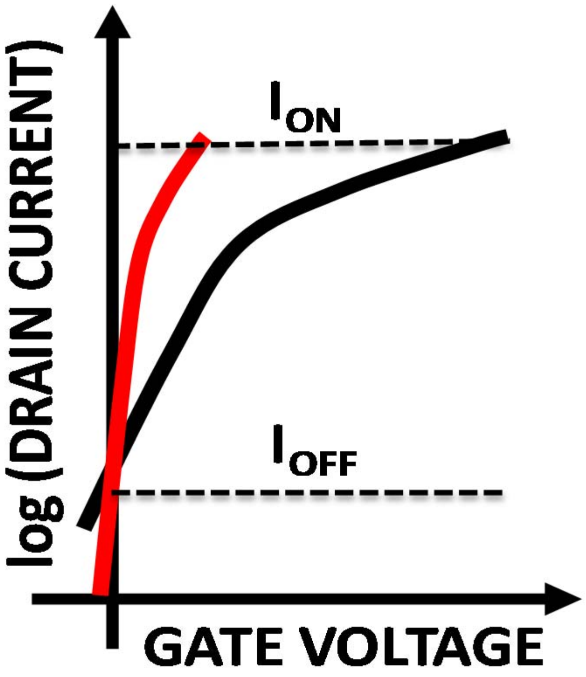
There is no limit to the amount of charge for very little energy.

Depends only on the energy slopes

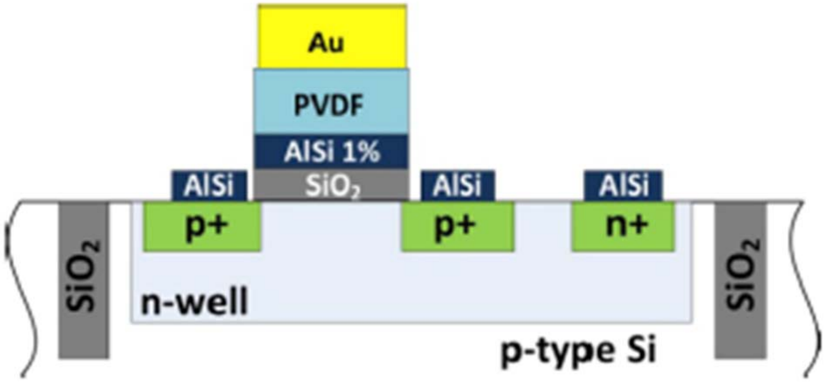
⇨

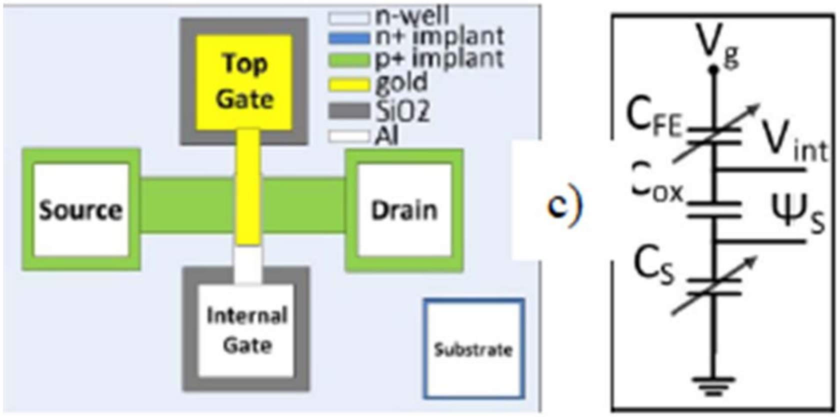
There is no minimum gate voltage for the required current.





"Negative Capacitance" FET



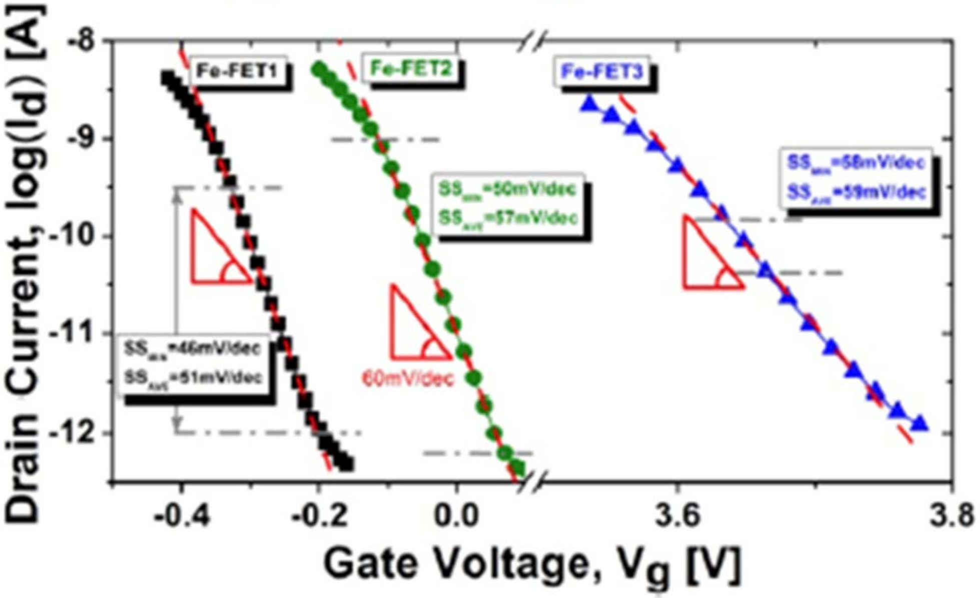


Subthreshold swing:

$$S \equiv \frac{\partial V_g}{\partial(\log_{10} I)} = \underbrace{\frac{\partial V_g}{\partial \psi_s}}_{\equiv m} \frac{\partial \psi_s}{\partial(\log_{10} I)}$$

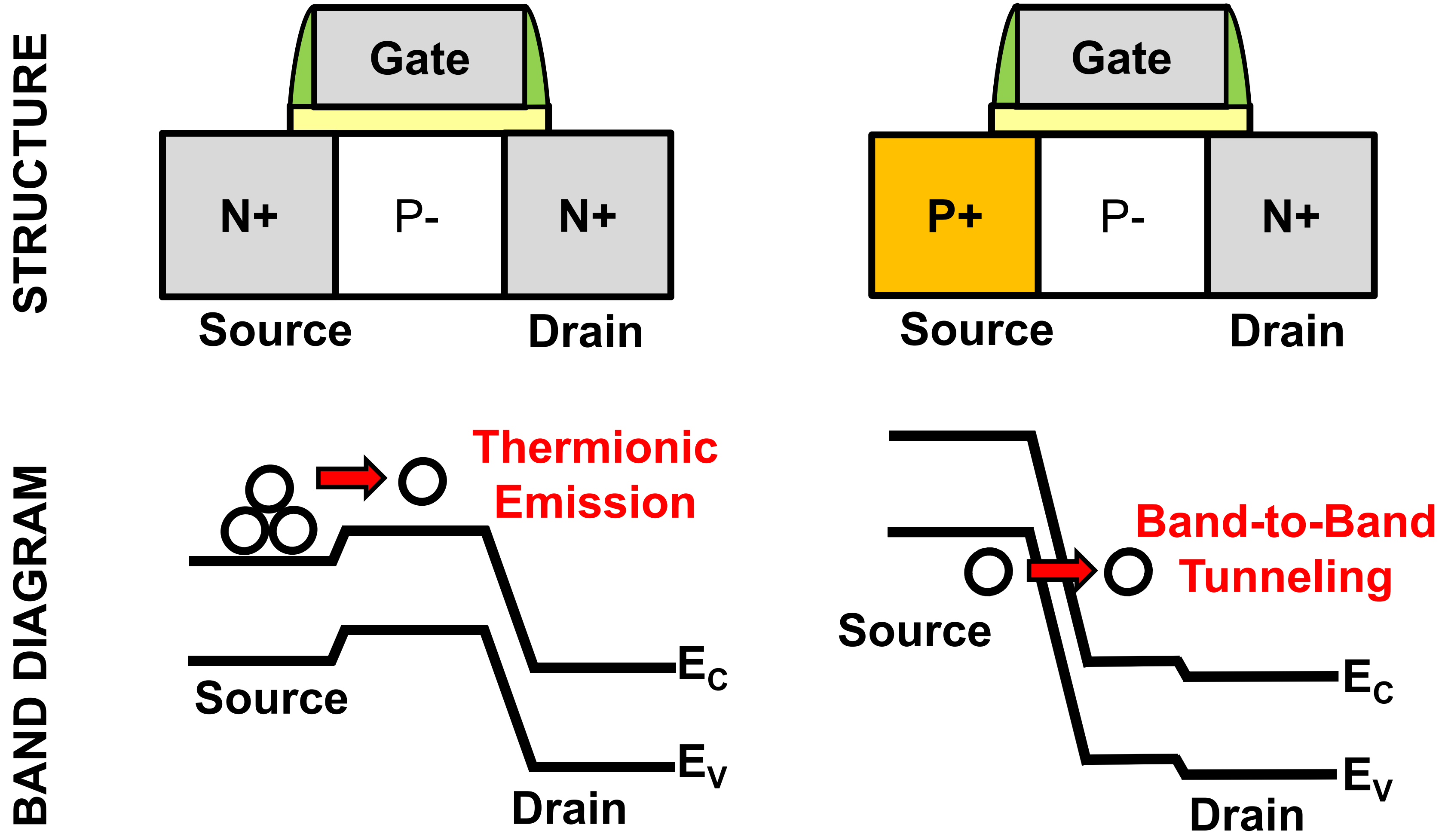
Body factor:

$$\frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_s}{C_{ins}}$$ **< 1 if C_{ins} < 0**



A. Rusu *et al.*, *IEDM* 2010

MOSFET *vs.* Tunnel FET

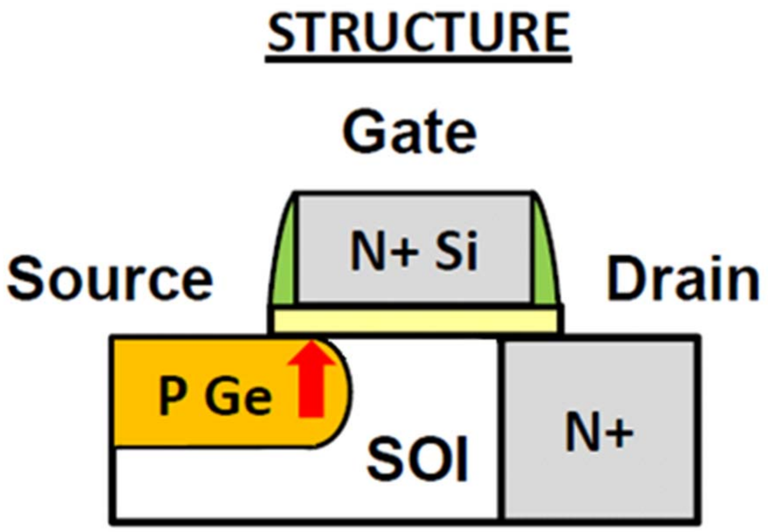


$I_D \propto \exp(qV_{GS}/nkT)$

$I_D = AE_S\exp(-B/E_S)$

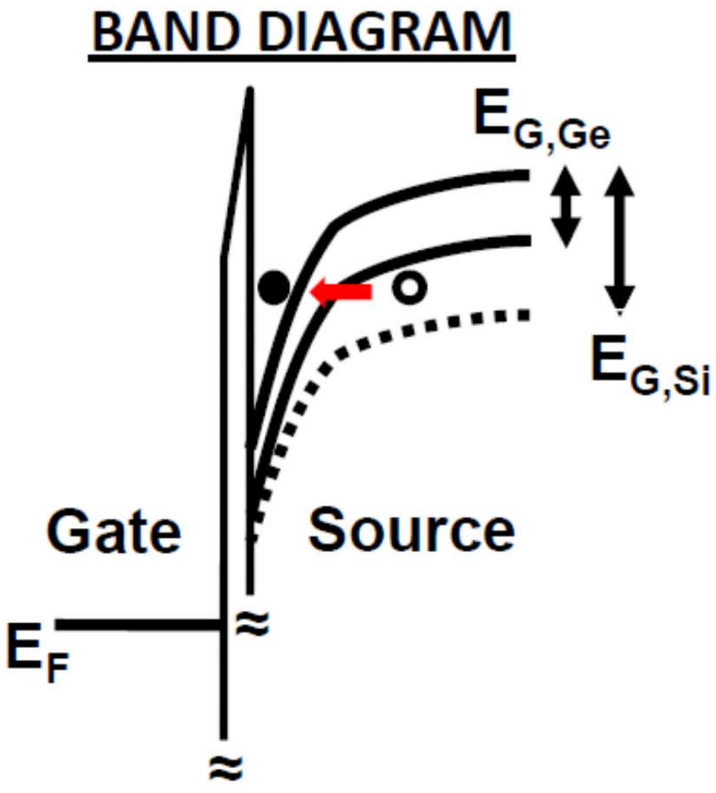
(E_S = electric field)

Ge-Source Tunnel FET



$I_D = AE_S\exp(-B/E_S)$

$A \propto (m^*/E_G)^{0.5}$ $B \propto (m^*E_G^{3})^{0.5}$



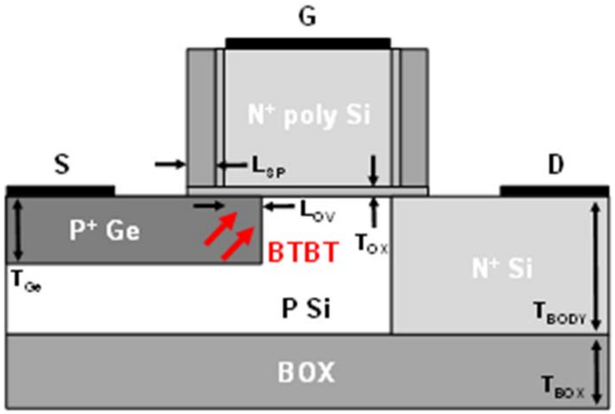
- **Tunneling occurs in the source (Ge) region**

small bandgap: E_G = 0.66eV; small effective mass: m^* = 0.06m$_o$

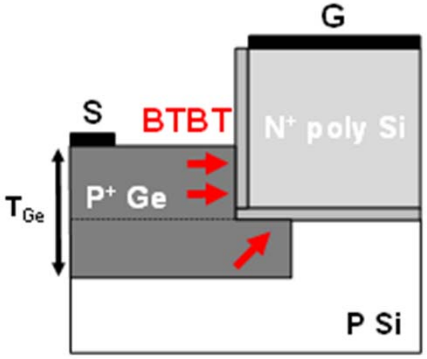
S. H. Kim *et al.*, *Symp. VLSI Technology* 2008

Ge-Source Structure Optimization

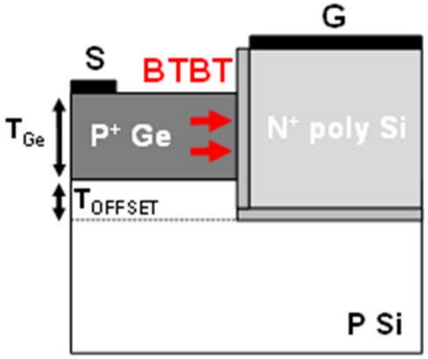
Planar Source:



Partially Elevated Source:



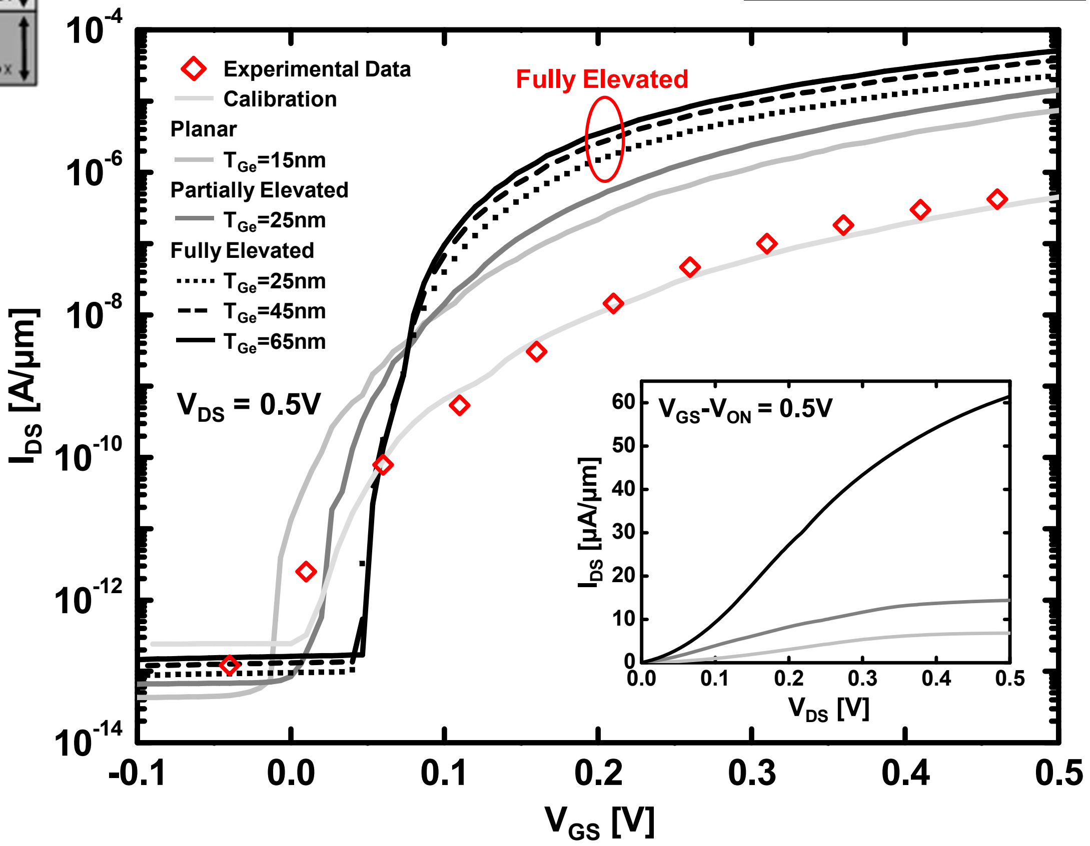
Fully Elevated Source:



I_{ON}/I_{OFF} ↑ by

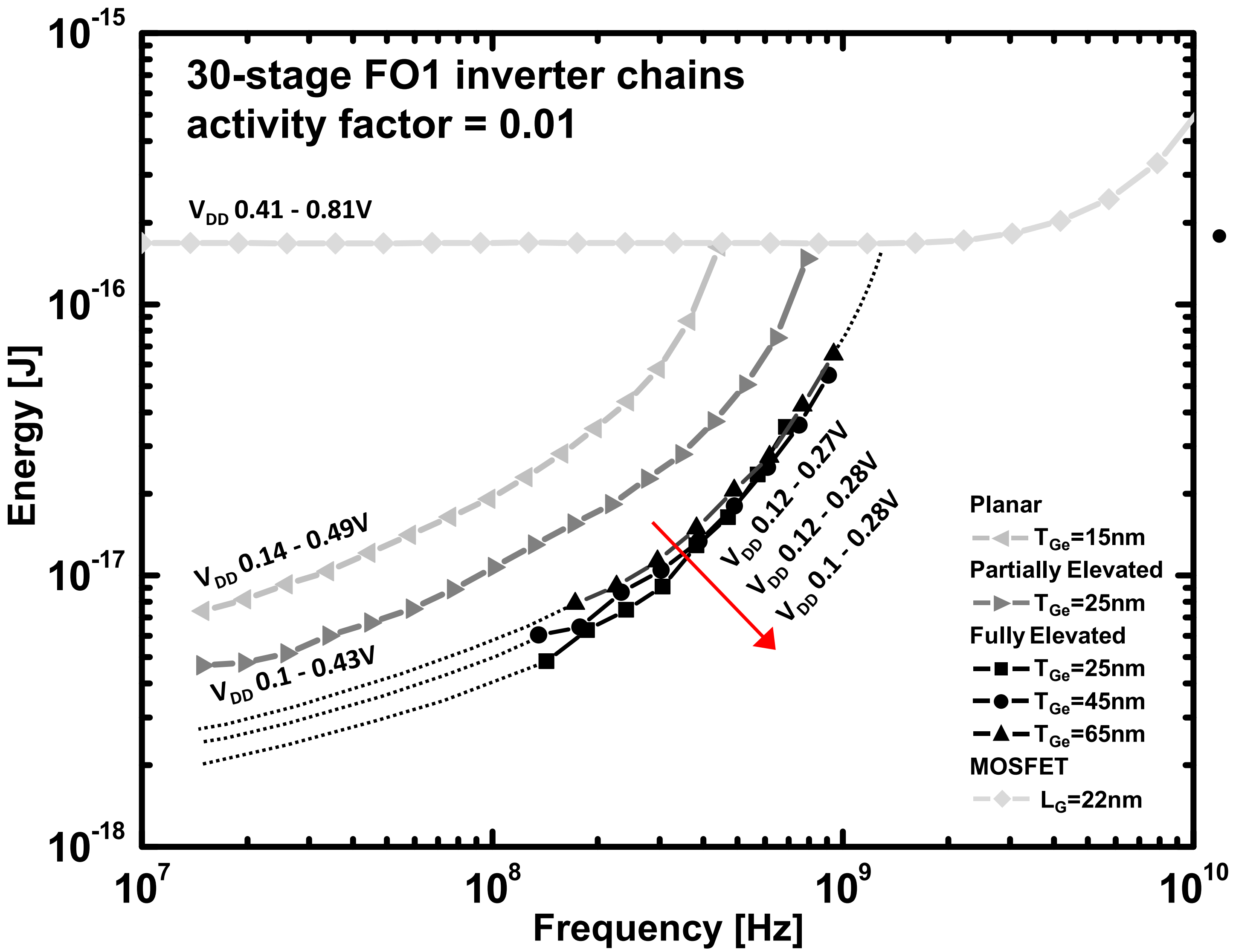
- optimizing Ge & Si thickness and doping
- elevating source

Parameter	Value
L_G	30 nm
T_{OX} (EOT)	1 nm
T_{BODY}	100 nm
T_{OFFSET}	5 nm
N_{SRC}	10^{19} cm^{-3}
N_{BODY}	10^{18} cm^{-3}
N_{DRAIN}	10^{19} cm^{-3}



S. H. Kim *et al.*, *IEEE Electron Device Letters*, Vol. 31, No. 10, pp. 1107-1109, 2010

Energy-Performance Comparison

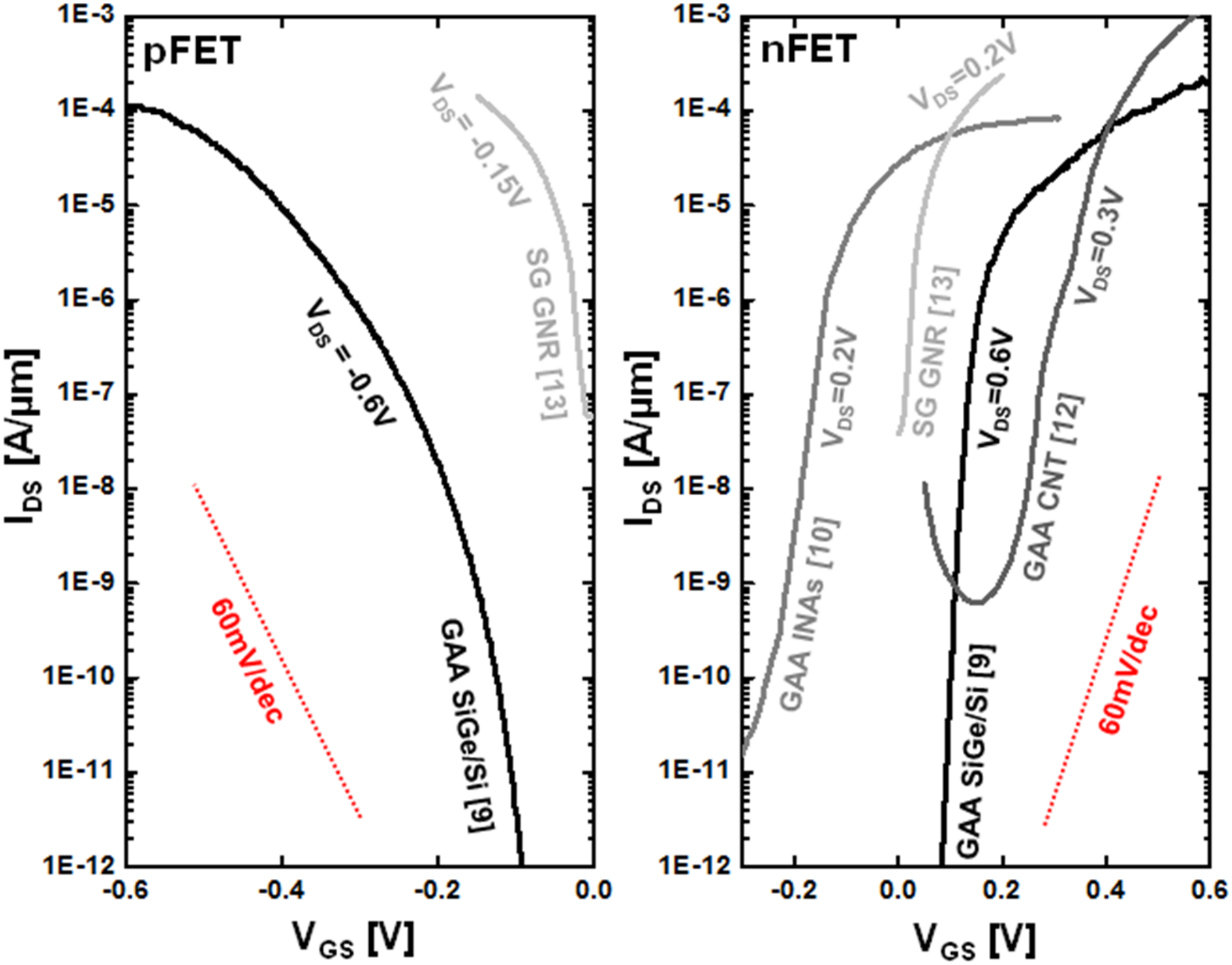


- **Ge-source TFETs are projected to achieve lower E/op than CMOS below 1 GHz**

S. H. Kim *et al.*, *IEEE Electron Device Letters*, Vol. 31, No. 10, pp. 1107-1109, 2010

Advanced Devices & Materials for TFETs

Comparison of simulated TFET I_D-V_{GS} curves



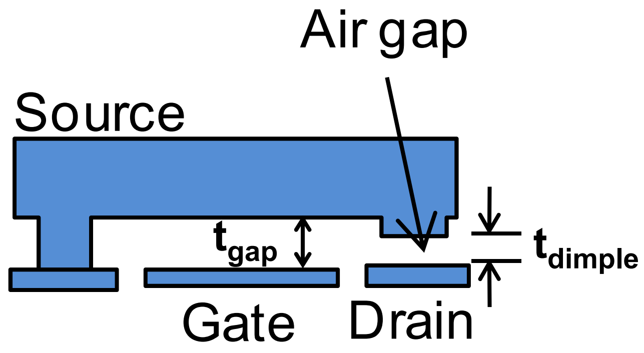
T.-J. K. Liu *et al.*, *SSDM* 2010

Why Mechanical Switches?

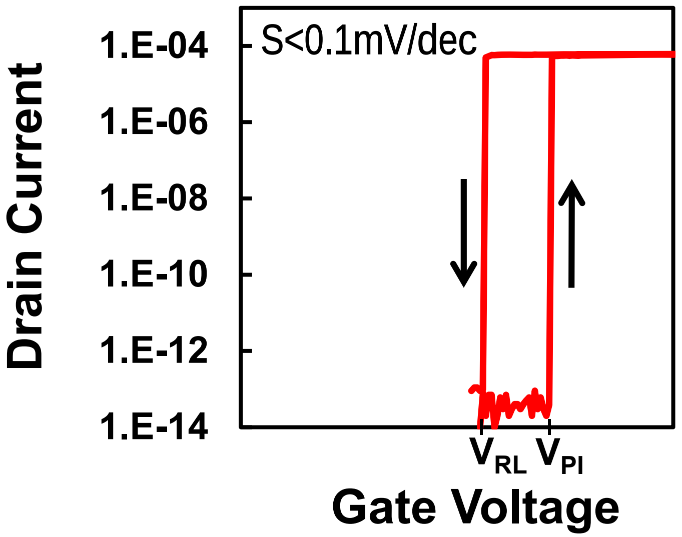
- **Zero off-state leakage**
  → zero leakage energy

- **Abrupt switching behavior**
  → allows for aggressive V_{DD} scaling (ultra-low dynamic energy)

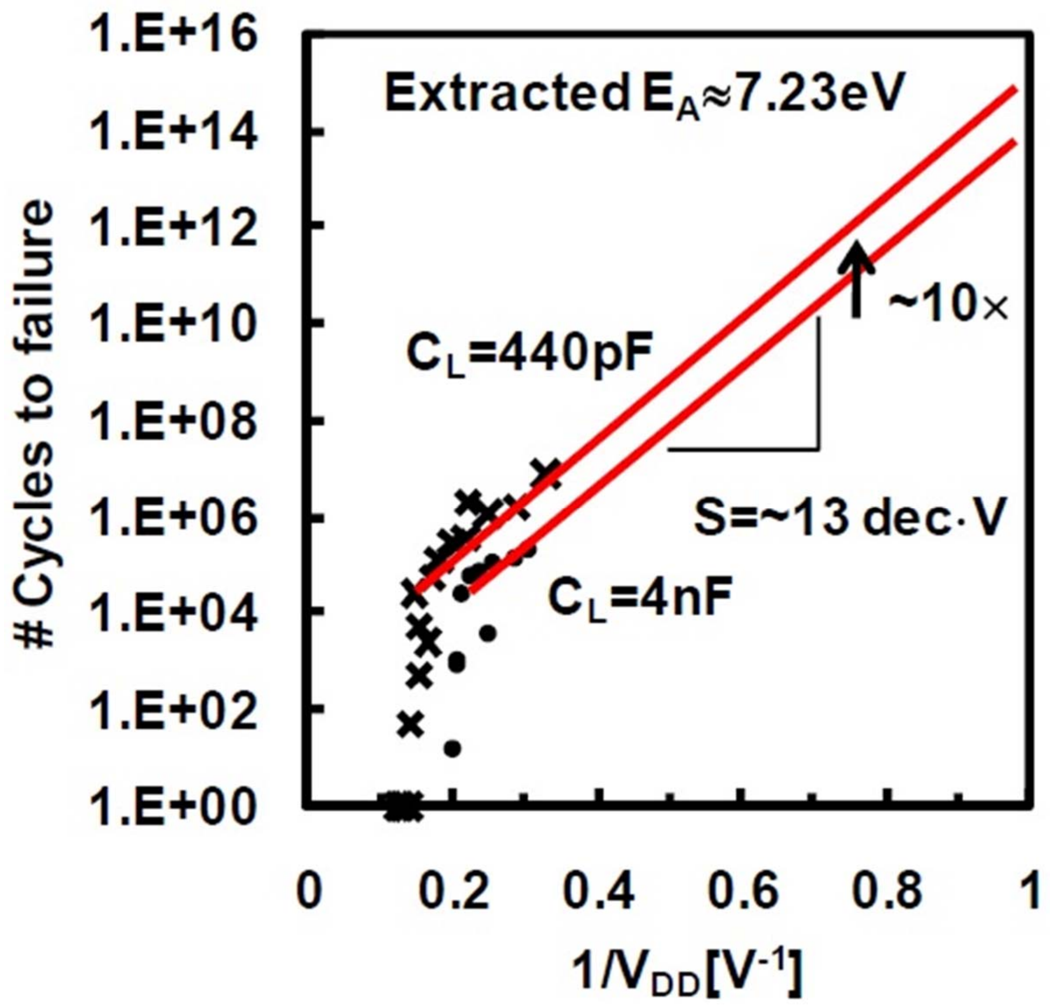
3-Terminal Switch



Measured *I-V*



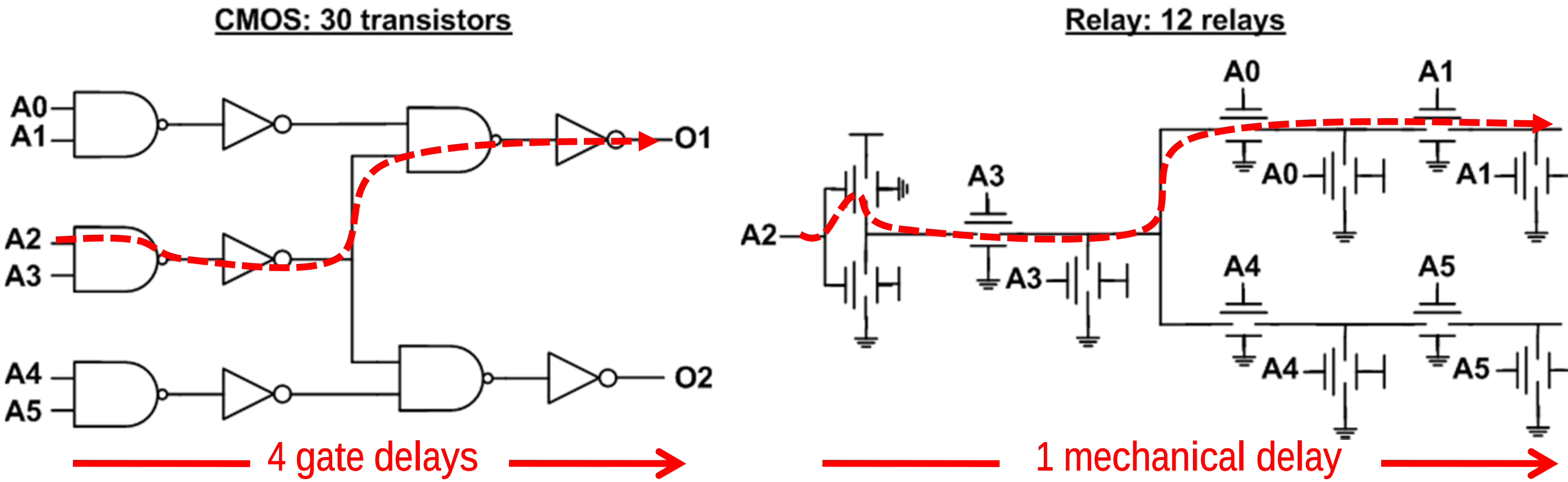
Relay Reliability



- **MCTF increases exponentially with decreasing V_{DD}**
- **MCTF increases linearly with decreasing C_L**
- **Endurance is projected to exceed 10^{15} cycles at V_{DD} = 1 V**

H. Kam *et al.*, *IEDM* 2010

Digital IC Design with Relays



- **CMOS: delay is set by electrical time constant**
  - **Quadratic delay penalty for stacking devices**

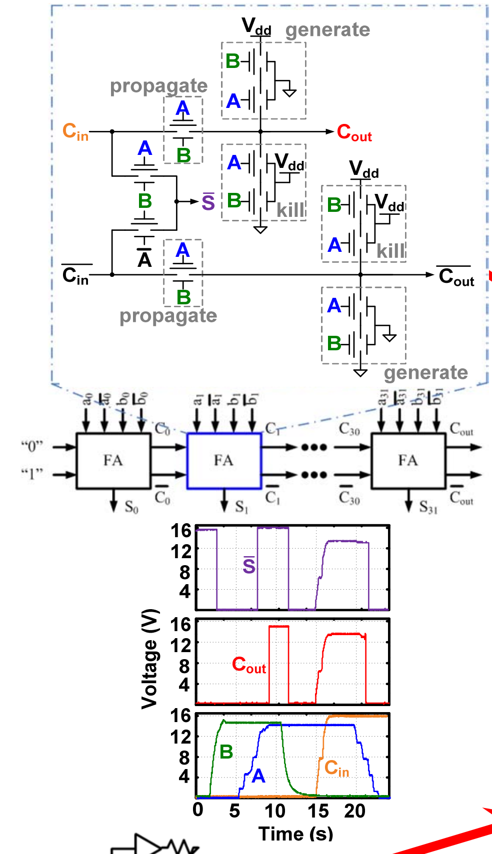
  → Buffer & distribute logical/electrical effort over many stages

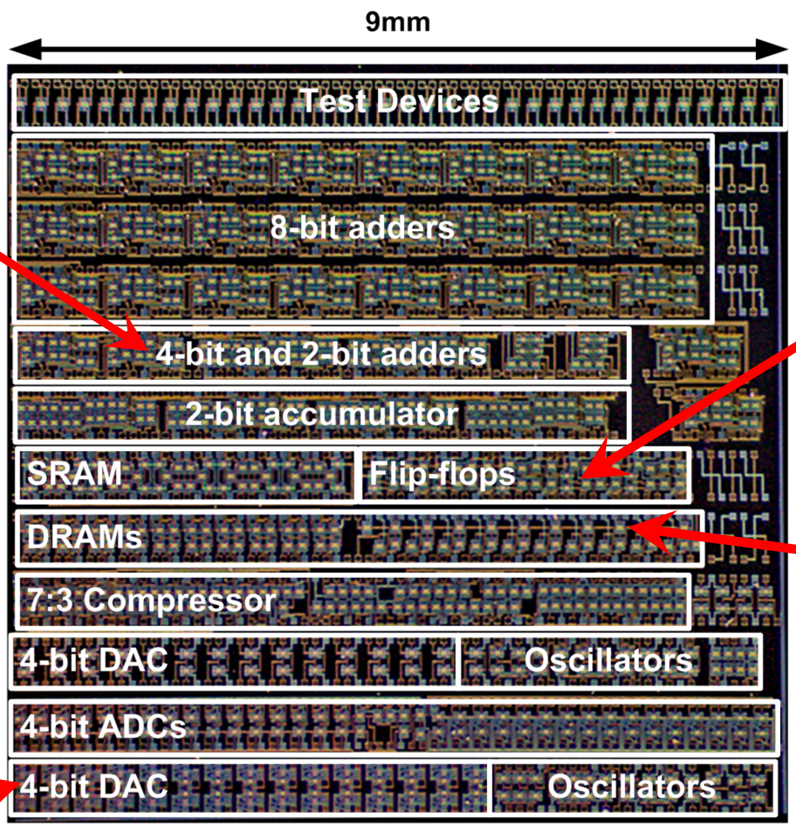
- **Relays: delay is dominated by mechanical movement**
  - **Can stack ~100 devices before $t_{elec} \approx t_{mech}$**

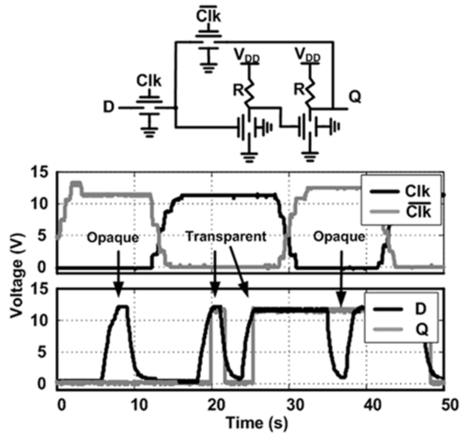
  → Implement relay logic as a single complex gate

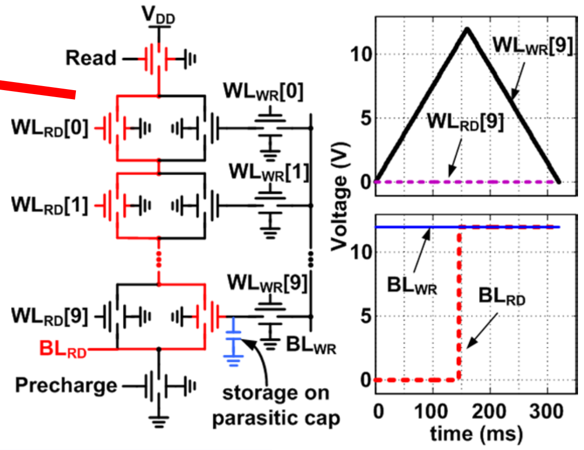
F. Chen *et al.*, *ICCAD* 2008

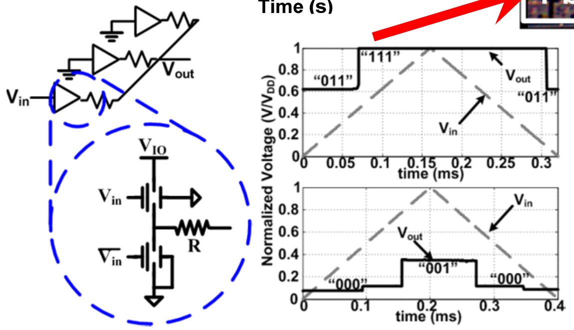
Micro-Relay-Based VLSI Building Blocks







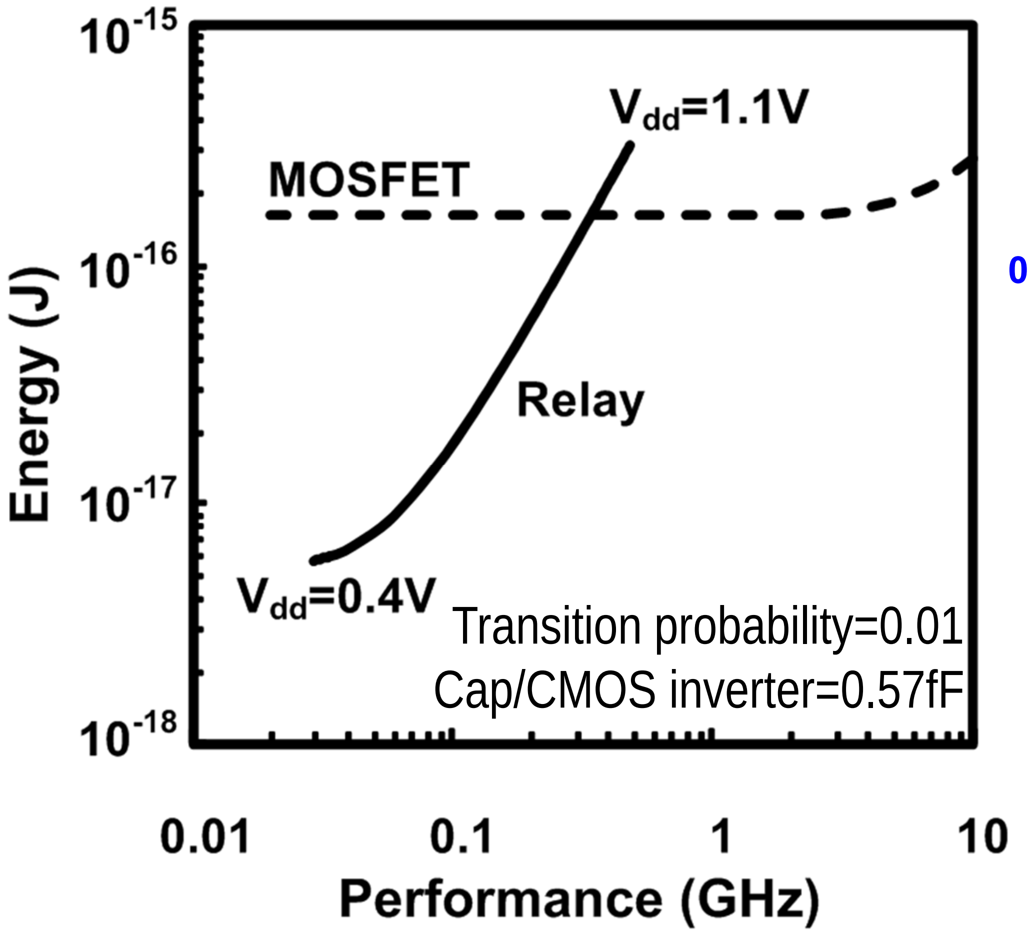




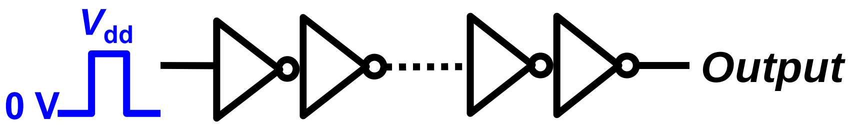
2010 ISSCC Jack Raper Award for Outstanding Technology Directions

F. Chen *et al.*, *ISSCC* 2010

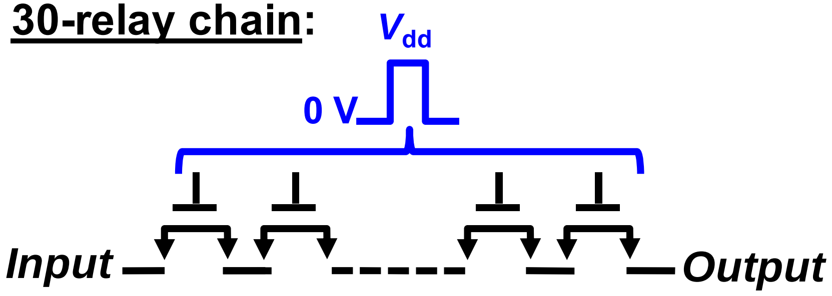
Energy-Delay Comparison



30-stage FO4 inverter chain:



30-relay chain:



- Scaled relay technology is projected to provide for >10x energy savings, at clock rates up to ~100MHz

V. Pott *et al.*, *Proc. IEEE*, Vol. 98, pp. 2076-2094, 2010

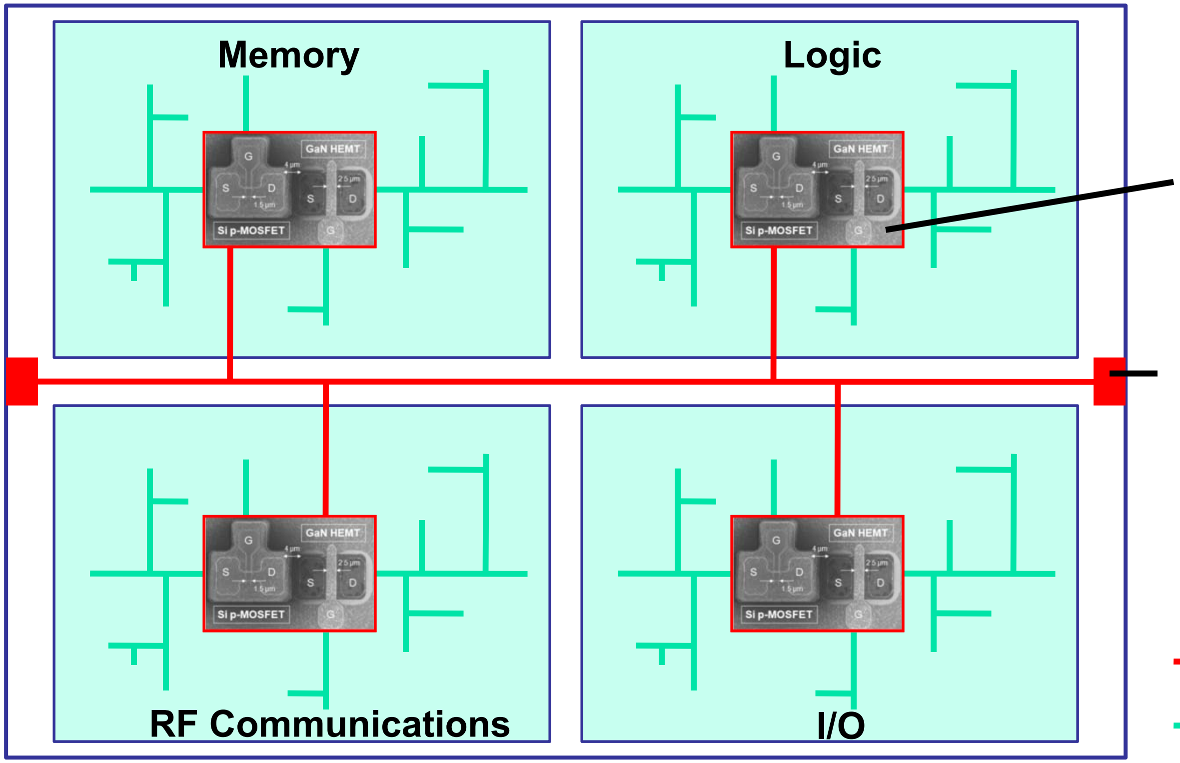
Diversification for More of Moore's Law

- MOSFET structures
- MOSFET gate-stack materials
- Alternative switch designs
  - Tunnel FET
  - Mechanical switch
- **III-V MOSFETs**

Power Distribution in Microprocessors

Today: Power distribution at low voltages, high currents
→ conductive losses

Future: Power distribution at high voltages, low currents
→ Local conversion to low voltages, high currents



12-to-1 V GaN/Si Converter

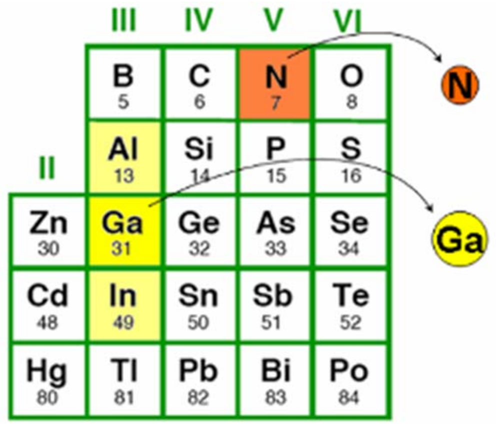
12 V Input Voltage Pad

12 V power lines

~1 V power lines

courtesy Tomás Palacios (MIT)

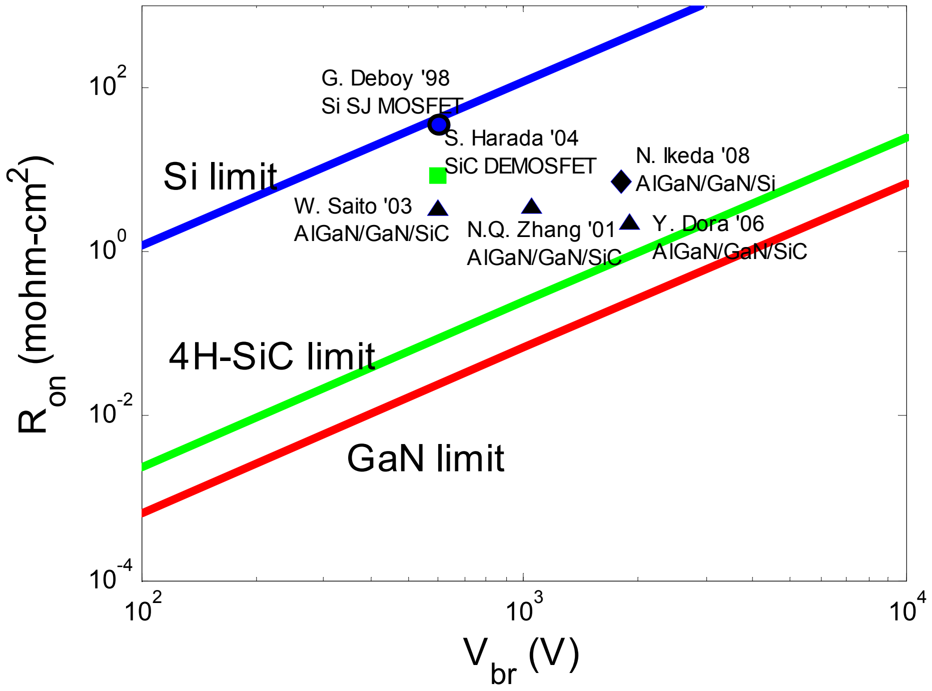
Why GaN?



Outstanding properties of AlGaN/GaN:

- **High E_{br}: 3.3 MV/cm**
- **High electron density: > 1×10^{13} /cm^2**
- **High mobility: > 1500 cm^2/Vs**
- **Low C_{in}, C_{out} → high switching speed**
- **High thermal stability**
  - **$n_i < 1 \times 10^7$/cm^3 at 400°C**

- **Improved efficiency**
- **Simplified circuit designs**
- **Reduced cooling requirements**



courtesy Tomás Palacios (MIT)

Diversification for More than Moore’s Law

Functional Diversification

- **Both <u>energy efficiency</u> and <u>functional capabilities</u> beyond the limits of ultimately scaled CMOS will be needed for electronics to expand into new applications.**

Mobile Internet Devices
- high speed (>2 GHz)
- low operating voltage
- low standby power

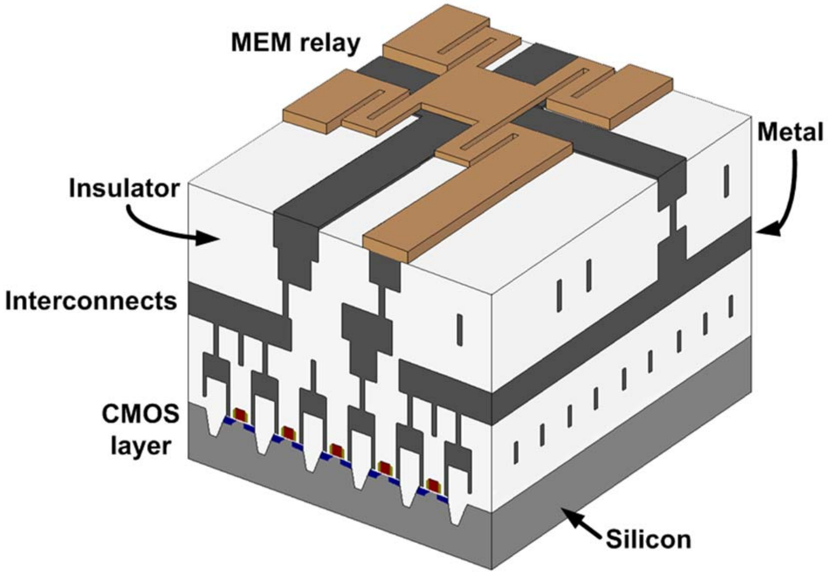
Micro/Nano Electronics

RF

MEMS

Photonics

Sensors



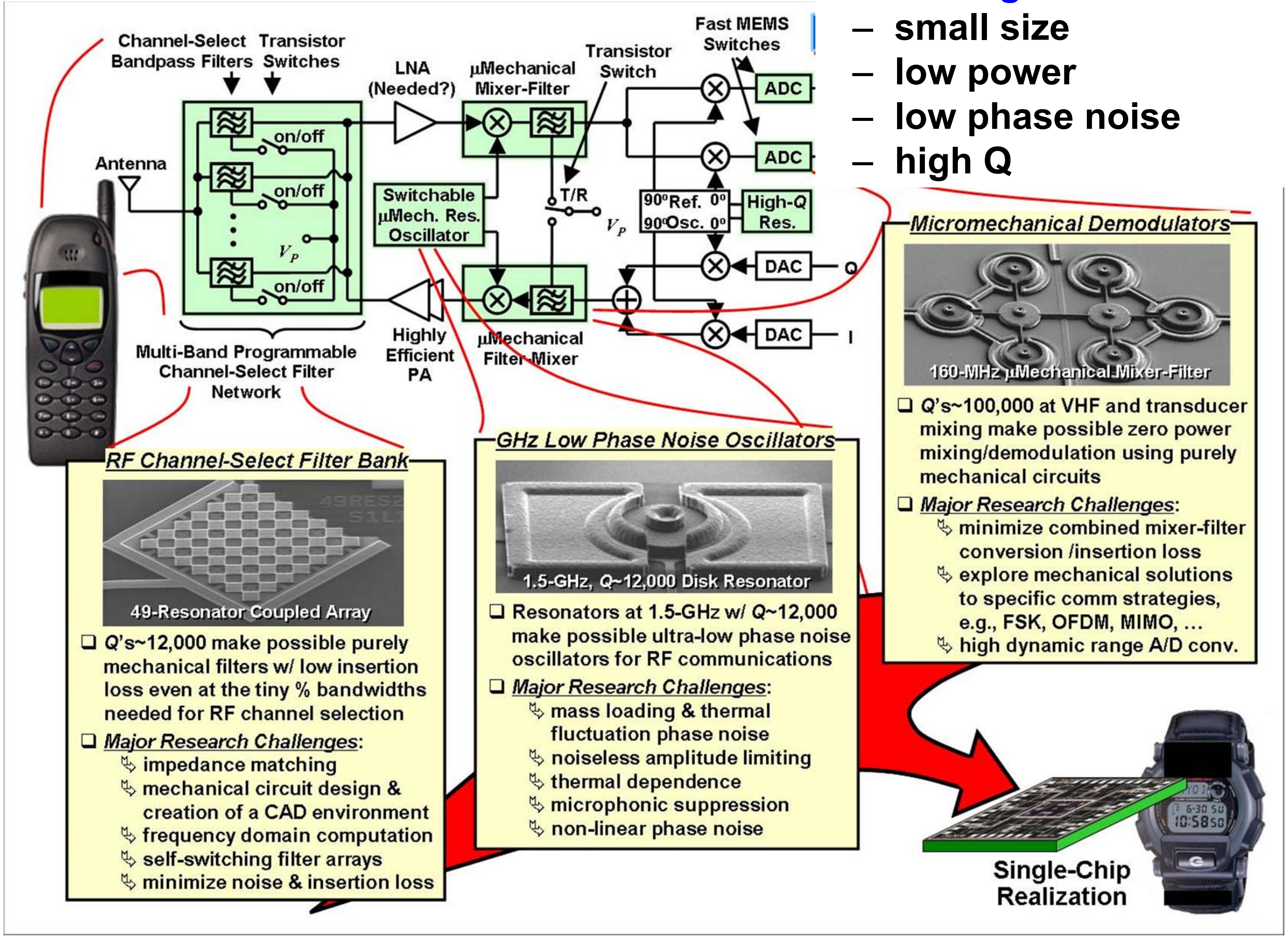
- **Heterogeneous integration with CMOS**

→ compact form factor

Adapted from T. Skotnicki, *IEDM Short Course* 2010

MEMS for Wireless Communications

- **Advantages of MEMS RF filters:**
  - small size
  - low power
  - low phase noise
  - high Q



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RF Channel-Select Filter Bank

- ☐ Q's~12,000 make possible purely mechanical filters w/ low insertion loss even at the tiny % bandwidths needed for RF channel selection
- ☐ *Major Research Challenges*:
  - impedance matching
  - mechanical circuit design & creation of a CAD environment
  - frequency domain computation
  - self-switching filter arrays
  - minimize noise & insertion loss

GHz Low Phase Noise Oscillators

- ☐ Resonators at 1.5-GHz w/ Q~12,000 make possible ultra-low phase noise oscillators for RF communications
- ☐ *Major Research Challenges*:
  - mass loading & thermal fluctuation phase noise
  - noiseless amplitude limiting
  - thermal dependence
  - microphonic suppression
  - non-linear phase noise

Micromechanical Demodulators

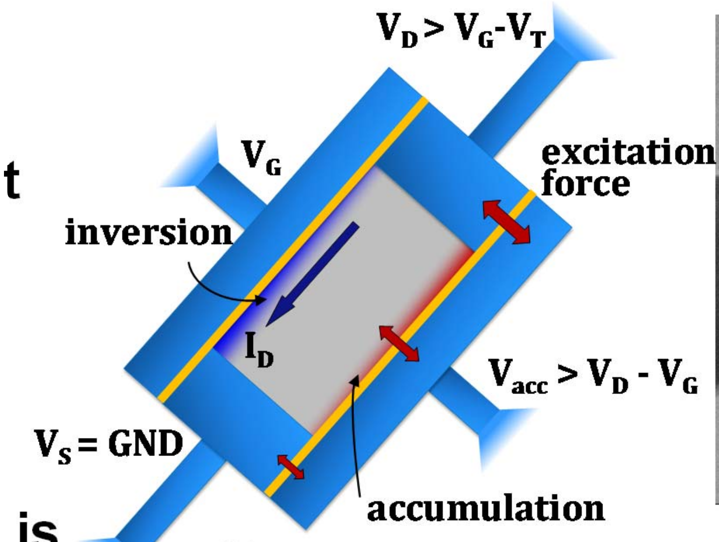
- ☐ Q's~100,000 at VHF and transducer mixing make possible zero power mixing/demodulation using purely mechanical circuits
- ☐ *Major Research Challenges*:
  - minimize combined mixer-filter conversion /insertion loss
  - explore mechanical solutions to specific comm strategies, e.g., FSK, OFDM, MIMO, …
  - high dynamic range A/D conv.

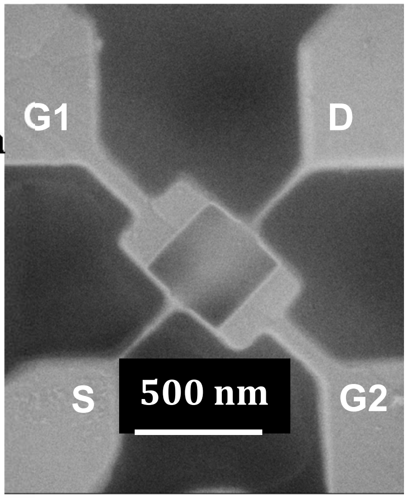
courtesy Clark Nguyen (UC-Berkeley)

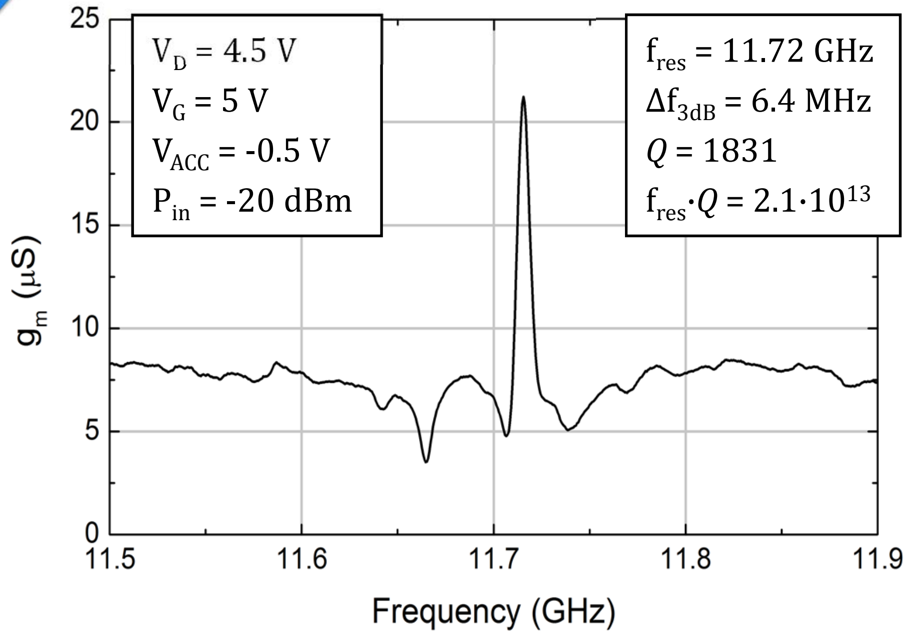
The Resonant Body Transistor

- **Drive gate is biased in accumulation (V_{acc}). Capacitive force due to input signal (v_{in}) drives resonant motion.**
- **Sense gate biased to strong inversion (V_G). As the body vibrates, the drain current I_D is modulated piezoresistively.**
- **RBT demonstrated at 11.7 GHz with quality factor Q of 1831**

  Fabricated side-by-side with FinFETs
- **To avoid the need for release, CMOS layers can be used to form acoustic Bragg reflectors to localize vibrations**





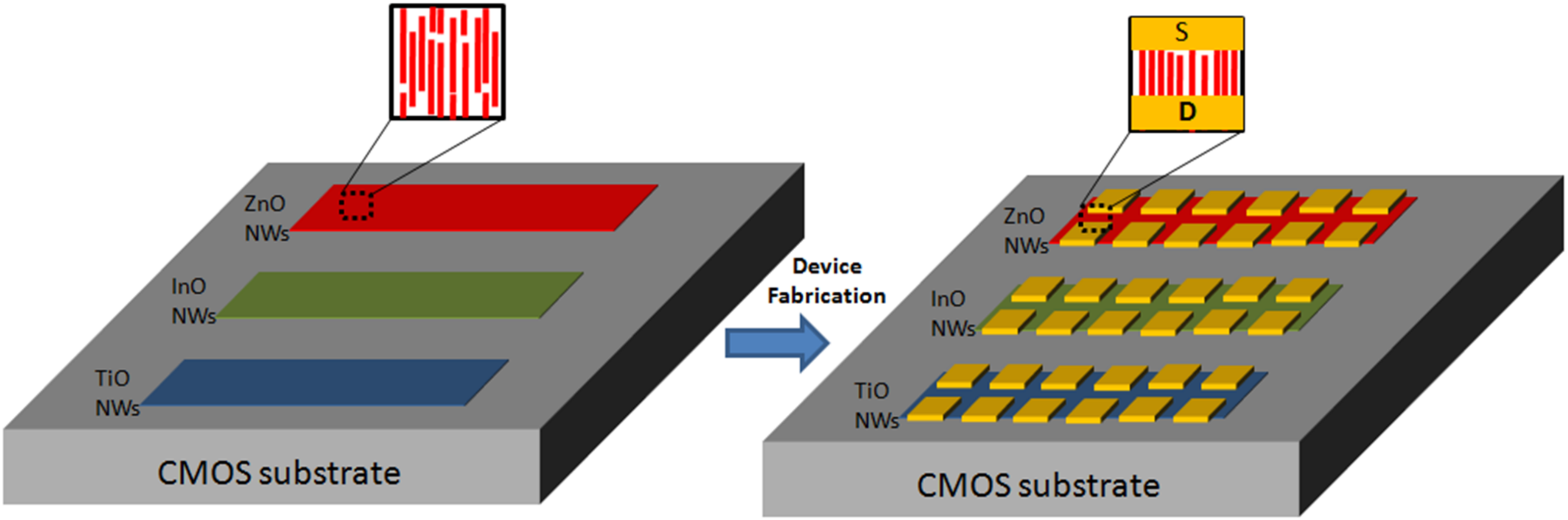


D. Weinstein and S. A. Bhave, *Nano Letters* 10(4) 1234-37 (2010)

Nanowire Sensor Arrays

CMOS-integrated sensors for detection of chemical and biomolecular species with high sensitivity and specificity.

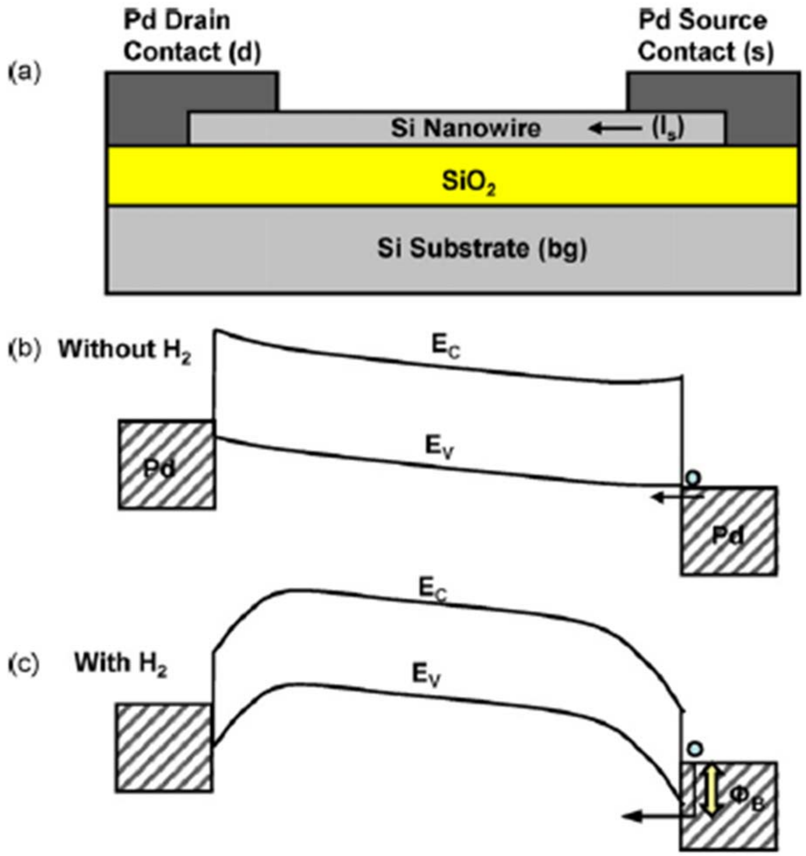
Heterogeneous Nanowire FET Array Fabrication:

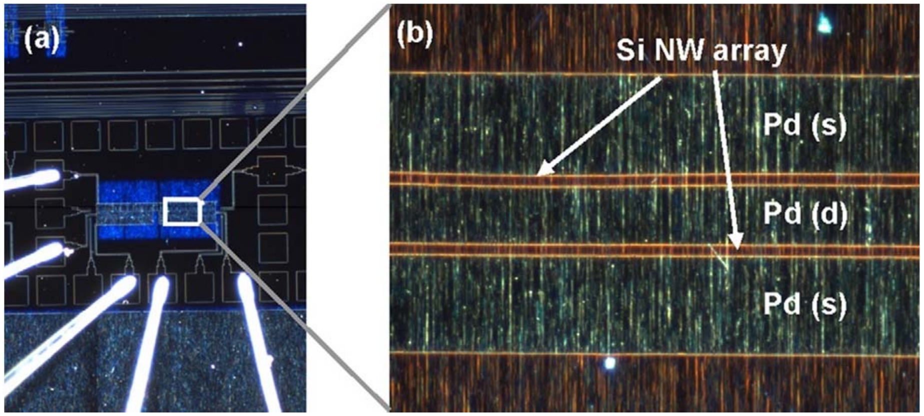


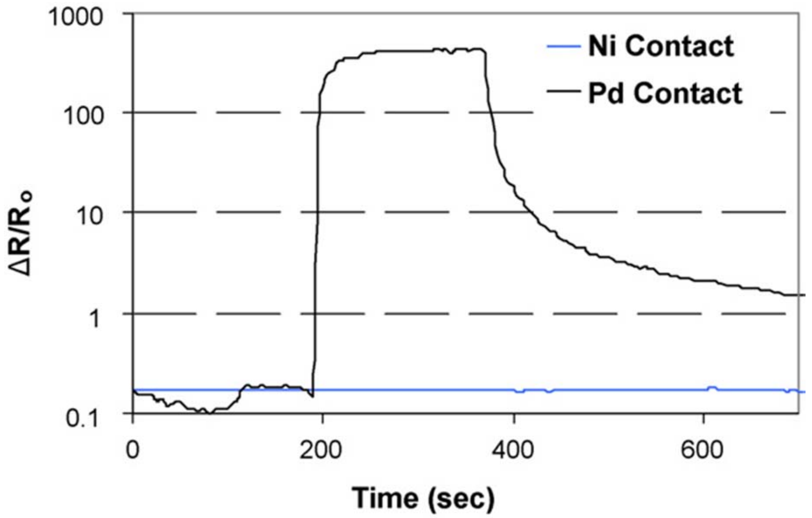
courtesy Ali Javey (UC-Berkeley)

Pd/Si Nanowire H_2 Sensors

- Without H_2: ohmic contact
- With H_2:Schottky contact



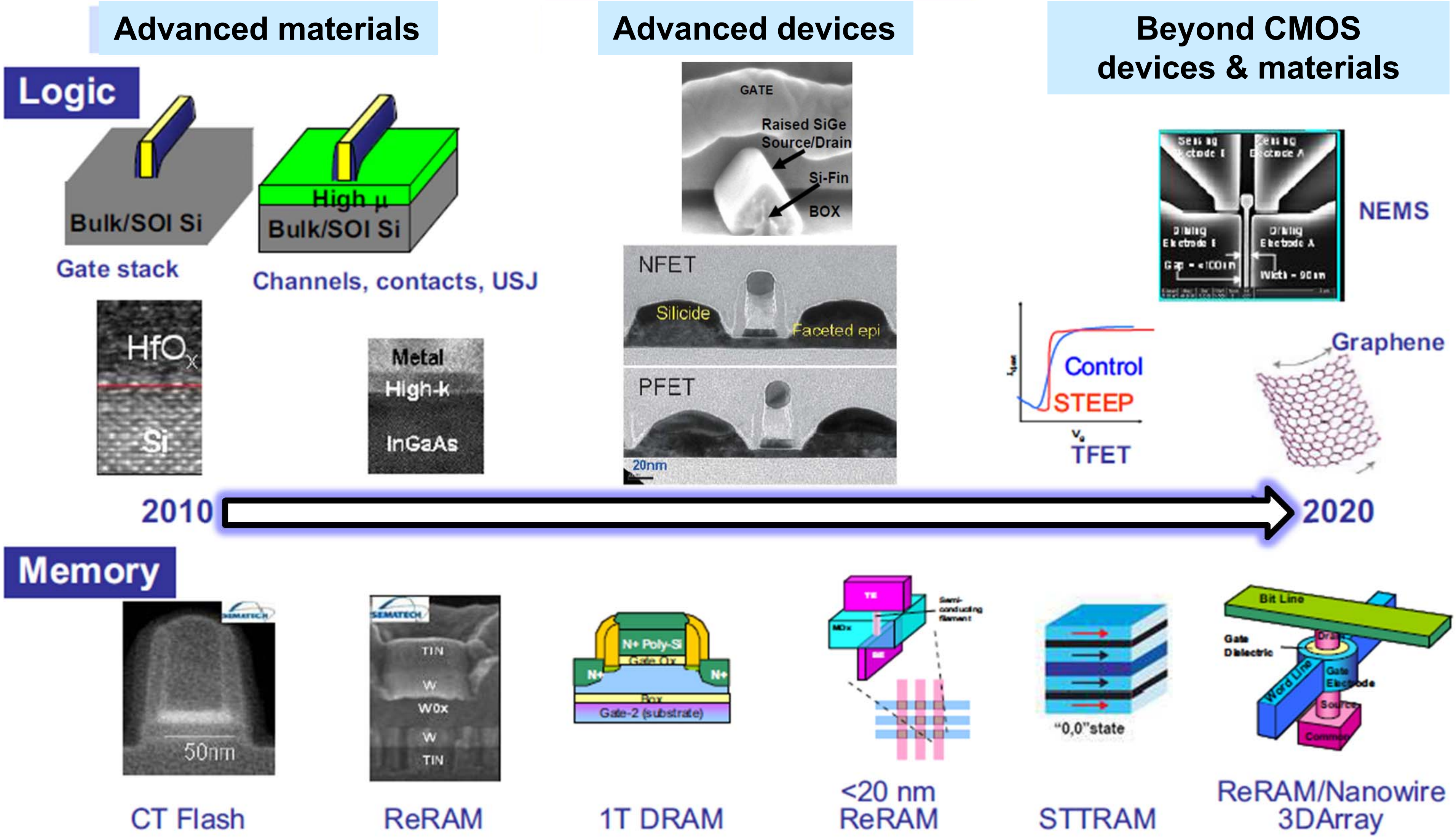




K. Skucha *et al., Sensors & Actuators B*, pp. 232-238, 2010

Summary

Diversification is the Key



Advanced materials

Advanced devices

Beyond CMOS devices & materials

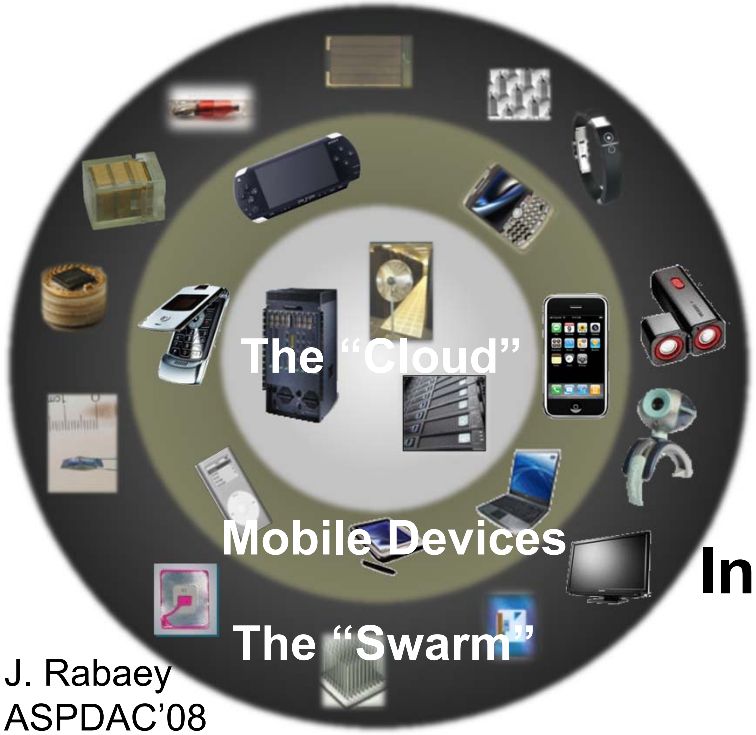
Logic

2010 → 2020

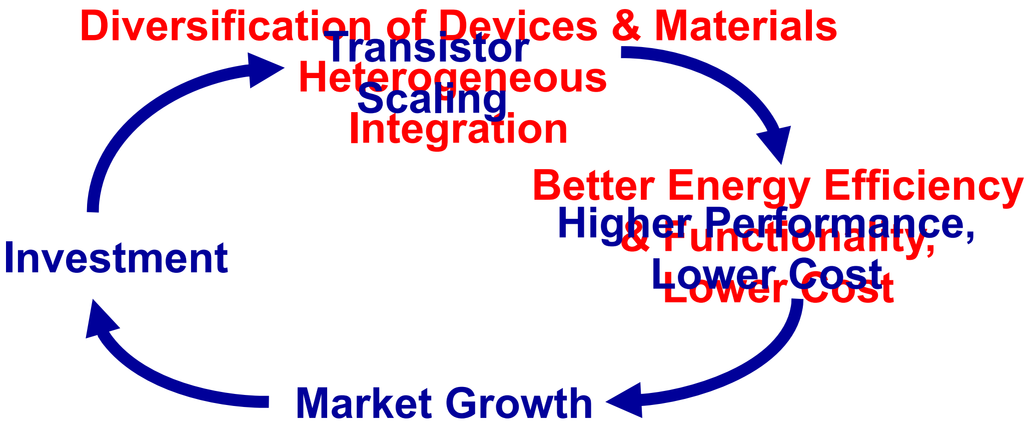
Memory

Courtesy Dan Armbrust, SEMATECH

A Vision of the Future



J. Rabaey
ASPDAC'08

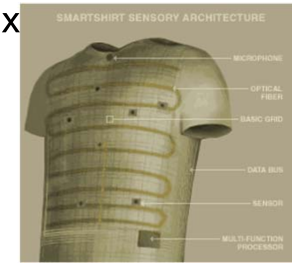


Information technology will be

- pervasive
- embedded
- human-centered
- solving societal scale problems

Philips

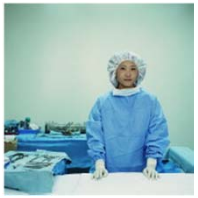
Sensatex



Transportation

Energy

Health care



Environment

Disaster response

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