Sustaining the Si Revolution:
From 3D Transistors to 3D Integration

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2015 SPIE Advanced Lithography Symposium

Impact of Moore's Law

Gordon E. Moore

Transistor Scaling

Lower Cost/Component
Higher Performance

Market Growth

Investment

Internet of Things (IoT)

Mobile Internet

Desktop Internet

PC

Minicomputer

Mainframe

Increasing Integration

DEVICES

10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}

1960 1970 1980 1990 2000 2010 2020 2030

YEAR

Source: Morgan Stanley Research

A Vision of the Future

Ultra-low-power operation required!

The Cloud (millions)

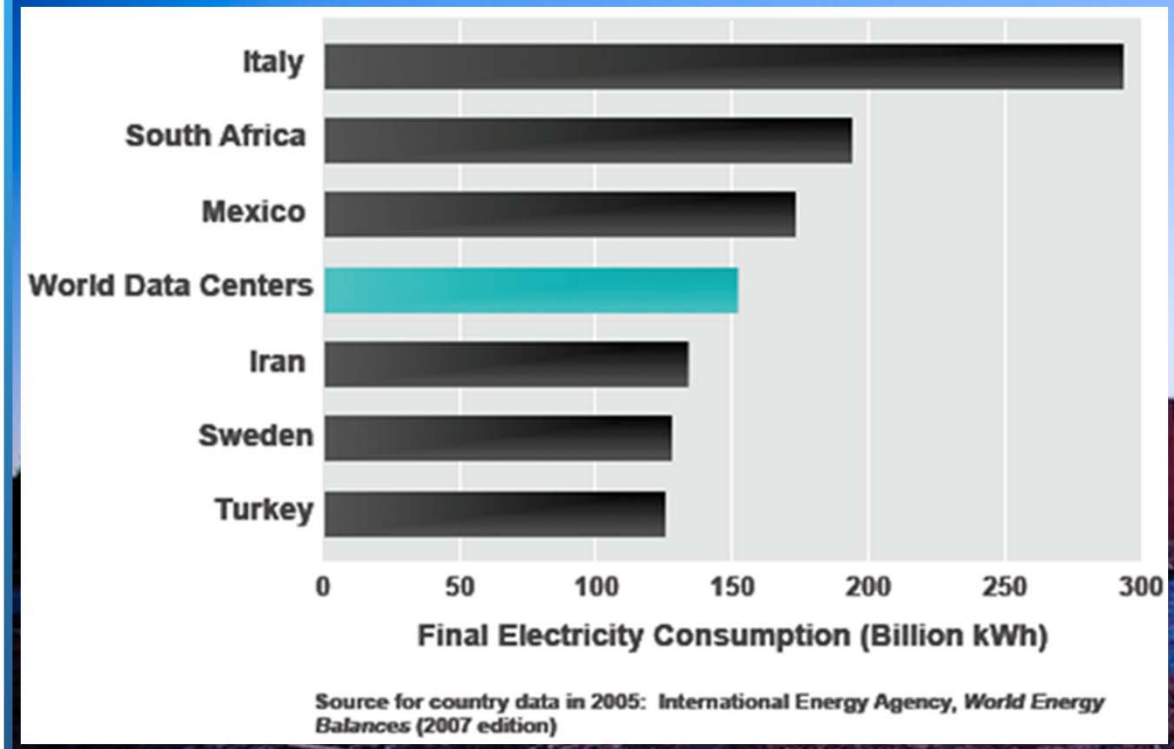
Mobile devices (billions)

The Swarm (trillions)

Source: J. Rabaey, *ASPDAC* 2008

Data Center Electricity Usage

Data centers accounted for ~1.4% of electricity use worldwide in 2010*



Google's Finland data center uses frigid water from the Baltic Sea for cooling.

http://www.wired.com/2012/01/google-finland/

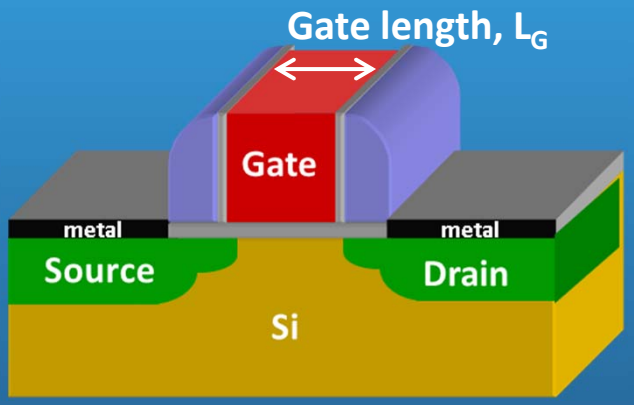
*J. Koomey, *Growth in Data center electricity use 2005 to 2010* (Analytics Press, Oakland, CA), 2011

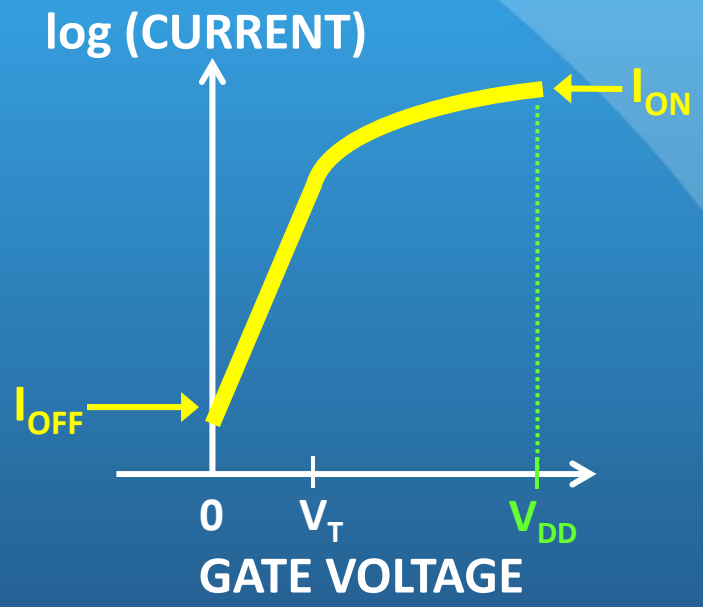
Outline

- The path to 3D Transistors
  - The CMOS Power Crisis
  - Improving Energy Efficiency
- Pathways to 3D Integration
- Summary

MOSFET Basics

Metal-Oxide-Semiconductor (MOS)
Field-Effect Transistor (FET)



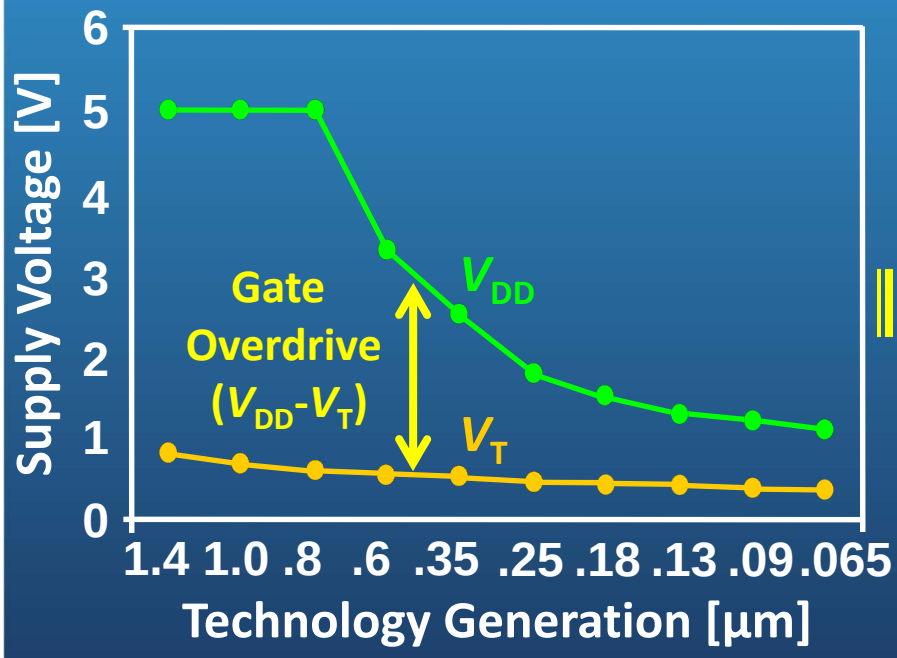


The CMOS Power Crisis

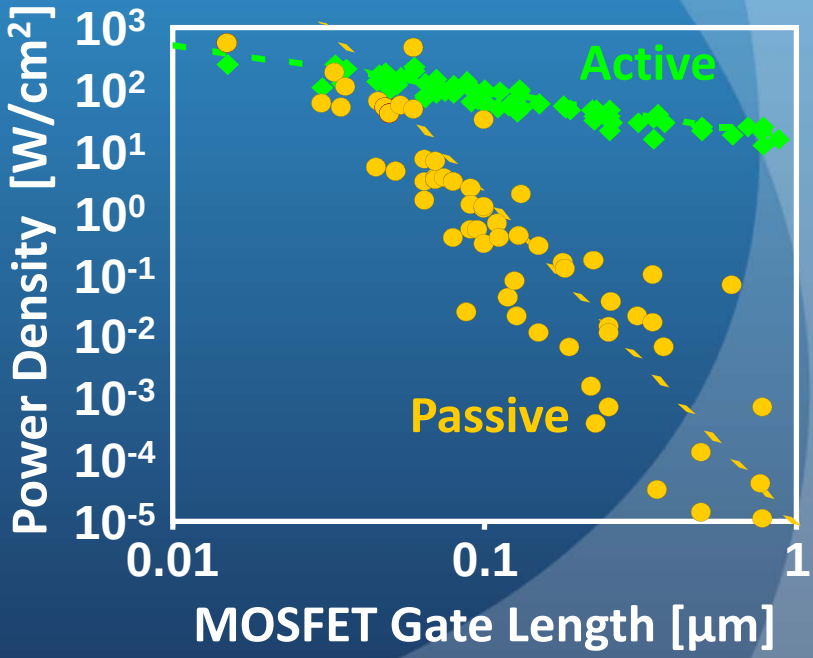
- Voltage scaling has not kept pace with transistor scaling!

Technology Node	45 nm	32 nm	22 nm	16/14 nm
Supply voltage, V_{DD}	1.0 V	0.9 V	0.8 V	0.7 V

➥ Power density limits now constrain IC design



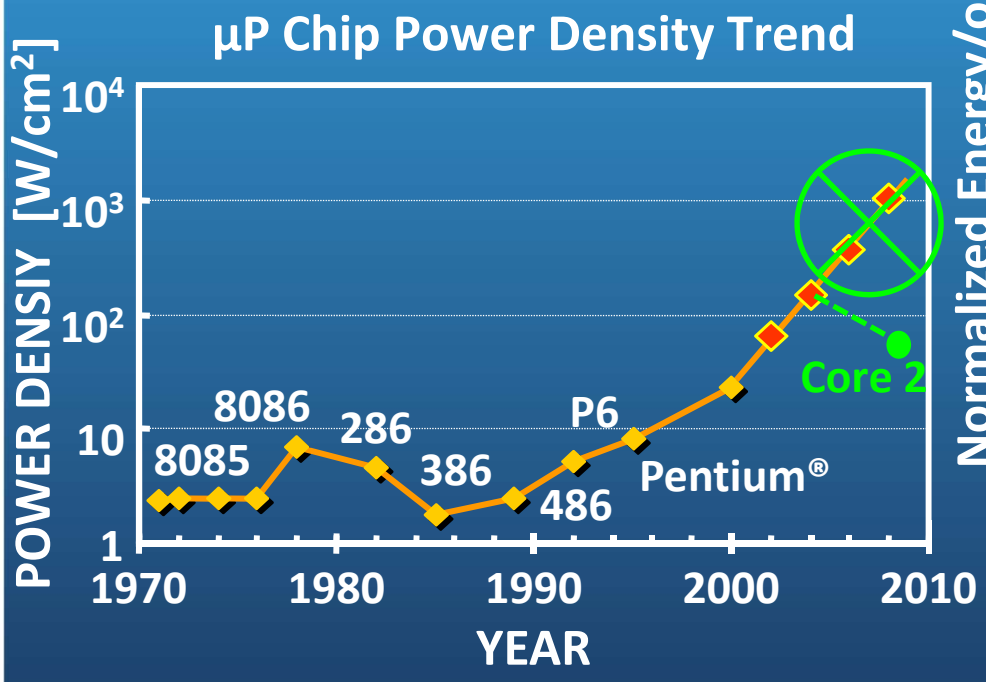
Source: P. Packan (Intel), *IEDM* Short Course, 2007

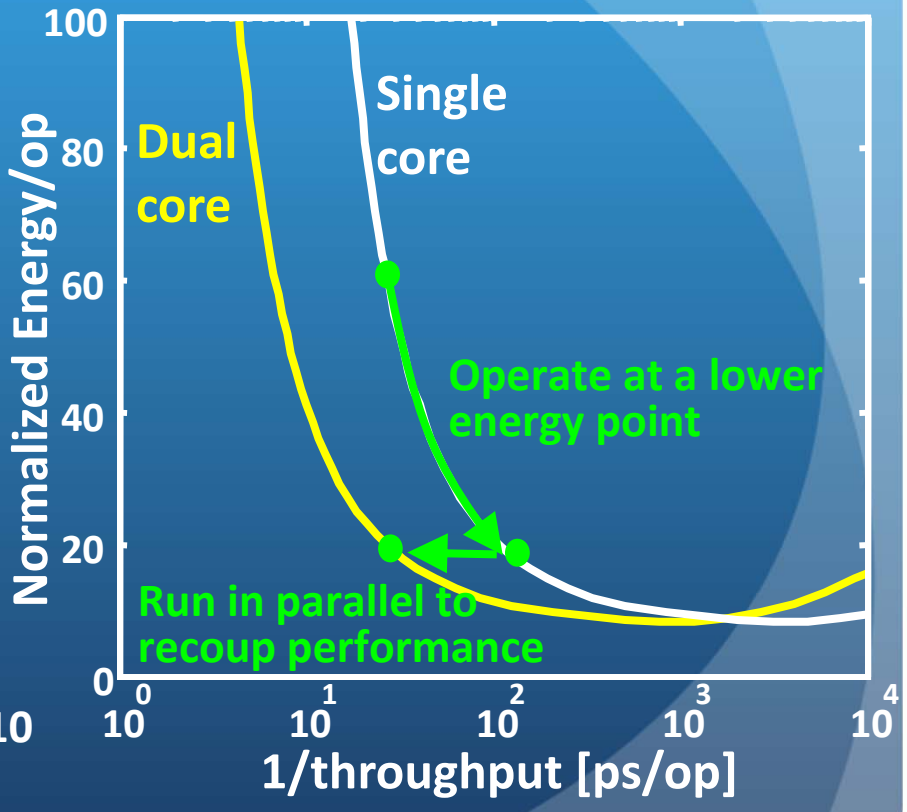


Source: B. Meyerson (IBM), *Semi. Conf.*, 2005

The Advent of Multi-Core Systems

- **Parallelism** is the main technique used to improve system performance under a power density constraint.





Source: S. Borkar (Intel)

CMOS Energy Efficiency Limit

- **A lower limit for E/op exists due to transistor OFF-state leakage.**

Active Energy Passive Energy

$$E_{Total} = \alpha L_d f C V_{DD}^2 + L_d f I_{OFF} V_{DD} t_{delay}$$

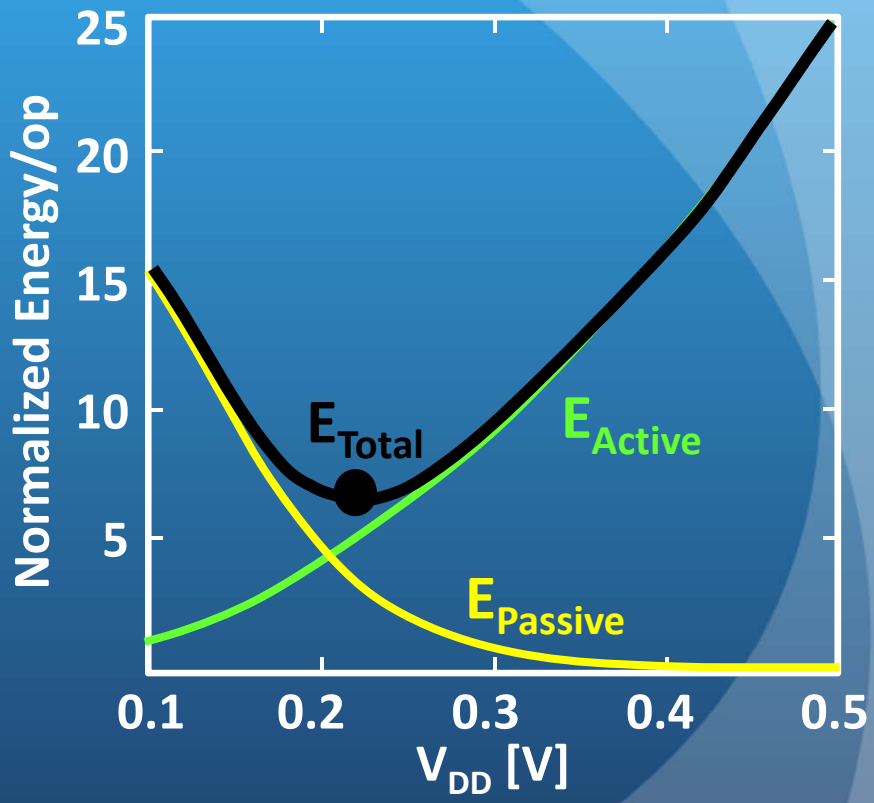
$$t_{delay} = L_d f C V_{DD} / (2 I_{ON})$$

α : Activity Factor

L_d: Logic Depth

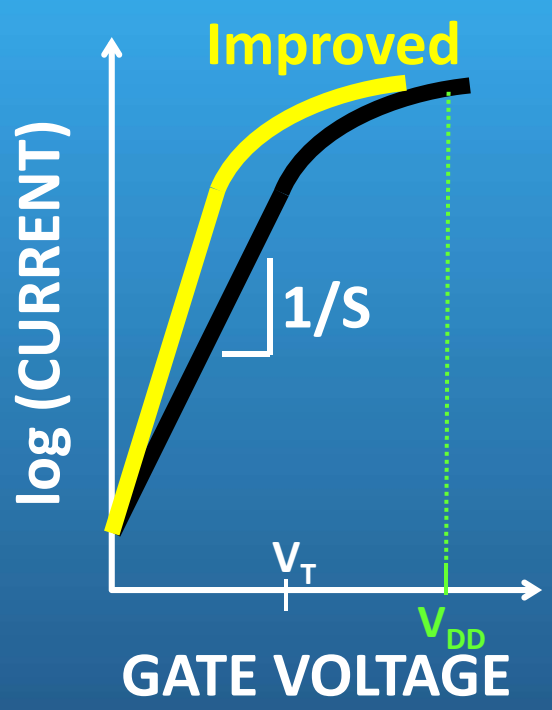
f : Fanout

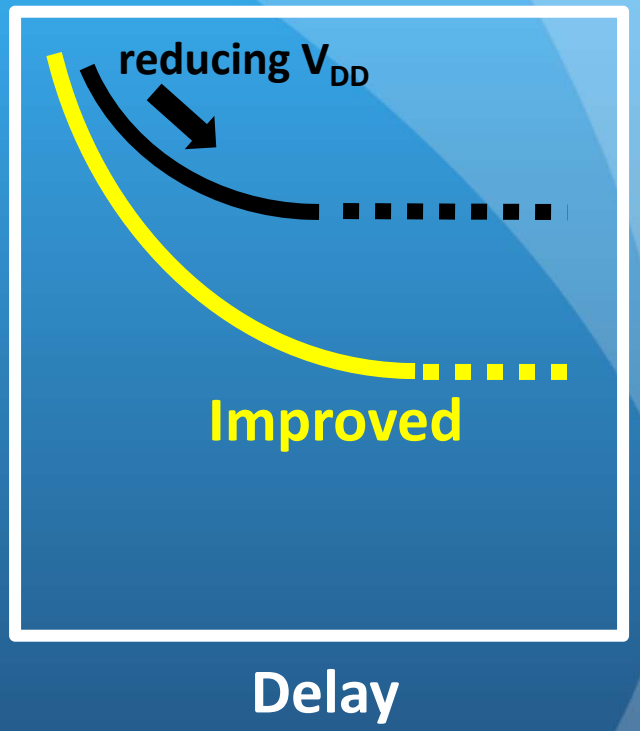
C : Capacitance per Stage



B. Calhoun *et al.*, *IEEE J. Solid State Circuits*, Vol. 50, pp. 1778-1786, 2005

$$E_{total} = \alpha L_d f C V_{DD}^2 [\, 1 + (L_d f / 2\alpha) / (I_{ON}/I_{OFF}) \,]$$

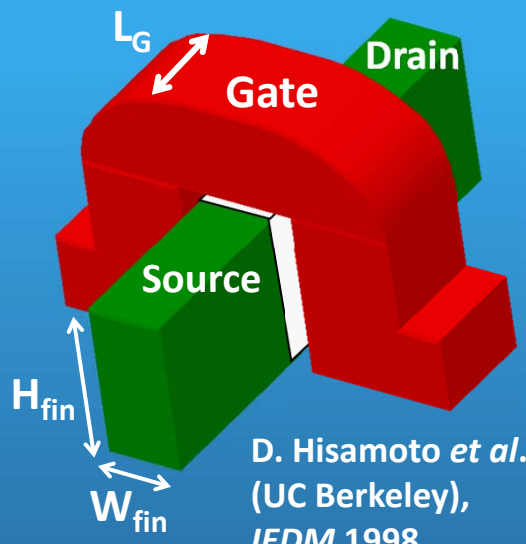




- Higher I_{ON}/I_{OFF} → lower Energy/op

→Steeper switching behavior is needed!

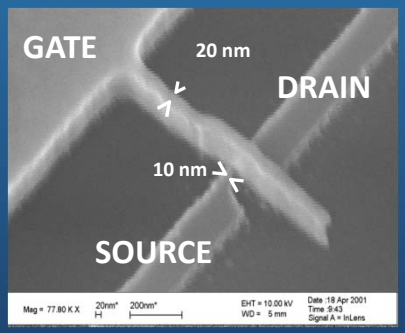
3-Dimensional (3D) Transistor



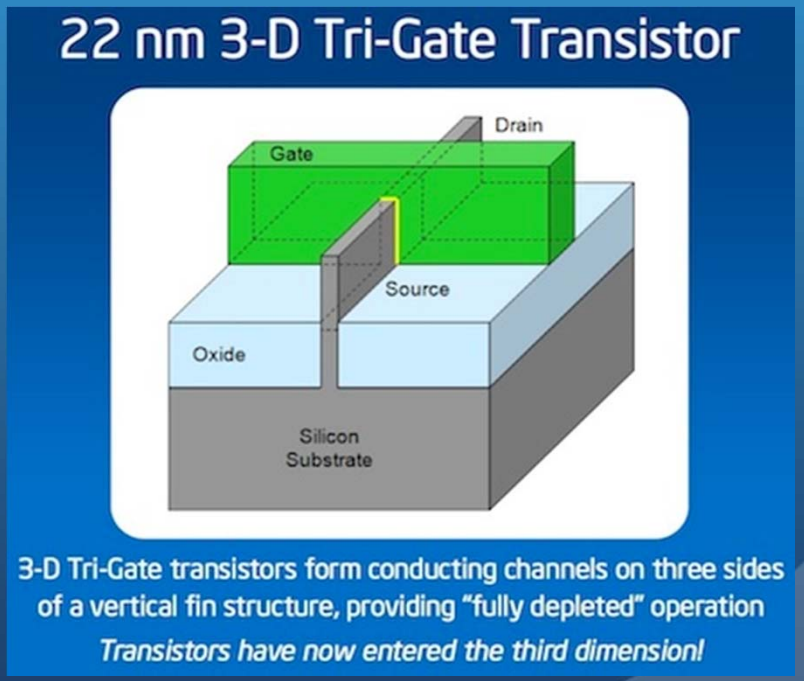
D. Hisamoto *et al.* (UC Berkeley), *IEDM* 1998

- Superior gate control → higher I_{ON}/I_{OFF}
- Multiple fins can be connected in parallel to achieve higher current

15nm L_g FinFET



Y.-K. Choi *et al.*, (UC Berkeley) *IEDM* 2001



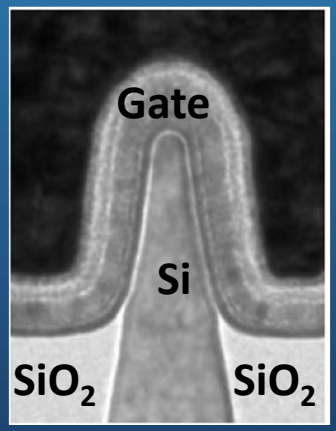
Intel Corp., May 2011

3D Transistor Technology Roadmap

Year:	2012	2014	2016?
Intel Technology Node	22 nm	14 nm	10 nm

Year:	2015		
Foundry Technology Node:	14 nm	10 nm	7 nm
Gate length, L_G	25 nm	20 nm	15 nm
Fin width, W_{fin}	~10 nm	~8 nm	~6 nm
Equivalent oxide thickness	0.9 nm	0.85 nm	0.8 nm

X-SEM Images



C. Auth *et al.* (Intel Corp.)
VLSI Symp. 2012

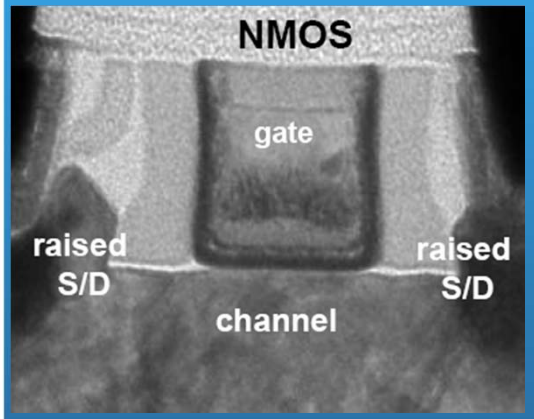
S. Natarajan *et al.* (Intel Corp.)
IEDM 2014

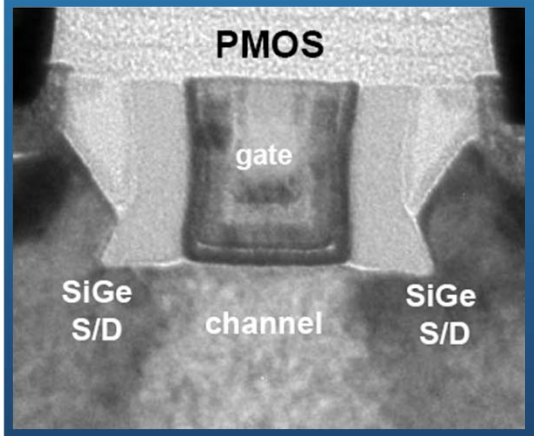
MOSFET Evolution

32/28 nm
planar

22 nm
thin body

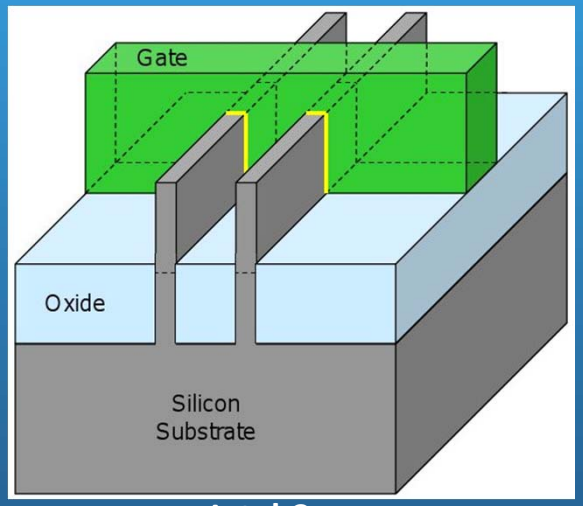
beyond 10 nm
nanowires (NWs)?





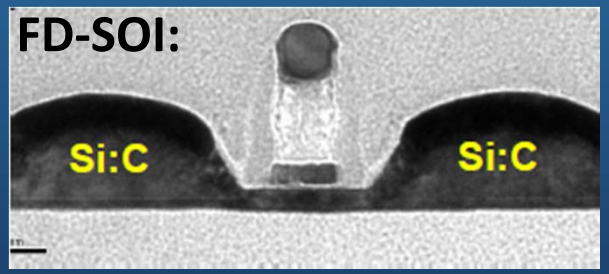
P. Packan *et al.* (Intel), *IEDM* 2009

FinFET:

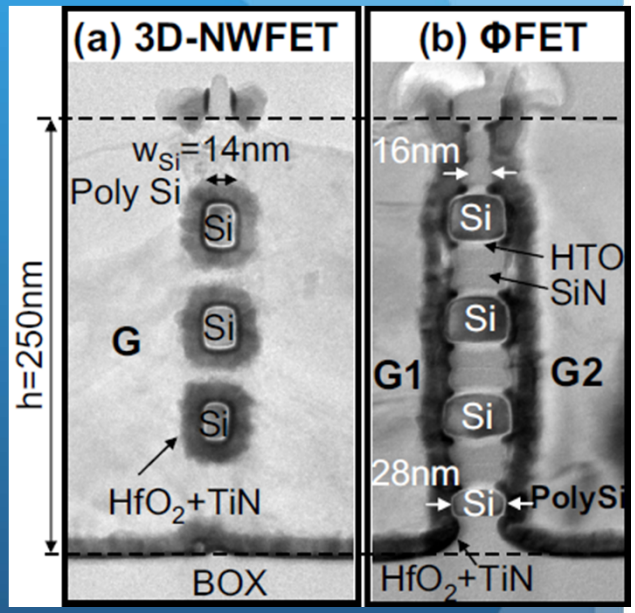


Intel Corp.

FD-SOI:



K. Cheng *et al.* (IBM), *VLSI Symp.* 2011

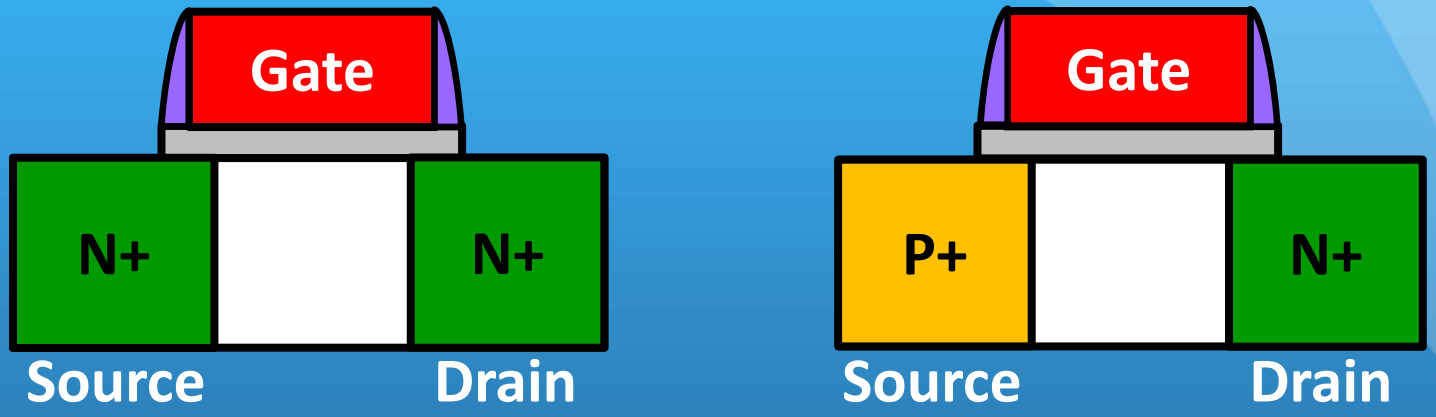


C. Dupré *et al.* (CEA-LETI) *IEDM* 2008

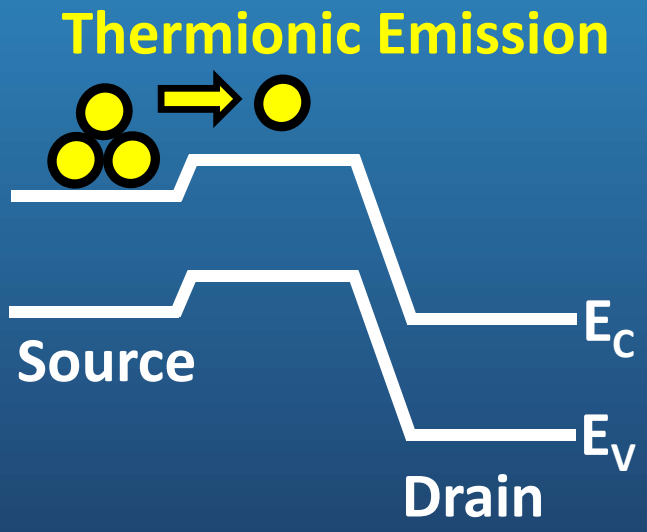
Gate-all-around FETs must comprise stacked NWs for good area efficiency.

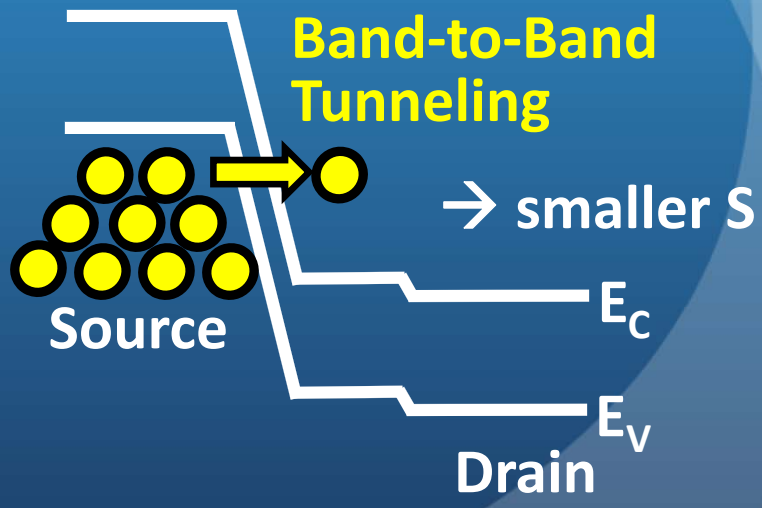
MOSFET *vs.* Tunnel FET

STRUCTURE



ENERGY BAND DIAGRAM





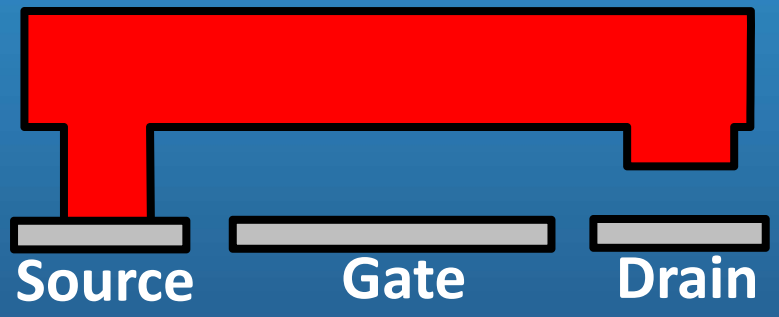
Small-bandgap (*e.g.* Ge or SiGe) Source provides for higher I_{ON}

Electro-Mechanical Switch

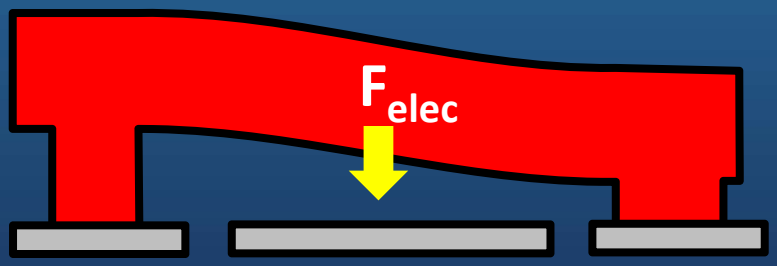
- Zero off-state leakage → Zero passive power consumption
- Abrupt switching behavior → Low V_{DD} (low active energy)

Three-Terminal Switch

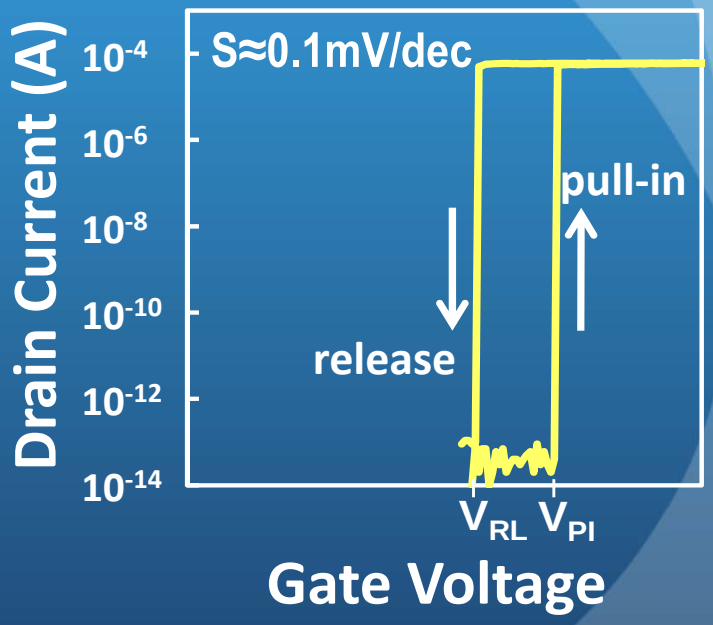
OFF State (as fabricated):



ON State:



I-V Characteristic

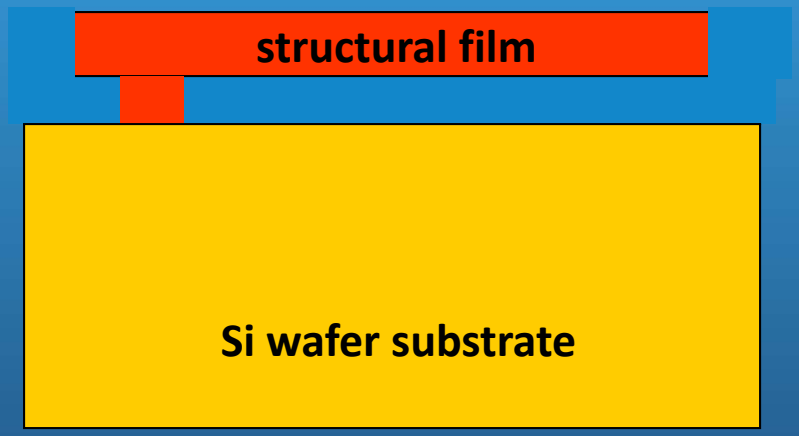


- Logic relay endurance > 10^{15} cycles for hot-switching below 1 Volt

H. Kam *et al.* (UC Berkeley), *IEDM* 2010

Surface Micromachining Process

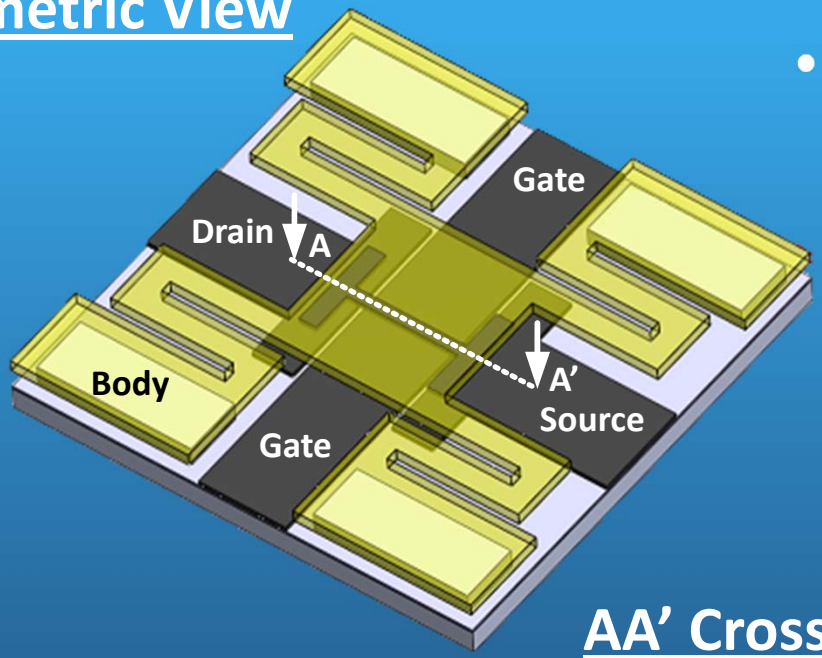
Cross-sectional View



- Mechanical structures can be made using conventional microfabrication techniques
- Structures are freed by selective removal of sacrificial layer(s)

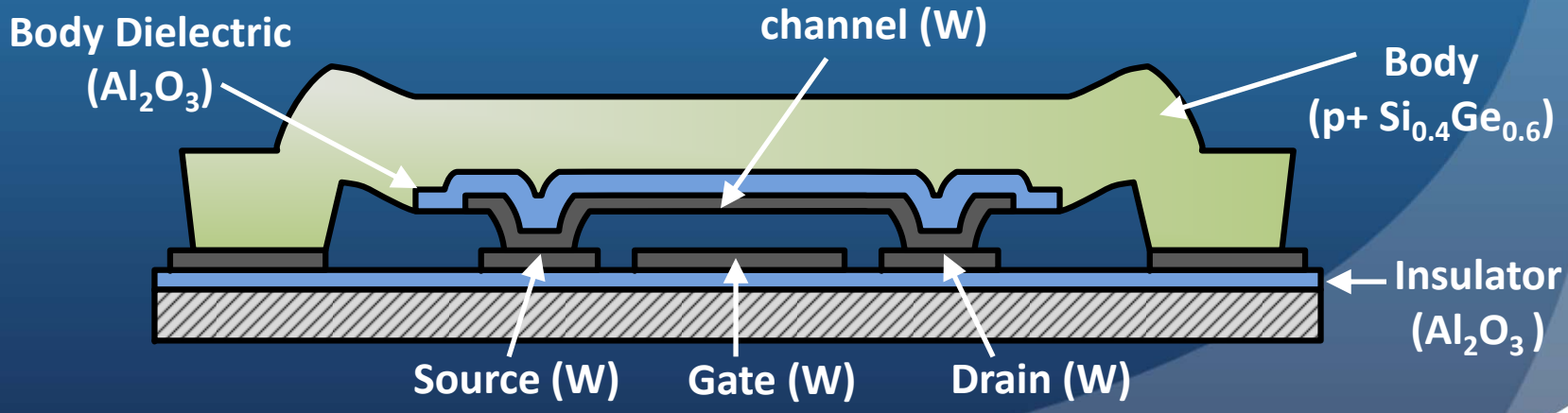
4-Terminal Logic Relay

Isometric View



- Voltage applied between the gate and movable body brings the channel into contact with source & drain
- Dielectric layer insulates body

AA' Cross-section



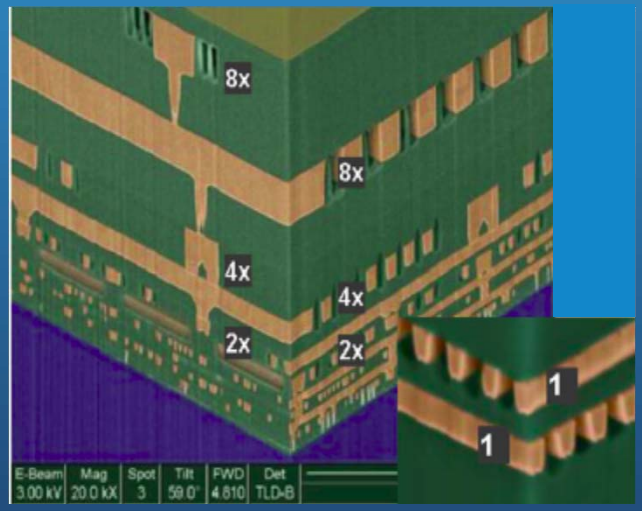
R. Nathanael *et al*. (UC Berkeley), *IEDM* 2009

3D Integration with CMOS

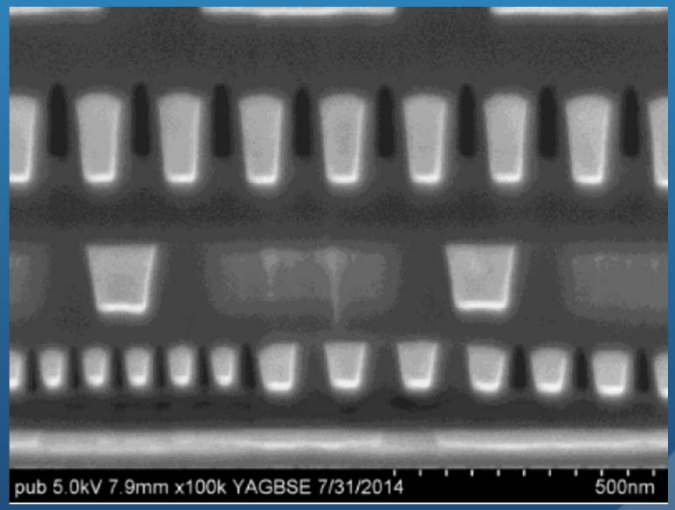
- Advanced back-end-of-line (BEOL) processes have multiple metal layers and air gaps

  → can be adapted for fabrication of compact relays!

Scanning Electron Micrographs

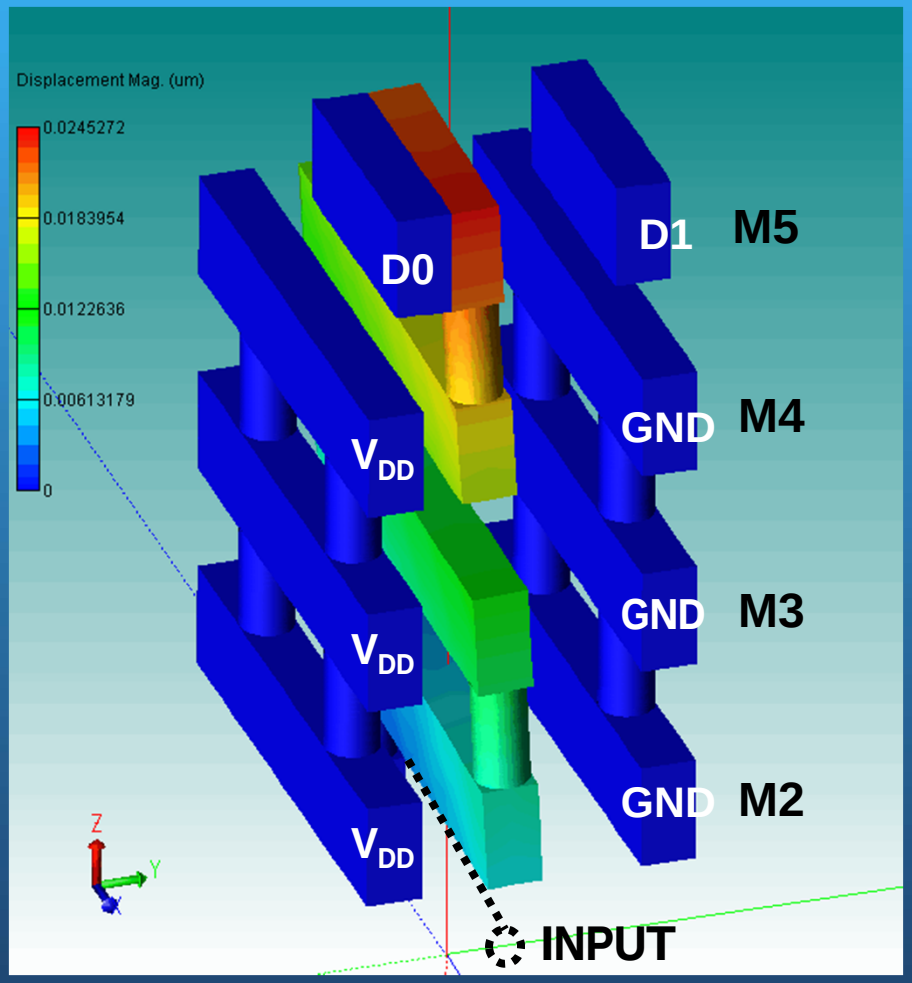


D. C. Edelstein (IBM),
214th ECS Meeting, Abstract #2073, 2008



S. Natarajan *et al*. (Intel), *IEDM* 2014

BEOL NEM Relay



courtesy of Dr. Kimihiko Kato (UC Berkeley)

- A 5-terminal switch can be implemented using 4 interconnect layers
  - Vias are used for electrical connection and as torsional elements for lower k_{eff}
- Fixed actuation electrodes on opposite sides of movable structure

→ 2 stable states (contacting D_0 or D_1)

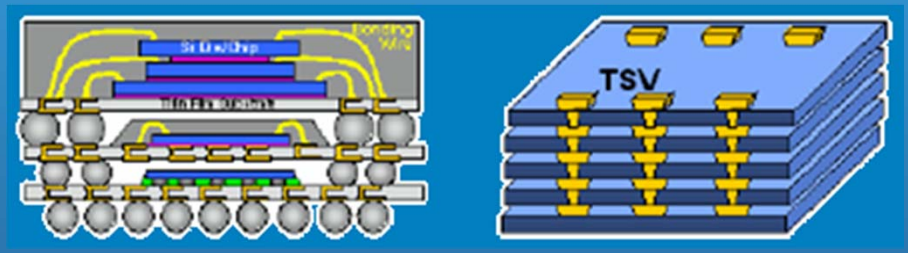
Outline

- The path to 3D Transistors
  - The CMOS Power Crisis
  - Improving Energy Efficiency
- **Pathways to 3D Integration**
- Summary

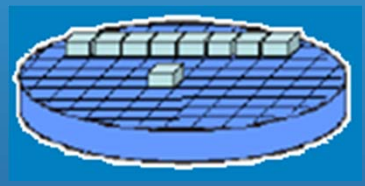
3D Packaging

System in Package (SiP), Package on Package (PoP), *etc.*

- **Enabled by wire bonding and/or flip-chip bonding**



Packaging-based Chip Stack



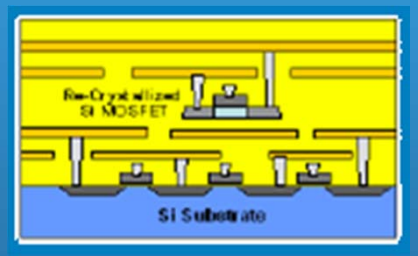
Die-to-Wafer Bonding

- ✓ **Smaller form factor**
- ✓ **Reduced packaging cost**
- ✓ **Reduced power consumption**
- × **Limited interconnection density**

J. J.-Q. Lu *et al.*, *Future Fab International*, Issue 23, 2007

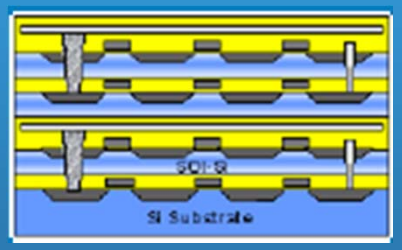
3D Transistor Stacking

- Transistor layers can be embedded between interconnect layers



Laser-crystallized Si

Polycrystalline Si

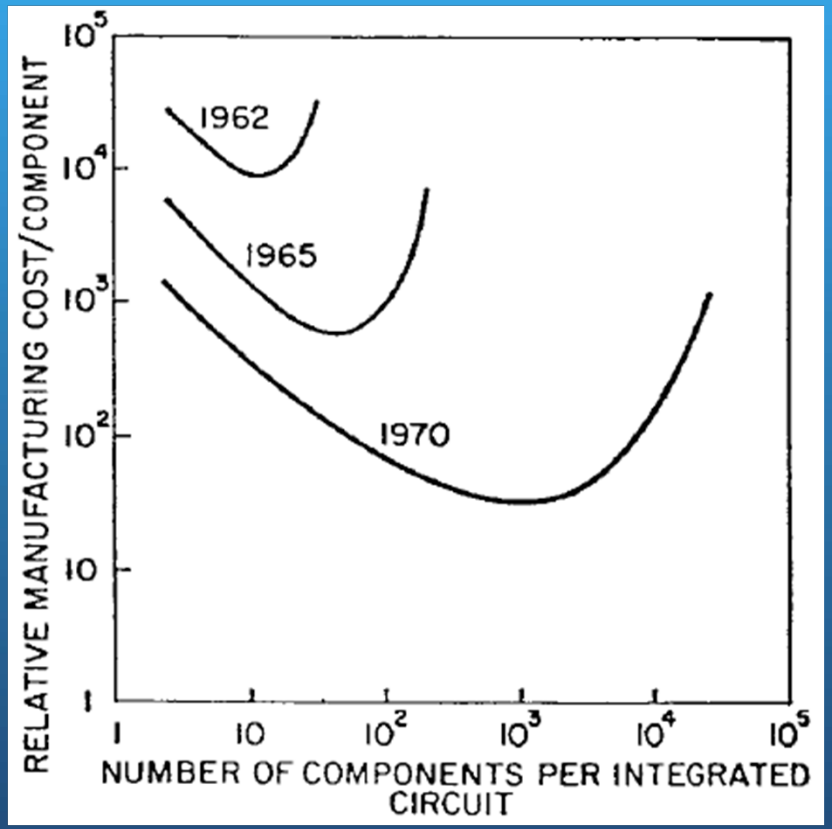


Bonded Si (on oxide)

- ✓ Higher transistor density
- ✗ Heat dissipation
- ✗ Thermal process limitations
- ✗ EDA tool adaptation

J. J.-Q. Lu *et al.*, *Future Fab International*, Issue 23, 2007

Moore's 1965 Paper Revisited

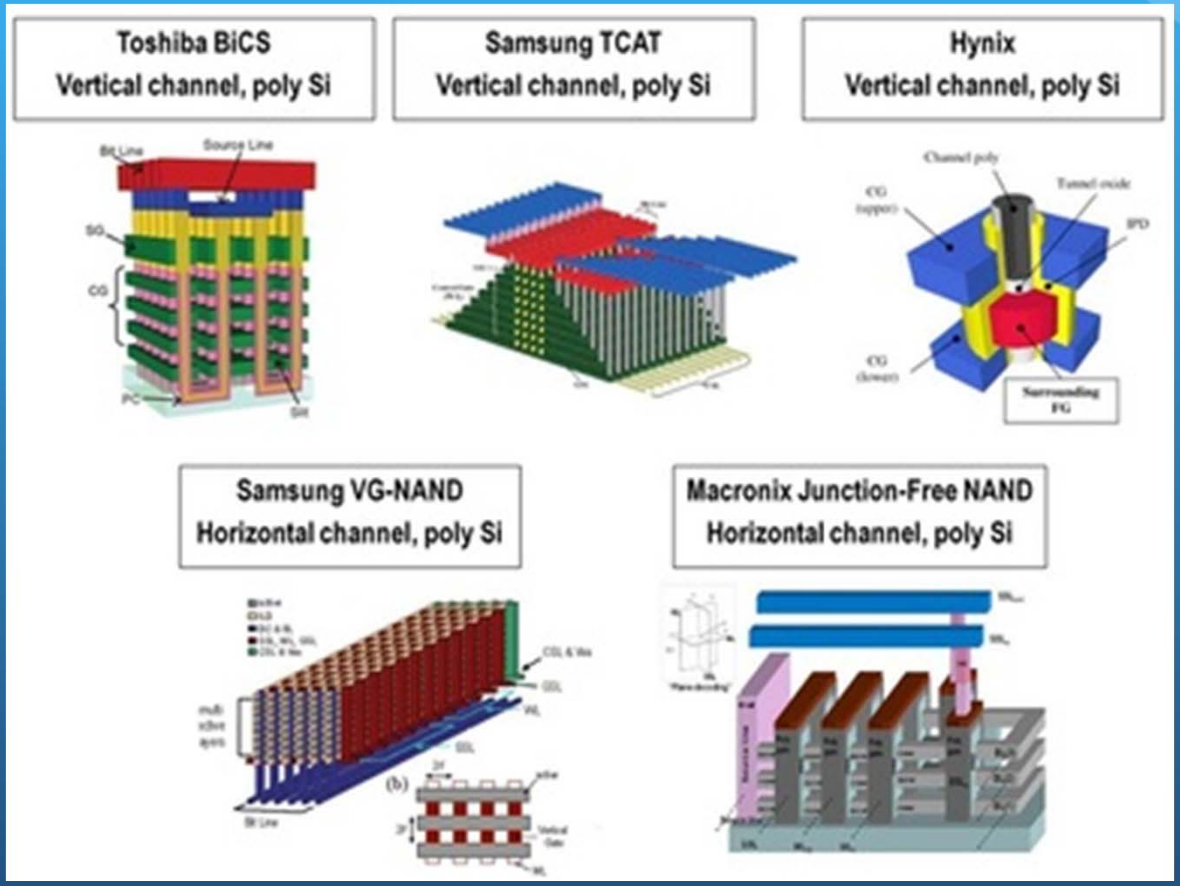


- The minimum cost point moves to a larger number of components per IC over time, as manufacturing technology advances (*i.e.* yield improves).

➔The primary reason for increasing the number of components per IC was (and still is) lower cost.

*Gordon E. Moore, "Cramming more Components onto Integrated Circuits," *Electronics*, pp. 114-117, April 1965

3D NAND Flash Technology

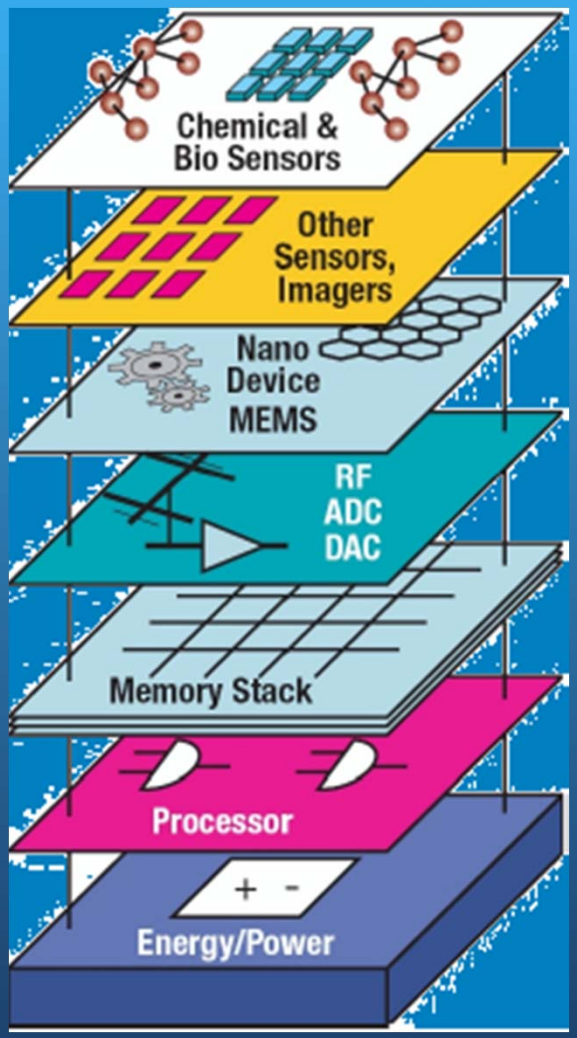


- Poly-Si is used as the semiconductor material.
- Lithography steps for multiple memory layers are shared.

- Density scaling is not driven by lithography.
- Aspect ratios of etched and filled features are very large (>40:1).

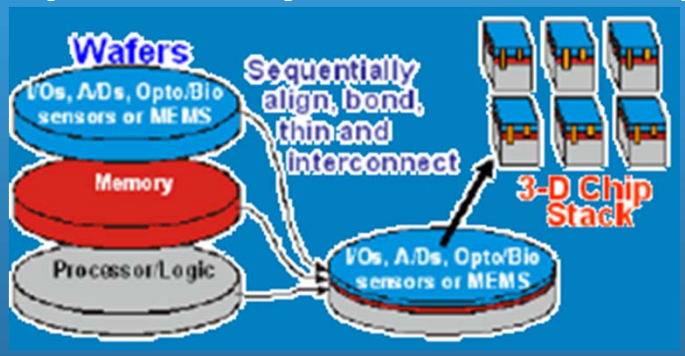
http://www.monolithic3d.com/uploads/6/0/5/5/6055488/695394.jpg?388

Heterogeneous Integration

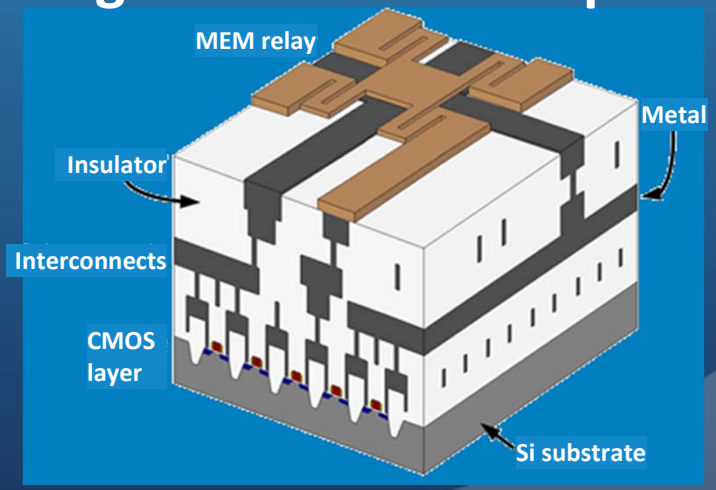


Enhanced performance & functionality in a compact form factor

- **Separate layer fabrication processes**



- **Integrated fabrication process**



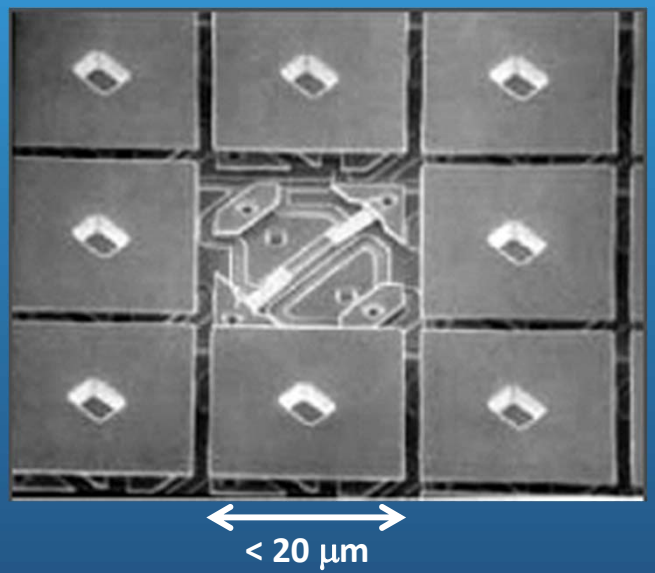
J. J.-Q. Lu *et al.*, *Future Fab Int'l*, Issue 23, 2007

V. Pott *et al.*, *Proc. IEEE*, Vol. 98, 2010

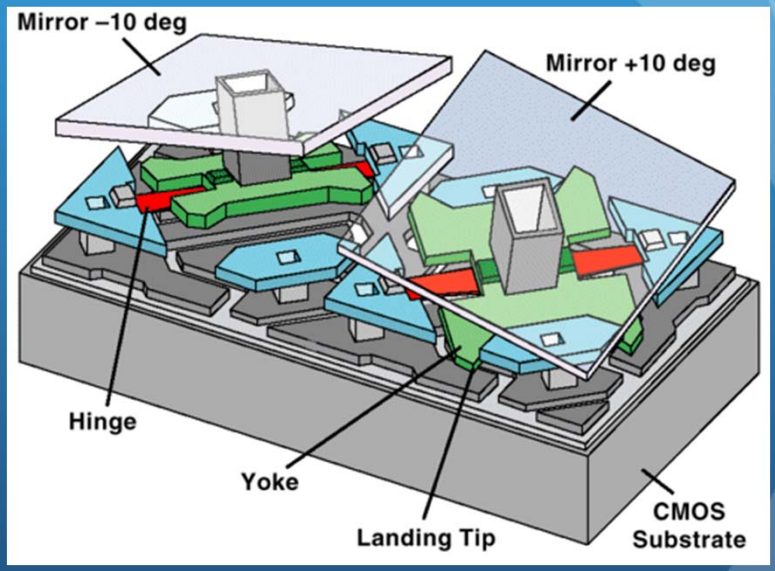
DMD™ Projection Display Chip

- Electrostatically actuated mirrors built over CMOS circuitry
  - Structural layers comprise Al alloys; sacrificial material is photoresist

SEM image of pixel array



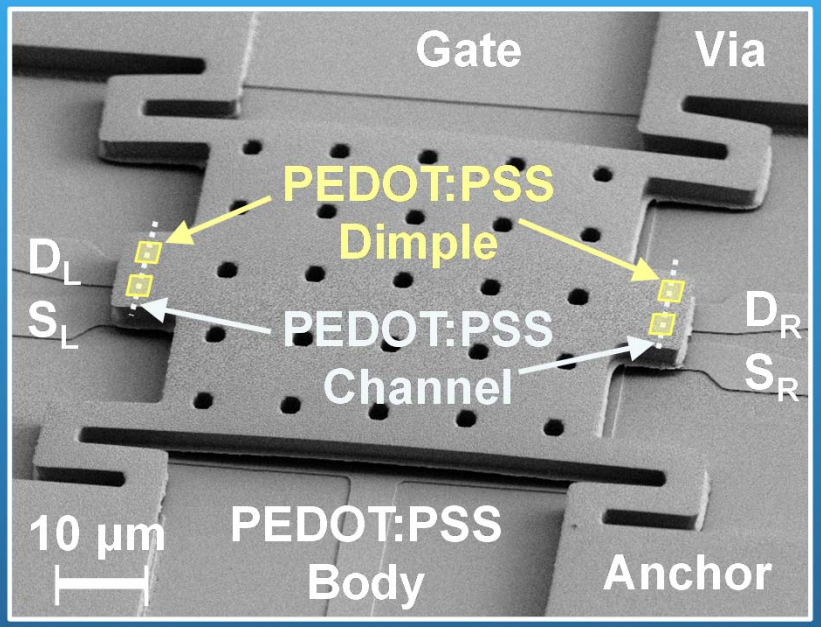
Schematic of 2 pixels



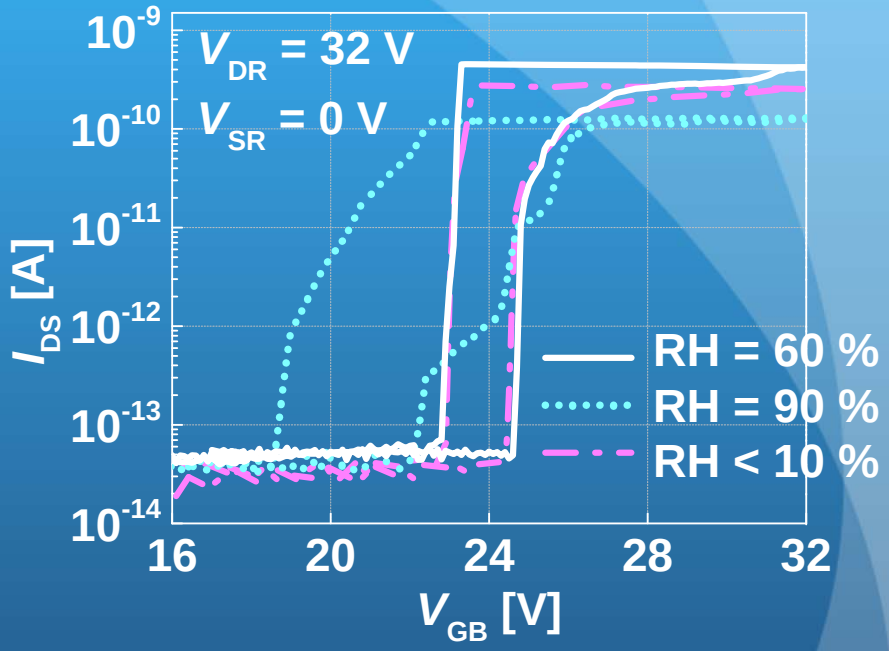
Each mirror corresponds to a single pixel, programmed by an underlying memory cell to deflect light either into a projection lens or light absorber.

Polymeric Relay

Plan-View SEM



Measured *I-V* Characteristics



- Transparent relay fabricated with a CMOS-compatible process:
  - SU-8 photoresist as structural material
  - Fluorinated photoresist (OSCoR 4000) as dielectric material
  - SiO_2 as sacrificial material
- Can be used as a humidity sensor

Y. Pan *et al.*, *28th IEEE Int'l Conf. MEMS*, pp. 940-943, 2015

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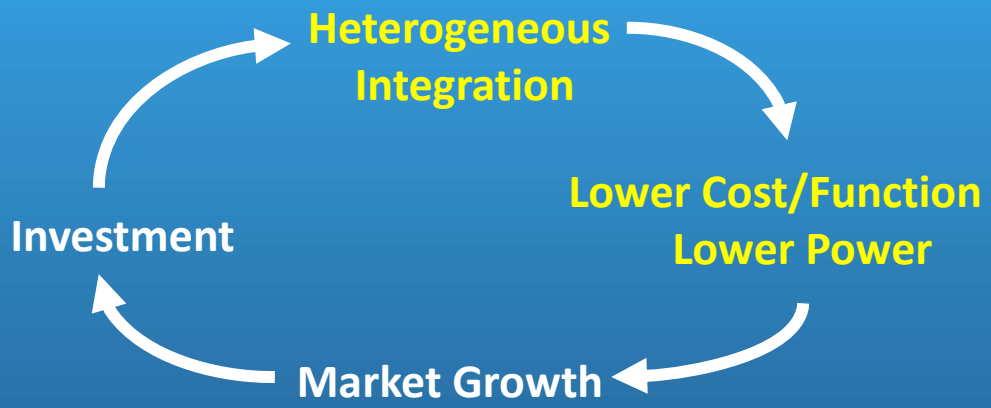
- Pathways to 3D Integration
- Summary

Summary

- 3D transistors and 3D integration provide for improvements in IC energy efficiency and functionality, to sustain the Si revolution.



- Information technology will be
  - pervasive
  - embedded
  - human-centered
  - solving societal-scale problems