14 nm chip X-SEM from www.intel.com/content/dam/www/public/us/en/documents/pdf/foundry/mark-bohr-2014-idf-presentation.pdf

There's Plenty of Room at the Bottom - and at the Top

Tsu-Jae King Liu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley

August 16, 2016

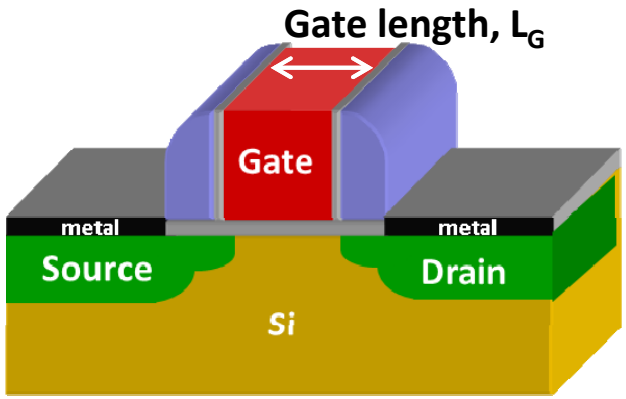
SFBA Nano Seminar

Outline

- **Introduction**
  - Transistor scaling limit
- **Extending the Era of Moore's Law**
- **Beyond Moore: Mechanical Computing Redux**
- **Summary**

MOSFET Operation: Gate Control

Metal-Oxide-Semiconductor (MOS)
Field-Effect Transistor (FET)

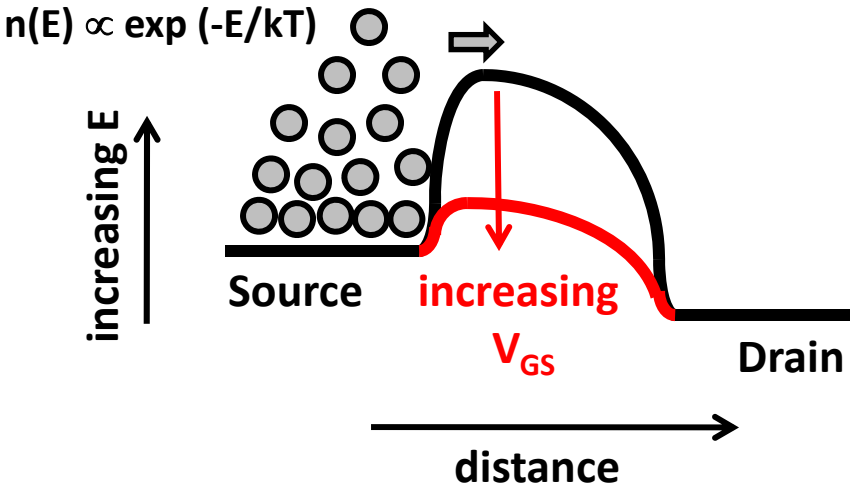


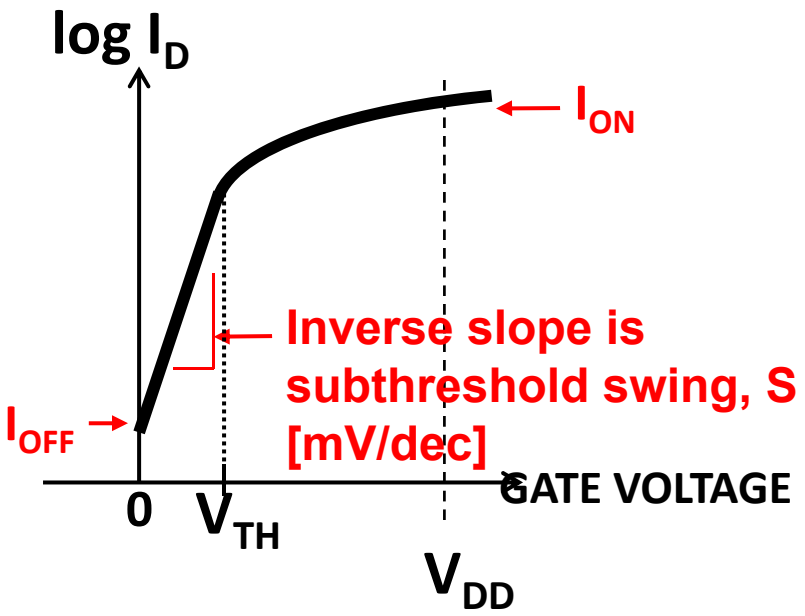
Current flowing between Source & Drain is controlled by the Gate voltage.

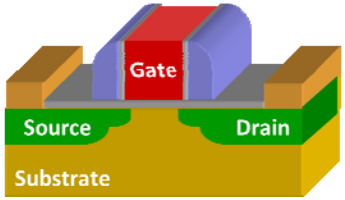
Desired characteristics:

- **High ON current**
- **Low OFF current**

Electron Energy Band Profile



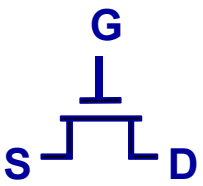




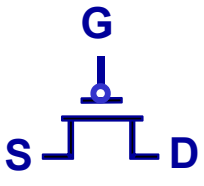
CMOS Circuits

CIRCUIT SYMBOLS

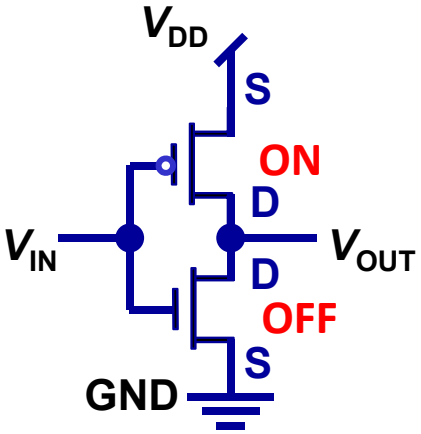
N-channel MOSFET

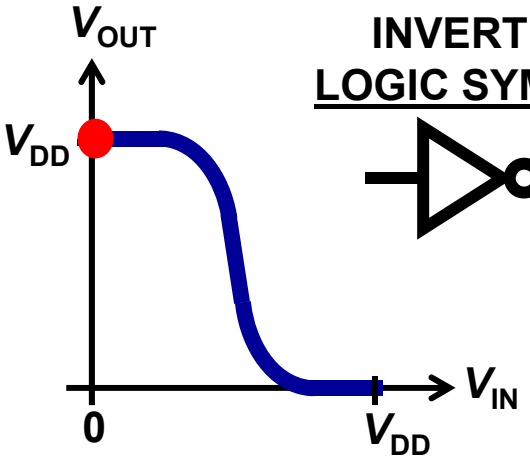


P-channel MOSFET



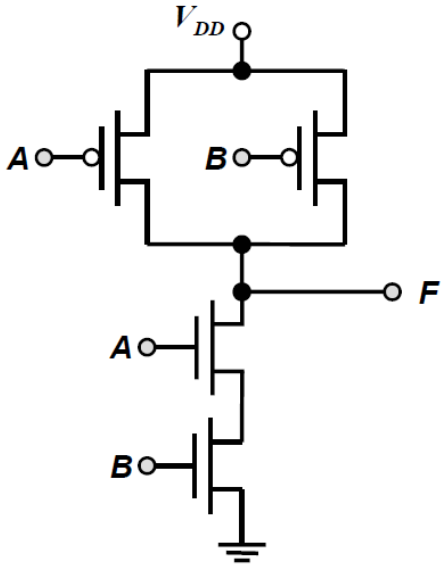
CMOS INVERTER CIRCUIT





INVERTER LOGIC SYMBOL

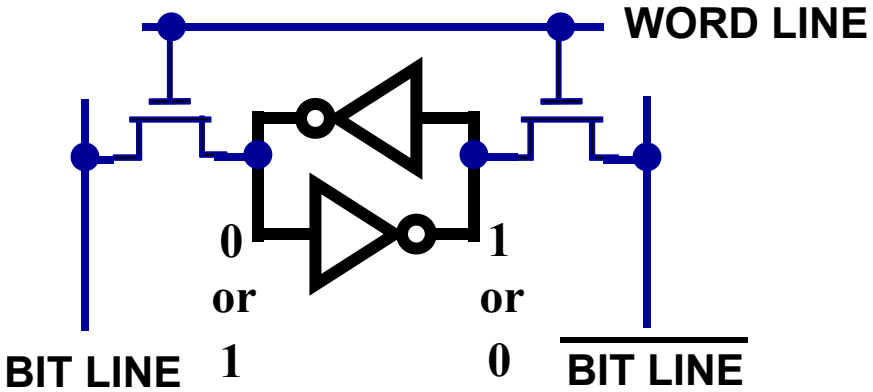
CMOS NAND GATE



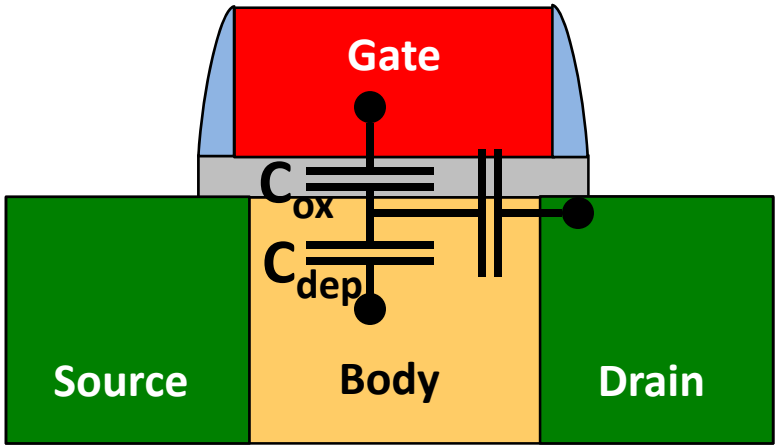
NOT AND (NAND) TRUTH TABLE

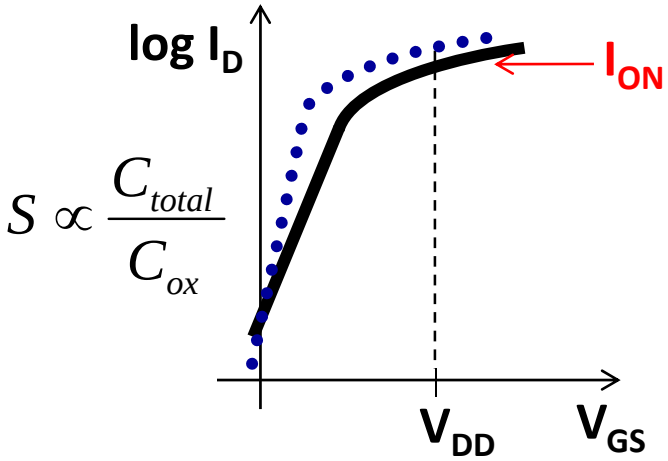
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

STATIC MEMORY (SRAM) CELL



Improving I_{ON}/I_{OFF}

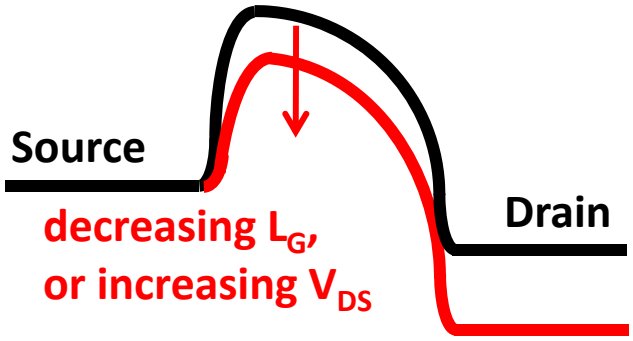


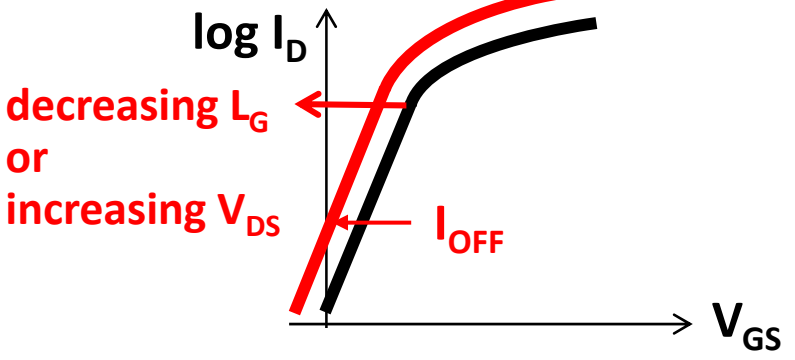


- **The greater the capacitive coupling between Gate and channel, the better control the Gate has over the channel potential.**

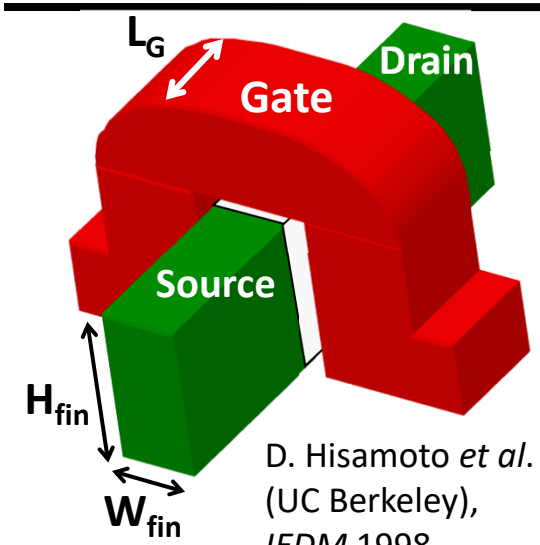
  →higher I_{ON}/I_{OFF} for fixed V_{DD}, or lower V_{DD} to achieve target I_{ON}/I_{OFF}

  →reduced short-channel effect and drain-induced barrier lowering:

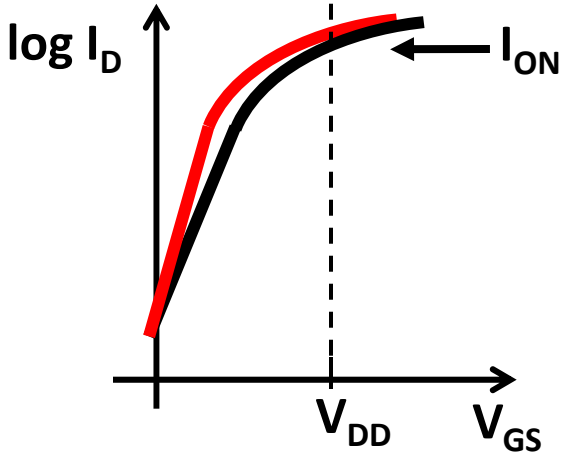




FinFET/Tri-Gate Transistor



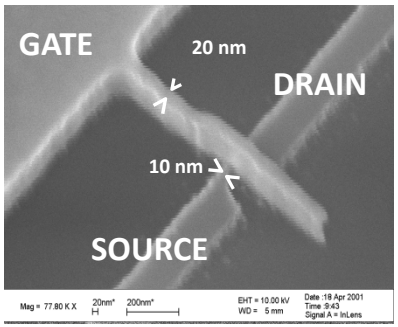
D. Hisamoto *et al*. (UC Berkeley), *IEDM* 1998



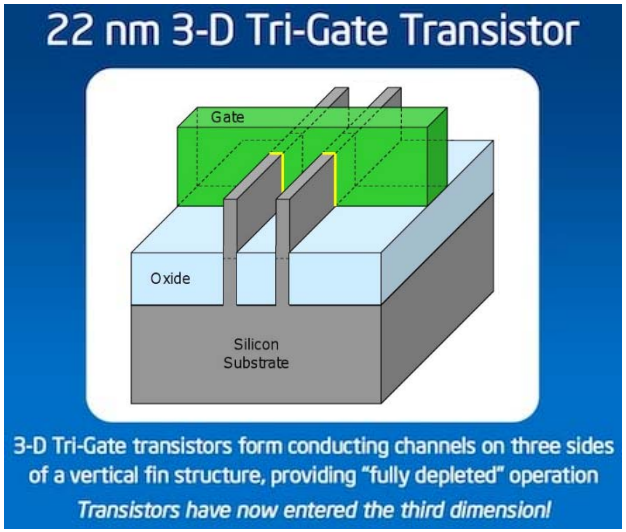
- **Superior gate control**

→higher I_{ON}/I_{OFF} or lower V_{DD}

15nm L_g FinFET



Y.-K. Choi *et al*., (UC Berkeley) *IEDM* 2001



Intel Corp., May 2011

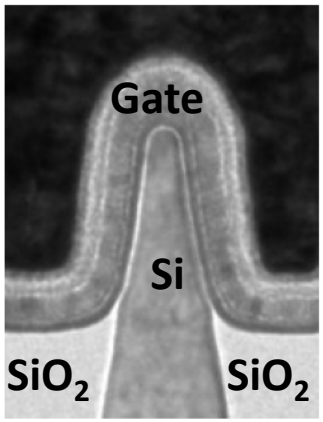
- **Multiple fins can be connected in parallel to achieve higher drive current.**

3-D Transistor Technology Roadmap

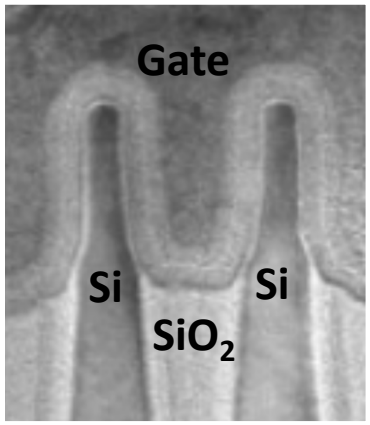
Year:	2012	2014	2017
Intel Technology Node	22 nm	14 nm	10 nm

Year:	2015		
Foundry Technology Node:	14 nm	10 nm	7 nm
Gate length, L_G	25 nm	20 nm	15 nm
Fin width, W_{fin}	~10 nm	~8 nm	~6 nm
Equivalent oxide thickness	0.9 nm	0.85 nm	0.8 nm

X-SEM Images



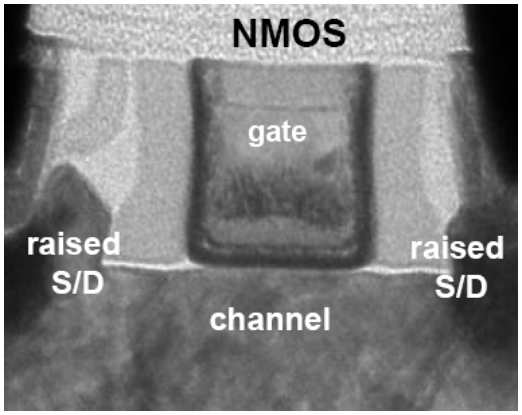
C. Auth *et al*. (Intel Corp.)
VLSI Symp. 2012

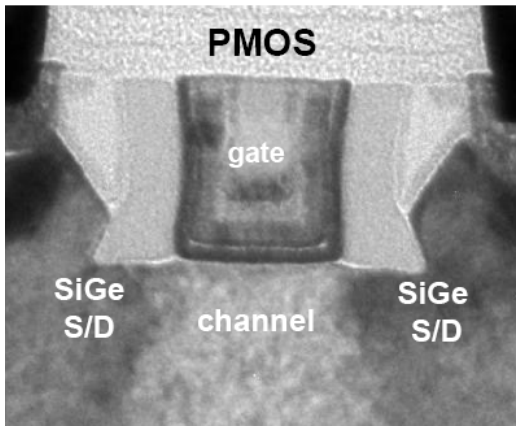


S. Natarajan *et al*. (Intel Corp.)
IEDM 2014

MOSFET Evolution

32 nm
planar

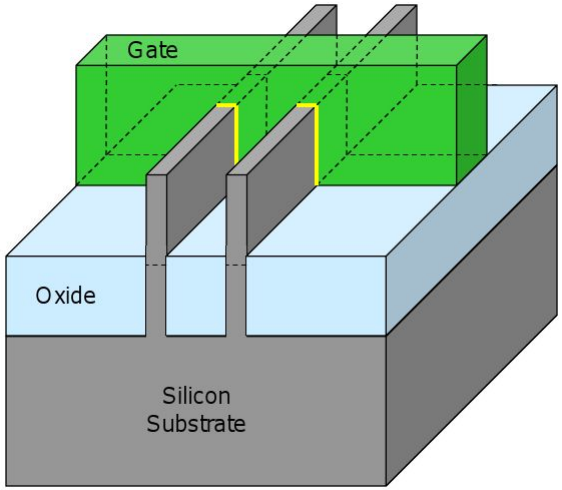




P. Packan *et al*. (Intel), *IEDM* 2009

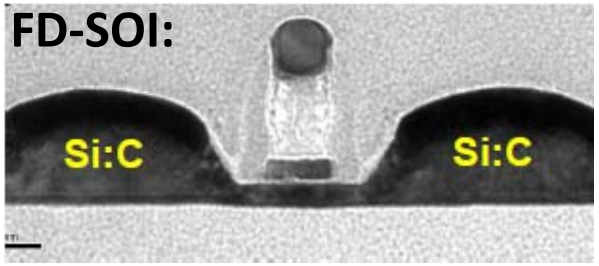
22 nm
thin body

FinFET:



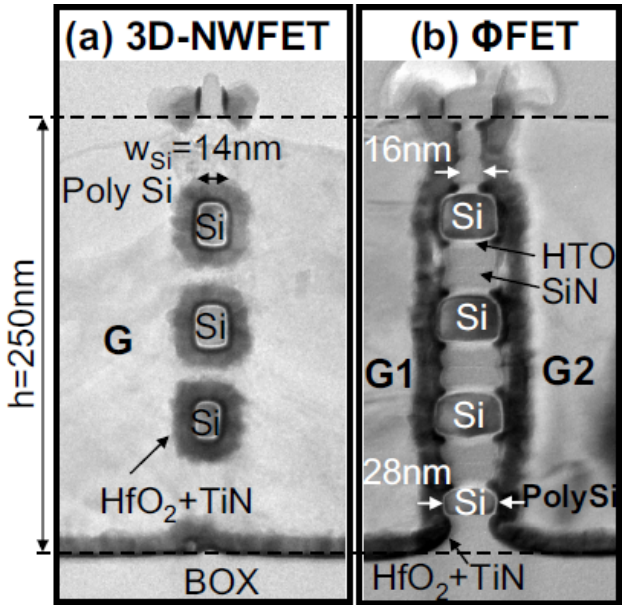
Intel Corp.

FD-SOI:



K. Cheng *et al.* (IBM), *VLSI Symp.* 2011

beyond 7 nm
stacked nanowires?

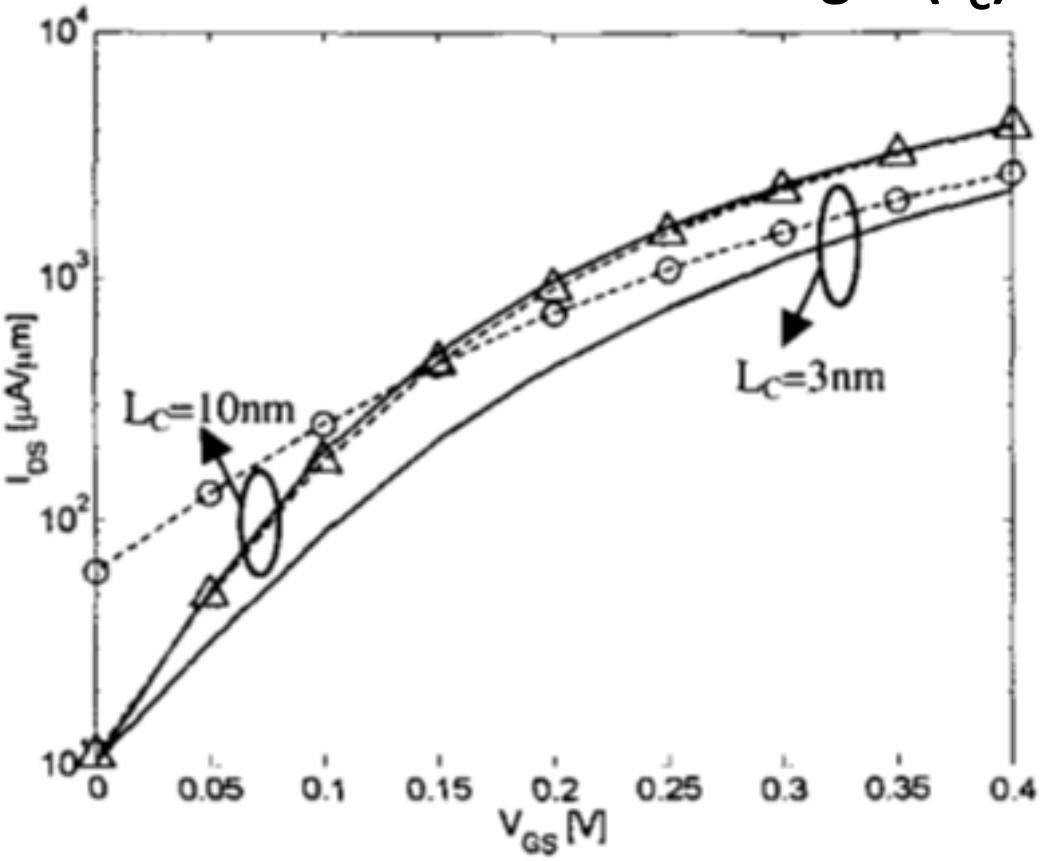


C. Dupré *et al*. (CEA-LETI) *IEDM* 2008

Stacked gate-all-around (GAA) FETs achieve the highest layout efficiency.

Channel-Length Scaling Limit

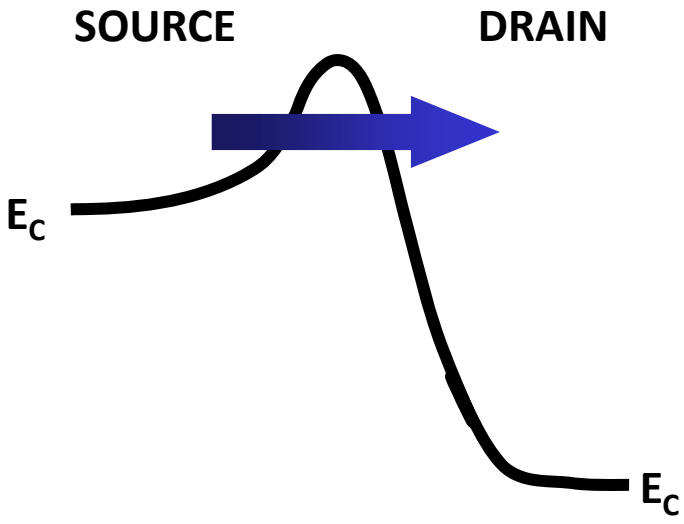
- **Quantum mechanical tunneling sets a fundamental scaling limit for the channel length (L_C).**



J. Wang *et al.*, *IEDM Technical Digest*, pp. 707-710, 2002

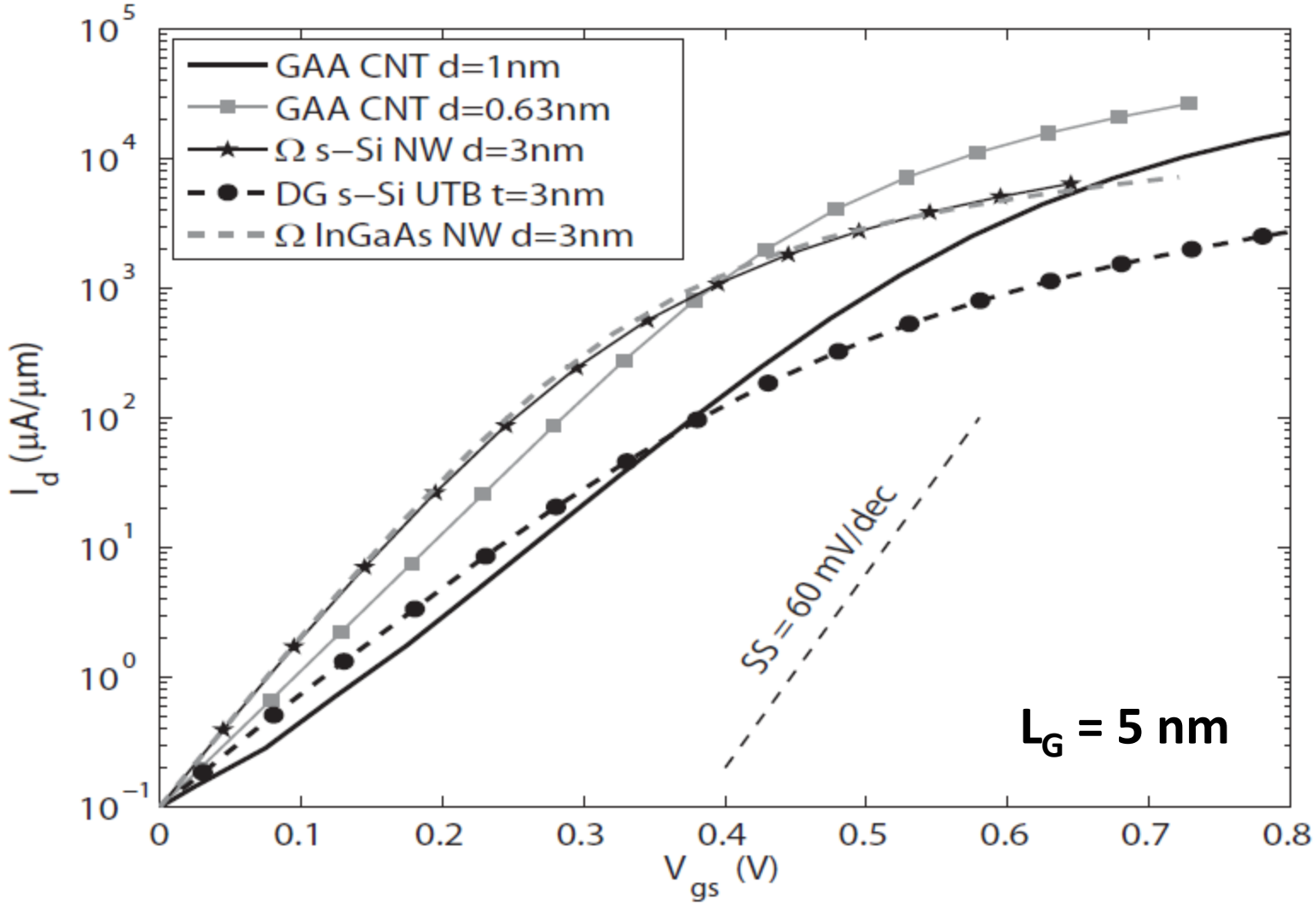
If electrons can easily tunnel through the source potential barrier, the gate cannot shut off the transistor.

nMOSFET Energy Band Diagram
(OFF state)



Ultimately Scaled MOSFETs

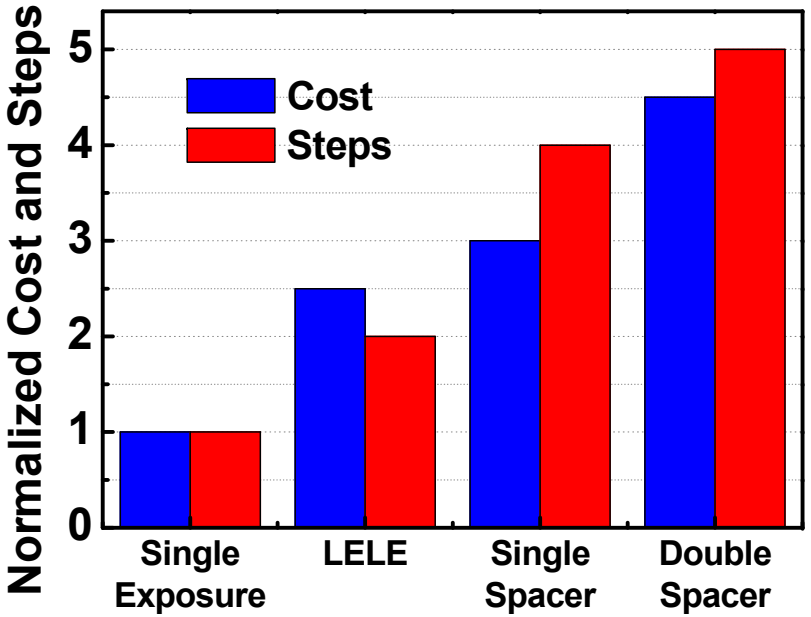
M. Luisier *et al.*, *IEDM* 2011



Outline

- Introduction
- **Extending the Era of Moore's Law**
- Beyond Moore: Mechanical Computing Redux
- Summary

Multiple-patterning techniques have extended Moore's Law beyond the lithographic resolution limit – at increasing cost



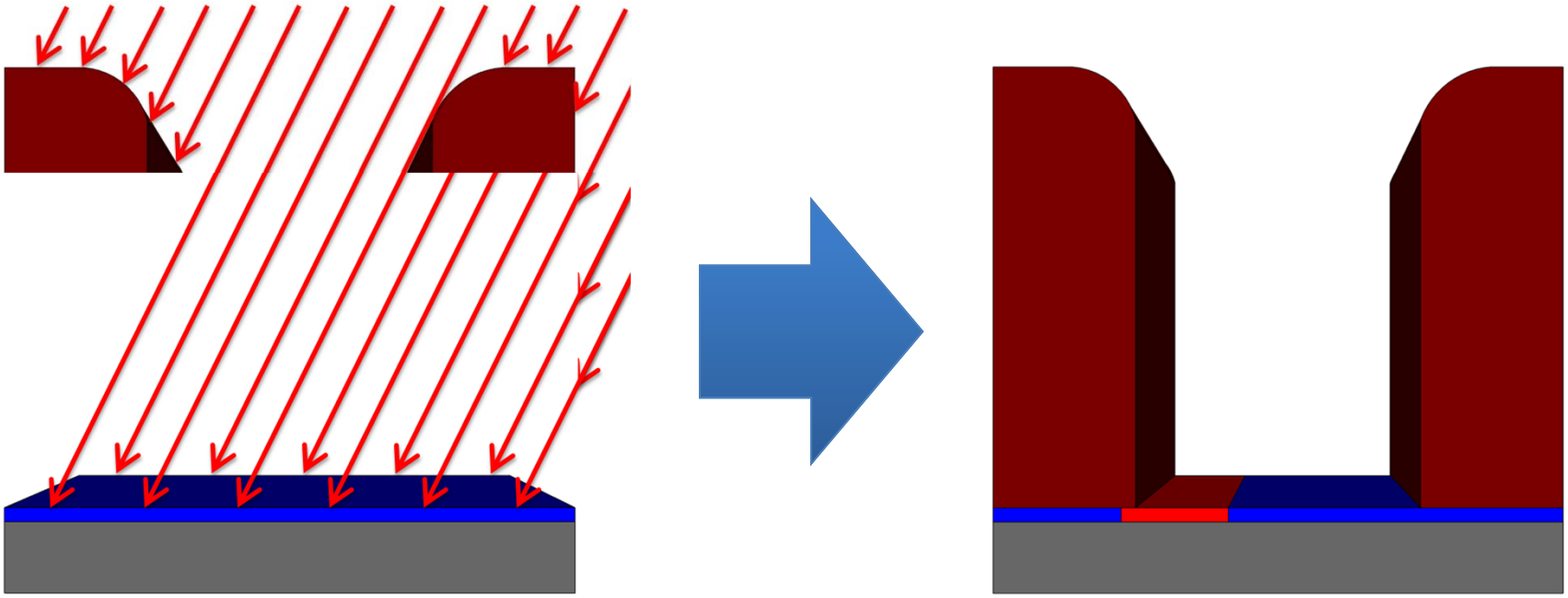
Samsung, EUVL Symposium 2009
ASML, SPIE Advanced Lithography 2012

"The sheer cost and complexity of this lithographic solution could dissuade chipmakers from jumping to future nodes, thereby stunting the growth rates of the IC industry."

- *Semiconductor Engineering*, April 17th, 2014

Tilted ion implantation (TII) Approach

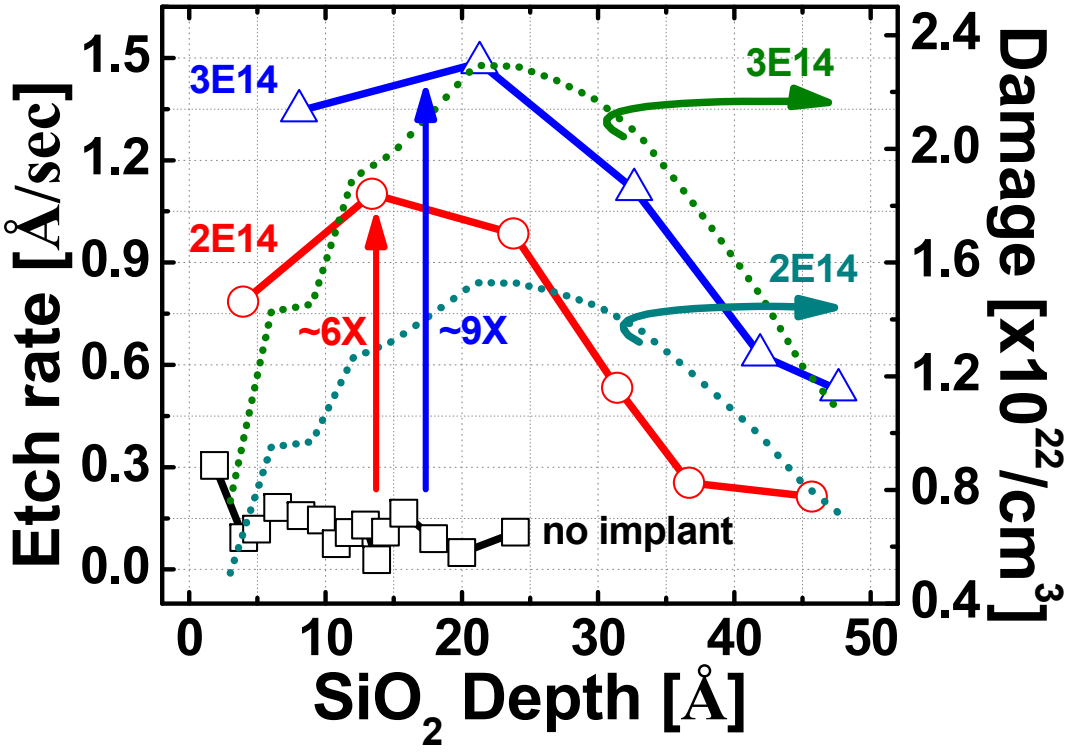
- **A sub-lithographic damage region can be achieved by tilted ion implantation (TII) + photoresist/hard mask**
  - **self-aligned to pre-existing mask features on surface**



Impact of TII on SiO_2 Etch Rate

S. W. Kim *et al.* (UC Berkeley), SPIE Advanced Lithography 2016

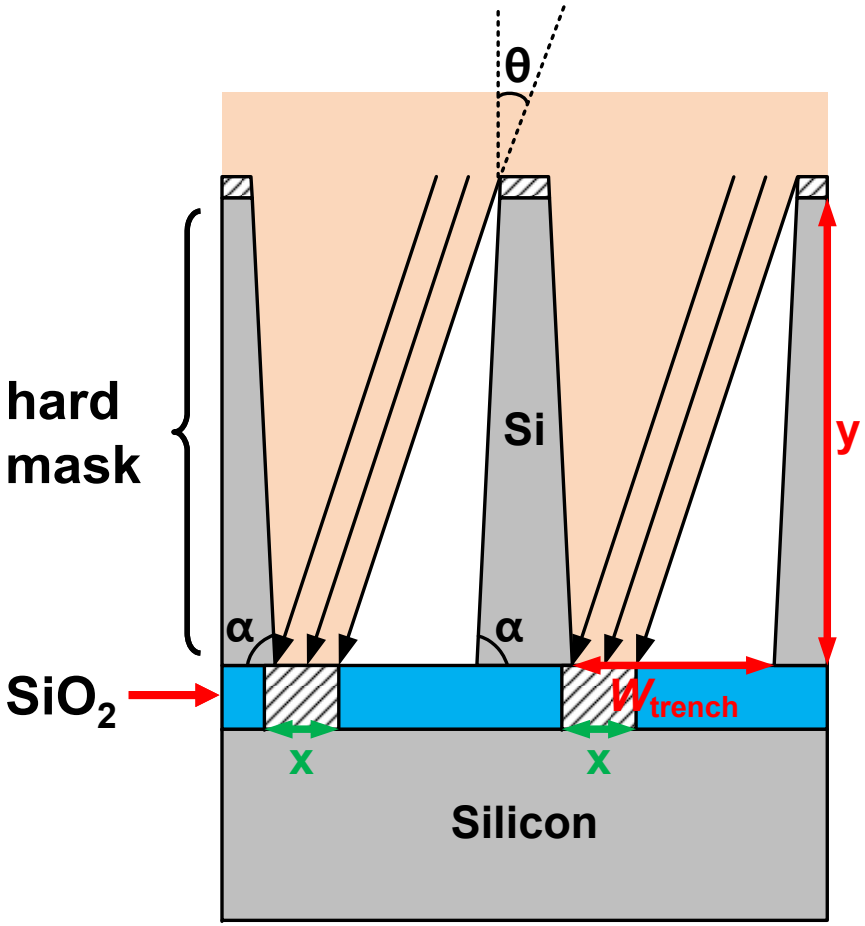
Ar^+ implant conditions: 15° tilt; 1.5 keV; dose = 0, 2 or 3 x $10^{14}/cm^2$



Symbols & solid lines: etch rate in 200:1 DHF

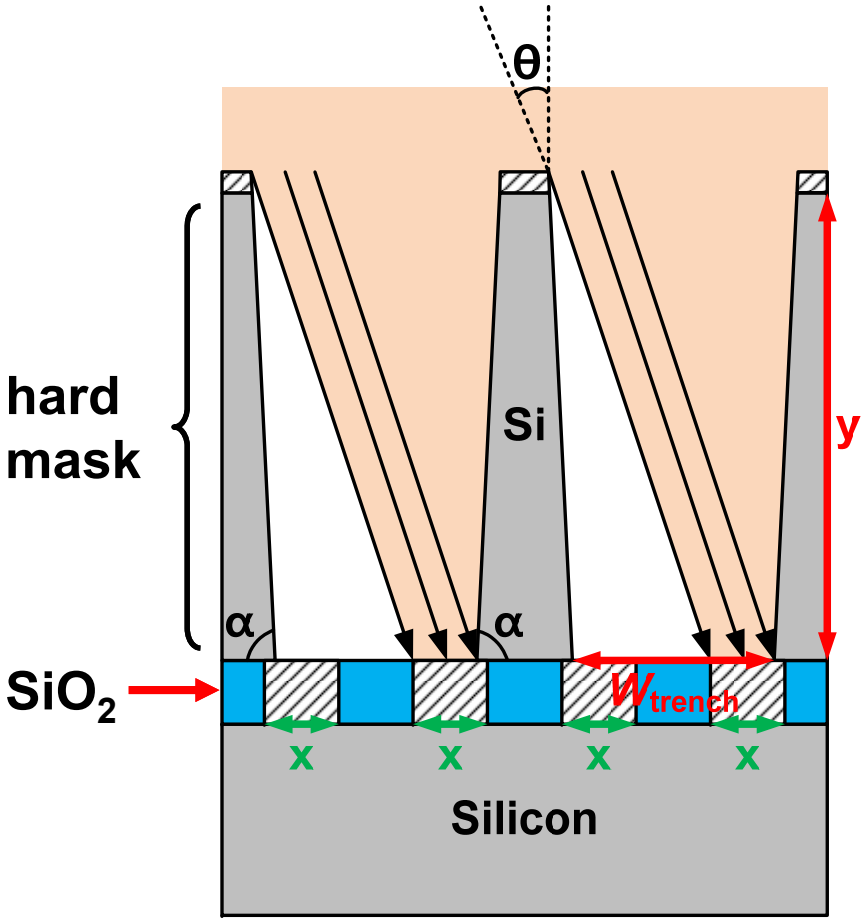
Dotted lines: damage profile (SRIM)

Double-Patterning by TII



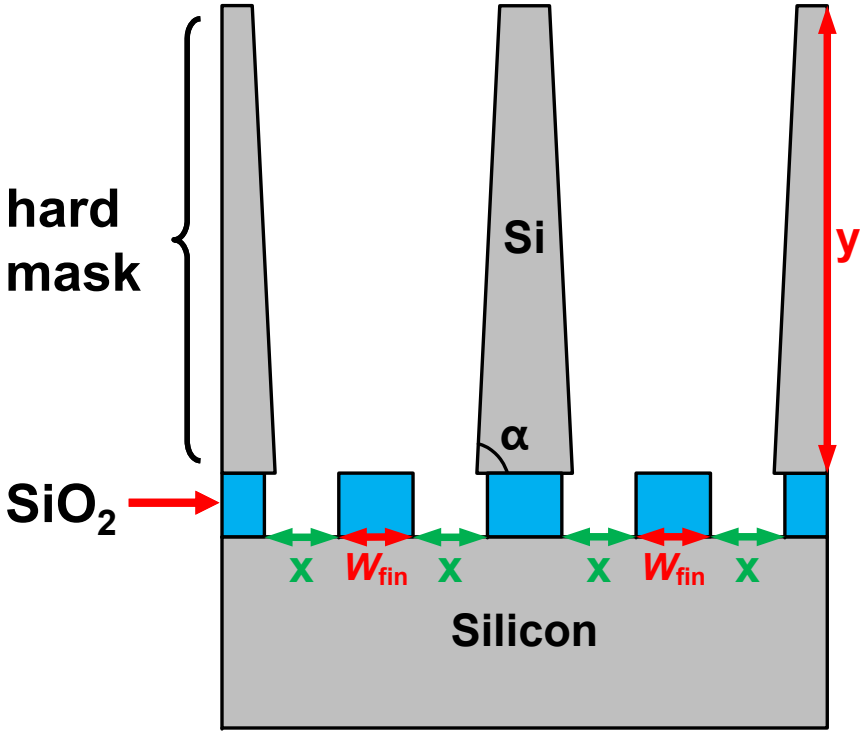
- Thermal SiO_2: masking layer
- Formation of linear a-Si hard-mask features by spacer patterning
- **First implant: positive tilt angle**
  $x \cong W_{trench} - y(\tan(\theta) - \cot(\alpha))$

Double-Patterning by TII



- Thermal SiO_2: masking layer
- Formation of linear a-Si hard-mask features by spacer patterning
- First implant: positive tilt angle
  $x \cong W_{trench} - y(\tan(\theta) - \cot(\alpha))$
- **Second implant: negative tilt angle**
  $x \cong W_{trench} - y(\tan(\theta) - \cot(\alpha))$

Double-Patterning by TII

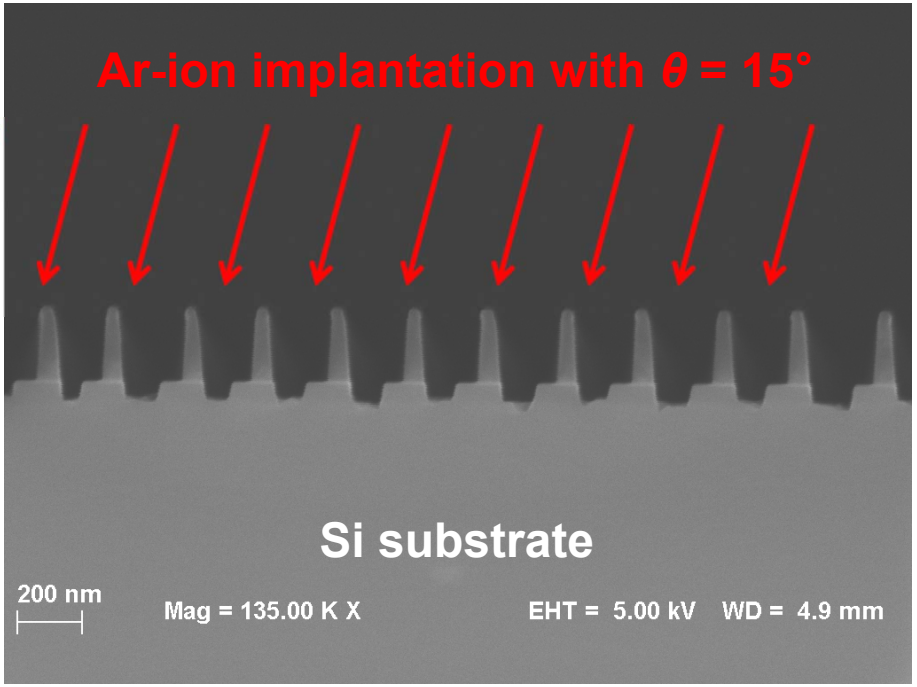


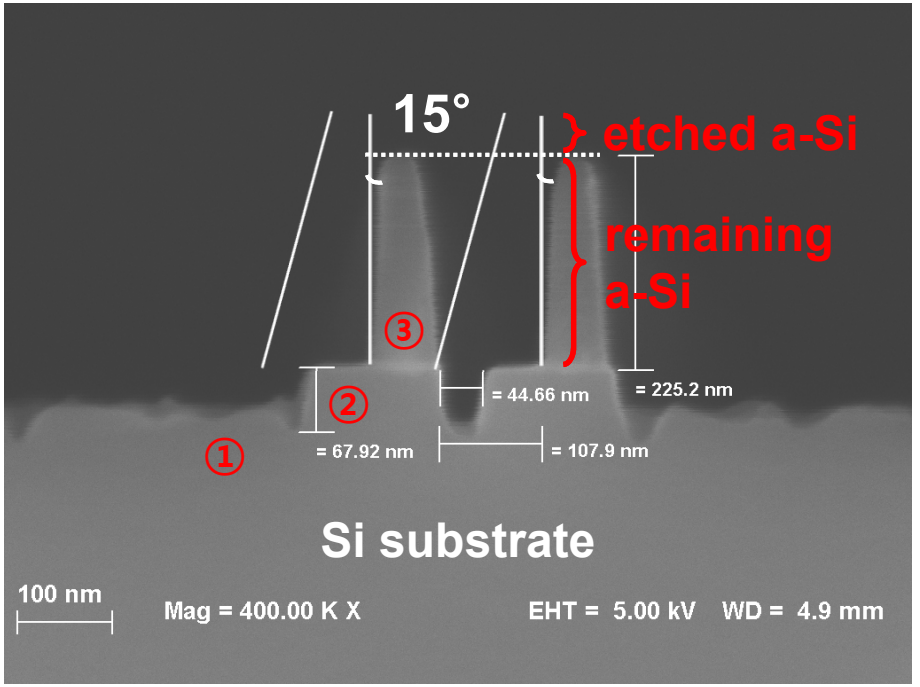
- Thermal SiO_2: masking layer
- Formation of linear a-Si hard-mask features by spacer patterning
- First implant: positive tilt angle
  $x \cong W_{trench} - y(\tan(\theta) - \cot(\alpha))$
- Second implant: negative tilt angle
  $x \cong W_{trench} - y(\tan(\theta) - \cot(\alpha))$
- **Selective removal of damaged SiO_2**
- **Si substrate dry etch**
  $W_{fin} \cong 2y(\tan(\theta) - \cot(\alpha)) - W_{trench}$

Proof of Concept: Single Implant

S. W. Kim *et al.* (UC Berkeley), SPIE Advanced Lithography 2016

Cross-sectional Scanning Electron Micrographs

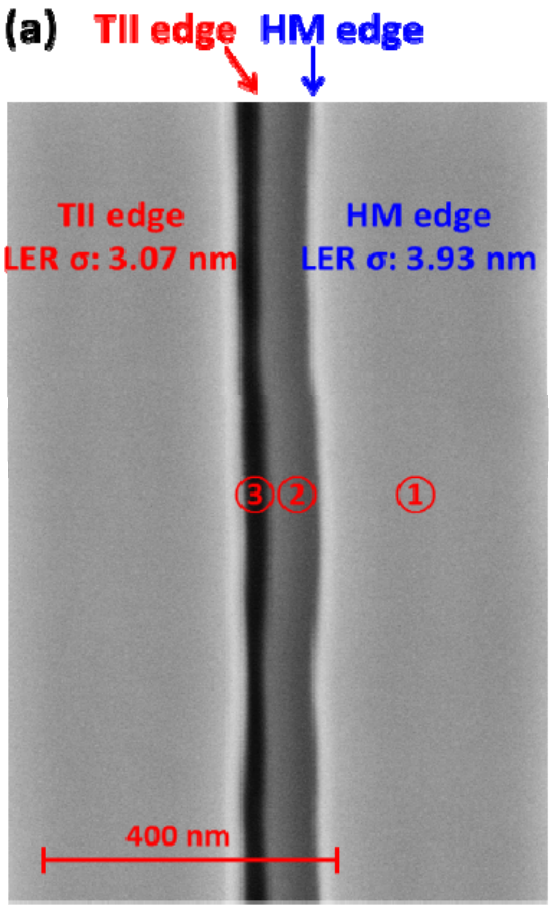


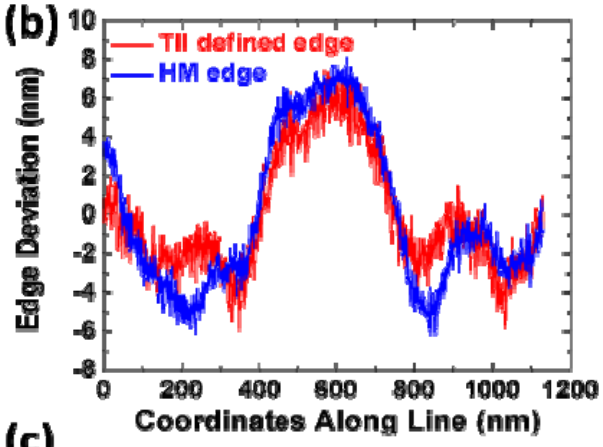


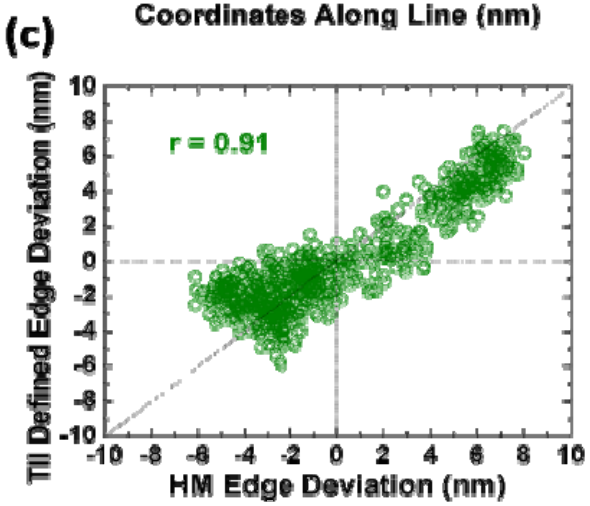
- **Sub-lithographic features (~45 nm) achieved by 15° tilt, 3.0 keV Ar^+ implant into 10 nm-thick SiO_2 hard mask**
  - **→ dilute HF etch**
  - **→ Si dry etch**

Self-Aligned Nature of TII Patterning

P. Zheng *et al.* (UC Berkeley), to be published







- **The TII-defined edge closely tracks the HM edge**

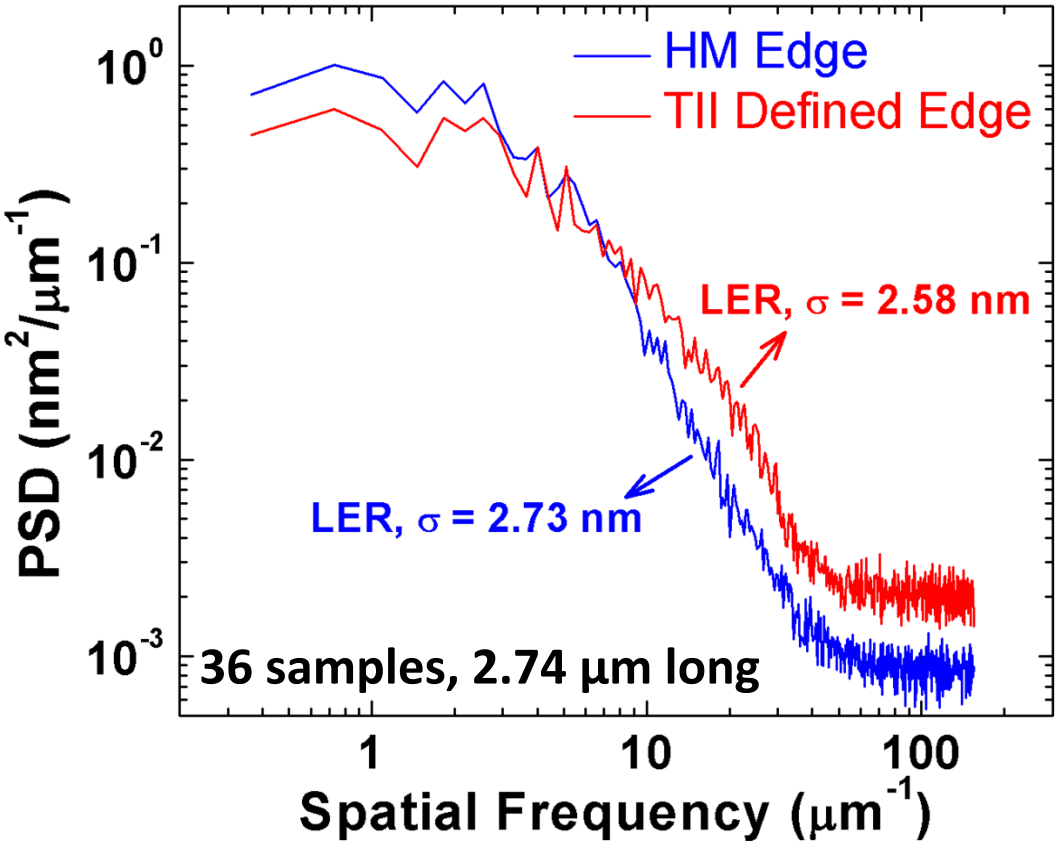
① = a-Si hard mask

② = un-etched c-Si

③ = etched c-Si

Line-Edge Roughness Comparison

P. Zheng *et al.* (UC Berkeley), to be published

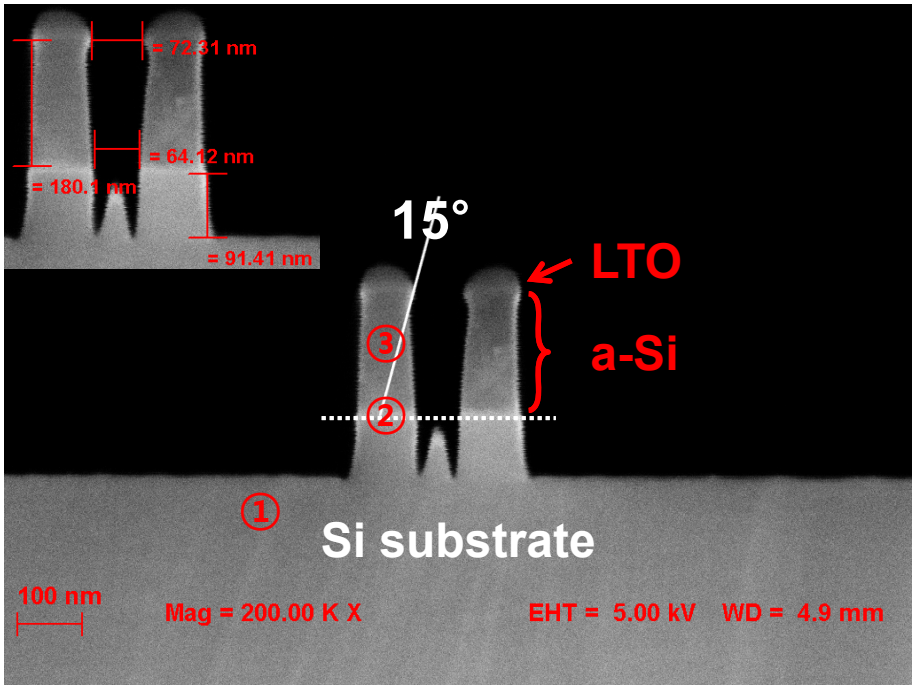


- **TII improves low- and mid-frequency line-edge roughness**

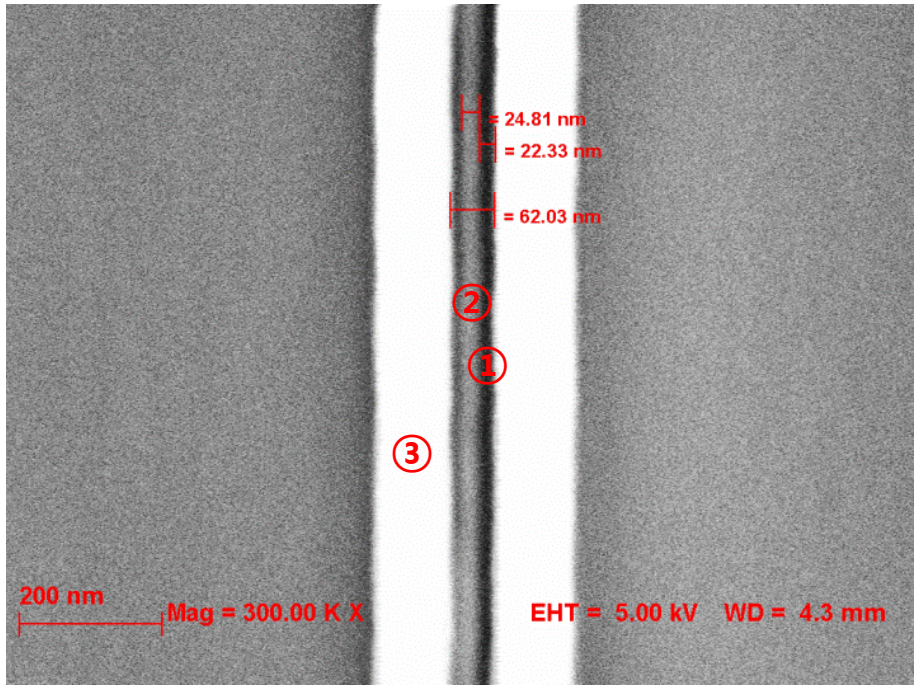
Double Tilted Implant Results

S. W. Kim *et al.* (UC Berkeley), SPIE Advanced Lithography 2016

Cross-sectional SEM



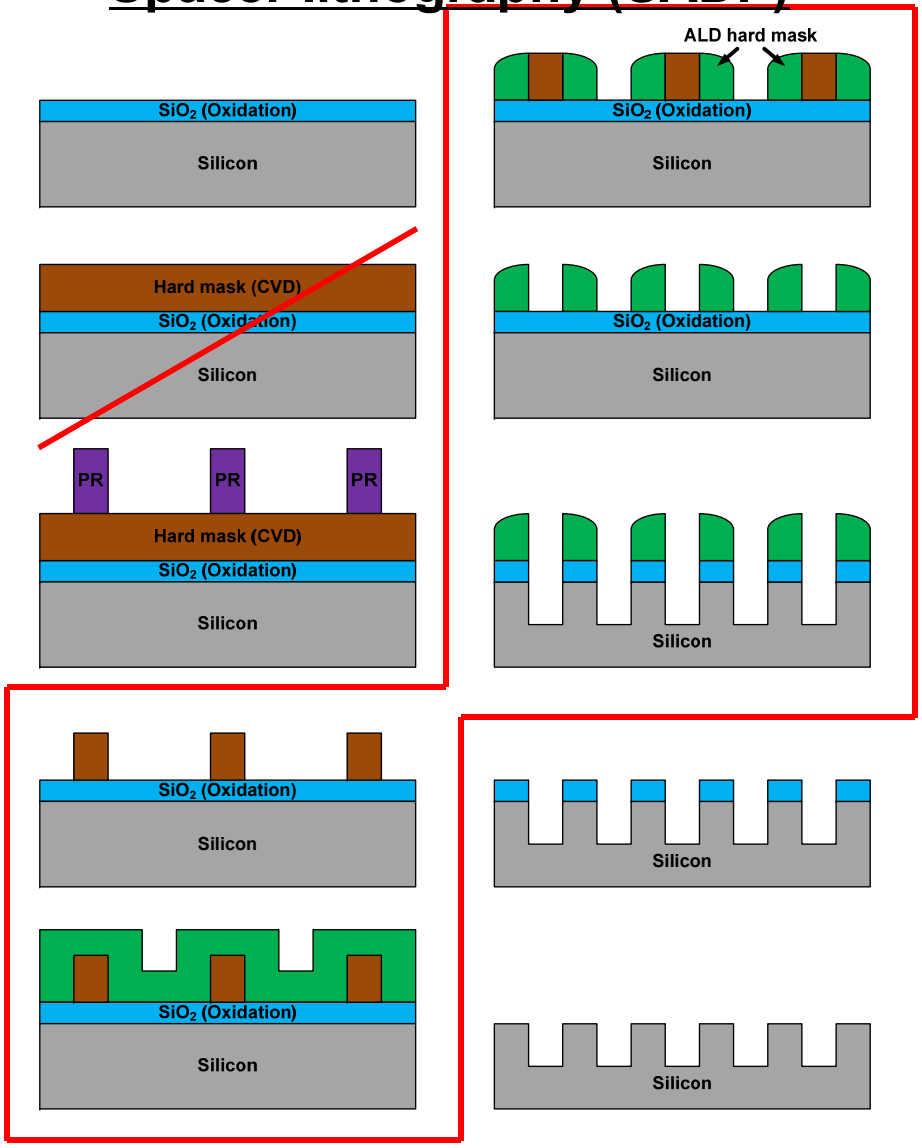
Plan-view SEM



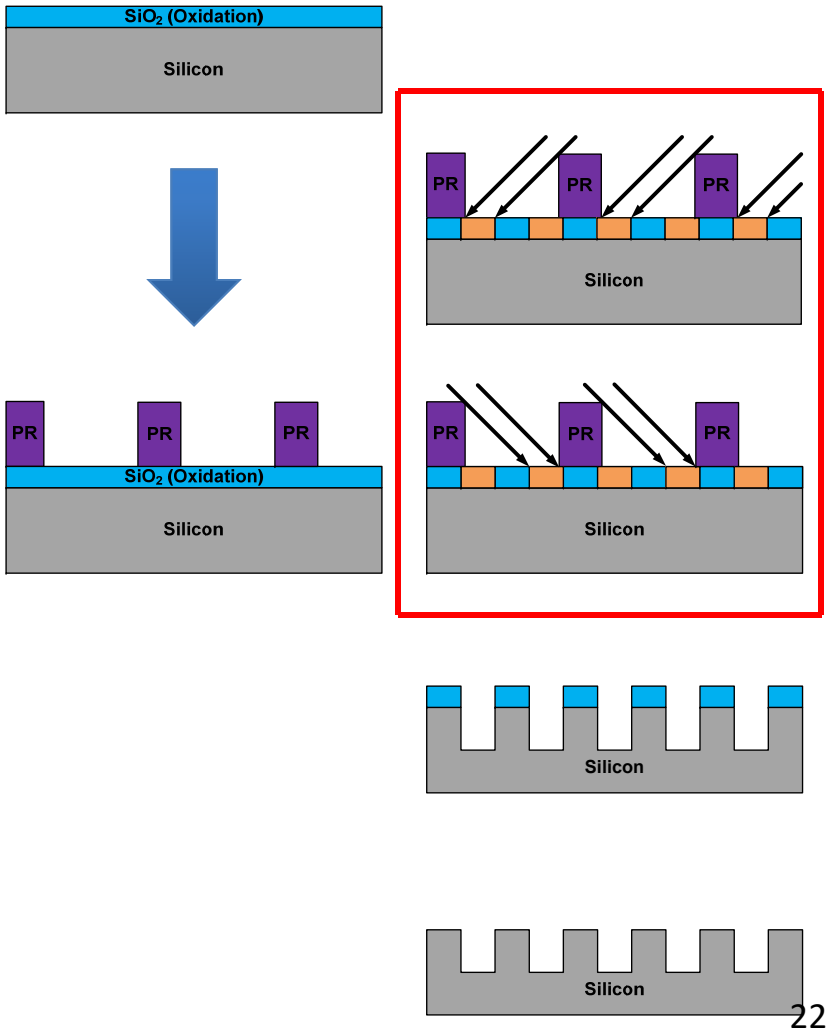
- **Local pitch-halving achieved with ±15° tilt, 3.0 keV Ar^+ implants**
- **~21 nm half-pitch of the etched Si features**

Double-Patterning Approaches

Spacer lithography (SADP)



Tilted Ion Implantation (TII)



Cost Comparison

P. Zheng *et al.* (UC Berkeley), to be published

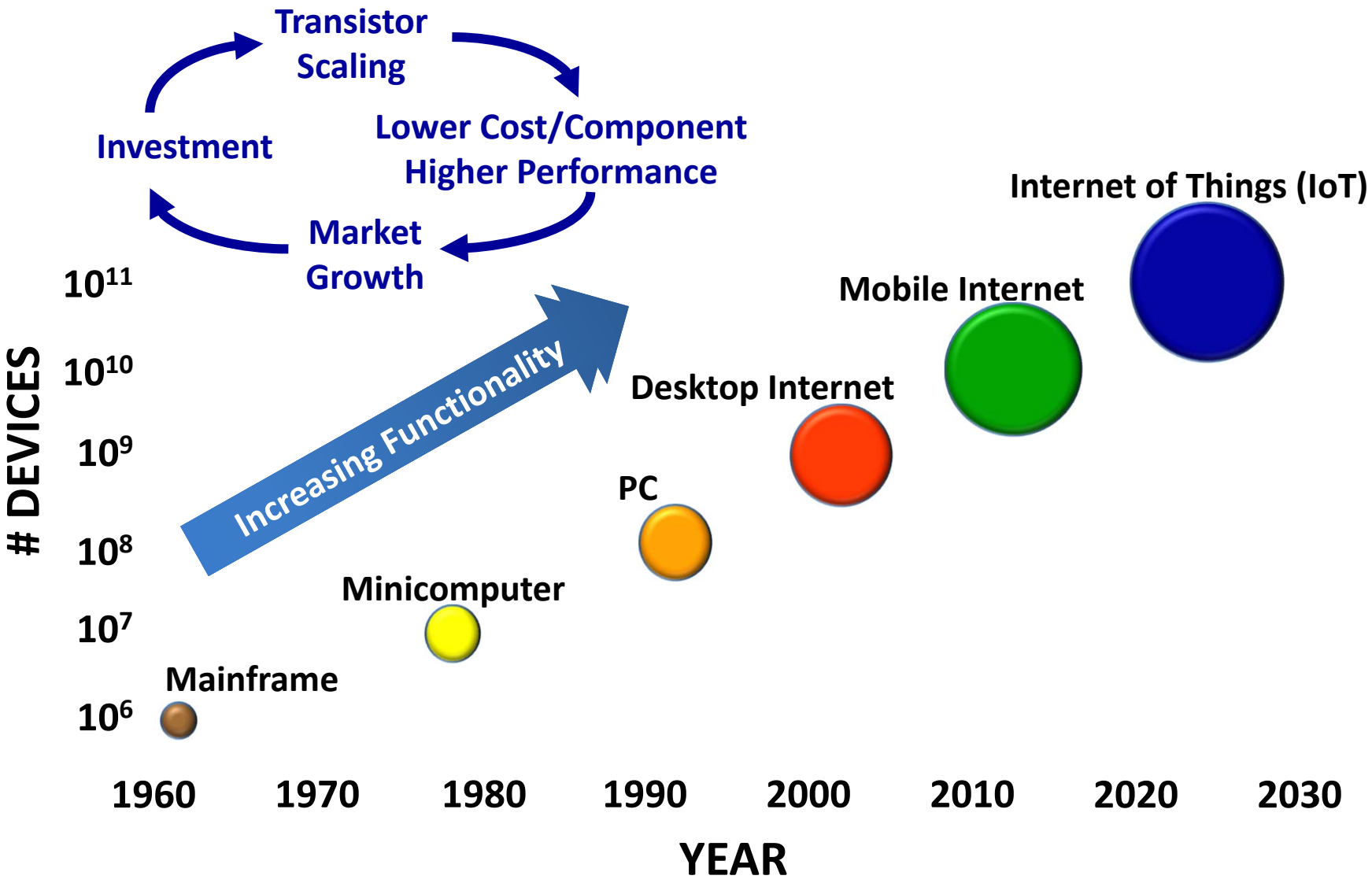
Self-aligned Double Patterning			TII Double Patterning		
Process Steps		Cost	Process Steps		Cost
Process	Description	(a.u./wafer)	Process	Description	(a.u./wafer)
PECVD	Etch stop layer	1.5	LPCVD	Mask layer	2
CVD	Mandrel layer	2	CVD	Mandrel layer	2
Photolithography	Patterning	30	Photolithography	Patterning	30
Dry etch	Mandrel etch	10	Dry etch	Mandrel etch	10
ALD	Spacer deposition	3	Ion implantation	Double implants	1.7
Dry etch	Spacer etch Mandrel pull	16	Wet etch	Selective mask etch	1
Wet clean	Clean	1	Dry etch	Mandrel removal Pattern transfer	16
Dry etch	Pattern transfer Pattern transfer	16	Wet etch	Mask removal	1
Wet etch	Spacer removal	1			
Wet etch	Etch stopper strip	1			
	Total:	81.5		Total:	63.7

- **If photoresist is used as the mandrel layer, the cost of TII double-patterning can be only ~50% of the cost of SADP.**

Outline

- Introduction
- Extending the Era of Moore's Law
- **Beyond Moore: Mechanical Computing Redux**
- Summary

Impact of Moore's Law



Source: Morgan Stanley Research

A Vision of the Future

Ultra-low-power μ-chips required!

The Cloud
(millions)

Mobile devices
(billions)

The Swarm
(trillions)

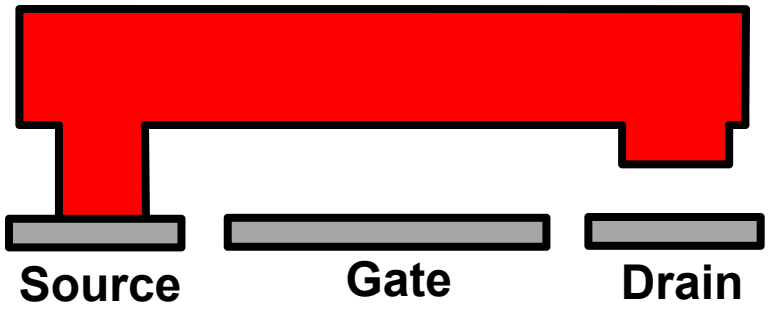
Source: J. Rabaey, *ASPDAC* 2008

Micro-Electro-Mechanical Switch

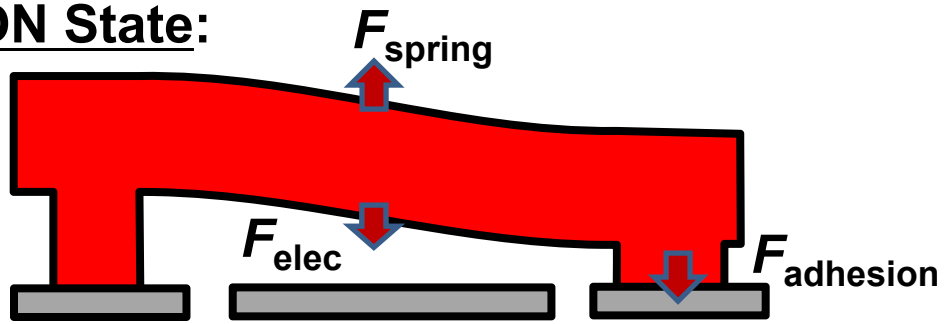
- Zero off-state leakage → Zero passive energy consumption
- Abrupt switching behavior → Low V_{DD} (low active energy)

Three-Terminal Switch

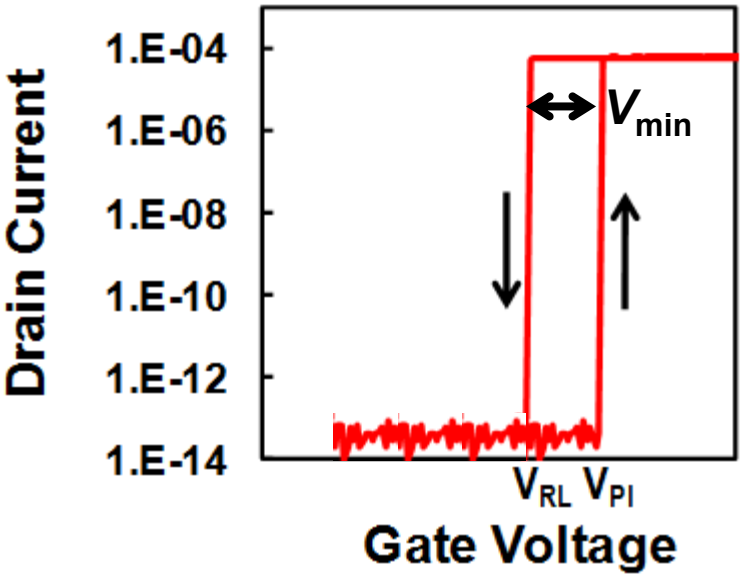
OFF State:



ON State:

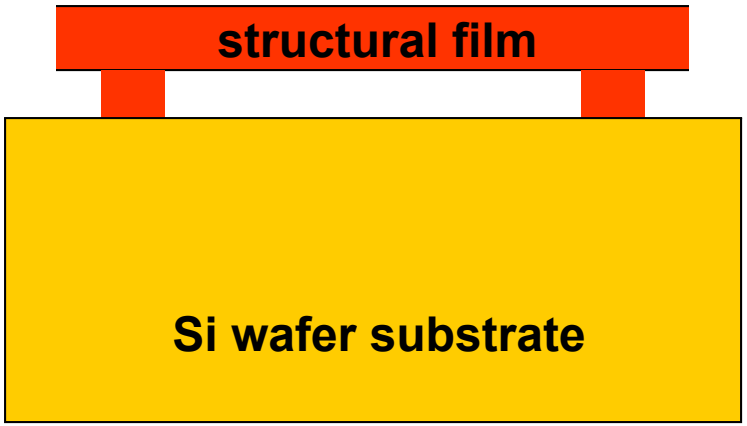


Measured *I-V* Characteristic



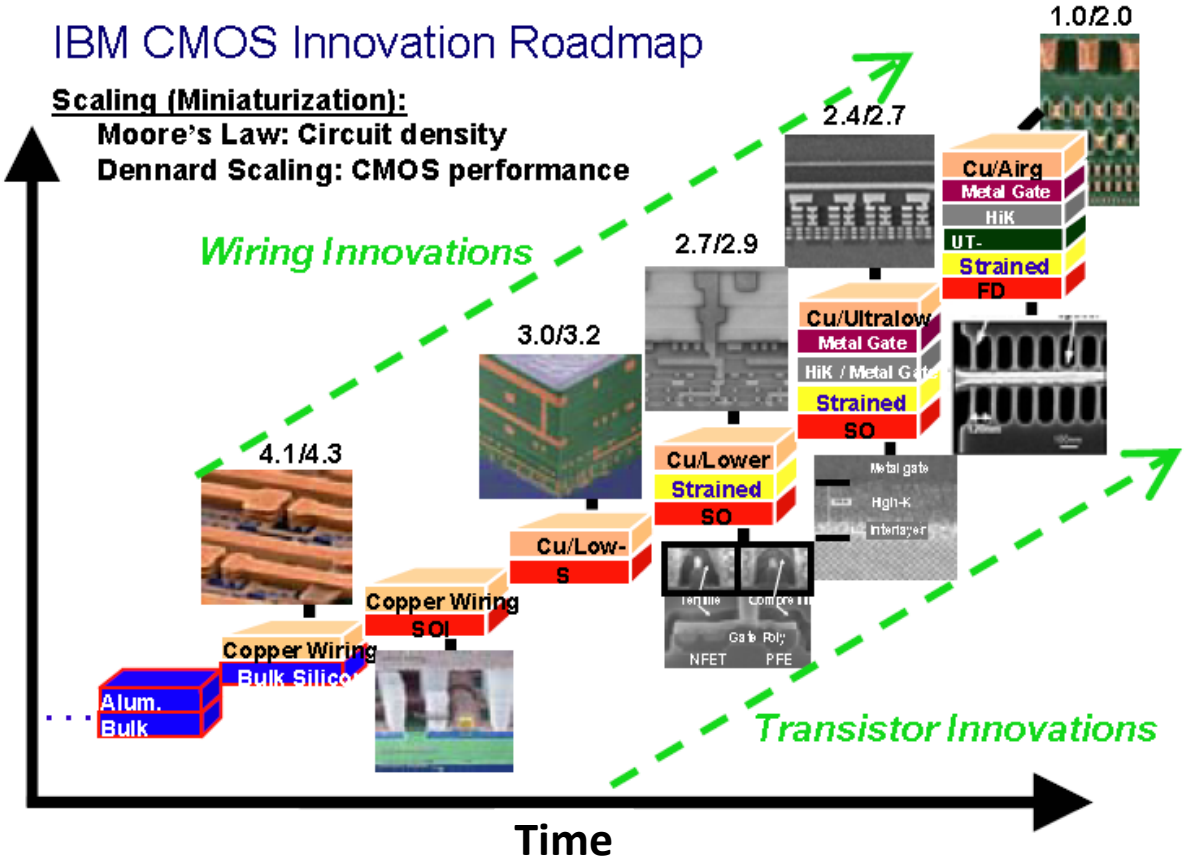
Surface Micromachining Process

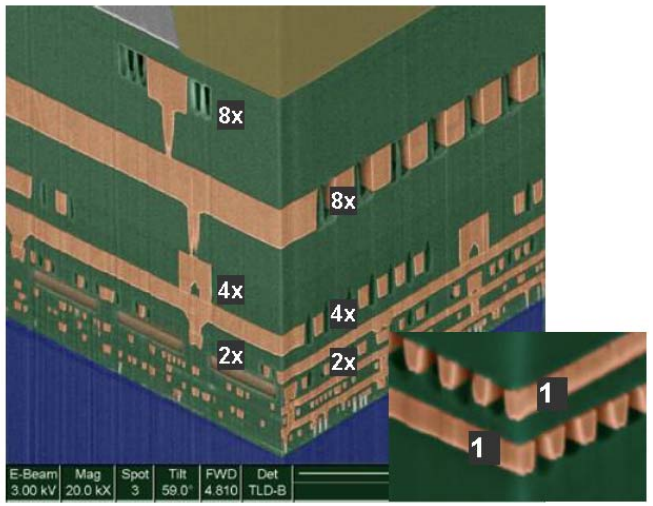
Cross-sectional View



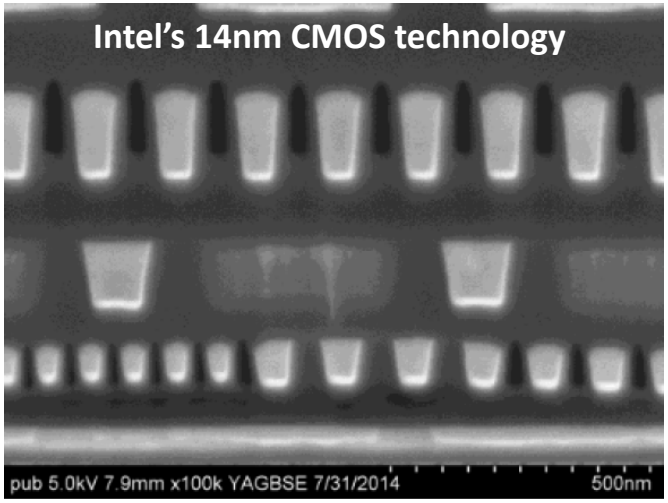
- **Mechanical structures can be made using conventional microfabrication techniques**
- **Structures are freed by selective removal of sacrificial layer(s)**

IC Technology Advancement





D. C. Edelstein, *214th ECS Meeting*, Abstract #2073, 2008



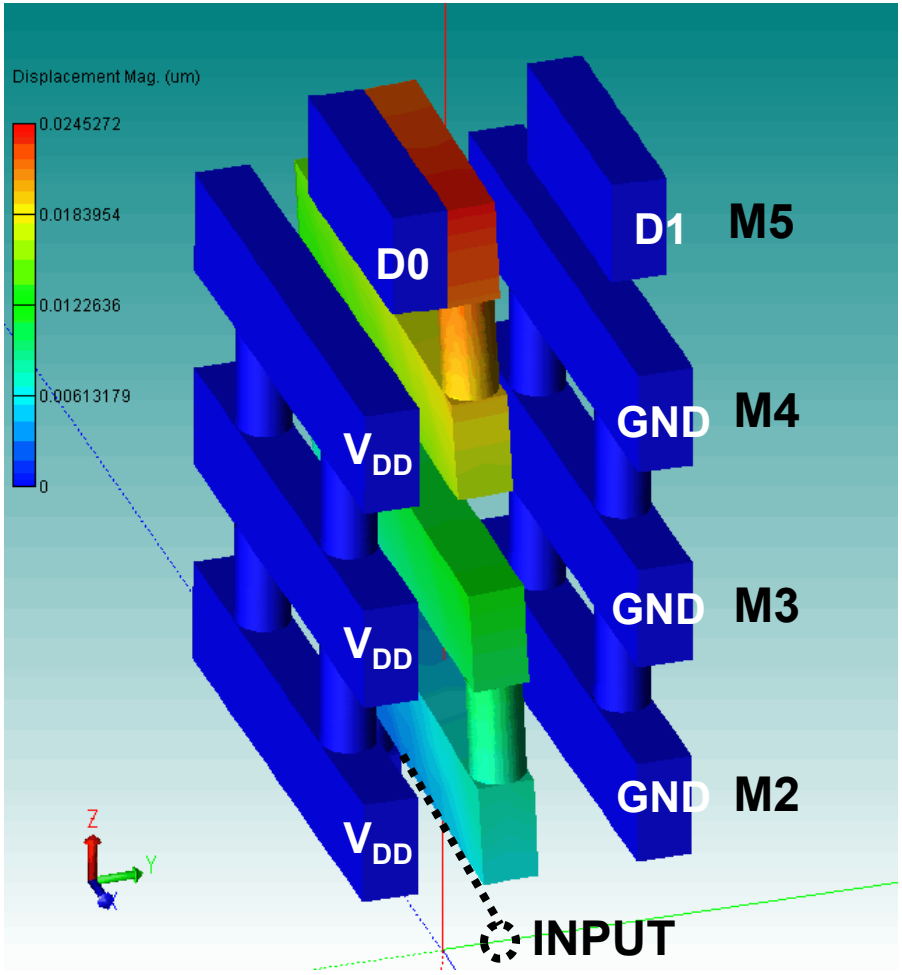
S. Natarajan *et al*. (Intel), *IEDM* 2014

- **Advanced back-end-of-line (BEOL) processes have air-gapped interconnects**

→ **can be adapted for fabrication of compact NEMS!**

BEOL NEM Switch

N. Xu *et al*. (UC Berkeley), 2014 IEEE International Electron Devices Meeting



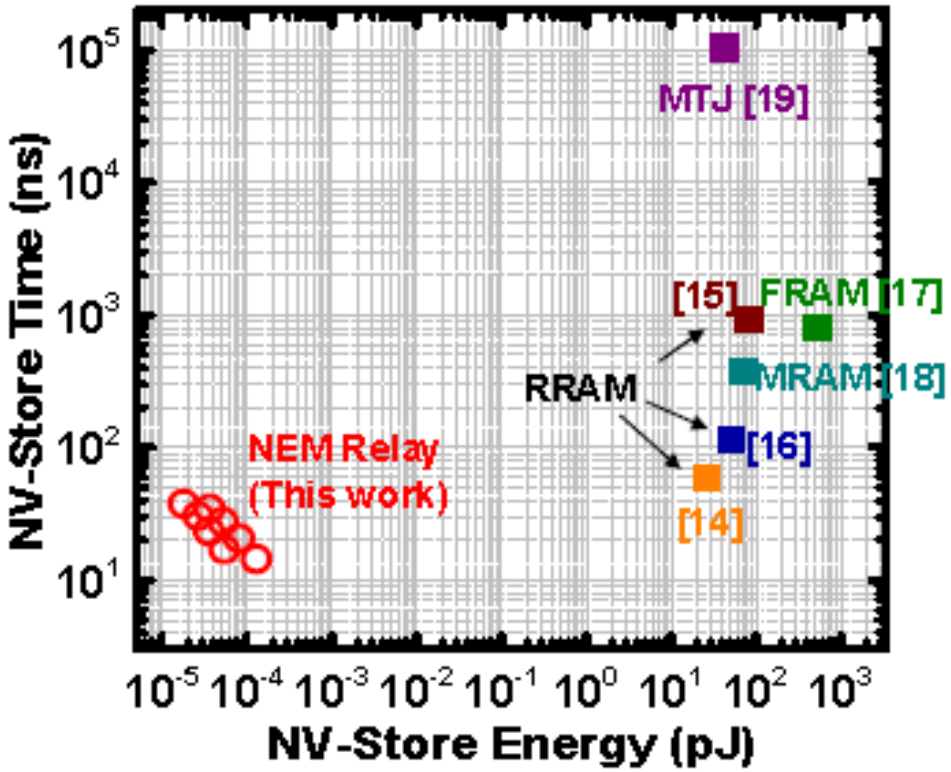
courtesy of Dr. Kimihiko Kato (UC Berkeley)

- **A relay can be implemented using multiple metal layers**
  - **Vias can be used for electrical connection and as torsional elements for lower k_{eff}**
- **Actuation electrodes on opposite sides of movable electrode structure**

  → 2 stable states (contacting D0 or D1)
- **Low-voltage (<1 V) operation can be achieved with small footprint (< 0.1 μm²).**

Non-Volatile Device Comparison

N. Xu *et al*. (UC Berkeley), 2014 IEEE International Electron Devices Meeting



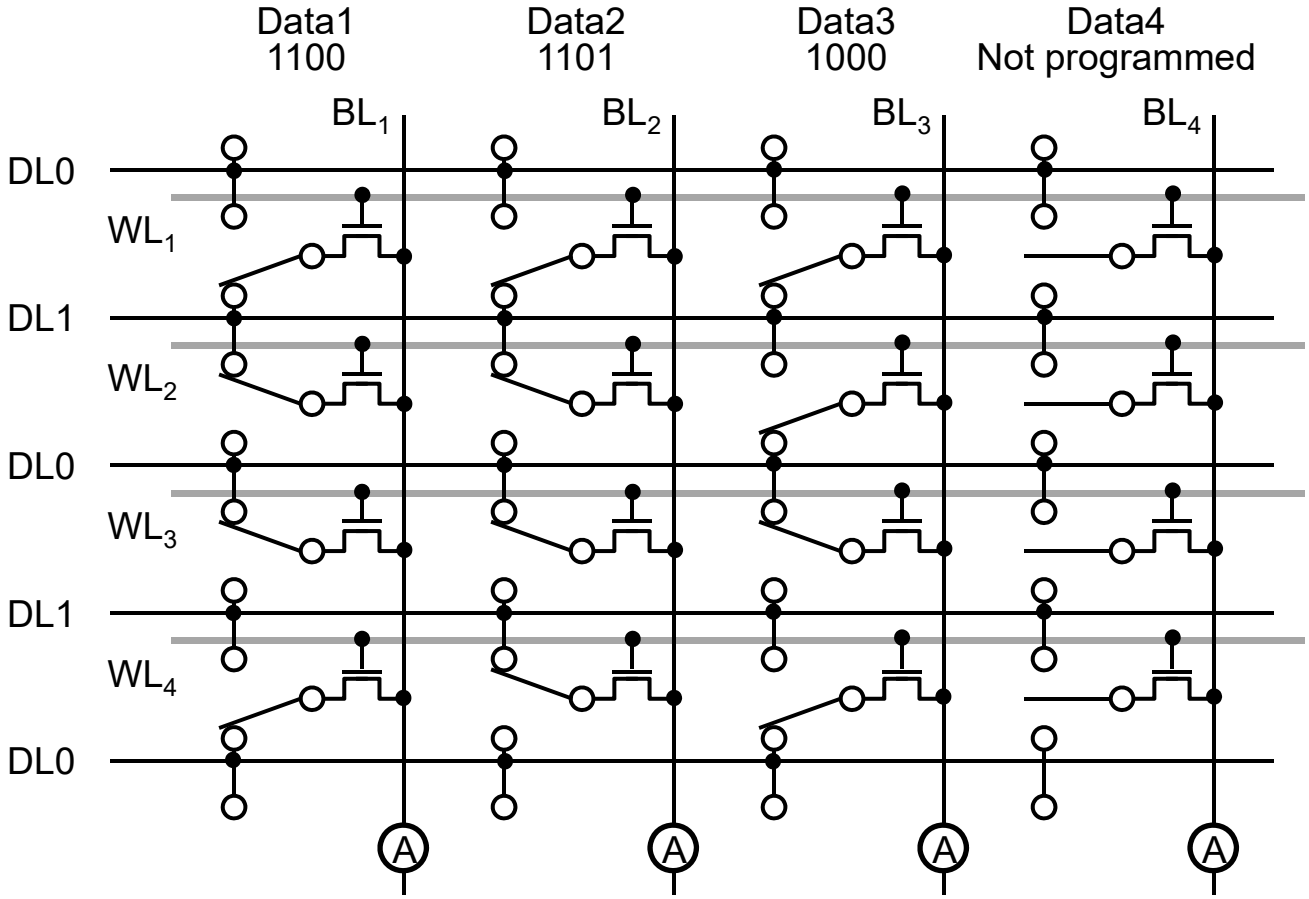
- **A bi-stable NEM switch is projected to operate with much less energy and delay than other non-volatile switching devices**

→can be used to continually shadow the information stored in an SRAM cell

In-Memory Computing

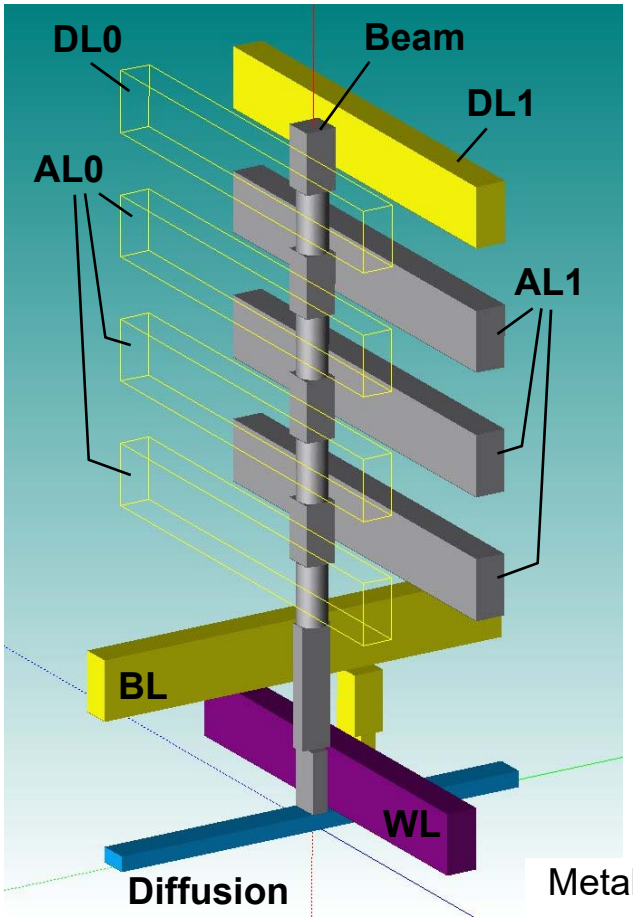
K. Kato *et al.*, *IEEE Electron Device Letters*, Vol. 37, pp. 31-34, 2016

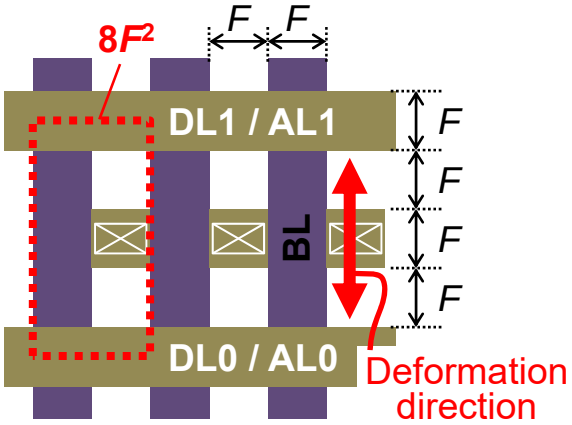
- **NV-NEMory cell array for memory-based super-parallel data searching**

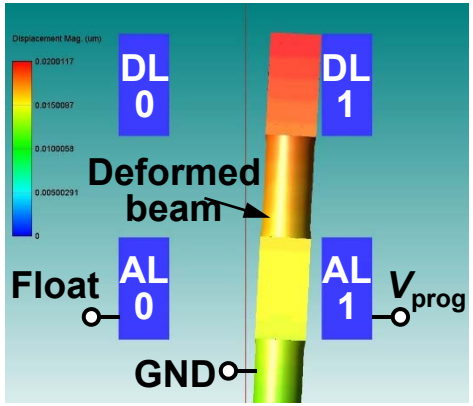


Non-Volatile NEMory Cell Structure

K. Kato *et al.*, *IEEE Electron Device Letters*, Vol. 37, pp. 31-34, 2016







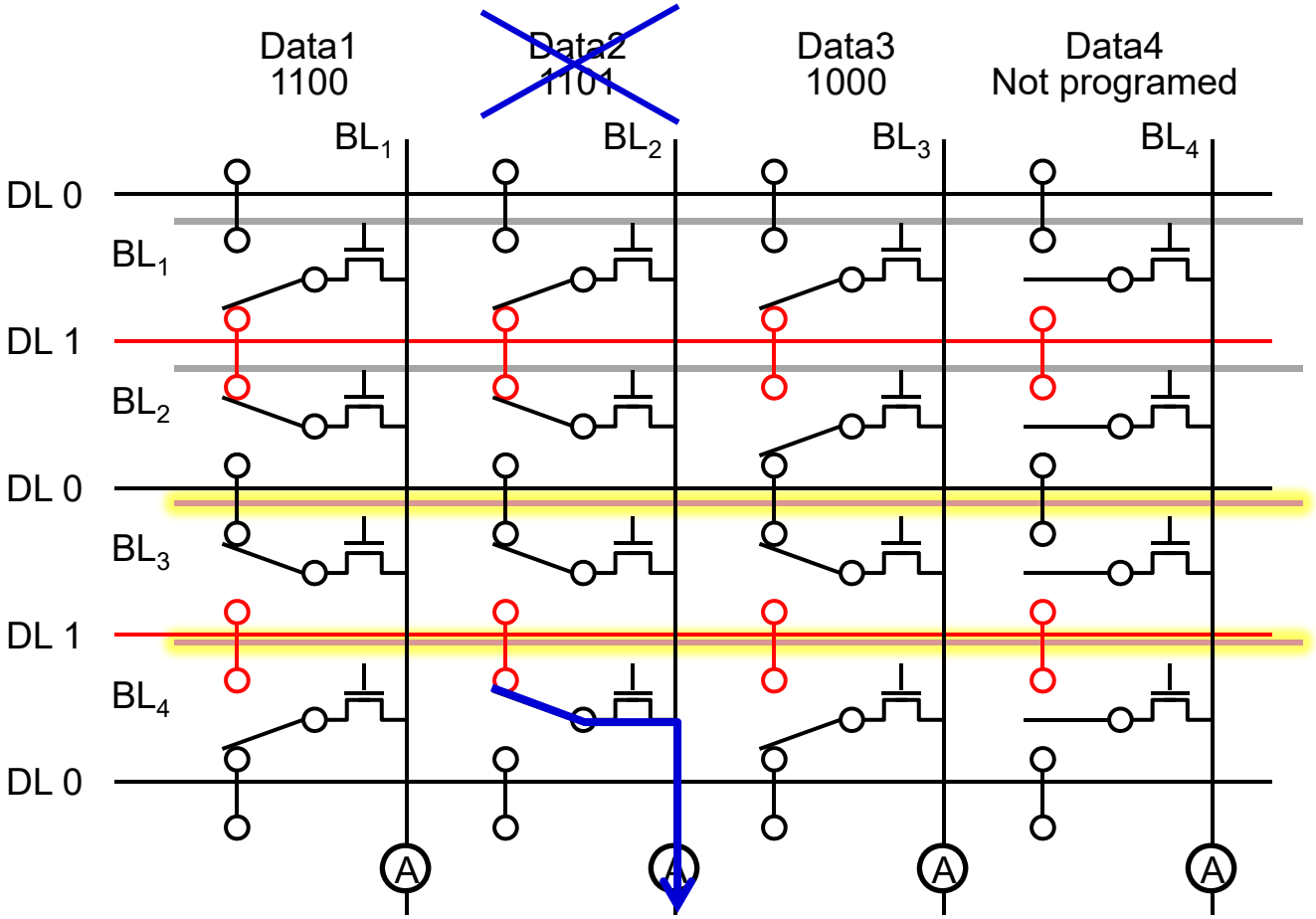
Metal: Al (Young's modulus: 70 GPa)
Gap: Air

Year	2015	2017	2019	2021	2023	2025
Half pitch, *F* (nm)	25.3	20.1	15.9	12.6	10.0	7.09

Data Search Step 1: Match "0"

K. Kato *et al.*, *IEEE Electron Device Letters*, Vol. 37, pp. 31-34, 2016

Reference Data: 1100



a) Activate DL1 lines

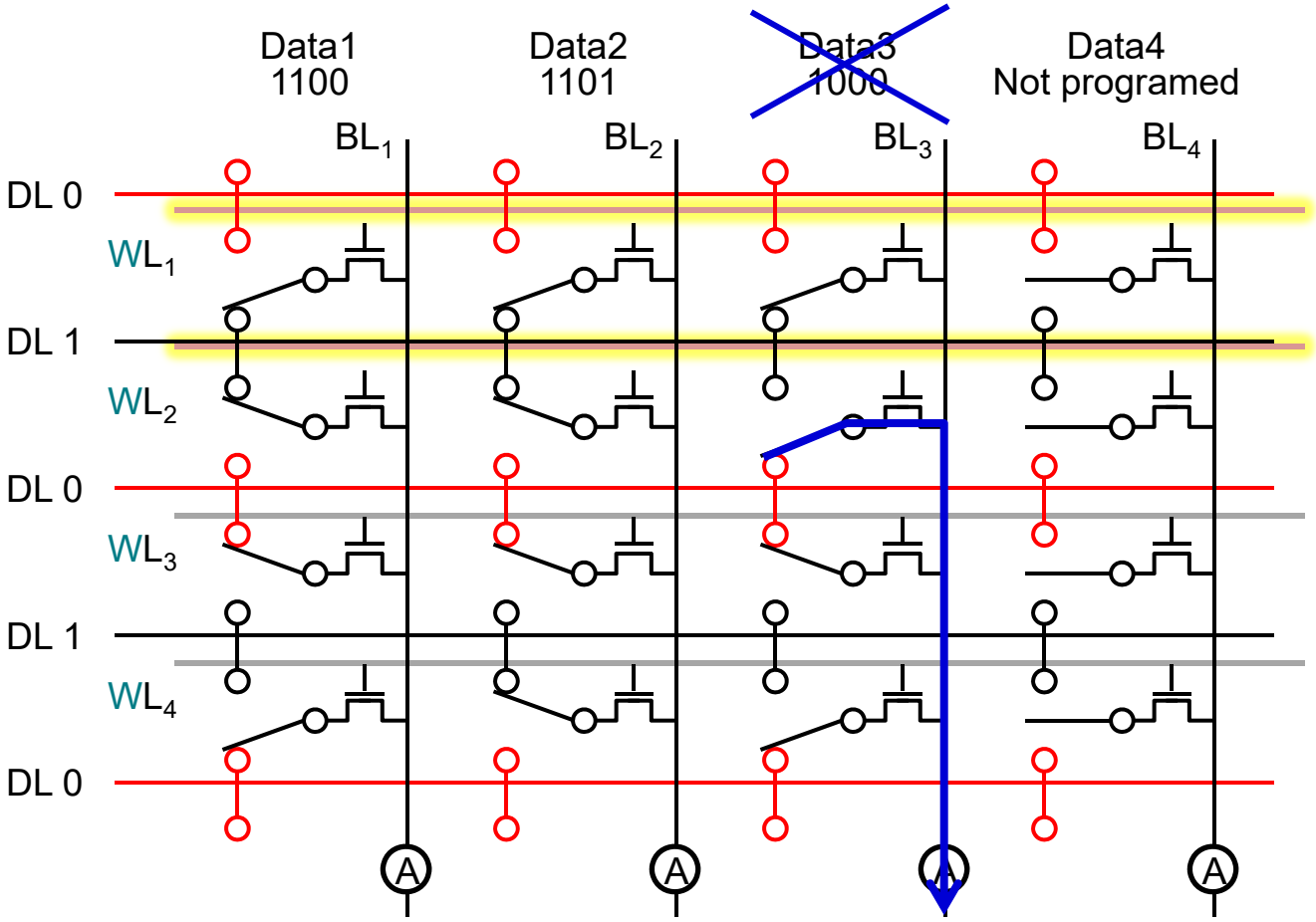
b) Access rows for 0 bits in reference

c) Zero BL current → Matched 0s

Data Search Step 2: Match "1"

K. Kato *et al.*, *IEEE Electron Device Letters*, Vol. 37, pp. 31-34, 2016

Reference Data: 1100



a) Activate DL0 lines

b) Access rows for 1 bits in reference

c) Zero BL current → Matched 1s

Energy and Delay for Data Search

K. Kato *et al.*, *IEEE Electron Device Letters*, Vol. 37, pp. 31-34, 2016

256 × 256 NV-NEMory Array

	Energy			Delay
Cells involved:	1 column × 1 row	1 column × 256 rows	256 columns × 256 rows	
Program (V_{prog} = 2.5 V)	15 fJ	2.0 pJ	N/A	< 10 ns
Match "0" or Match "1"	N/A	N/A	1.2 pJ	< 0.2 ns

- The location of a data string can be found in <0.5 ns with less than 2.5 pJ.

→ For a die size of 42 mm^2 (same as DDR4 DRAM) at F = 20 nm and cell density of 65% (similar to DRAM), a NV-NEMory chip would have the capacity 8 Gb and would consume only 300 nJ to find a match on the whole chip.

→ In comparison, it would take CPU+DRAM ~90 mJ, 80 ms for the same task.

Relatively fast read speed & low power consumption make NV-NEMory technology well-suited for real-time data searching applications!

Outline

- Introduction
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- Beyond Moore: Mechanical Computing Redux
- **Summary**

Summary

- **Tilted ion implantation (TII) is an effective sub-lithographic patterning and pitch-halving technique**
  - **features are self-aligned to pre-existing mask**
  - **process flow is much simpler (lower cost) than SADP**

  → shows promise for extending Moore's Law!
- **Electronic devices which enable more energy-efficient computation and data storage, at ever lower cost per function, will be required for ubiquitous computing.**
  - **BEOL NEM devices show promise in this regard**

Acknowledgements

- **TII-Enhanced Lithography:**
  - Dr. Sang Wan Kim (UC Berkeley)
  - Dr. Peng Zheng (now with Intel Corporation)
  - Dr. Leonard Rubin (Axcelis Technologies)
  - UC Berkeley Marvell Nanofabrication Laboratory
  - Funding from Applied Materials, Lam Research
- **BEOL NEM Relays Technology:**
  - Dr. Nuo Xu (now with Samsung Semiconductor, Inc.)
  - Dr. Kimihiko Kato (now at University of Tokyo)
  - Prof. Vladimir Stojanović (UC Berkeley)
  - Funding from National Science Foundation
    - Center for Energy Efficient Electronics Science