NEM Relay Design for Compact, Ultra-Low-Power Digital Logic Circuits

T.-J. K. Liu[1], N. Xu[1], I.-R. Chen[1], C. Qian[1], J. Fujiki[2]

[1]*Dept. of Electrical Engineering and Computer Sciences*
University of California, Berkeley, CA USA

[2]*Toshiba Corporation, Tokyo, Japan*

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Acknowledgement

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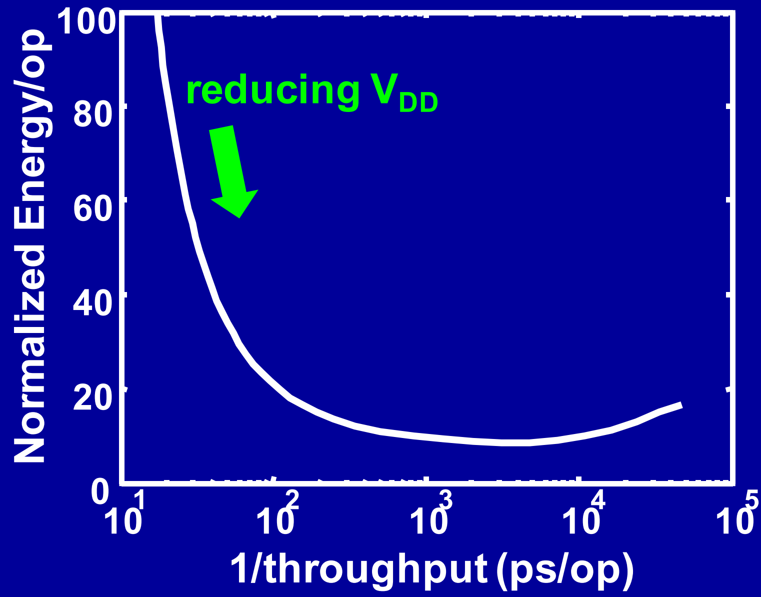
A Vision of the Future

Internet of Things → ultra-low-power required!

CMOS Energy-Efficiency Limit



- A lower limit in E/op exists for any CMOS technology, due to transistor OFF-state leakage.

Active Energy — Passive Energy

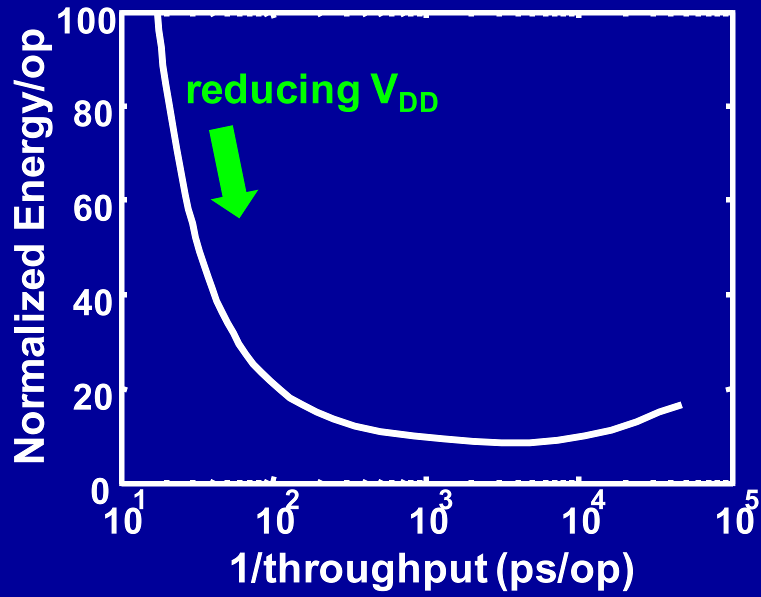
$$E_{total} = \alpha L_d f C V_{DD}^2 + L_d f I_{OFF} V_{DD} t_{delay}$$

$$t_{delay} = L_d f C V_{DD} / (2 I_{ON})$$

α: Activity Factor L_d: Logic Depth f: Fanout C: Capacitance per Stage

B. Calhoun *et al.*, *IEEE J. Solid State Circuits*, Vol. 50, pp. 1778-1786, 2005

CMOS Energy-Efficiency Limit



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Active Energy — Passive Energy

$$E_{total} = \alpha L_d f C V_{DD}^2 + L_d f I_{OFF} V_{DD} t_{delay}$$

$$E_{total} = \alpha L_d f C V_{DD}^2 [\ 1 + (L_d f/2\alpha) / (I_{ON}/I_{OFF})\ ]$$

α: Activity Factor L_d: Logic Depth f: Fanout C: Capacitance per Stage

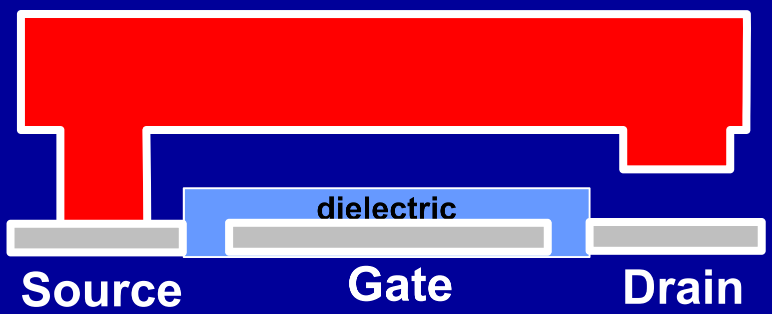
B. Calhoun *et al.*, *IEEE J. Solid State Circuits*, Vol. 50, pp. 1778-1786, 2005

Why Nano-Electro-Mechanical Relays?

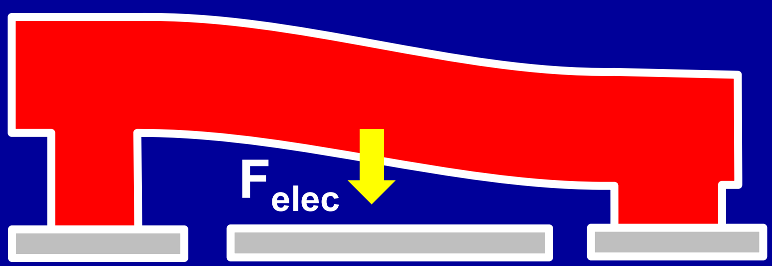
- Zero off-state leakage → Zero static power
- Abrupt switching → Low V_{DD} (low dynamic power)

Basic Electro-Mechanical Switch

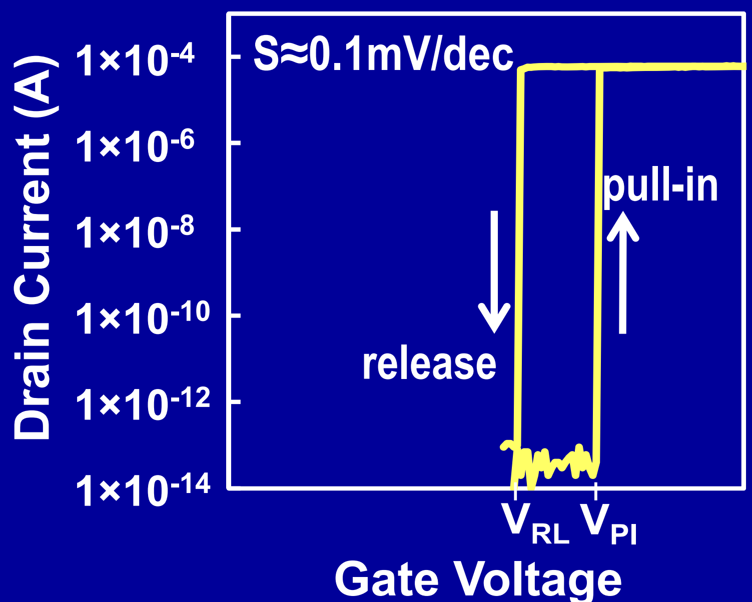
OFF State (as fabricated):



ON State:



***I-V* Characteristic**



- Relay endurance > 10^{15} cycles for hot-switching below 1 Volt

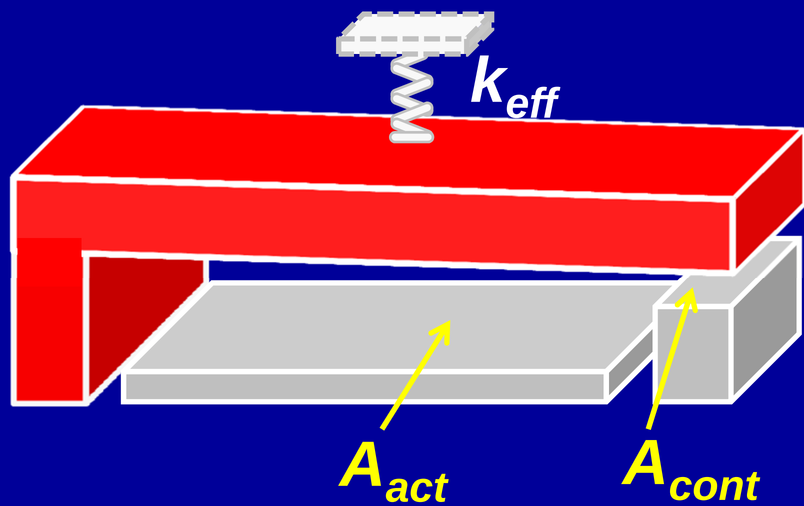
H. Kam *et al.*, *2010 IEDM*

Outline of Presentation

- Overcoming Surface Adhesion Energy Limit
- Compact BEOL Relay Design
- Zero Crowbar Current Relay-Based Circuits
- Conclusion

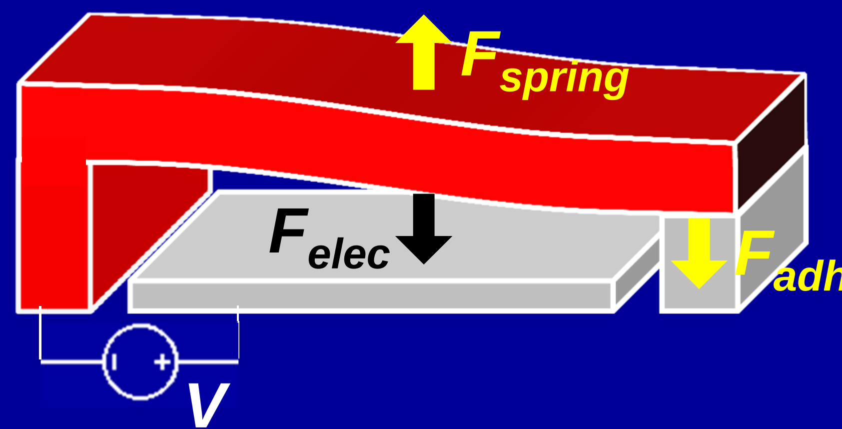
Normally-OFF Switch Design

OFF State (as fabricated)



- Turn OFF by spring force
  → $F_{spring} > F_{adh}$

ON State

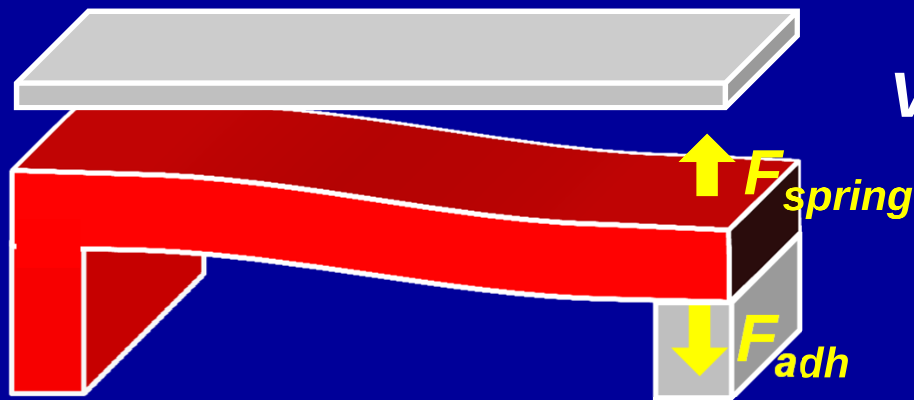


- Turn ON by electrostatic force
  → $F_{elec} > F_{spring} > F_{adh}$

- **Minimum operating energy is limited by adhesion**
  → **Limits actuation area and/or voltage scaling**

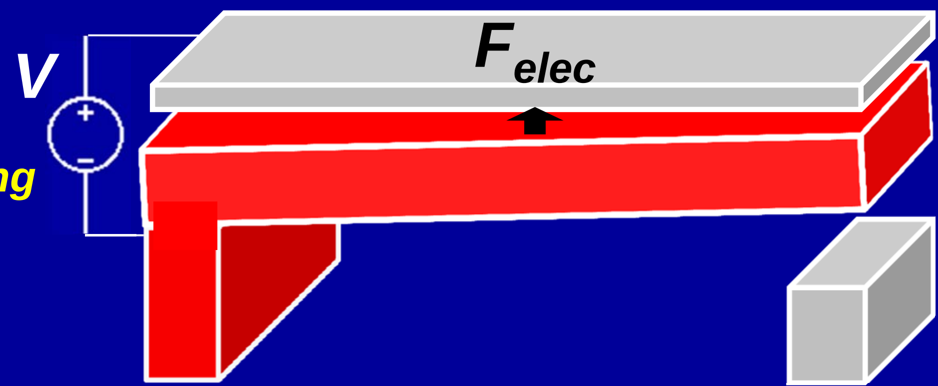
Normally-ON Switch Design

ON State (as fabricated)



- Spring force counteracts adhesive force

OFF State



- Turn OFF by electrostatic force

  → $F_{elec} < F_{adh}$

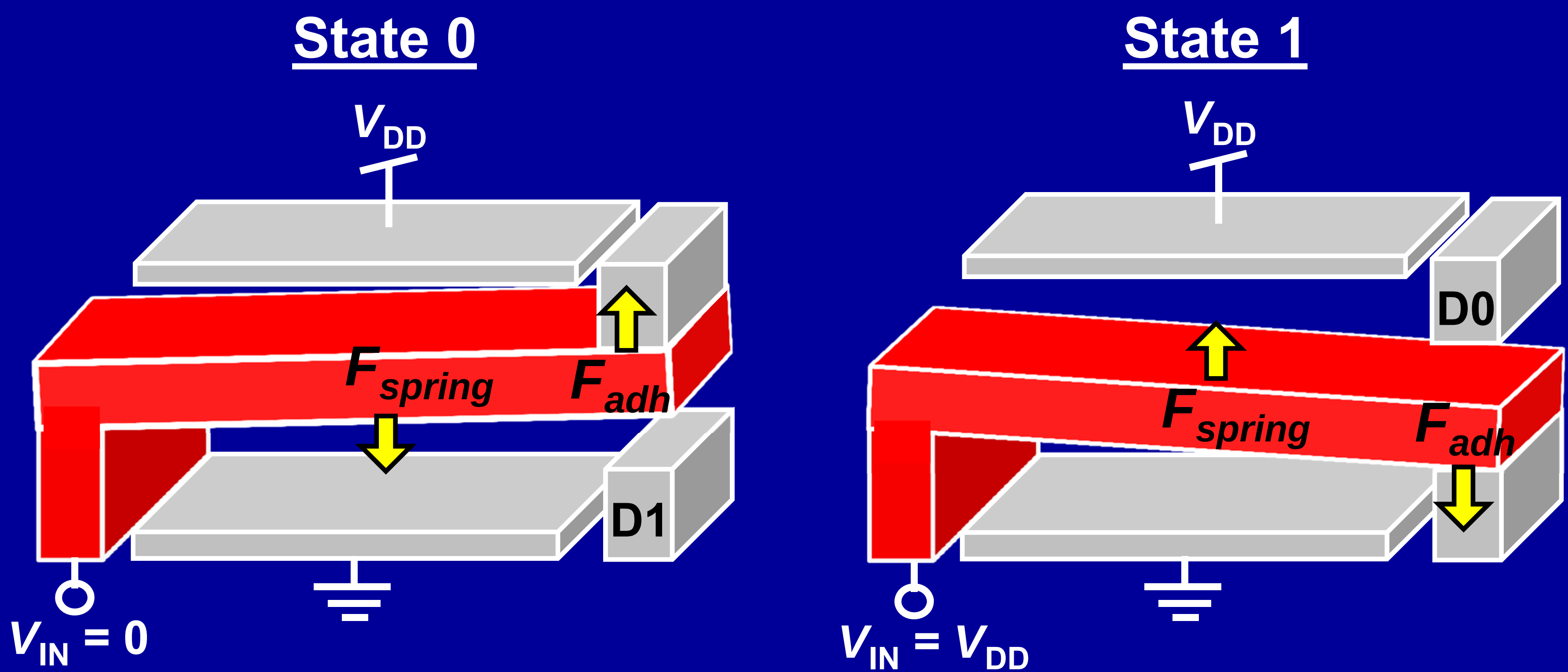
- Operating energy can be smaller than $E_{adhesion}$

  Challenge: Ultra-small (~1 nm) contact gap required

I-R. Chen *et al.* (UC Berkeley), to be published

Bi-stable Switch Design

Single-pole double-throw (SPDT)



- Electrostatic force is applied to switch between states
- Contacting state is non-volatile if $F_{adh} > F_{spring}$

I-R. Chen *et al.* (UC Berkeley), to be published

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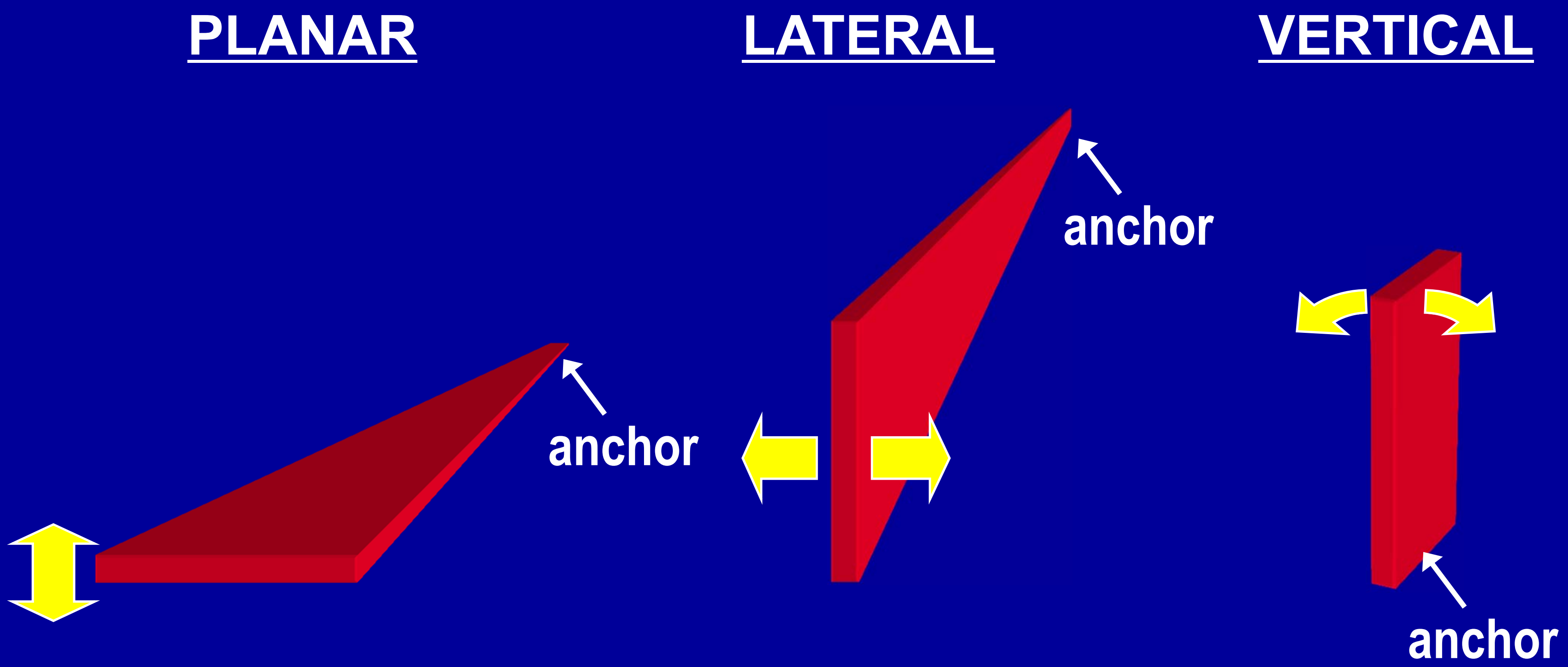
Basic NEM Switch Designs



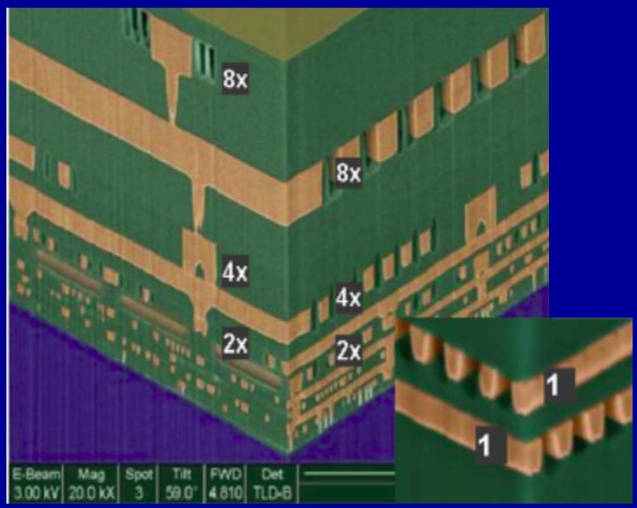
✓ Fewer fabrication process steps

✓ Smaller footprint

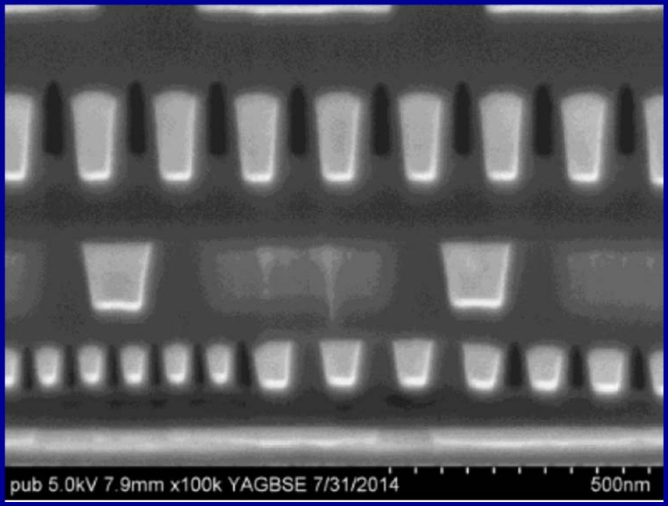
3-D Integration with CMOS

- **Advanced back-end-of-line (BEOL) processes have multiple metal layers and air gaps**
  → can be adapted for fabrication of NEM relays!

<u>Scanning Electron Micrographs</u>

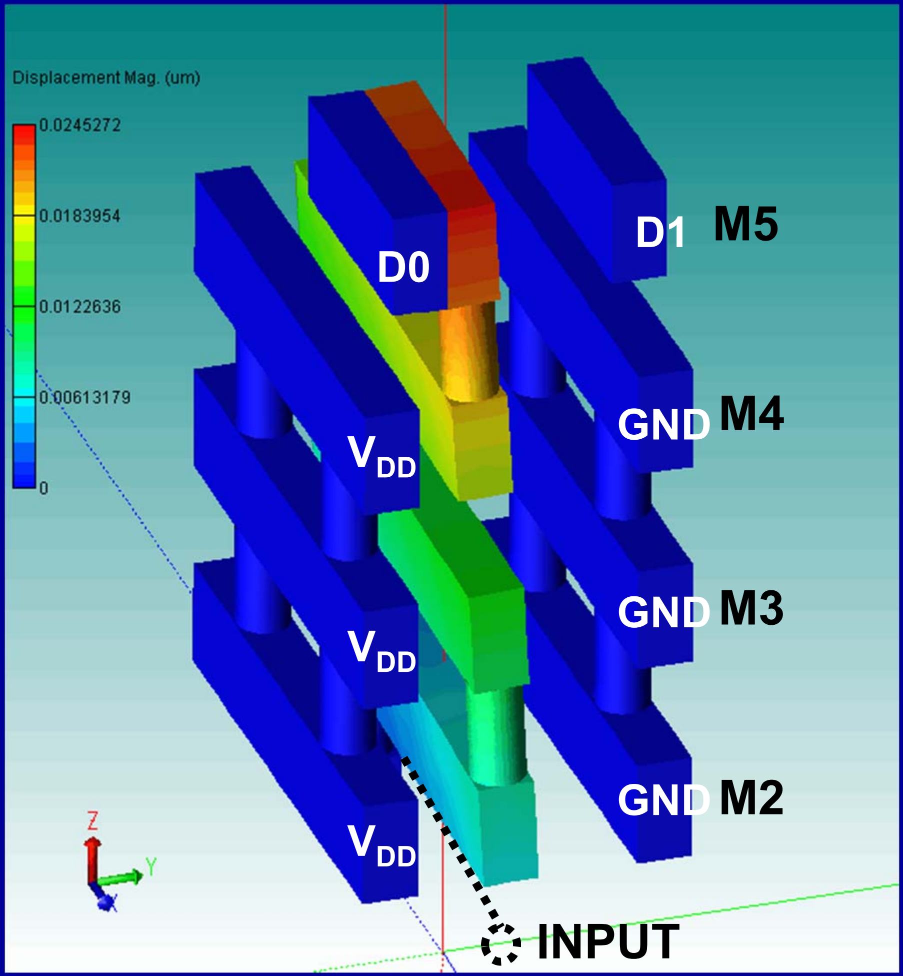


D. C. Edelstein (IBM),
214th ECS Meeting, **Abstract #2073, 2008**



S. Natarajan ***et al*****. (Intel),**
Paper 3.7, *2014 IEDM*

BEOL SPDT NEM Switch



courtesy of Dr. Kimihiko Kato (UC Berkeley)

- **5-terminal SPDT switch implemented using 4 interconnect layers**
  - **Vias are used for electrical connection and as torsional elements for lower k_{eff}**

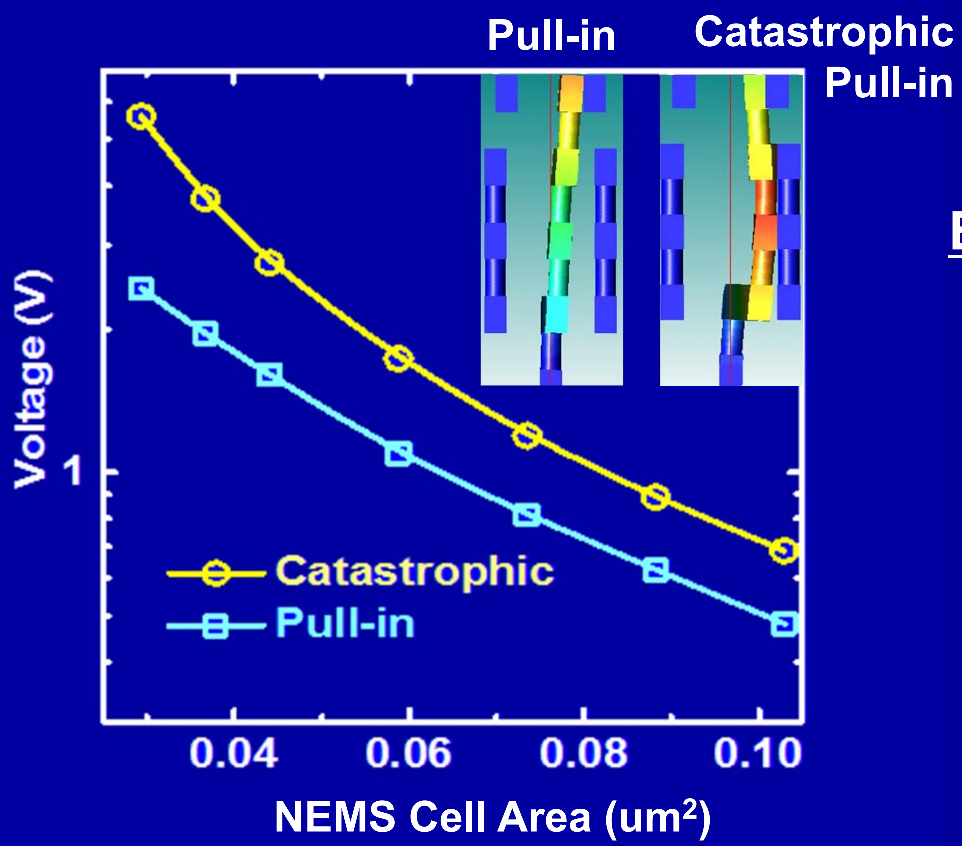
- **Fixed actuation electrodes on opposite sides of movable structure**

  → 2 stable states (contacting D_0 or D_1)

BEOL NEM Switch Operating Voltage

N. Xu *et al.*, (UC Berkeley), Paper 28.8, *IEDM 2014*

- Low-voltage (<1 V) operation can be achieved with a small device footprint (< 0.1 μm²).

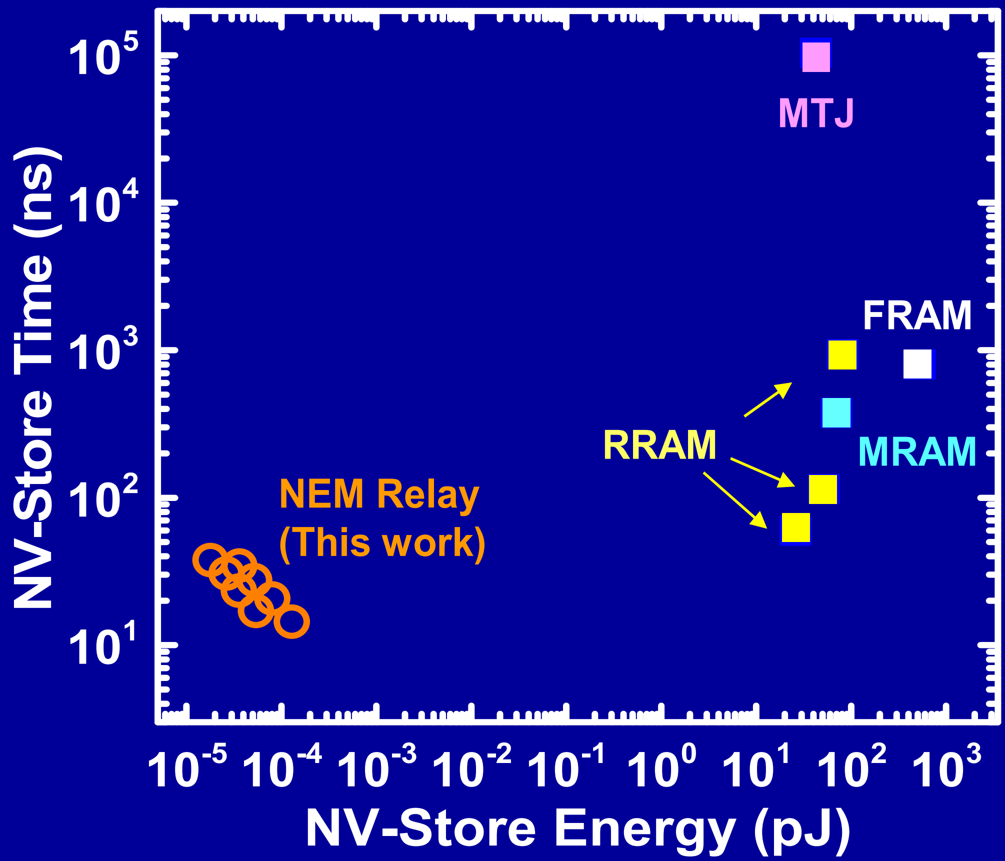


<u>BEOL Design Parameters</u>

Material	Al
Pitch	42 nm
Width	21 nm
Aspect Ratio	1.9

NVM Technology Comparison

- **A bi-stable NEM switch operates with much lower energy and delay than other NVM devices.**



→ 3-D integrated NEM switches are attractive for NV-SRAM application

See Paper 28.8

(12 noon tomorrow!)

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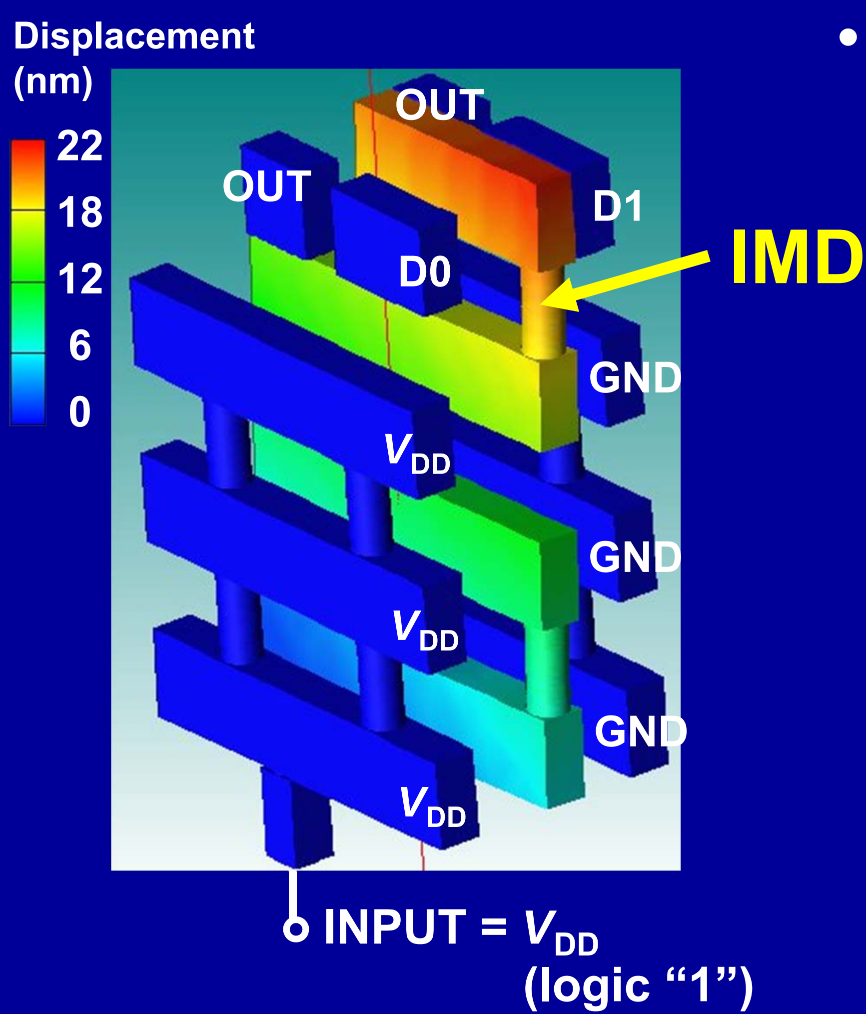
6-Terminal (6-T) SPDT NEM Relay



- If a common output electrode is used

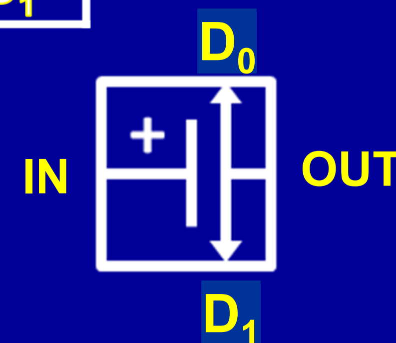
  insulated from the input

  then the relay functions as a 2:1 multiplexer (MUX)

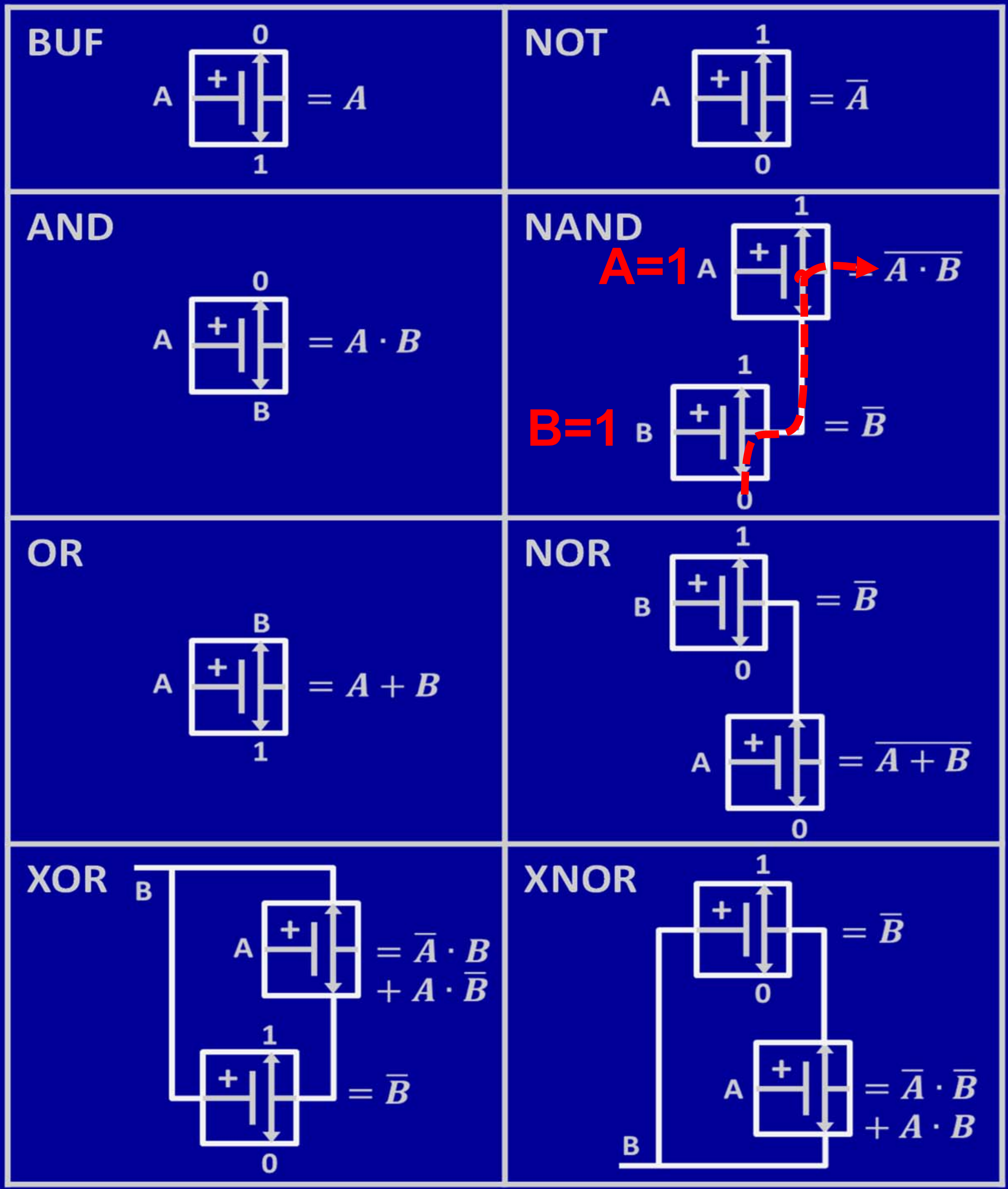
$$OUT = \overline{IN} \cdot D_0 + IN \cdot D_1$$

IN	OUT
0	D_0
1	D_1

Symbol:



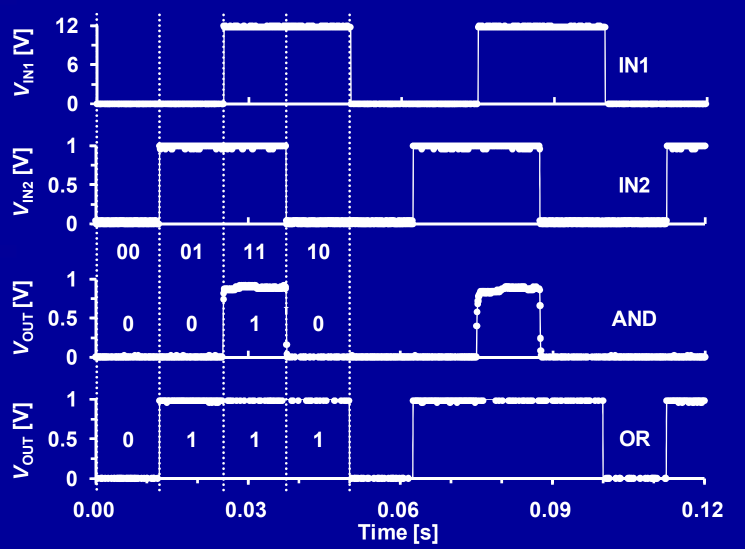
Basic 6-T Relay Logic Gates



- **OUT terminals each are connected to a D terminal**

  → **one mechanical delay, *i.e.* single-stage operation**

Measured Voltage Waveforms



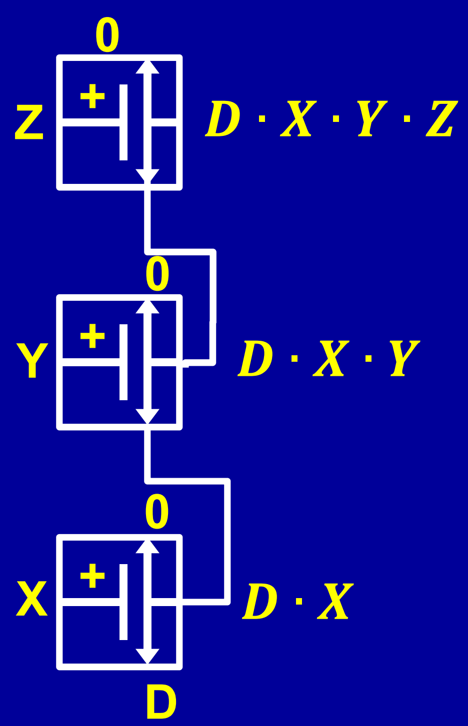
J. Jeon *et al.* (UC Berkeley), *IEEE/ASME J.MEMS*, Vol. 19, pp. 1012-1014, 2010

Multiple-Input AND and OR Gates

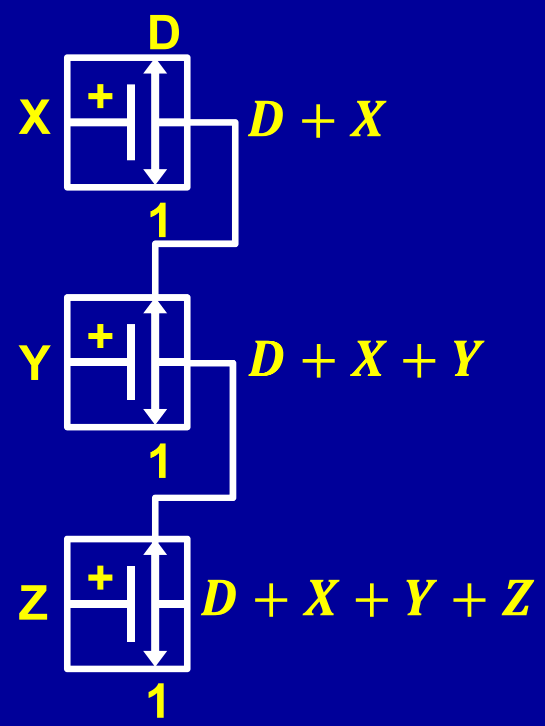
- **Any combinational logic function can be implemented with 2:1 MUX relays using binary decision diagram techniques**

D. Lee *et al*. (Stanford), *IEEE T-CADICS*, Vol. 32, pp. 653-666, 2013

3-input AND



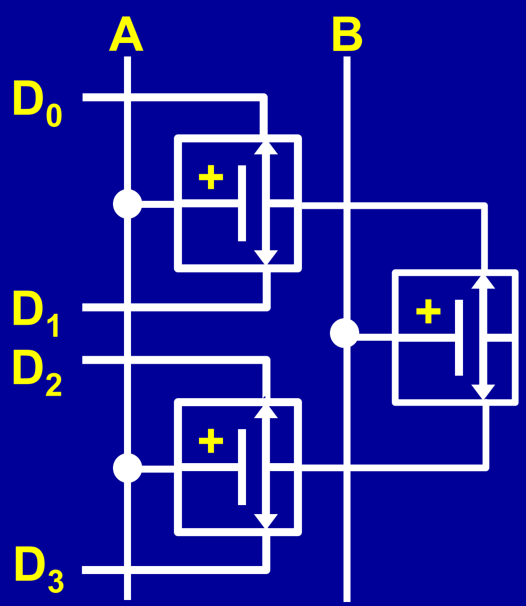
3-input OR



J. Fujiki *et al*. (UC Berkeley), *IEEE T-ED*, Vol. 61, pp. 3296-3302, 2014

4:1 Multiplexer …

- A **2N:1 multiplexer** is implemented with **N(N+1)/2** switches

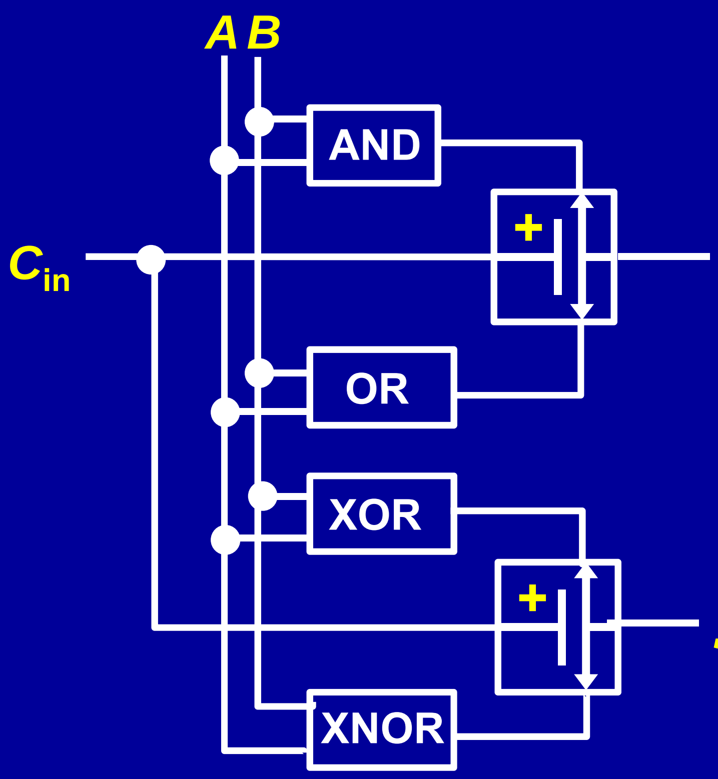


$$O = \overline{B} \cdot (\overline{A} \cdot D_0 + A \cdot D_1) + B \cdot (\overline{A} \cdot D_2 + A \cdot D_3)$$

- An **N-bit decoder** is implemented using 2^{N+1}-2 switches

Full Adder

- for carry-lookahead adder



$$C_{out} = \overline{C_{in}} \cdot (A \cdot B) + C_{in} \cdot (A \oplus B)$$

$$S = \overline{C_{in}} \cdot (A \oplus B) + C_{in} \cdot (\overline{A \oplus B})$$

Device Count Comparison

- **Relay-based implementation results in lower device count:**

FUNCTION	CMOS	6-T NEM RELAY
BUF	4	1
NOT	2	1
NAND	4	2
XOR	6	2
2:1 MUX	8	1
Full adder	24	8

- **Note that each of the relay-based circuits are single-stage (1 mechanical delay).**

J. Fujiki *et al*. (UC Berkeley), *IEEE T-ED*, Vol. 61, pp. 3296-3302, 2014

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Conclusion

- **Surface adhesion does not set a fundamental limit for NEM relay operating energy**

  if adhesion force is used to switch ON a relay

- **An advanced CMOS BEOL technology can be leveraged to fabricate vertical NEM relays**
  - **footprint < 0.1 μm^2 ; switching voltage < 1 V**

  See Paper 28.8 (12 noon tomorrow!)

- **A complementary (SPDT) relay design ensures zero crowbar current (as well as zero leakage)**

  and provides for substantial reduction in device count