The Path Toward Efficient Nano-Mechanical Circuits and Systems

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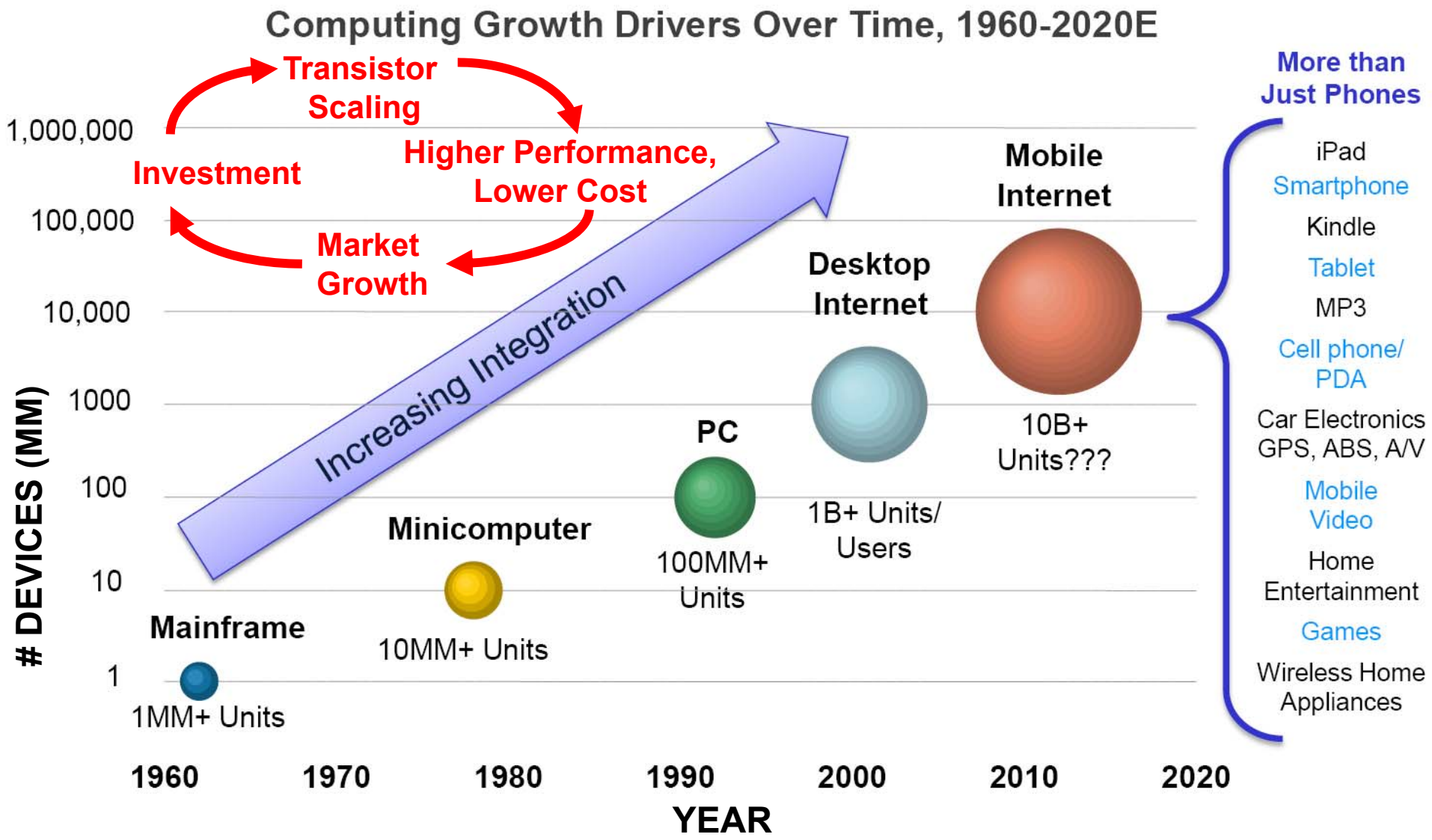
Proliferation of Electronic Devices



Source: ITU, Mark Lipacis, Morgan Stanley Research

Vision for 2020: Swarms of Electronics

Infrastructional core

Driver for More of Moore's Law

Mobile access

Driver for More Than Moore's Law

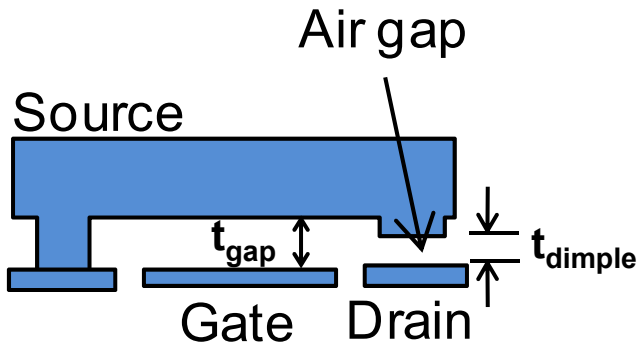
Sensory swarm (trillions of devices)

Why Mechanical Switches?

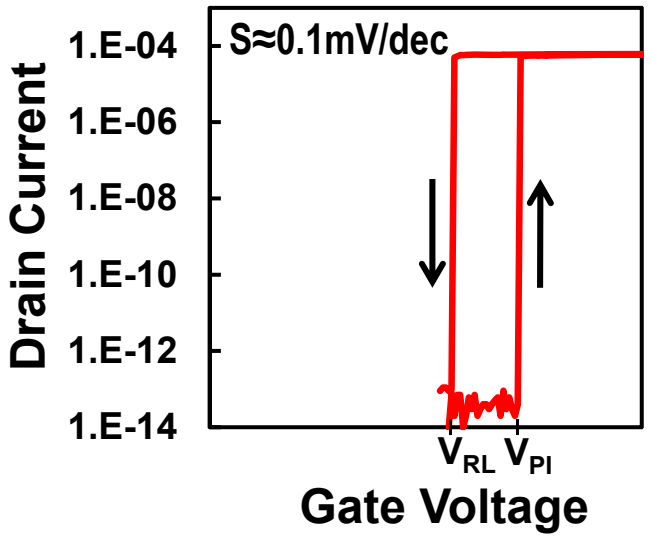
- **Relays have zero off-state leakage**
  → **zero leakage energy**

- **Relays switch on/off abruptly**
  → **allows for aggressive V_{DD} scaling (ultra-low dynamic energy)**

3-Terminal Switch



Measured *I-V*

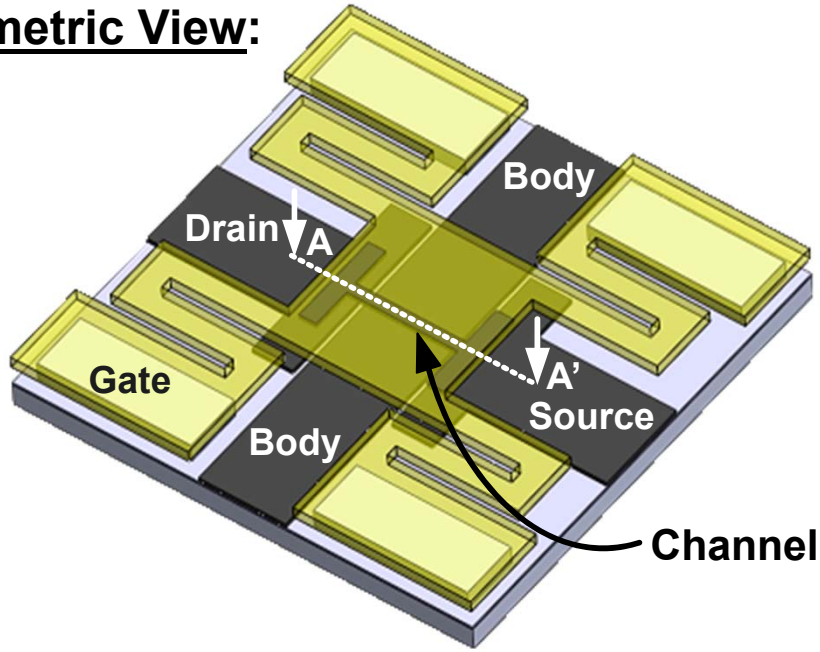


Outline

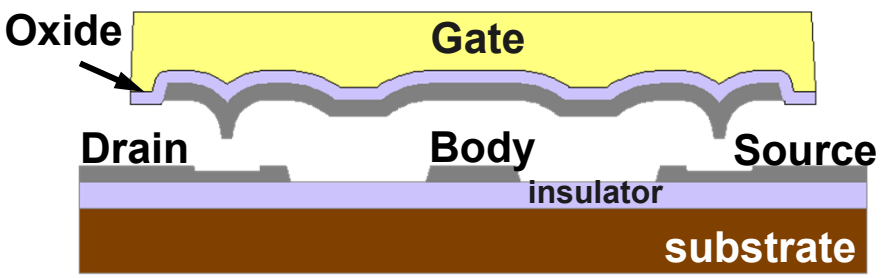
- **Electro-Mechanical Relay Design for Digital ICs**
- **Relay-Based IC Design**
- **Relay Reliability**
- **Summary**

4-Terminal Relay Structure

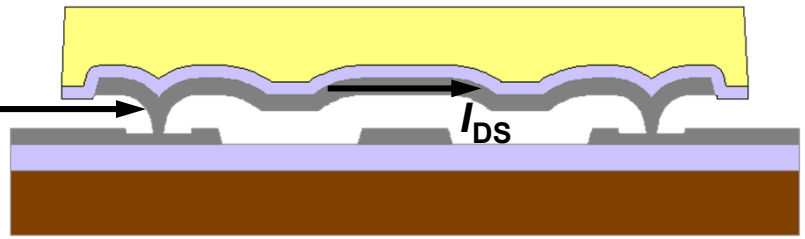
Isometric View:



AA' cross-section: OFF state



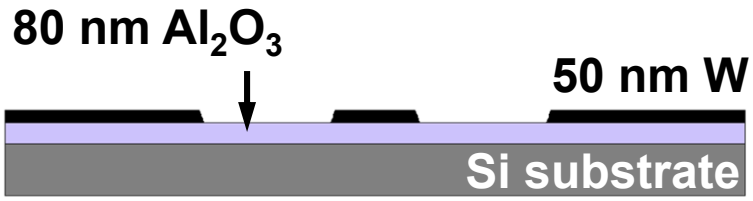
AA' cross-section: ON state



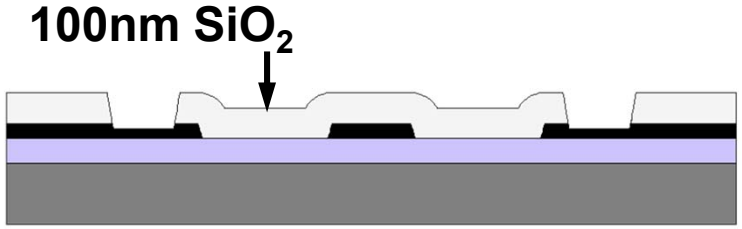
- **A voltage is applied between the *gate* and *body* to bring the channel into contact with the *source* and *drain*.**
  - ➥ **Folded-flexure design relieves residual stress.**
  - ➥ **Gate oxide layer insulates the channel from the gate.**

4-T Relay Process Flow (I)

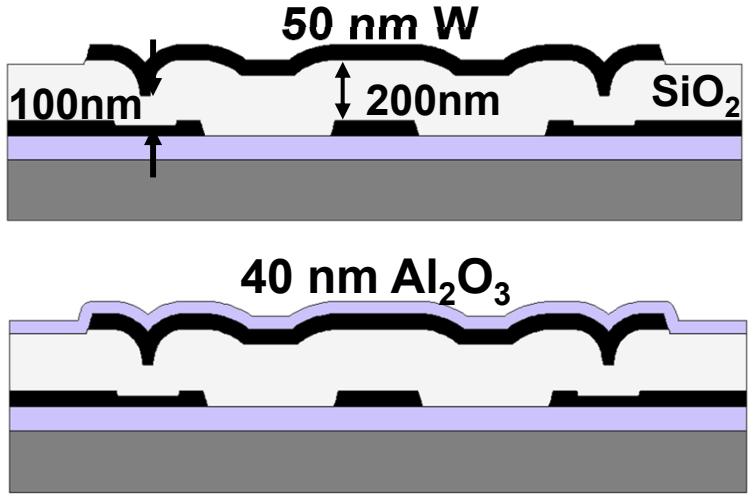
Mask 1: Electrode



Mask 2: Contact dimple



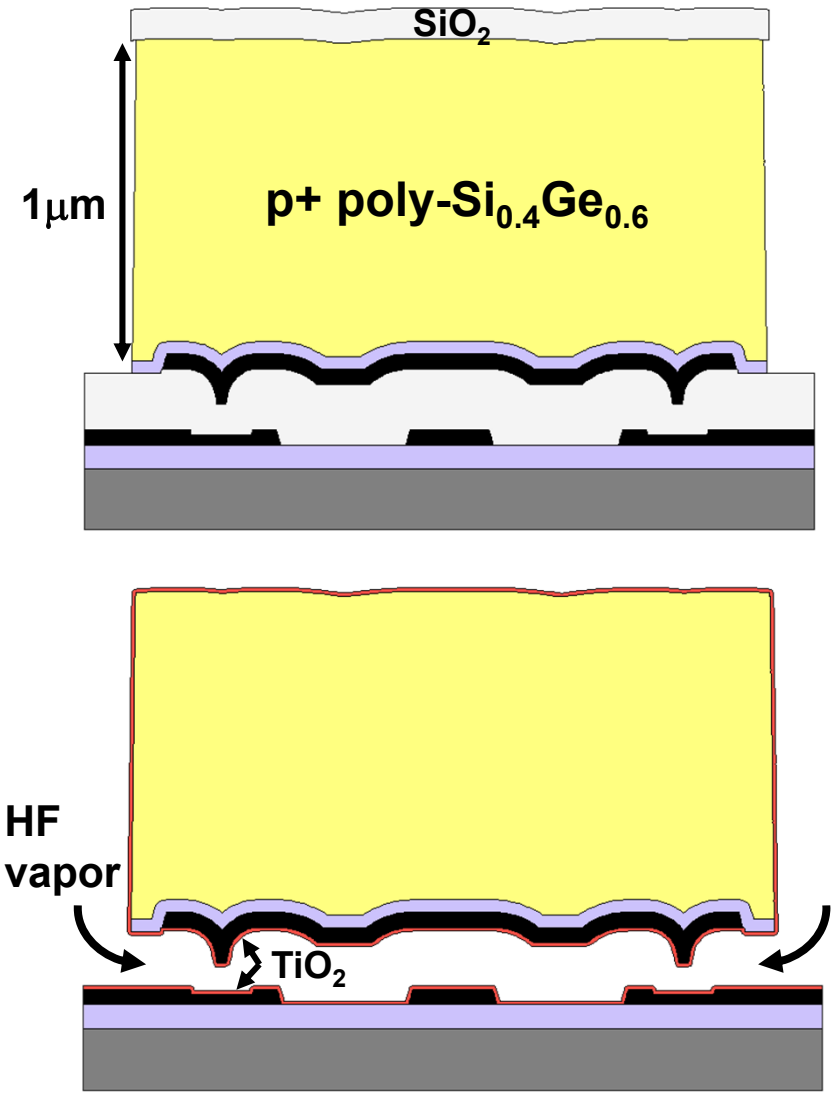
Mask 3: Channel



- Deposit Al_2O_3 substrate insulator
  - ALD at 300°C
- Deposit & pattern W electrodes
  - DC magnetron sputtering
- Deposit 1st sacrificial LTO
  - LPCVD at 400°C
- Define contact regions
- Deposit 2nd sacrificial LTO
- Deposit & pattern W channel
- Deposit Al_2O_3 gate oxide

4-T Relay Process Flow (II)

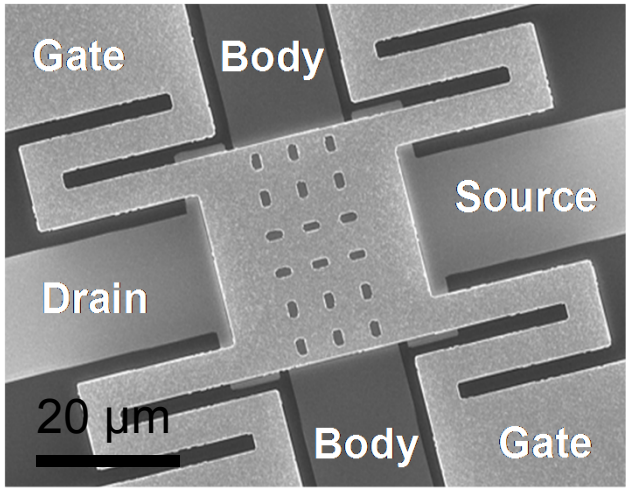
Mask 4: Structure

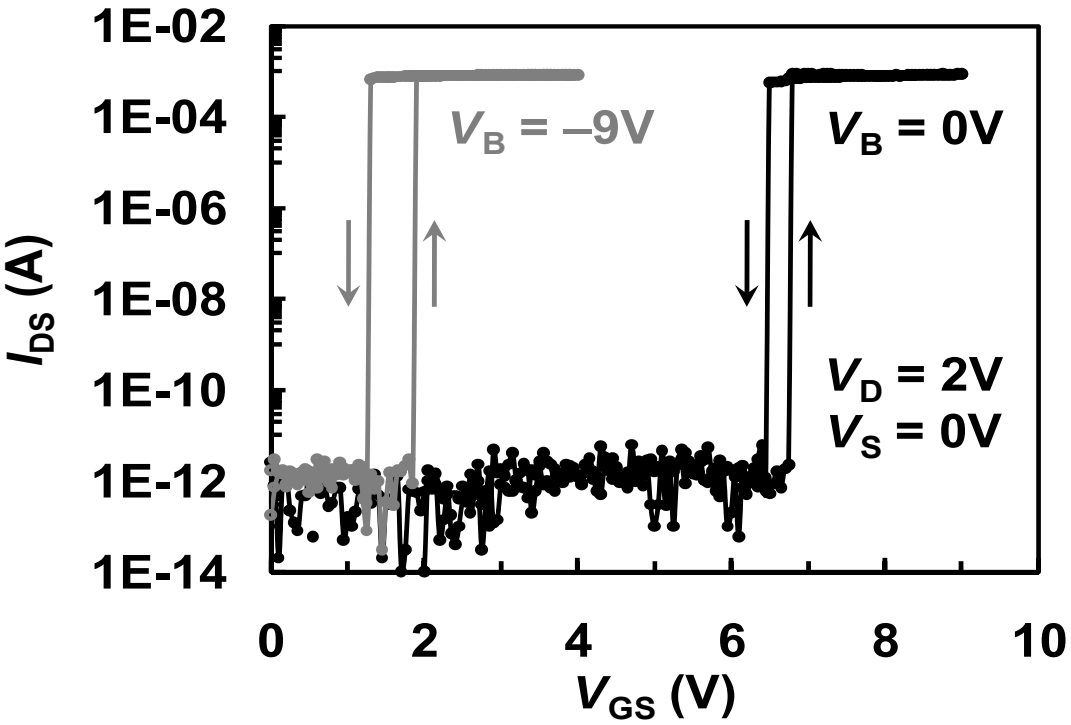


- **Deposit p+ poly-$Si_{0.4}Ge_{0.6}$ gate**
  - **LPCVD at 410°C**
- **Pattern gate & gate oxide layers using LTO as a hard mask**
- **Release in HF vapor**
- **Coat with ultra-thin (~0.3nm) TiO_2**
  - **ALD at 300°C**

4-T Relay I_D-V_G Characteristic

Plan View SEM of 4-T Relay

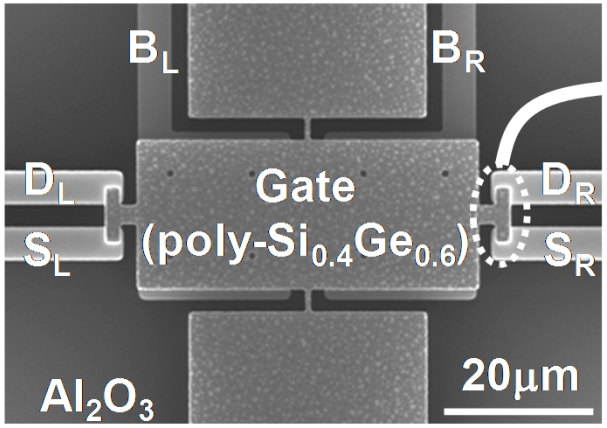




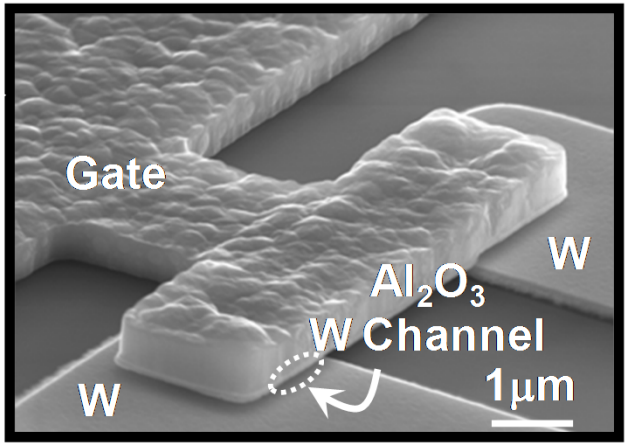
- **Zero I_{OFF}; S < 0.1 mV/dec**
- **Hysteresis is due to pull-in mode operation** ($t_{dimple} > t_{gap}/3$) **and surface adhesion.**

See-Saw Relay Structure

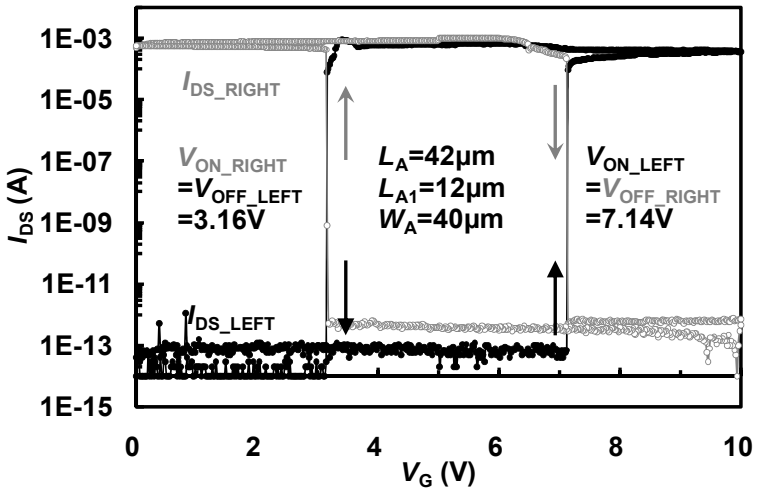
Plan View



Close-Up of Channel Region

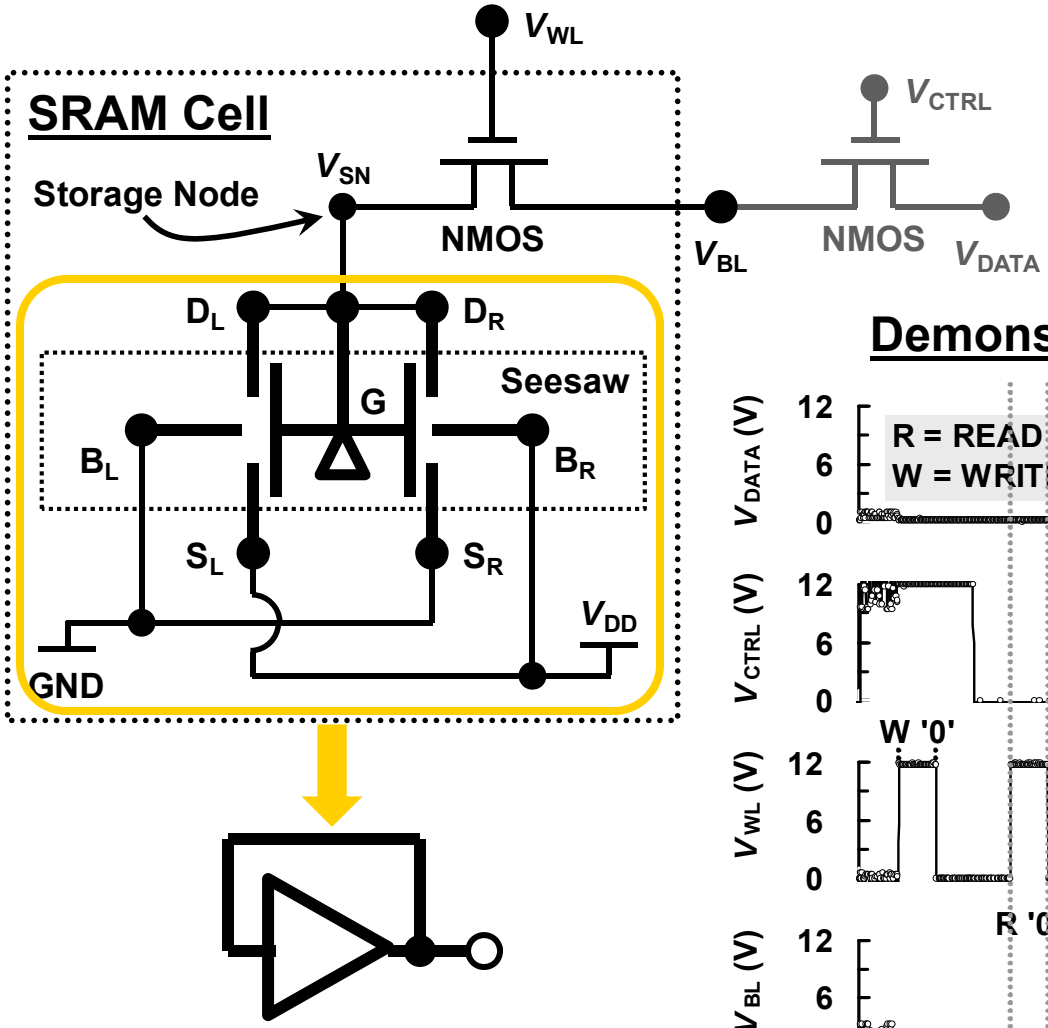


Measured I_D-V_G Characteristics

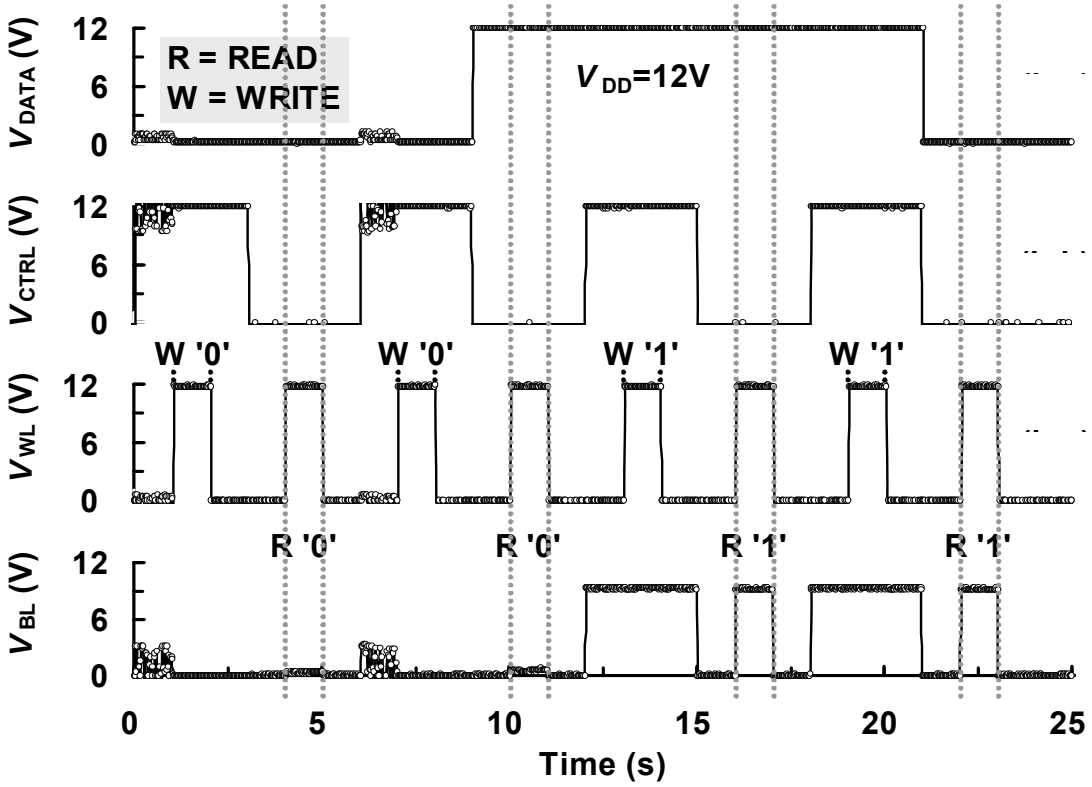


- **Perfectly complementary operation is achieved in left and right channels**
  - **V_{BL} = 0 V; V_{BR} = 10 V**

See-Saw Relay Latch

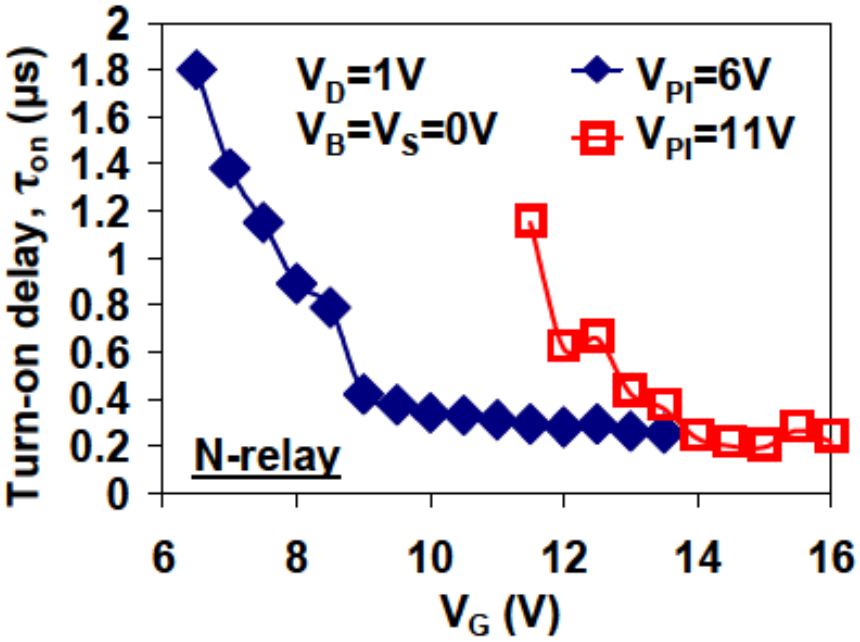


Demonstrated SRAM Cell Operation

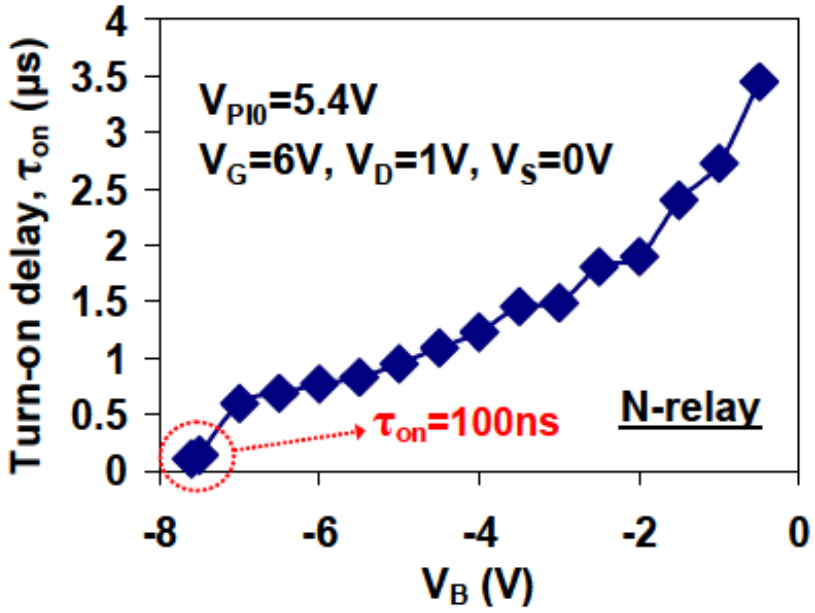


4-T Relay Turn-On Delay

Turn-ON Time *vs.* Gate Voltage



Turn-ON Time *vs.* Body Bias



- **Turn-on delay improves with gate overdrive, and saturates at ~200ns for V_B = 0V.**
- **Turn-on delay improves w/ body biasing to reduce V_{PI} → 100ns turn-on delay**

Relay Scaling

- **Scaling has similar benefits for relays as for MOSFETs.**

Pull-in Voltage: $V_{PI} \propto \sqrt{\frac{k_{eff} t_{gap}^3}{\varepsilon_0 A}}$

Pull-in Delay: $t_{PI} \propto \sqrt{\frac{m t_{dimple}}{k_{eff} t_{gap}}} \left(\frac{V_{PI}}{V_{DD}} \right)$

Relay Parameter	Scaling Factor
Spring constant	1 / κ
Mass	1 / κ^3
Pull-in voltage	1 / κ
Pull-in delay	1 / κ
Switching energy	1 / κ^3
Device density	κ^2
Power density	1

65 nm Relay Design

Parameter	Value
Actuation Area	65×260 nm^2
Actuation Gap	15 nm
Dimple Gap	10 nm
Pull-in voltage	0.4V - 1V
Pull-in delay	100ns – 10ns

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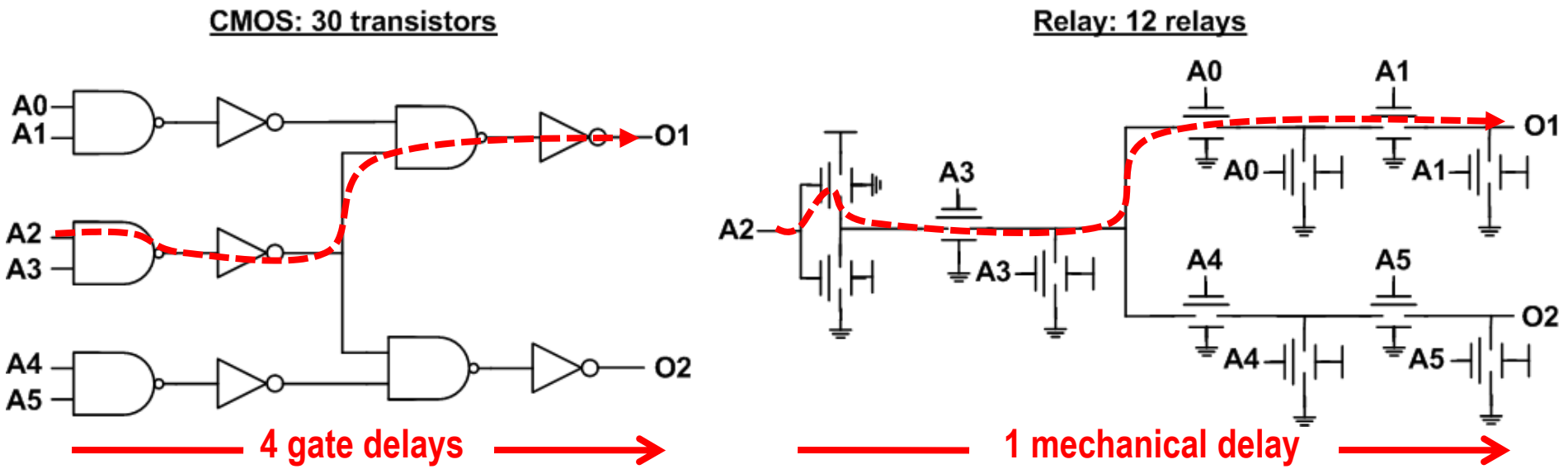
Digital IC Design with Relays

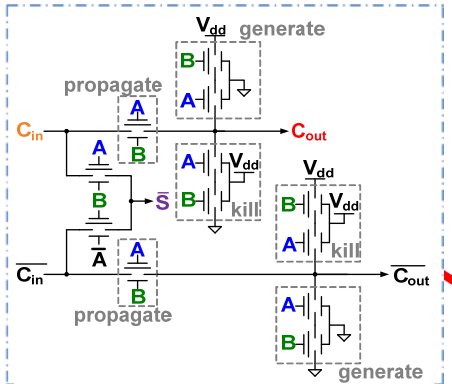


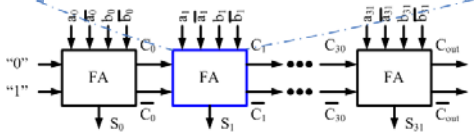
- **CMOS**: delay is set by electrical time constant
  - Quadratic delay penalty for stacking devices

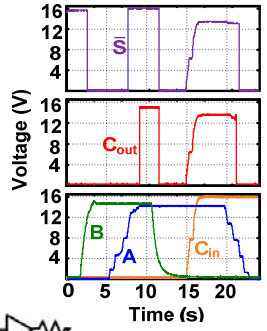
  → Buffer & distribute logical/electrical effort over many stages
- **Relays**: delay is dominated by mechanical movement
  - Can stack ~100 devices before $t_{elec} \approx t_{mech}$

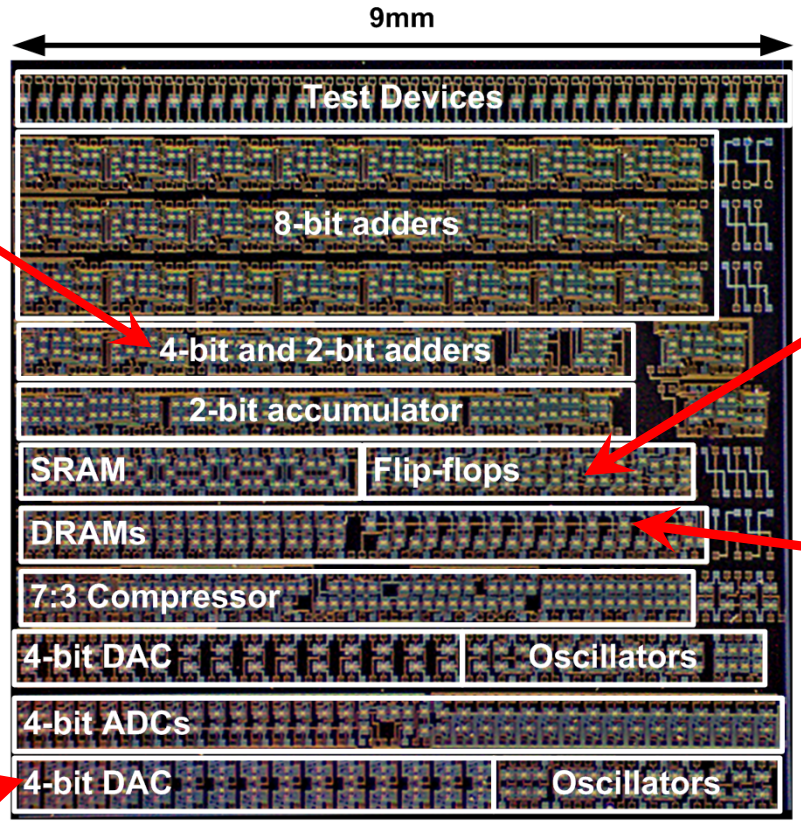
  → Implement relay logic as a single complex gate

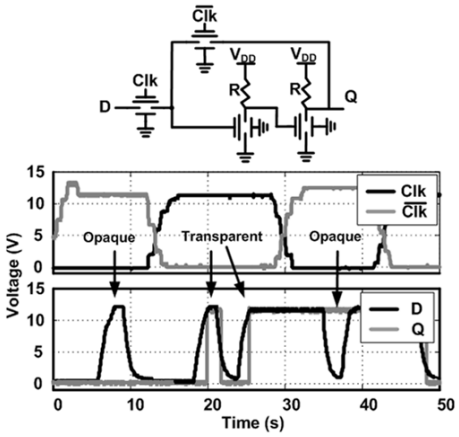
Relay-Based VLSI Building Blocks

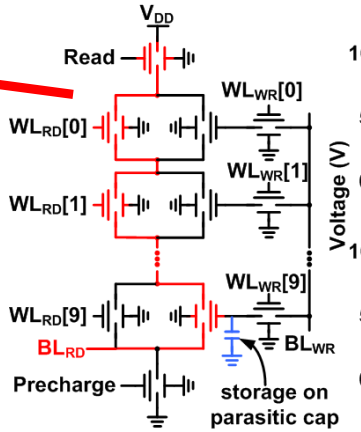


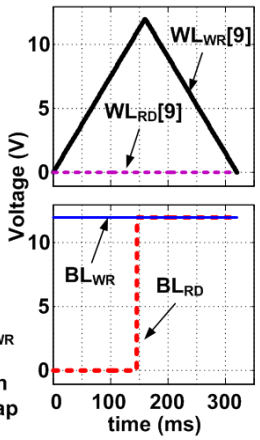


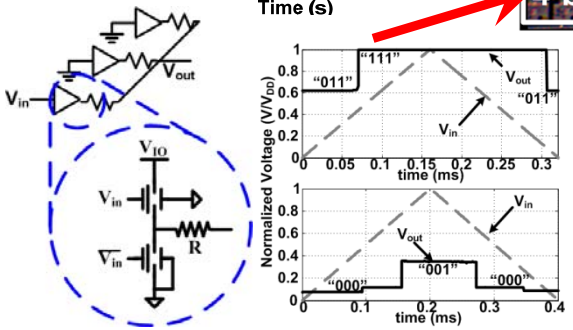








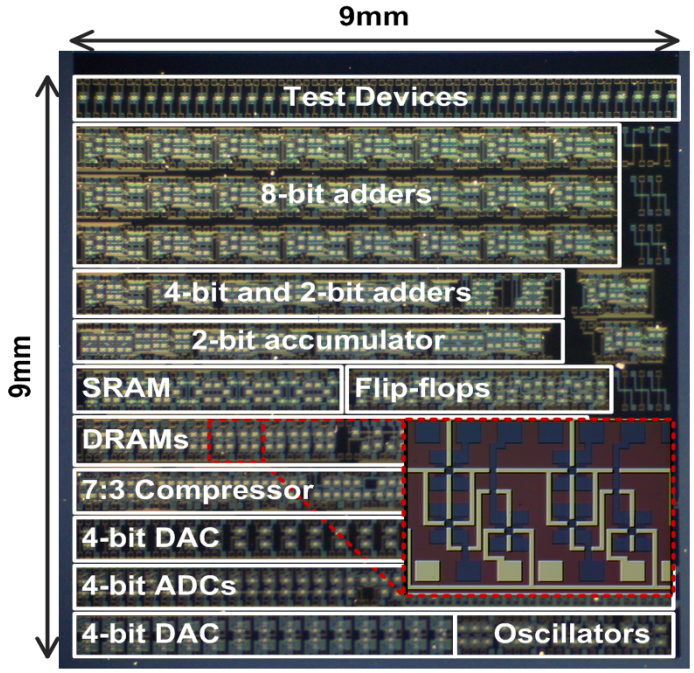




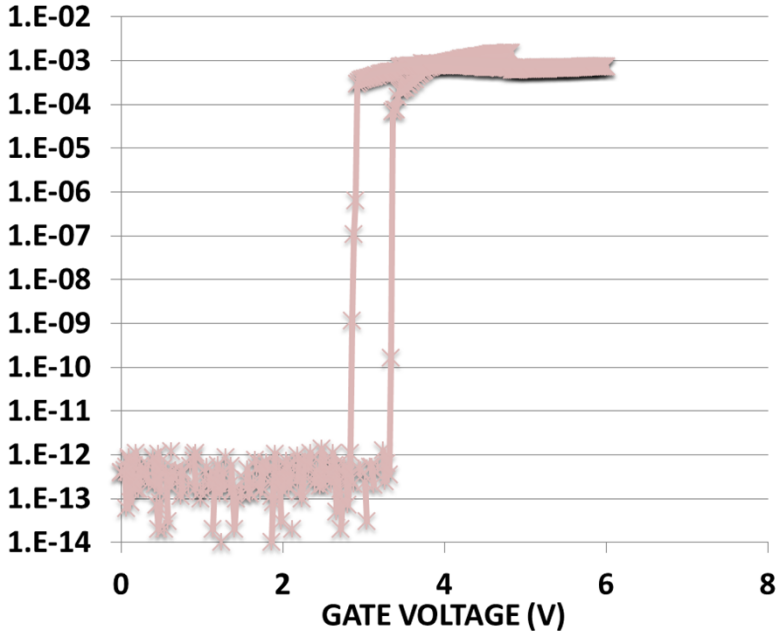
2010 ISSCC Jack Raper Award for Outstanding Technology Directions

Technology Transfer to SEMATECH

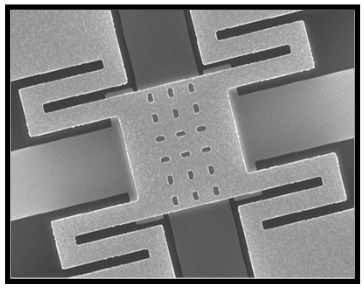
UC Berkeley: 1 µm litho



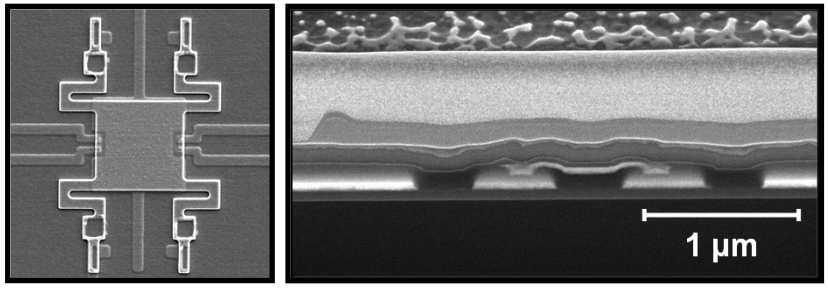
SEMATECH: 0.25 µm litho



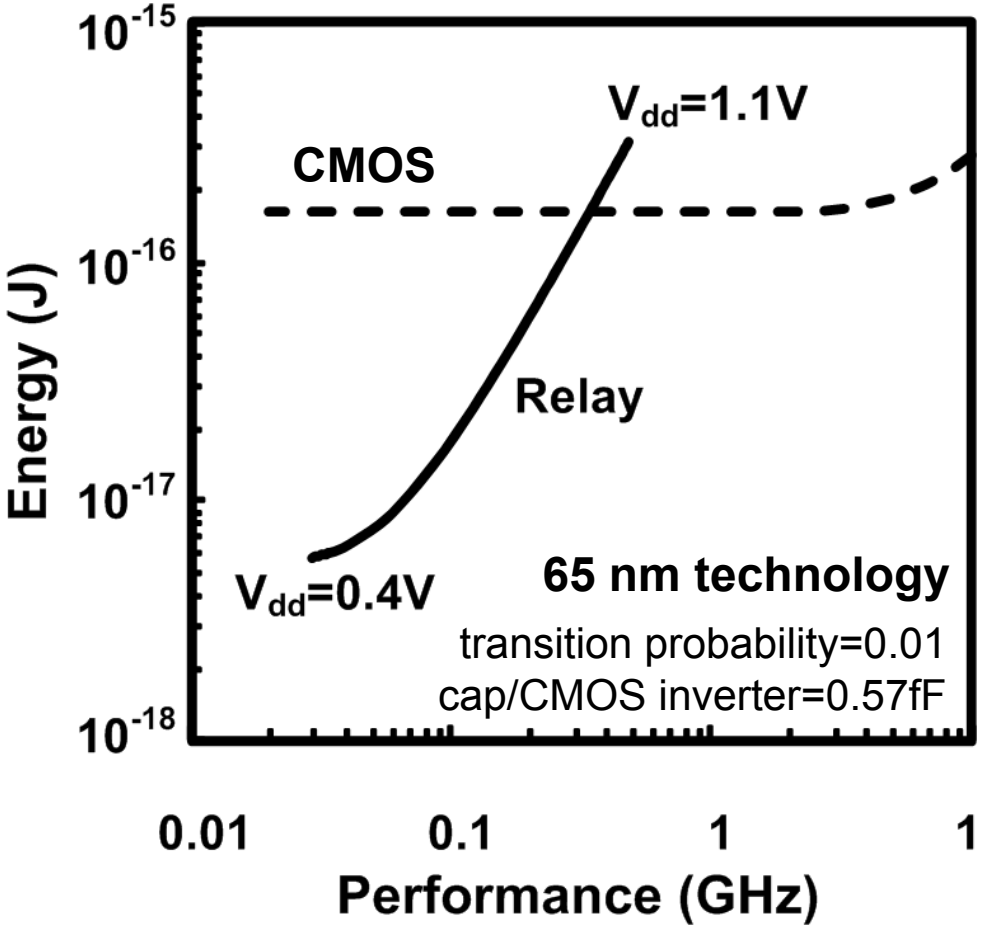
1st prototype: 120 µm x 150 µm

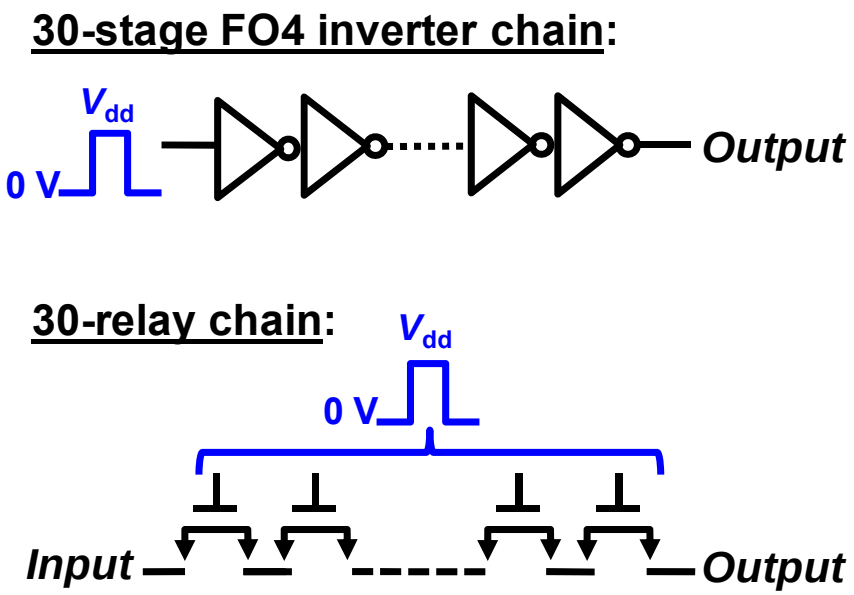


Scaled relay: 20 µm x 20 µm



Energy-Delay Comparison with CMOS





- **Scaled relay technology is projected to provide for >10x energy savings, at clock rates up to ~100MHz**

Outline

- Electro-Mechanical Relay Design for Digital ICs
- Relay-Based IC Design
- Relay Reliability
- Summary

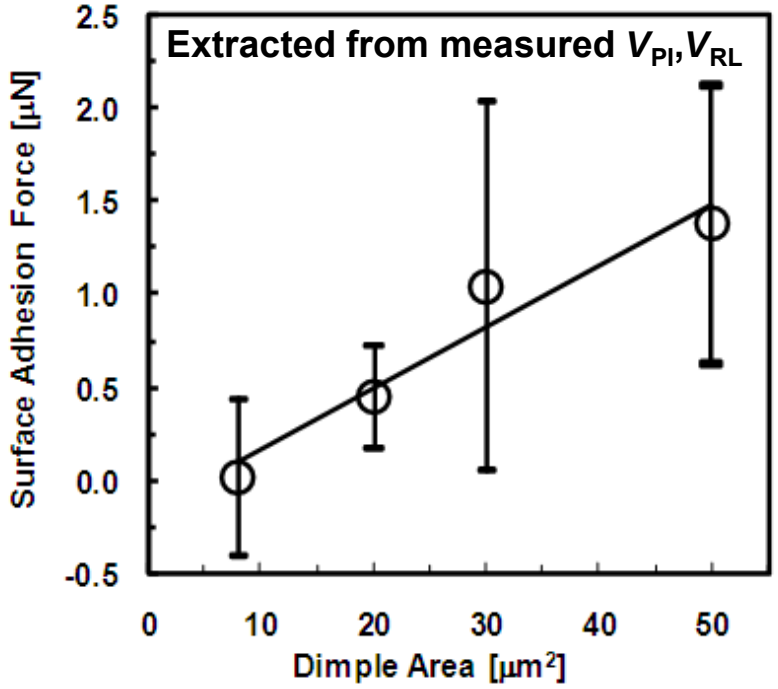
Stiction

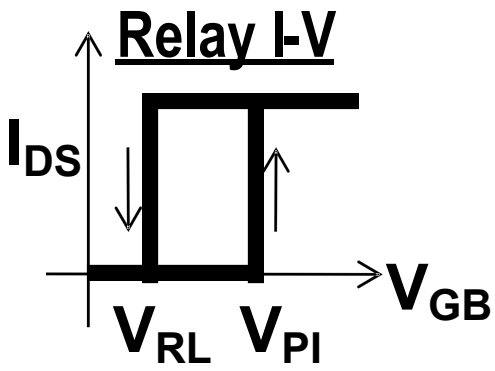
- **Hysteresis voltage (V_{PI}-V_{RL}) scales with the pull-in voltage (V_{PI})**

$$V_{PI} - V_{RL} = V_{PI}\left[1 - 2.6\sqrt{\frac{t_{dimple}}{t_{gap}}}\left(1 - \frac{t_{dimple}}{t_{gap}}\right)\right]$$

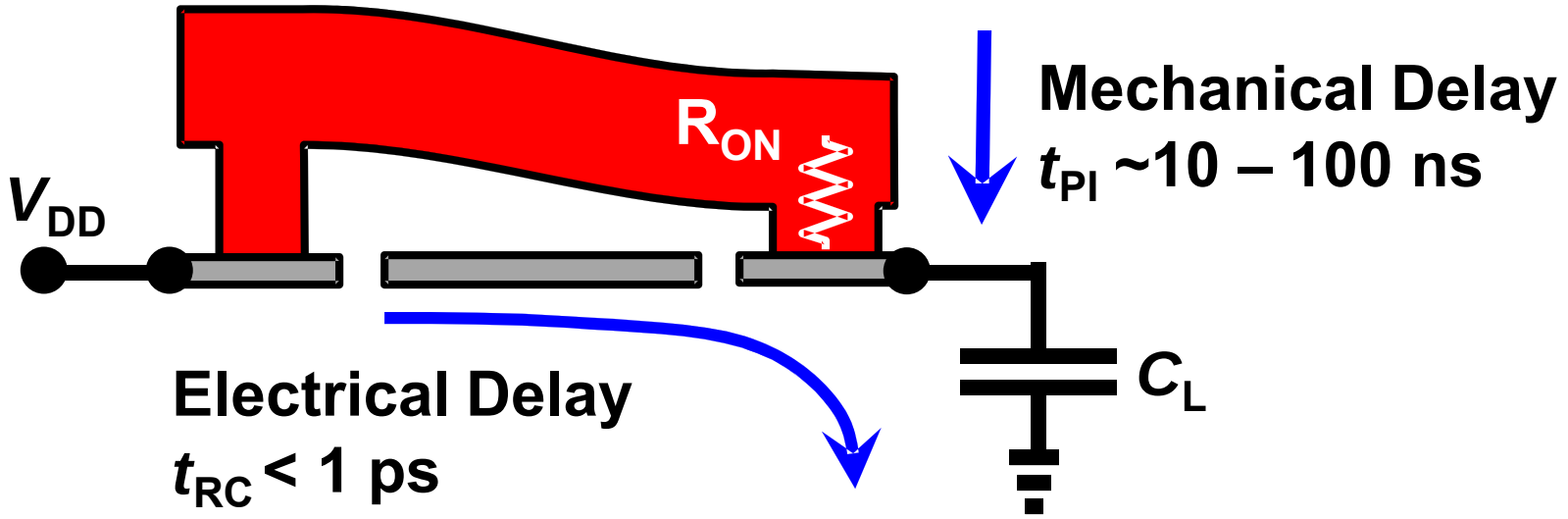
ignoring surface adhesion force

- **Surface adhesion force scales with area of contacting region(s):**





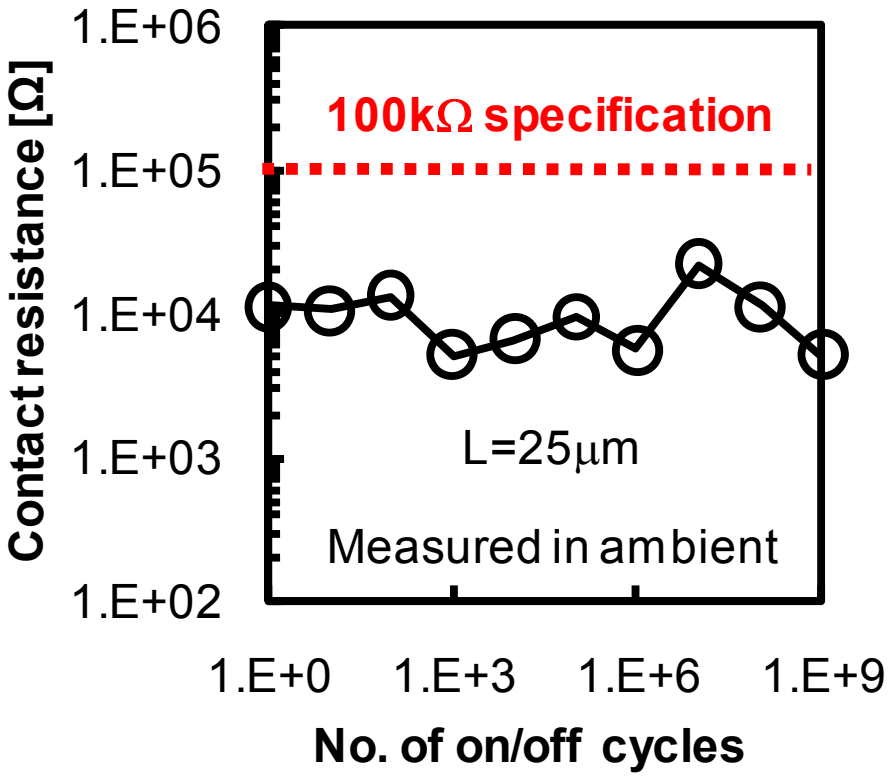
Contact Design for Logic Gates



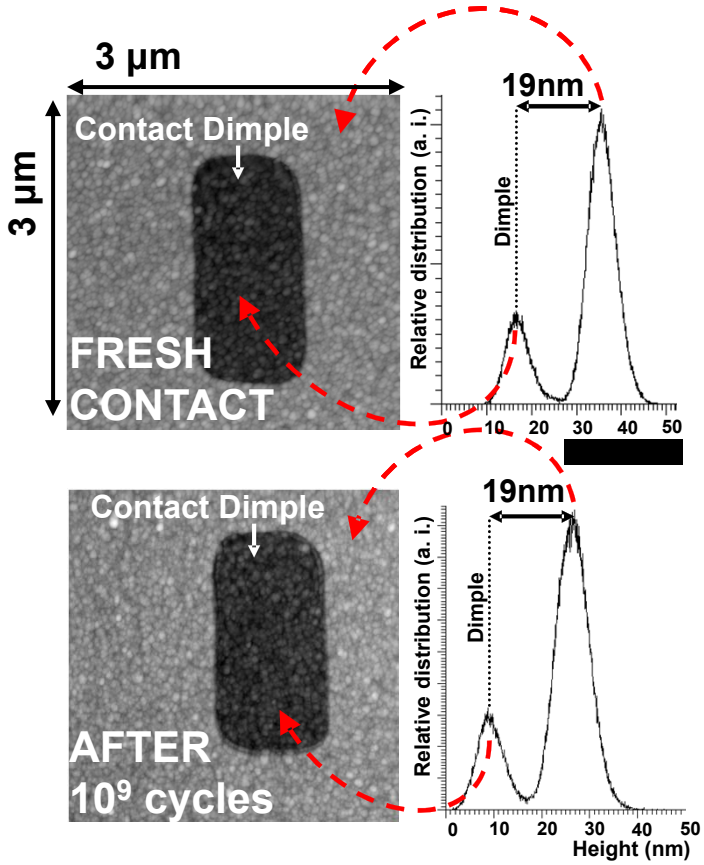
- High R_{ON} (up to ~10 kΩ) is acceptable
  - ➥ To achieve good endurance and reliability:
    1. Use hard electrode material → Tungsten
    2. Apply a surface coating to reduce surface force and current density → ALD TiO_2

Contact Stability

ON-state Resistance *vs.* # ON/OFF Cycles

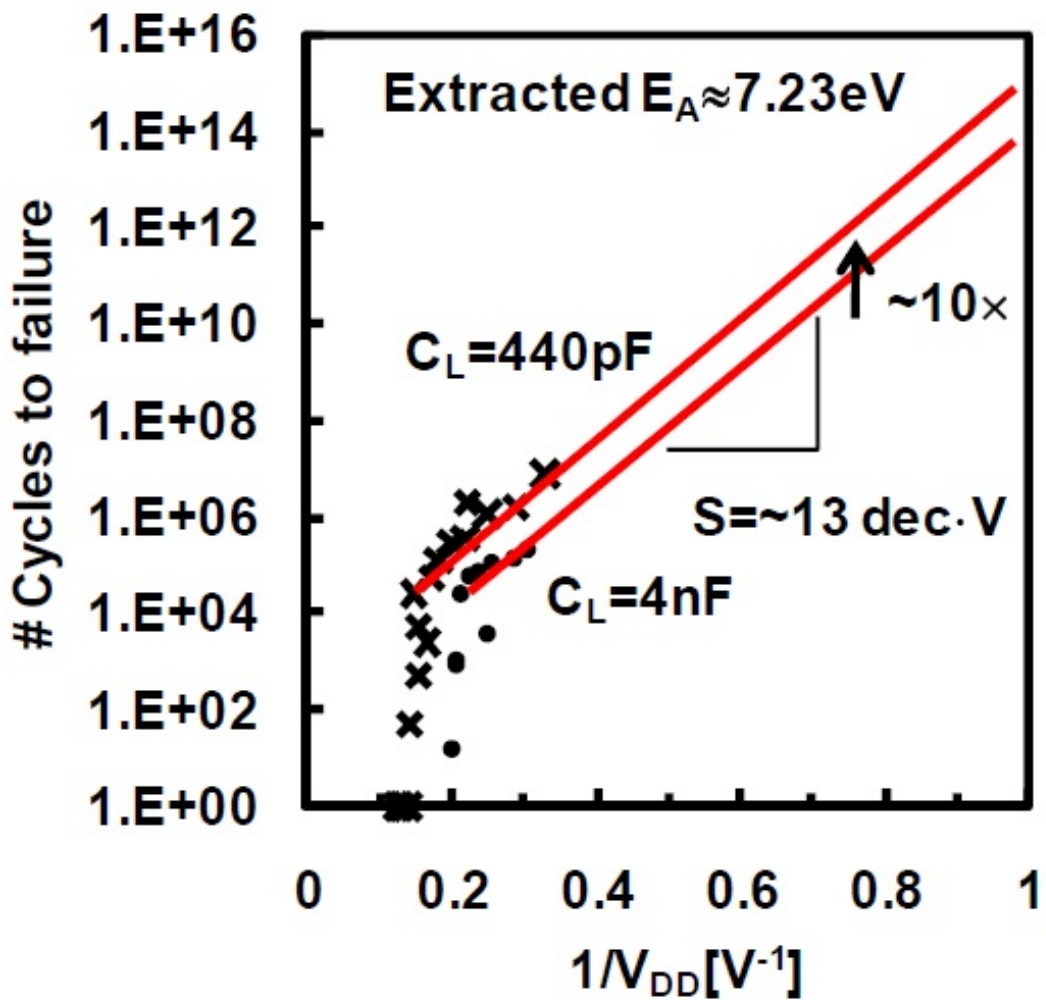


AFM Measurements



- **Variations are likely due to *W* oxidation**
- **No surface wear is seen after 1 billion ON/OFF cycles**

Relay Endurance



- Endurance increases exponentially with decreasing V_{DD}, and linearly with decreasing C_L
- Endurance is projected to exceed 10^{15} cycles @ 1V

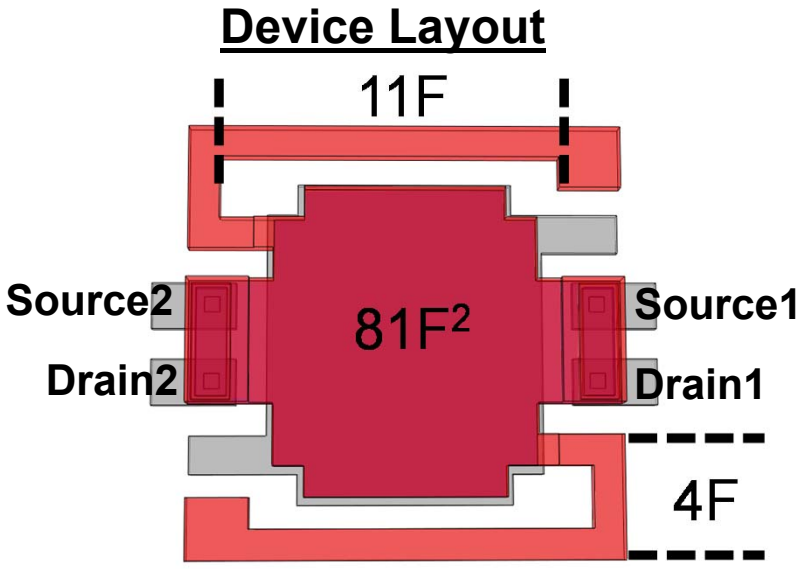
Nanoscale Relay Technology

- **Sub-100 mV operation is possible**
  - Zero I_{OFF} enables V_{DD} scaling without increasing leakage power
  - Hysteresis voltage scales with pull-in voltage

Node (nm)	15	11	8
Actuation Gap (nm)	5.5	4	3
Pull-in Voltage (mV)	113	100	86
Release Voltage (mV)	73	66	58

* All dimensions scaled with technology node

Node (nm)	15	11	8
Supply Voltage (V)	0.4	0.4	0.4
Mechanical Delay (ns)	6.2	3.8	2.5

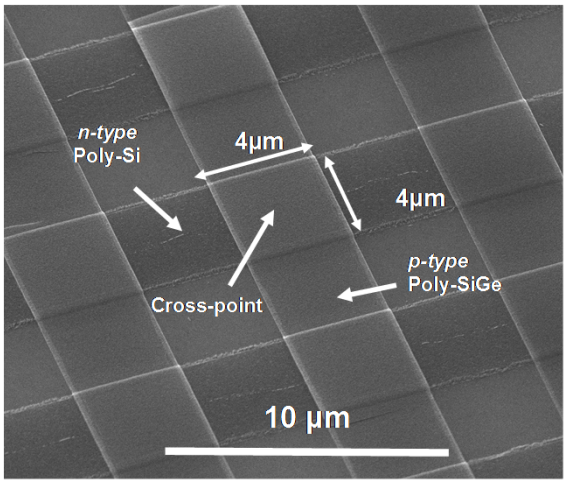


Footprint for two switches = 14×14F²

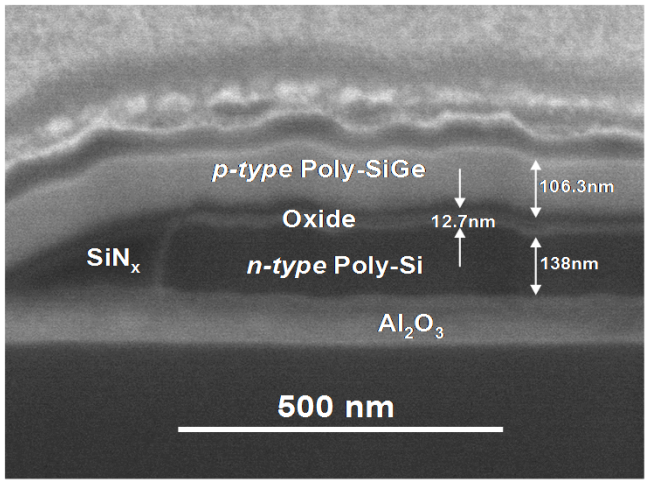
Cross-Point Electro-Mechanical NVM Array

- **Electro-mechanical diode cell design:**
  - **Open circuit in Reset state**
  - **Diode in Set state** (built-in electric-field → electrostatic force)

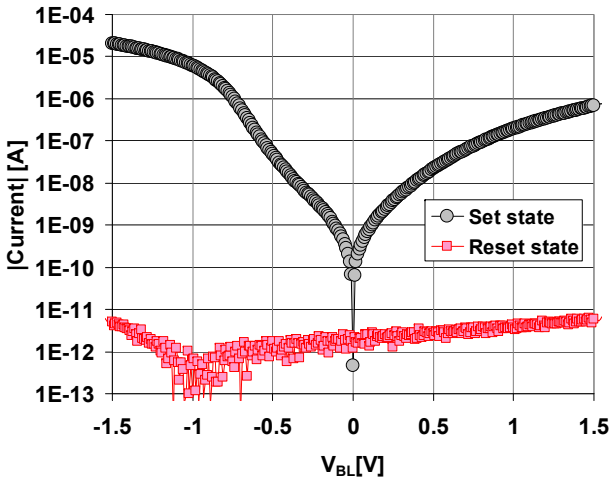
SEM of NVM Array



Cross-sectional SEM



Measured *I-V*



- ✓ **Smallest cell layout area ($4F^2$); 3-D stackable**
- ✓ **Low-voltage operation**
- ✓ **Excellent retention behavior**
- ✓ **Multiple-time programmable (> 10,000 cycles)**

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Summary

- Mechanical switches have the ideal properties of zero off-state leakage and abrupt turn-on/turn-off.

  → potential for achieving very low E/op (<1 aJ)

- Dimensional scaling is required to achieve low-voltage operation and adequate reliability
  - V_{DD} < 100 mV
  - endurance > 10^{15} cycles

  Materials optimization can yield further improvements.

- New circuit and system architectures are needed to fully realize the potential energy-efficiency benefits.

  → device and circuit design co-optimization is key!

Acknowledgements

- **NEM-Relay Team (current and former) members:**

  Post-docs: **Louis Hutin; Hei Kam** (now with Intel)**;**
  Vincent Pott (now with IME, Singapore)

  Students: **Rhesa Nathanael, Jaeseok Jeon** (now with Rutgers U.)**,**
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  Chengcheng Wang and Kevin Dwan (UCLA)

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  - **DARPA/MARCO Focus Center Research Program**
    - **Center for Circuits and Systems Solutions (C2S2)**
    - **Center for Materials, Structures, and Devices (MSD)**
  - **NSF Center of Integrated Nanomechanical Systems (COINS)**
  - **NSF Center for Energy Efficient Electronics Science (E3S)**

- **UC Berkeley Micro/Nanofabrication Laboratory**

Frequently Asked Questions

1. **Displacement (*x*) due to gravity?**

$$x = \frac{mg}{k_{eff}} \cong 0.1\,\mathrm{fm}$$

2. **Mechanical shock causing pull-in?**
   - **requires acceleration > $10^6 g$**

     due to small *m* (10^{-14} grams)

3. **Thermal vibration?**

$$\tfrac{1}{2} k_B T = \tfrac{1}{2} k_{eff} x^2$$ **→ x ≈ 1Å for T = 300K**