Nanomechanical Switches for Ultra-Low-Power Computation and Memory

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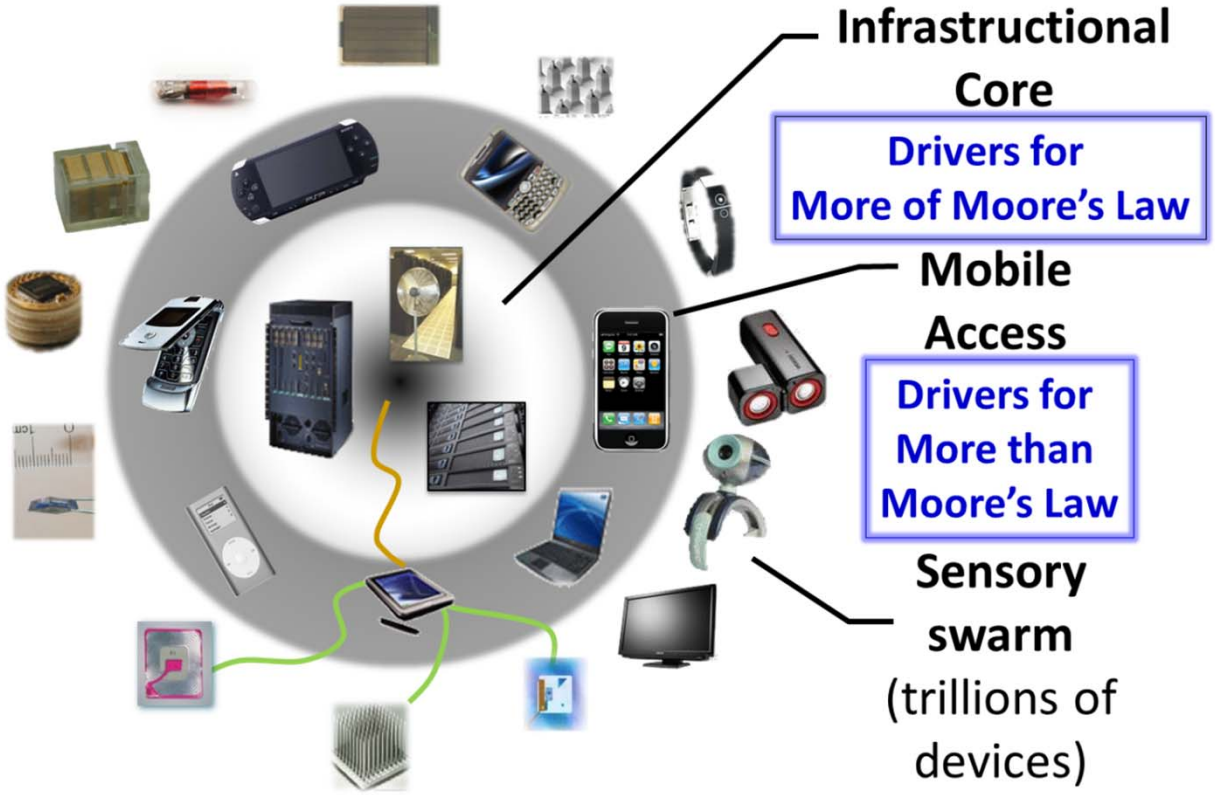
A Vision of the Future



Jan Rabaey, *ASPDAC* 2008

Smart Grid

Traffic management

Smart Buildings

Infrastructure maintenance

- **Emergence of Ambient Intelligence:**

  Sense/monitor, communicate and react to the environment

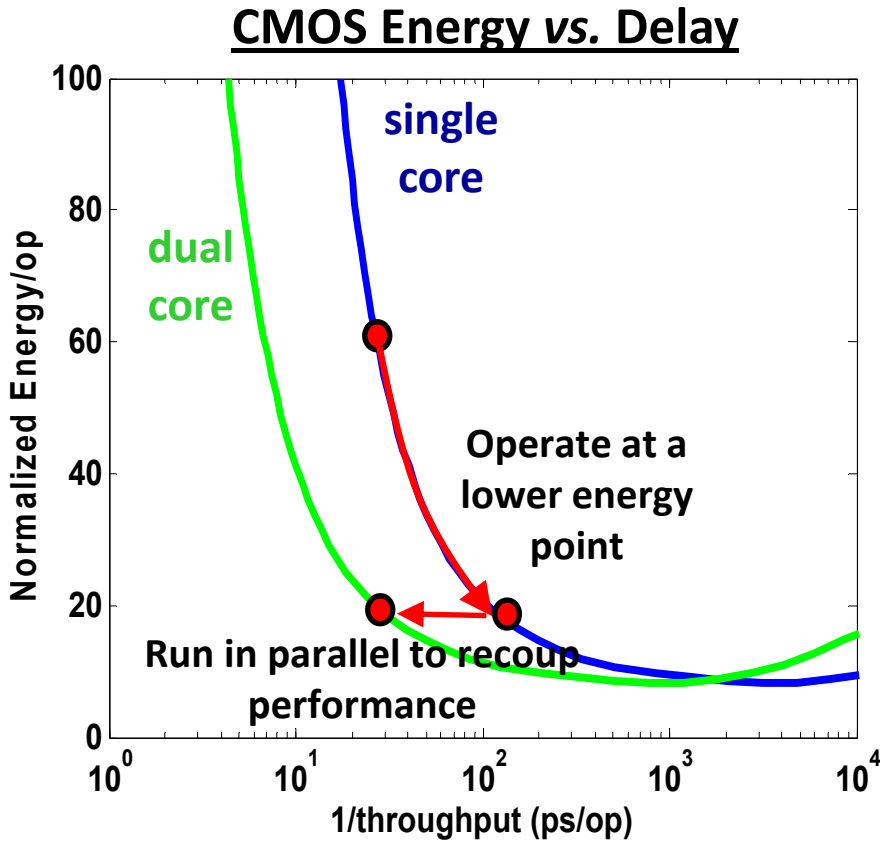
  → Ultra-low-power, robust computing technology required!

Outline

- **Introduction**
  - CMOS energy efficiency
  - Why mechanical switches?
- **Nanomechanical switches for computing**
- **Nanomechanical memory**
- **Summary**

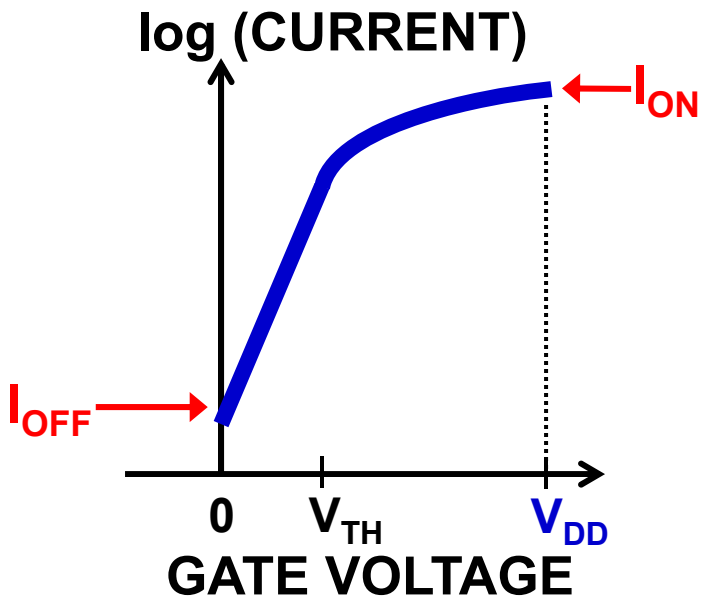
Improving CMOS Energy Efficiency

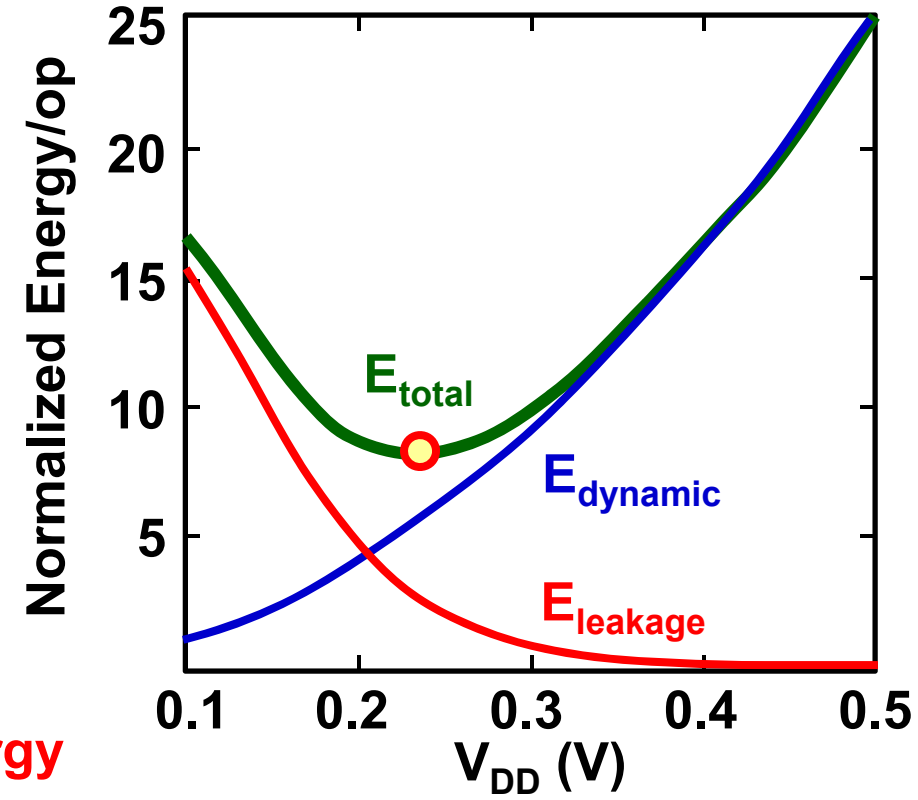
- **Parallelism is the main technique to improve system performance under a power density constraint.**



CMOS Energy Efficient Limit

- Leakage & sub-threshold slope define minimum Energy/op





Dynamic Energy Leakage Energy

$$E_{total} = \alpha L_d f C V_{DD}^2 + L_d f I_{OFF} V_{DD} t_{delay}$$

$$t_{delay} = L_d f C V_{DD} / (2 I_{ON})$$

α: Activity Factor

L_d: Logic Depth

f: Fanout

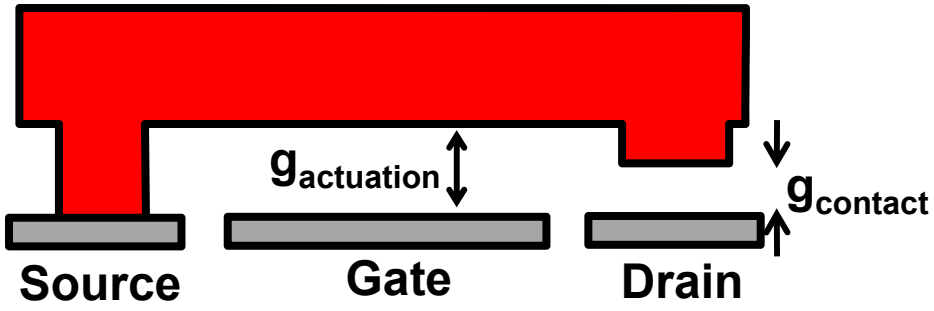
C: Capacitance per Stage

Future Logic Switch Requirements

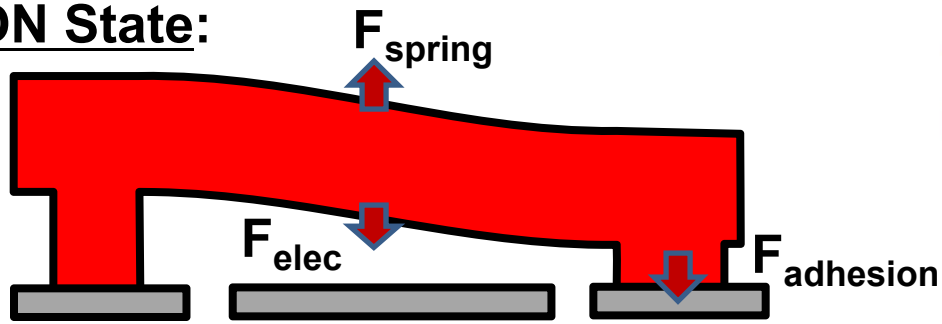
- **Zero leakage** → **Zero standby power**
- **Simple design** → **Low cost**
- **Robust** → **Wide applicability**
- **Reconfigurable** → **Versatility**
- **Low operating voltage** → **Low active power**

Micro-Electro-Mechanical Switch

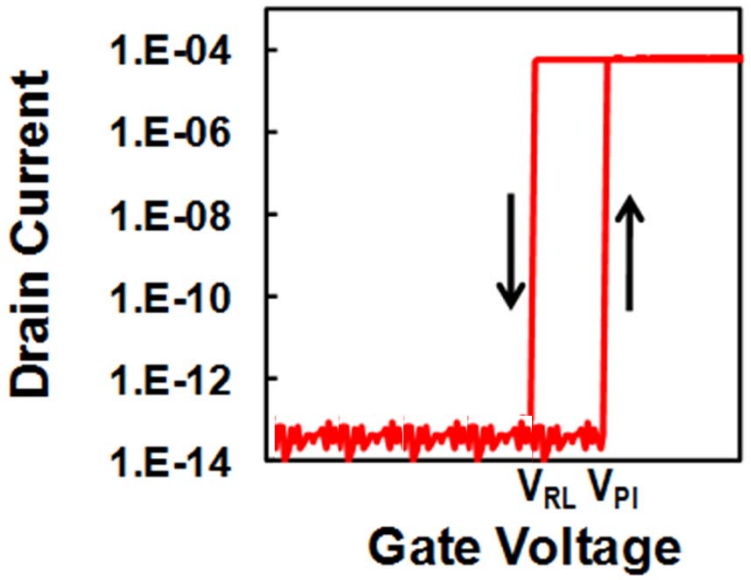
OFF State (as fabricated): NORMALLY OFF



ON State:



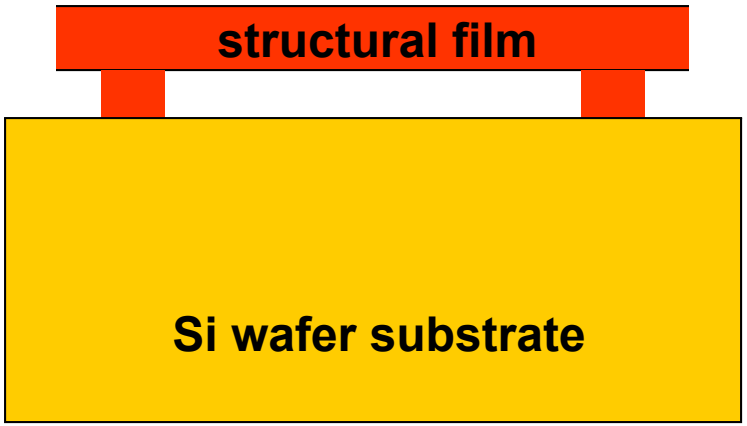
Measured *I-V* Characteristic



- Zero OFF-state current (I_{OFF}); abrupt switching
  - Turns on by electrostatic force when $|V_{GS}| \geq V_{PI}$
  - Turns off by spring restoring force when $|V_{GS}| \leq V_{RL}$

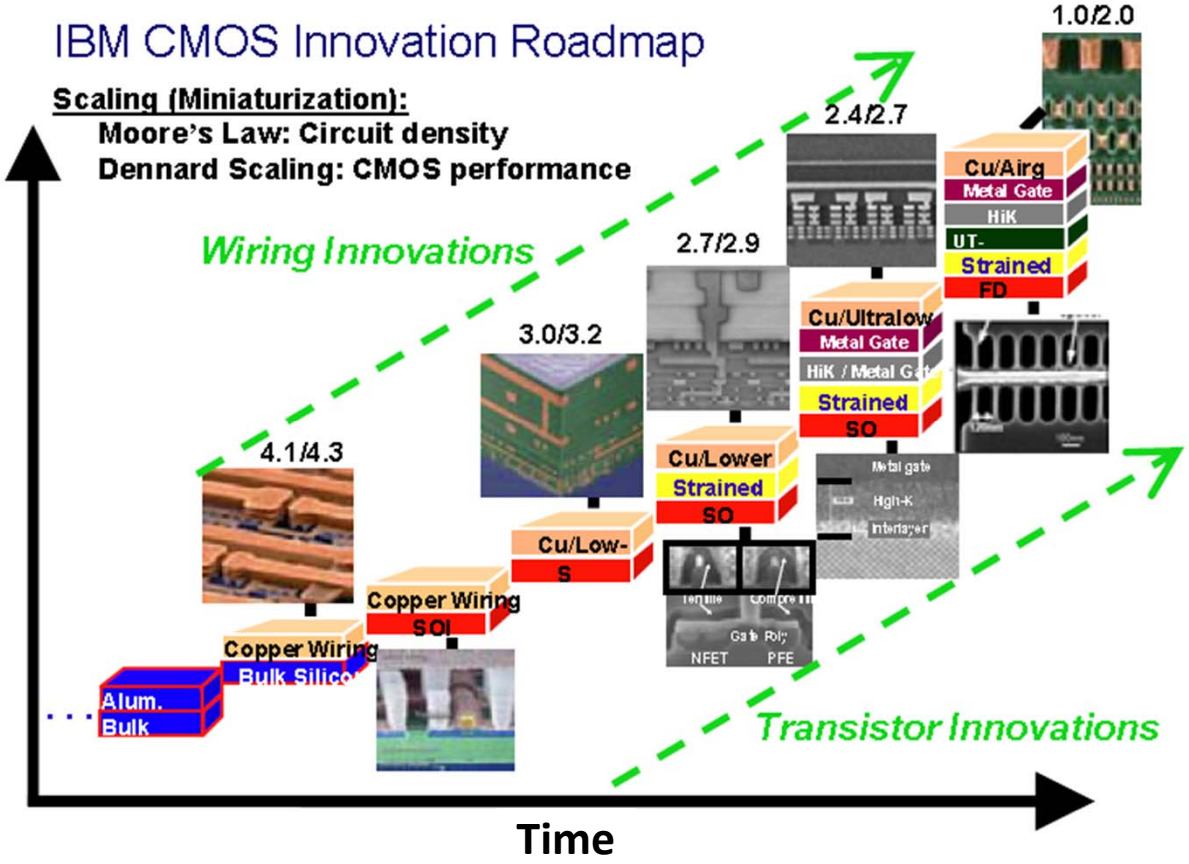
Surface Micromachining Process

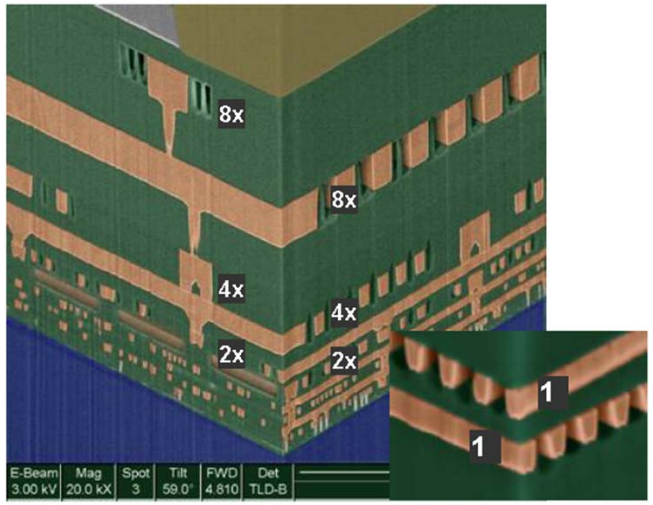
Cross-sectional View



- **Mechanical structures can be made using conventional microfabrication techniques**
- **Structures are freed by selective removal of sacrificial layer(s)**

Three-Dimensional (3-D) Integration





D. C. Edelstein, *214th ECS Meeting*, Abstract #2073, 2008

- **The semiconductor industry has developed air-gap back-end-of-line (BEOL) processes which can be leveraged to make MEM switches.**

Outline

- Introduction

- **Nanomechanical switches for computing**
  - Logic switch designs
  - Relay-based integrated circuit design
  - Relay scaling limit
- Nanomechanical memory

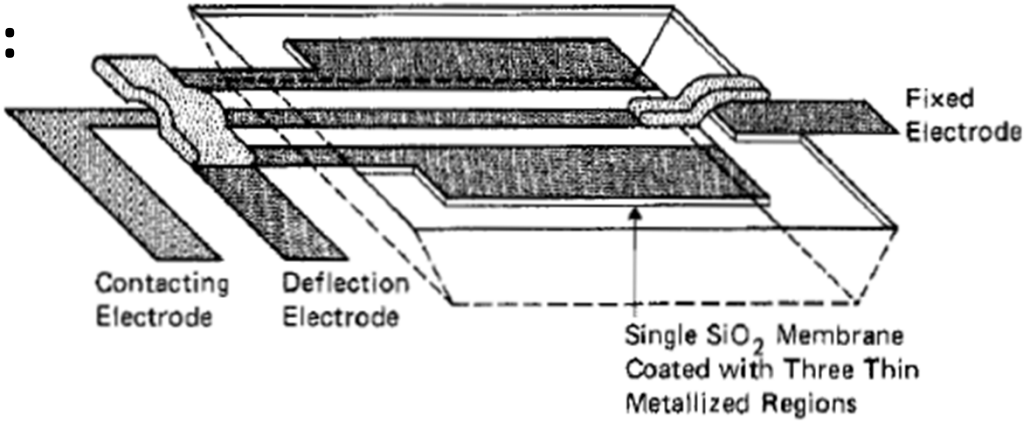
- Summary

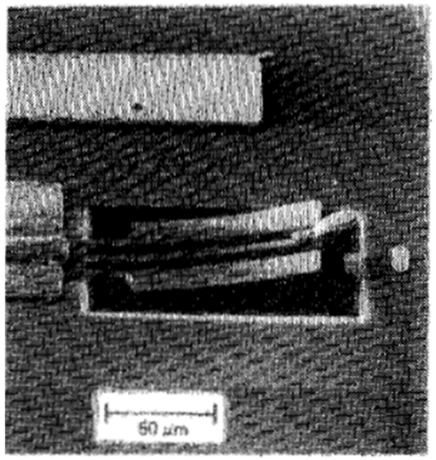
First Micro-Relay

K. E. Petersen, *IEEE Trans. Electron Devices*, Vol. 25, pp. 1241-1250, 1978

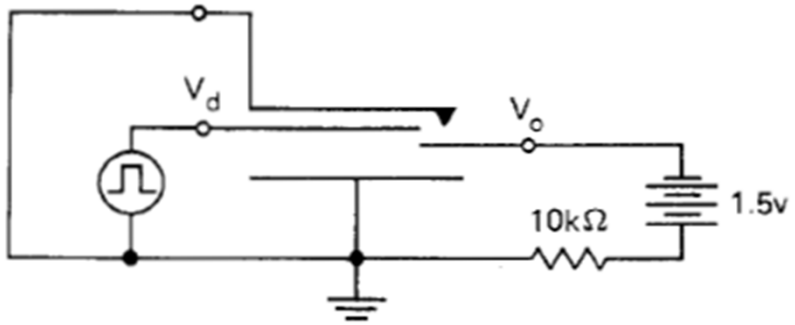
- **4-terminal (4-T) micro-electro-mechanical switch demonstrated**
  - **0.35 μm thick × 76 μm long SiO_2 membrane; 7 μm actuation gap**
  - **60 V switching voltage; 40 μs switching delay**

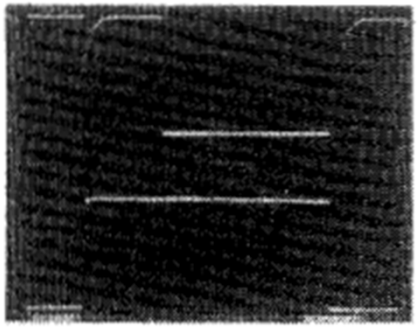
Structure:





Device Operation:

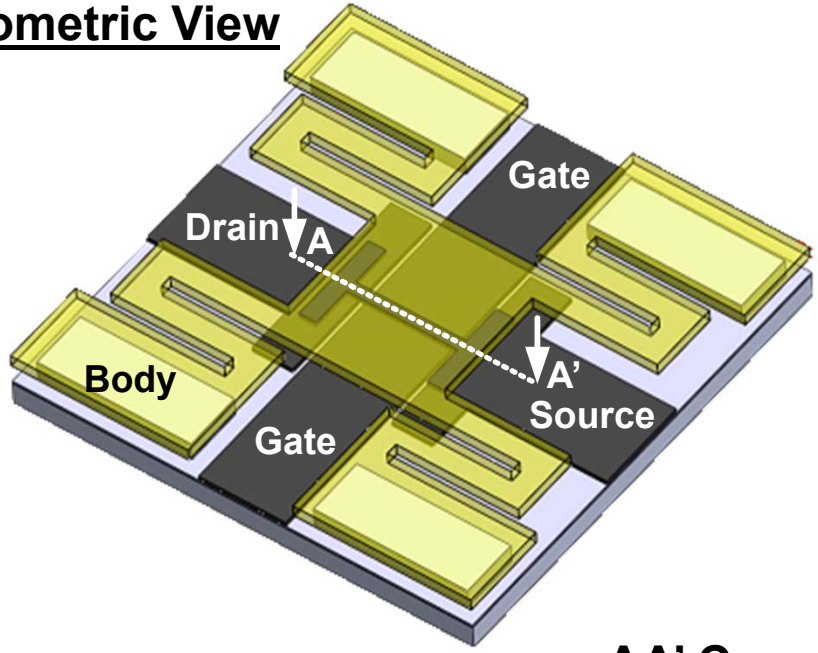




Scaled 4-T Electro-Mechanical Relay

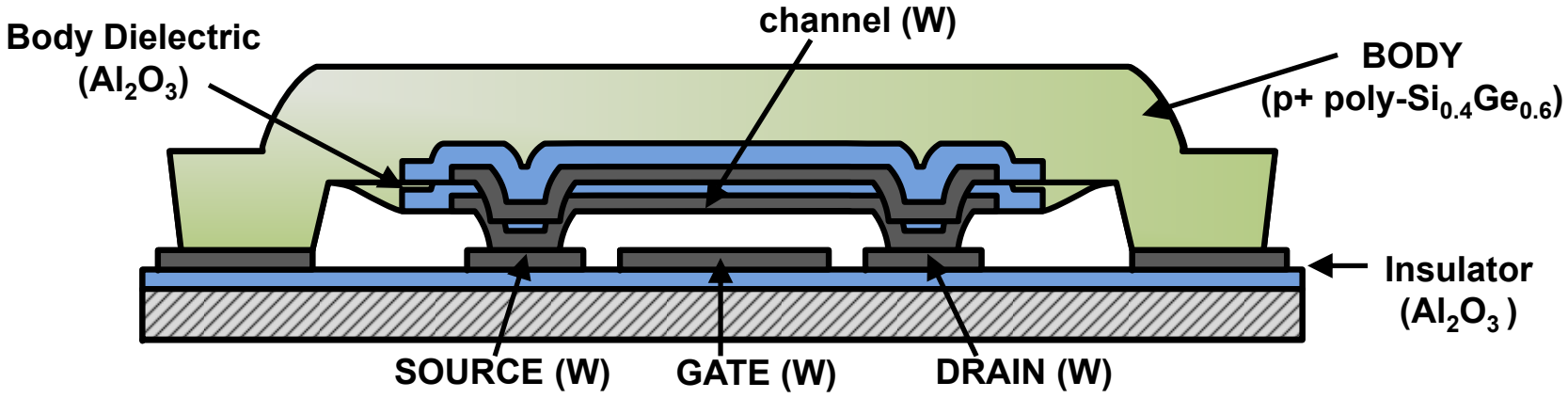
R. Nathanael *et al.*, *IEDM* 2009

Isometric View



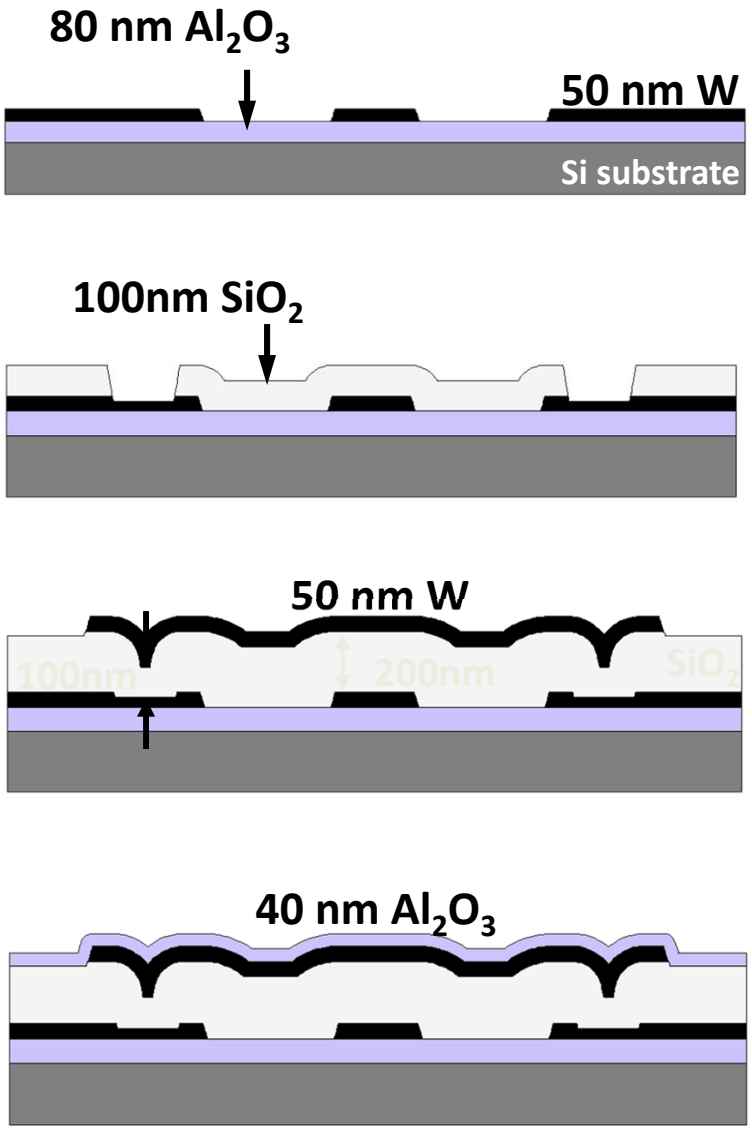
- **Voltage applied between the gate and movable body brings the channel into contact with source & drain**
  - **Oxide layer insulates body**

AA' Cross-section



4-T MEM Relay Process Flow

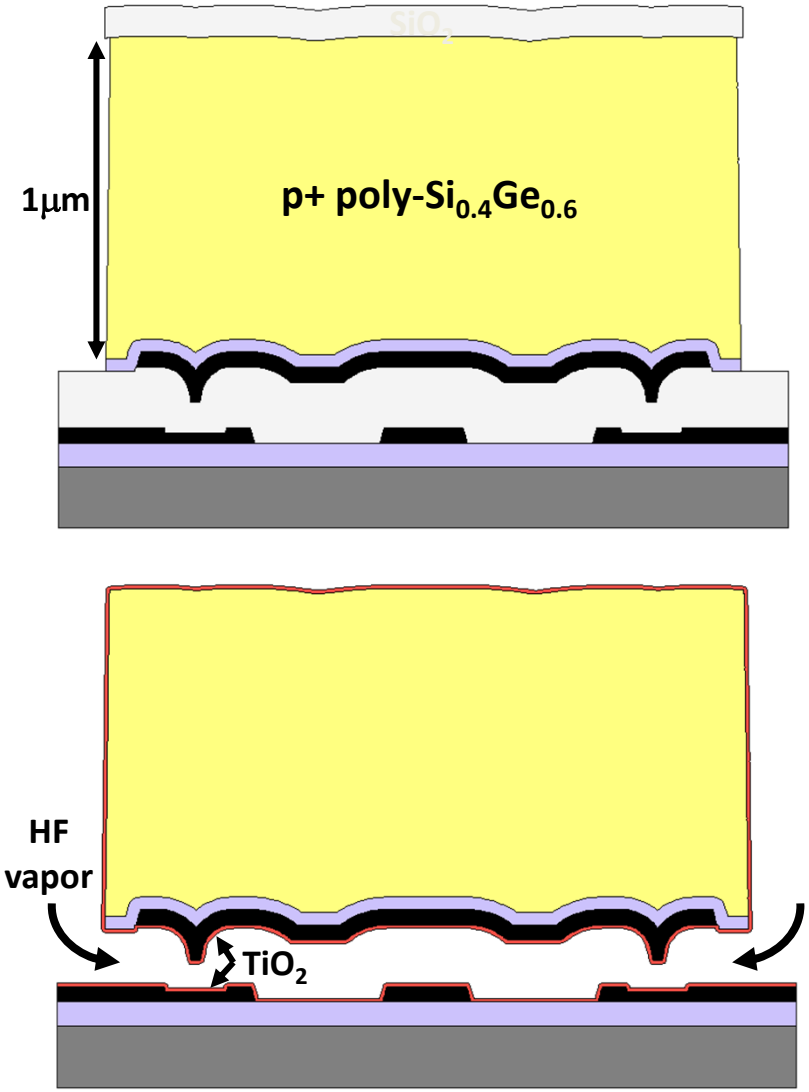
R. Nathanael *et al.*, *IEDM* 2009



- Deposit Al_2O_3 substrate insulator
  - ALD at 300°C
- Deposit & pattern W electrodes
  - DC magnetron sputtering
- Deposit 1st sacrificial LTO
  - LPCVD at 400°C
- Define contact regions
- Deposit 2nd sacrificial LTO
  - $t_{dimple} = t_{gap} / 2$
- Deposit & pattern W channel
- Deposit Al_2O_3 gate oxide

Process Flow (cont'd)

R. Nathanael *et al.*, *IEDM* 2009

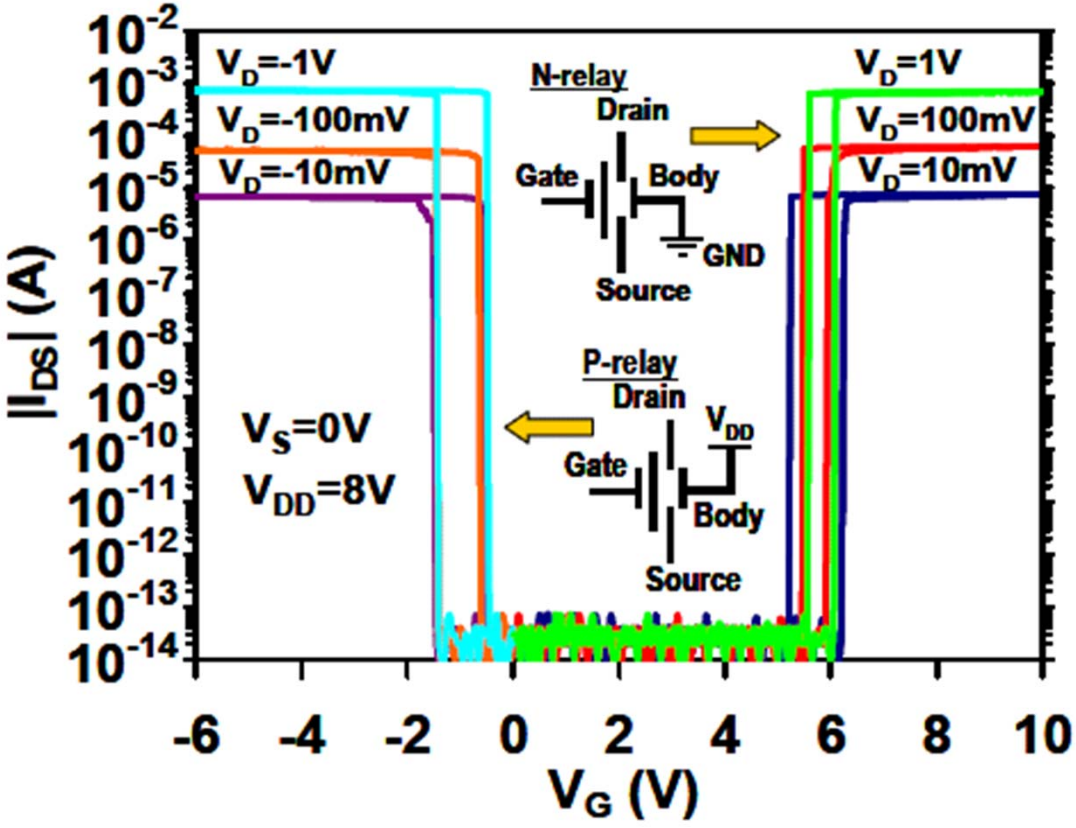


- Deposit p+ poly-$Si_{0.4}Ge_{0.6}$ gate
  - LPCVD at 410°C
- Pattern gate & gate oxide layers using LTO as a hard mask
- Release in HF vapor
- Coat with ultra-thin (~0.3nm) TiO_2
  - ALD at 300°C

I_D-V_G Characteristics

R. Nathanael *et al.*, *IEDM* 2009

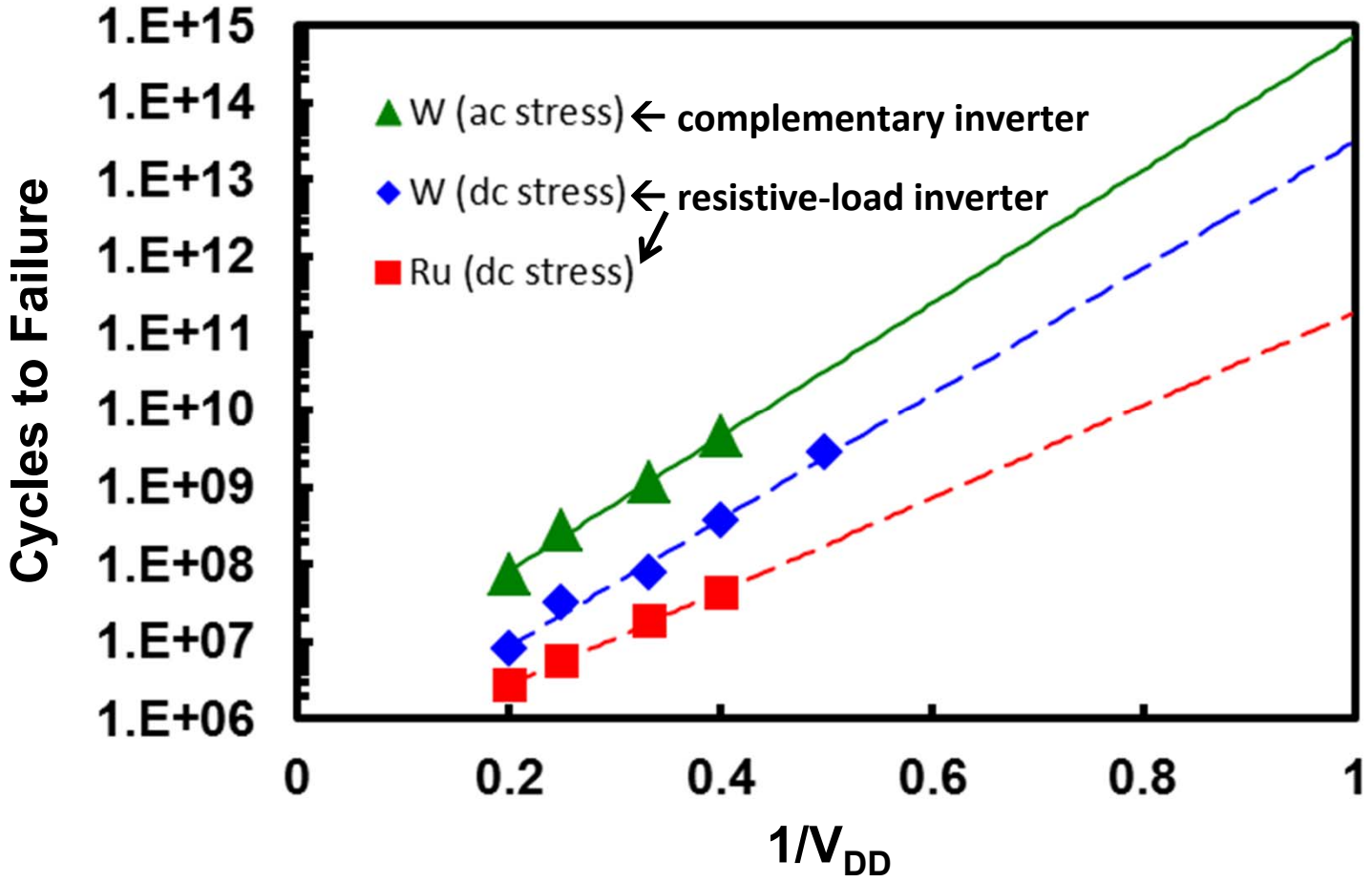
- **NMOS- or PMOS-like operation is achieved by applying an appropriate body bias voltage:**



✓ **Zero off-state leakage; abrupt switching (*SS* < 0.1 mV/dec)**

Contact Endurance

Y. Chen *et al.*, to be published

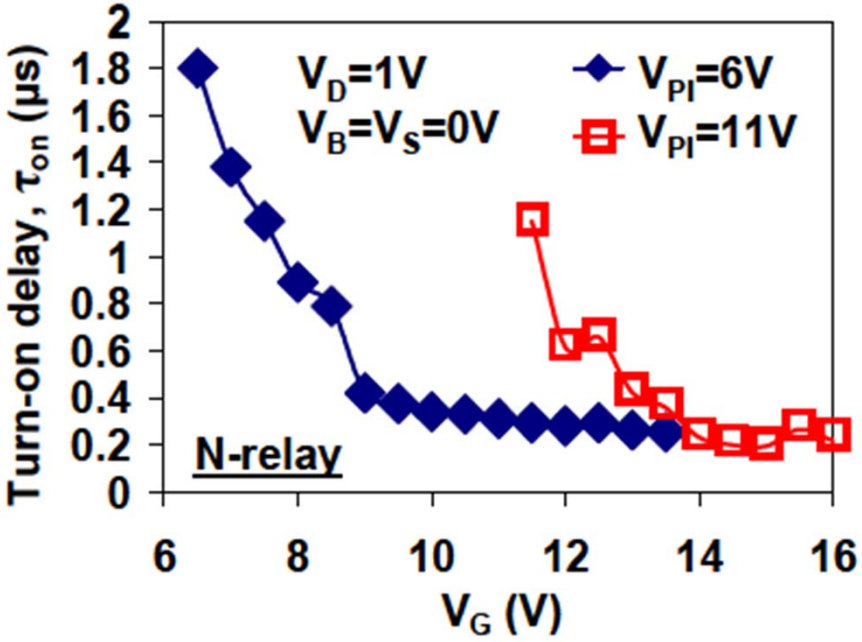


- **Endurance increases exponentially with decreasing V_{DD}**
  - projected to reach **10^{15} cycles at 1 Volt**, for W contacts

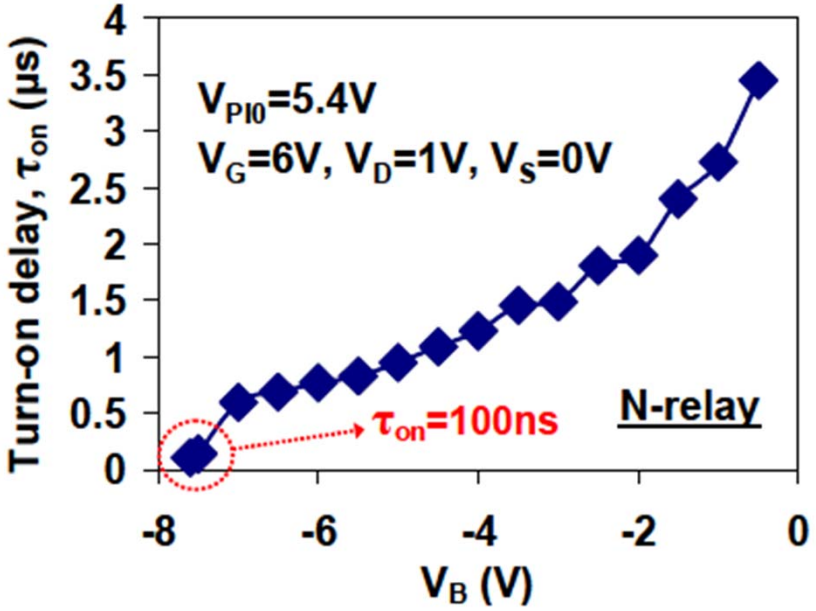
Switching Delay

R. Nathanael *et al.*, *IEDM* 2009

Turn-ON Time *vs.* Gate Voltage



Turn-ON Time *vs.* Body Bias



- **Turn-on delay improves with gate overdrive, saturates at ~200 ns for V_B = 0V.**
- **Turn-on delay improves w/ body biasing to reduce V_{PI} → 100 ns turn-ON delay**

Relay Scaling

- **Scaling has similar benefits for relays as for MOSFETs:** $k_{\text{eff}} \propto \frac{EWt^3}{l^3}$

Pull-in Voltage: $V_{\text{PI}} \propto \sqrt{\frac{k_{\text{eff}}\, g_{\text{actuation}}^3}{\varepsilon_0 A}}$

Pull-in Delay: $t_{\text{PI}} \propto \sqrt{\frac{m g_{\text{contact}}}{k_{\text{eff}}\, g_{\text{actuation}}}} \left(\frac{V_{\text{PI}}}{V_{\text{DD}}} \right)$

Relay Parameter	Scaling Factor
Spring constant, k_{eff}	$1 / \kappa$
Mass	$1 / \kappa^3$
Pull-in voltage, V_{PI}	$1 / \kappa$
Pull-in delay, t_{PI}	$1 / \kappa$
Switching energy	$1 / \kappa^3$
Device density	κ^2
Power density	1

Scaled Relay Design

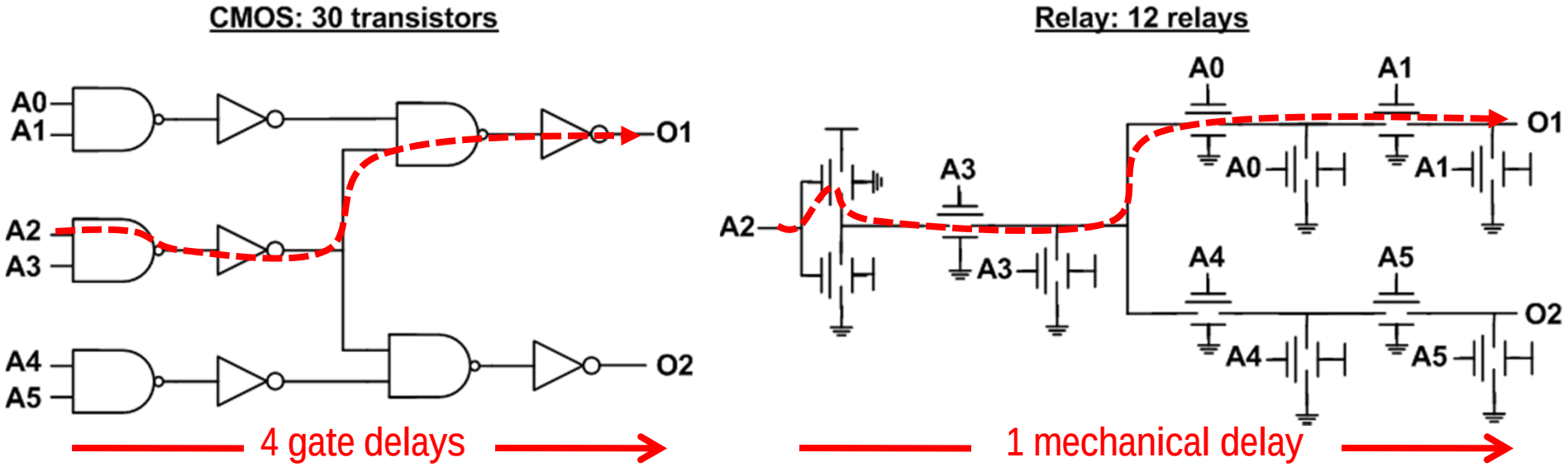
Parameter	Value
Actuation Area, A	1 μm^2
Actuation Gap, t_{gap}	4.3 nm
Dimple Gap, t_{dimple}	3 nm
Pull-in voltage, V_{PI}	9.4 mV
Release voltage, V_{RL}	6 mV*
^Pull-in delay, t_{PI}	25 ns

Beam length = 3.5 μm, thickness = 40 nm, width = 83 nm

^ $V_{DD}/V_{PI} = 3$ *Assumes negligible contact adhesion

Digital Circuit Design with Relays

F. Chen *et al.*, *ICCAD* 2008

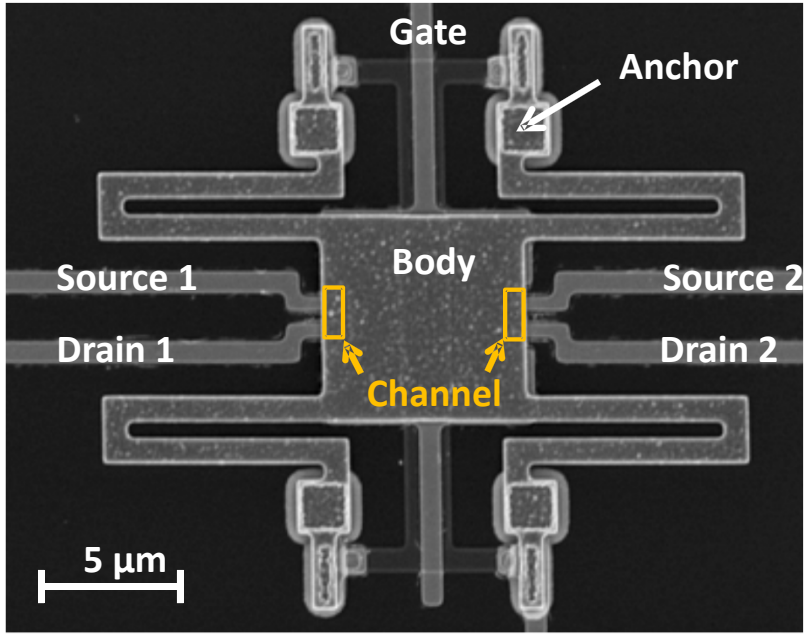


- **CMOS: delay is set by electrical time constant**
  - Quadratic delay penalty for stacking devices
  - → Buffer & distribute logical/electrical effort over many stages
- **Relays: delay is dominated by mechanical movement**
  - Can stack ~100 devices before $t_{d,elec} \approx t_{d,mech}$
  - →Implement relay logic as a single complex gate

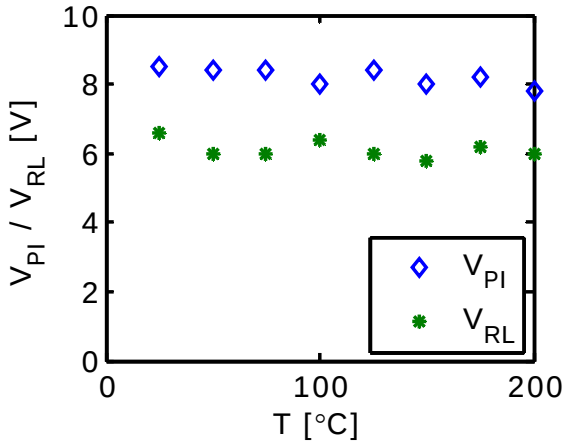
Single-Gate, Dual-Source/Drain Relay

I-R. Chen *et al.*, *ECS Spring Meeting* 2012 and *Transducers* 2013

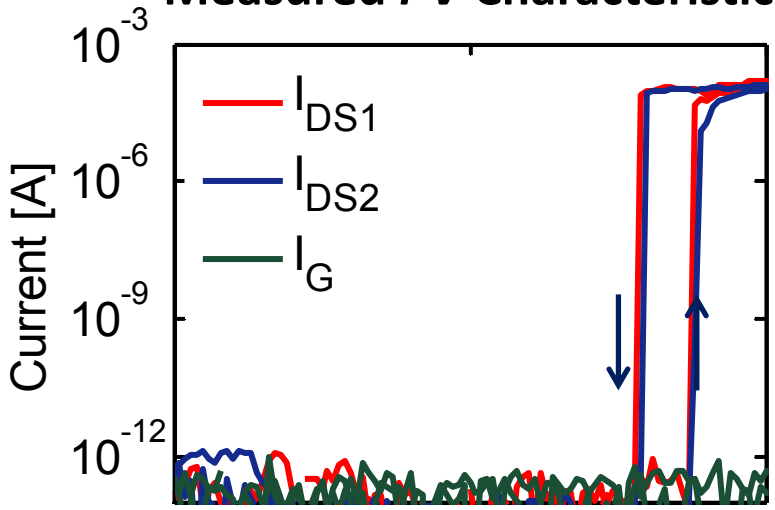
Plan-View SEM

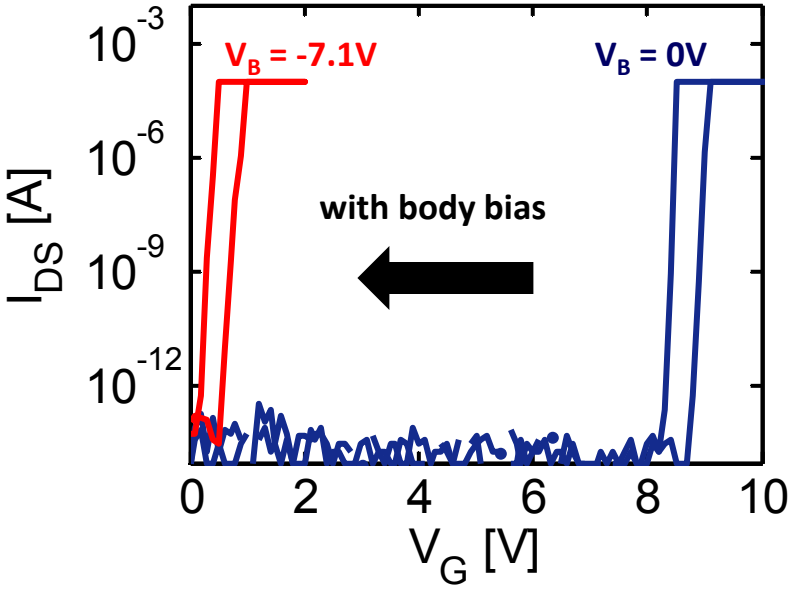


Temperature Dependence:



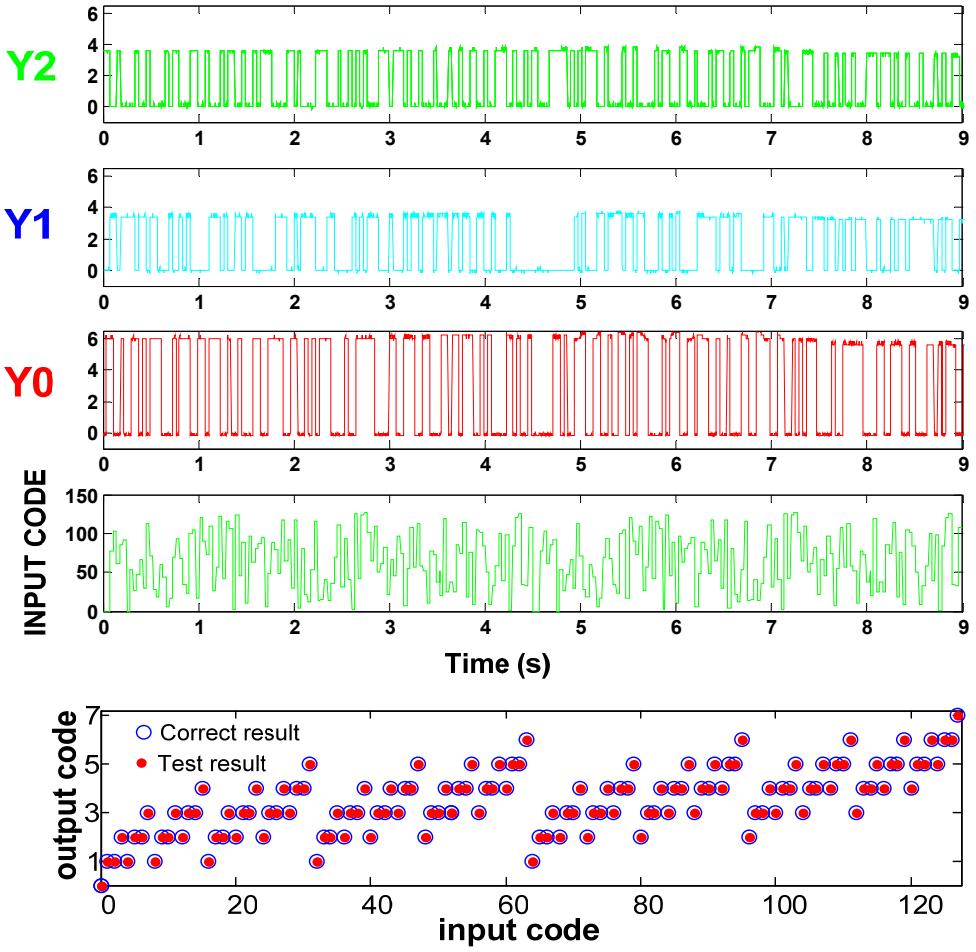
Measured *I-V* Characteristics



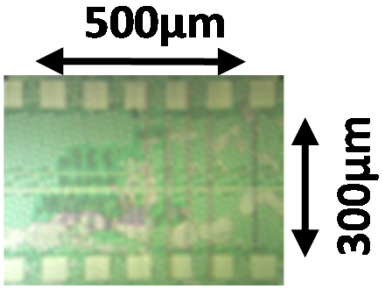


Relay Multiplier Sub-Ckt: (7:3) Compressor

Fariborzi *et al.*, *ASSCC* 2011



- Most complex scaled MEM-relay integrated circuit reported to date (46 relays)



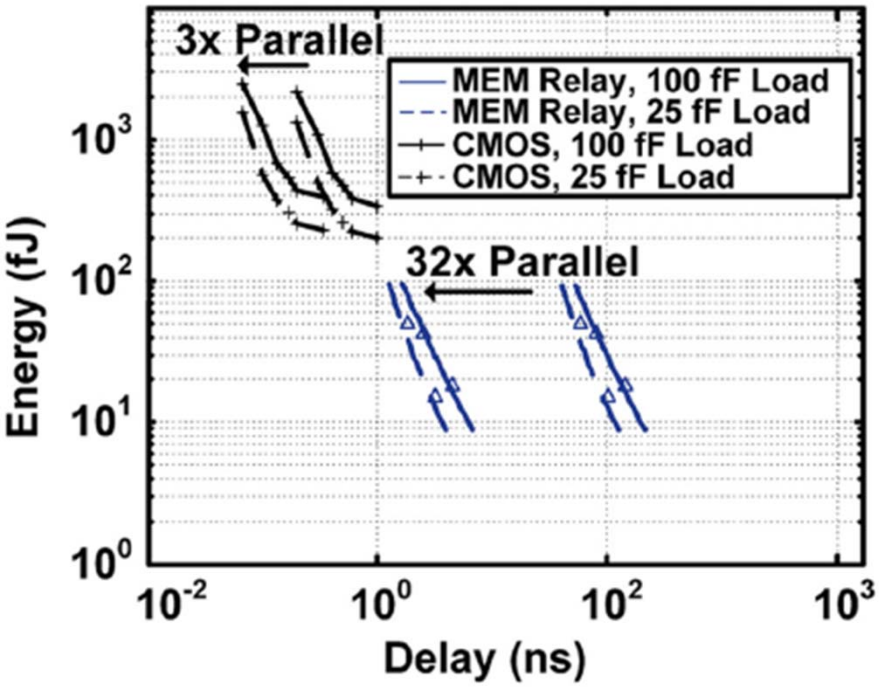
Energy-Delay Comparison with CMOS

M. Spencer *et al.*, *JSSC* 2011; H. Fariborzi *et al.*, *ESSCIRC* 2011

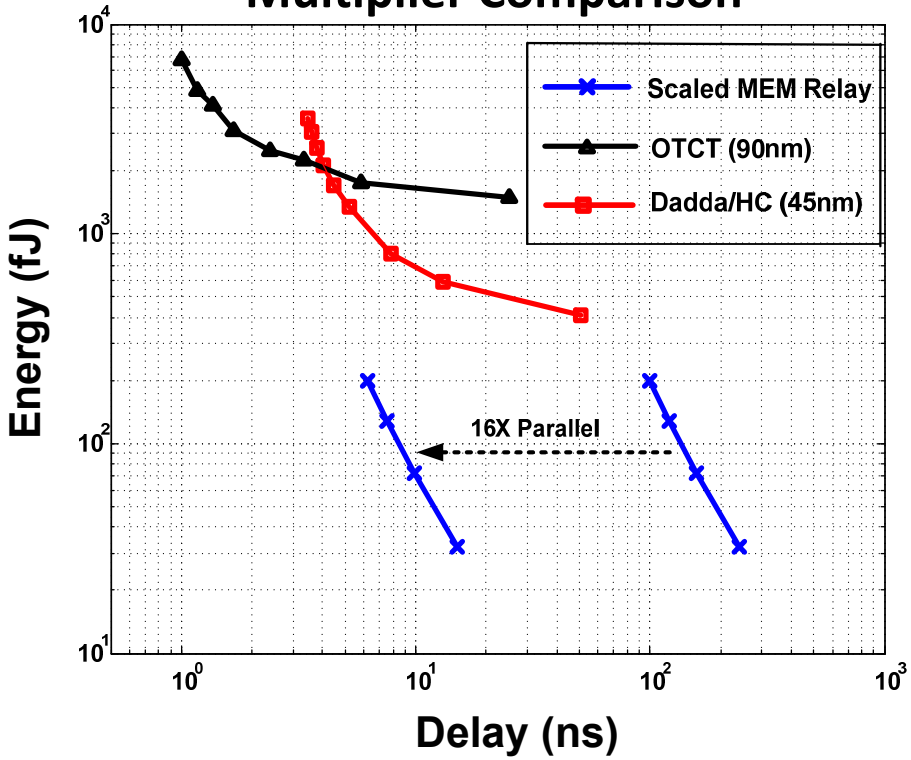
- **90nm relay *vs.* CMOS adders and multipliers:**

  >2-100× energy savings @ 3-100× higher delay

Adder Comparison

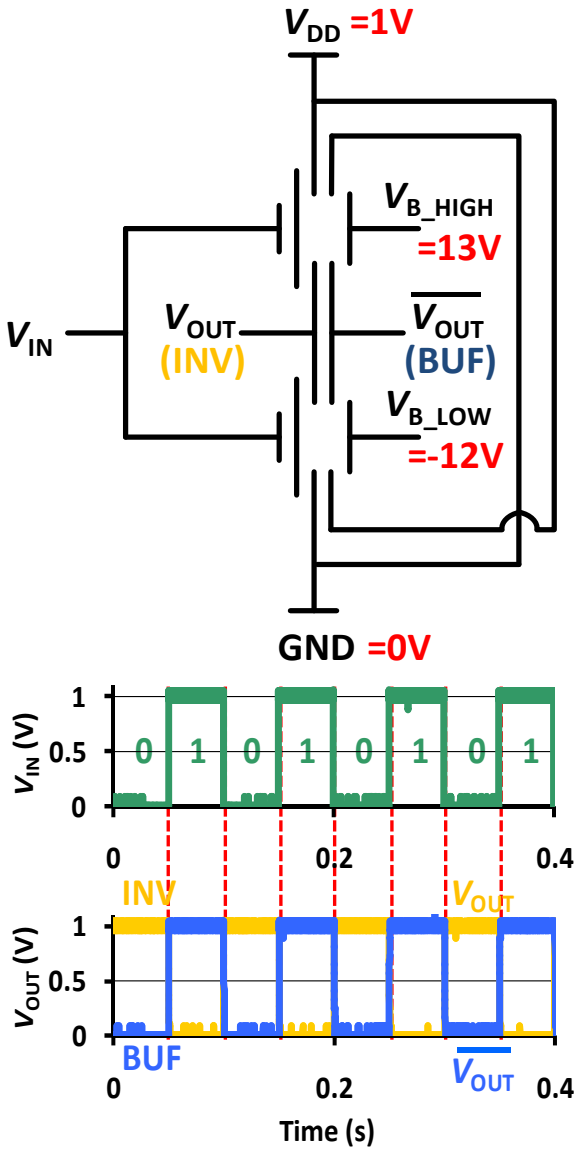


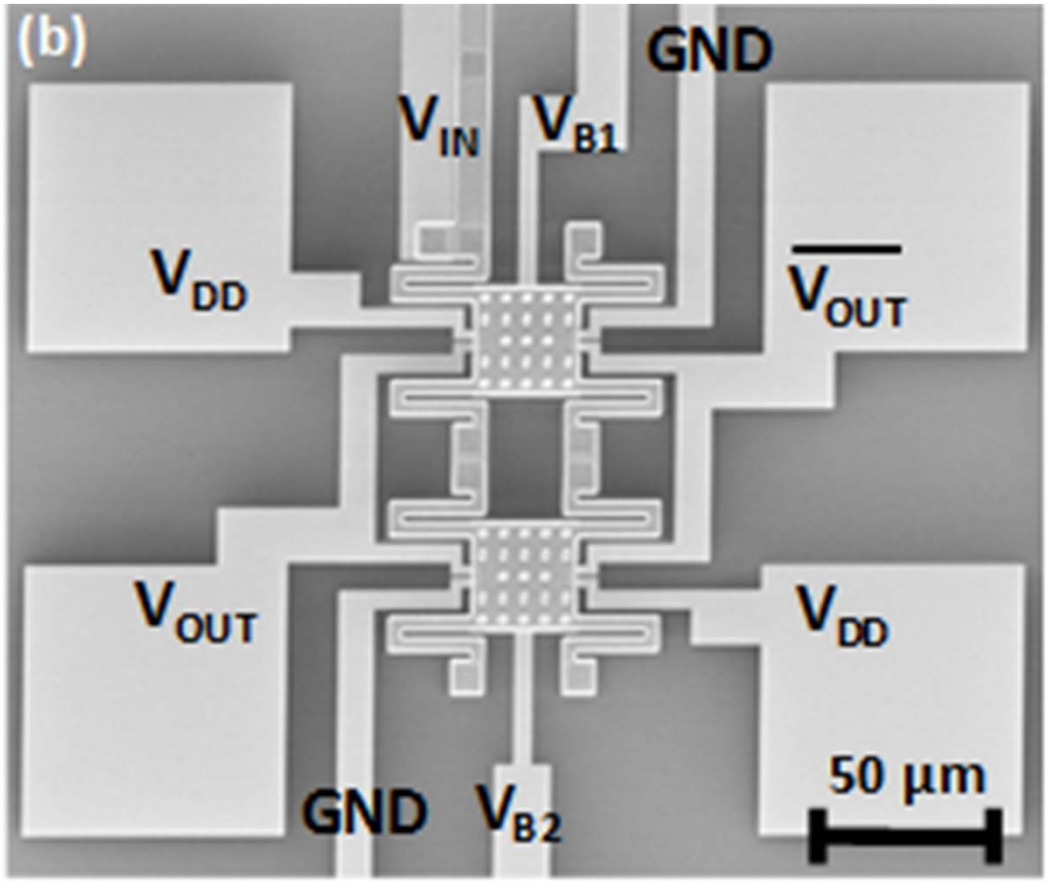
Multiplier Comparison



Single-Gate Relay Inverter/Buffer

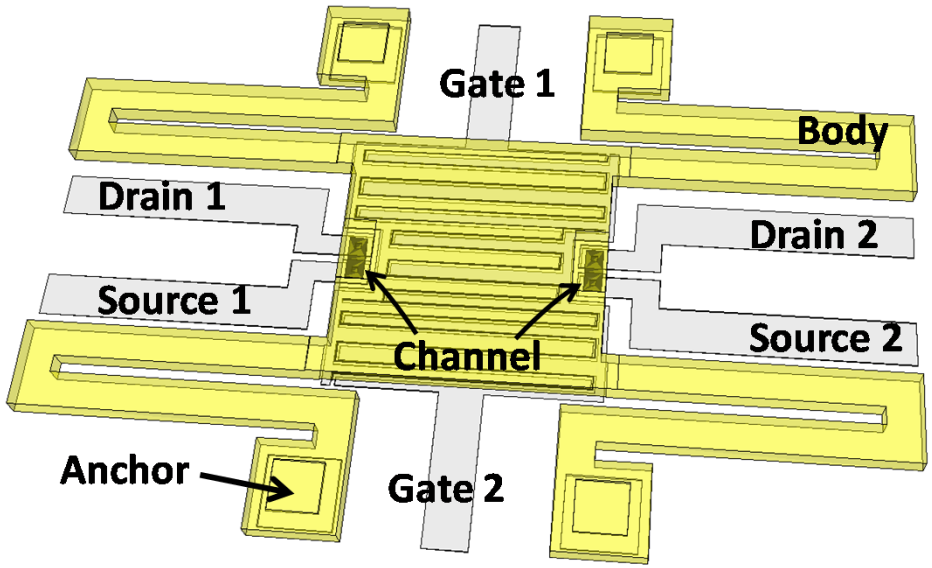
R. Nathanael *et al.*, *VLSI-TSA* 2012



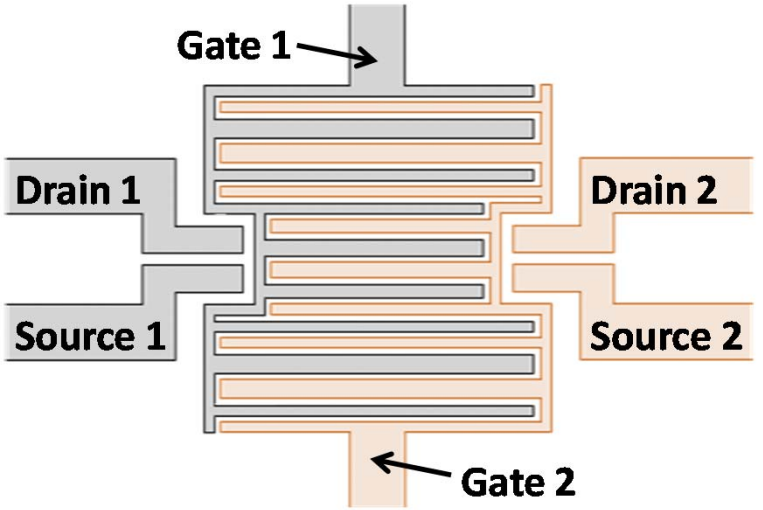


Dual-Gate, Dual Source/Drain Relay

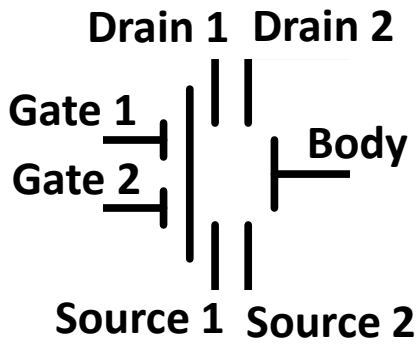
R. Nathanael *et al.*, *VLSI-TSA* 2012



Bottom (Gate) Electrode Layout



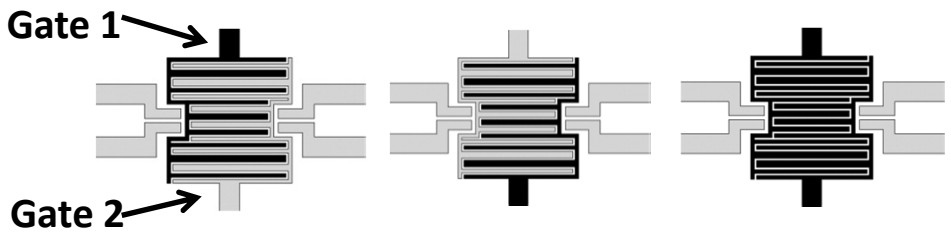
Circuit Symbol

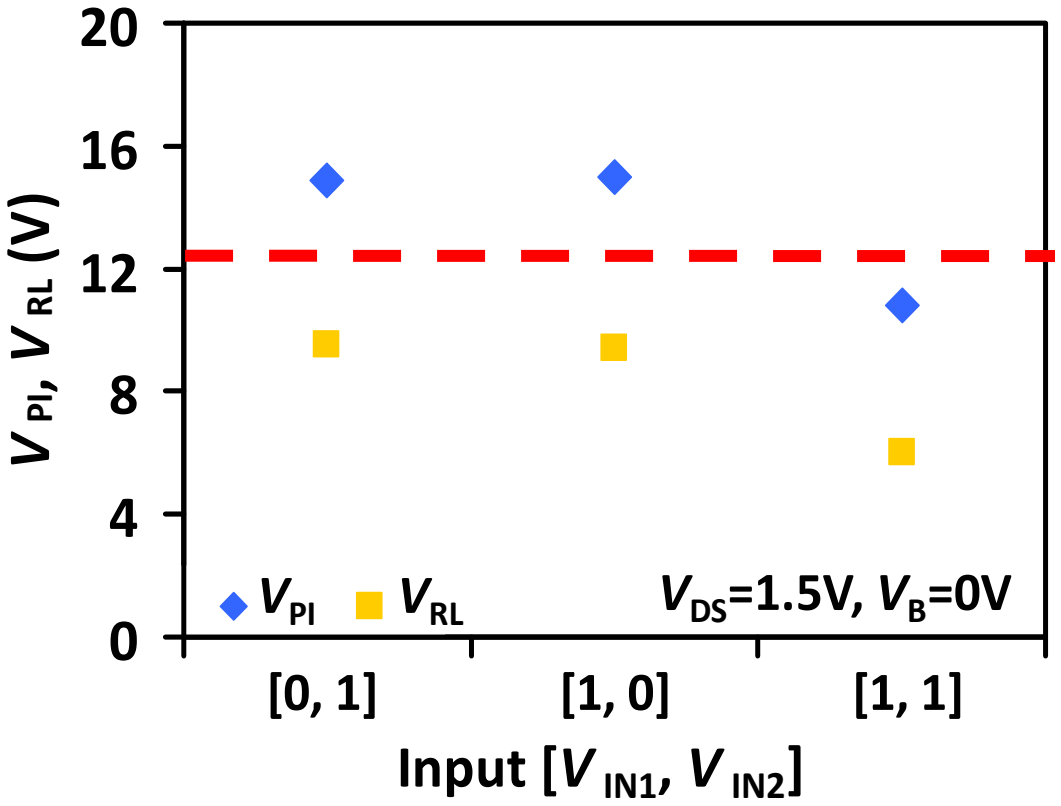


- **Gate electrodes are interdigitated to ensure that each gate has equal influence on the movable body**

Measured V_{PI} & V_{RL} of Dual-Gate Relay

R. Nathanael *et al.*, *VLSI-TSA* 2012

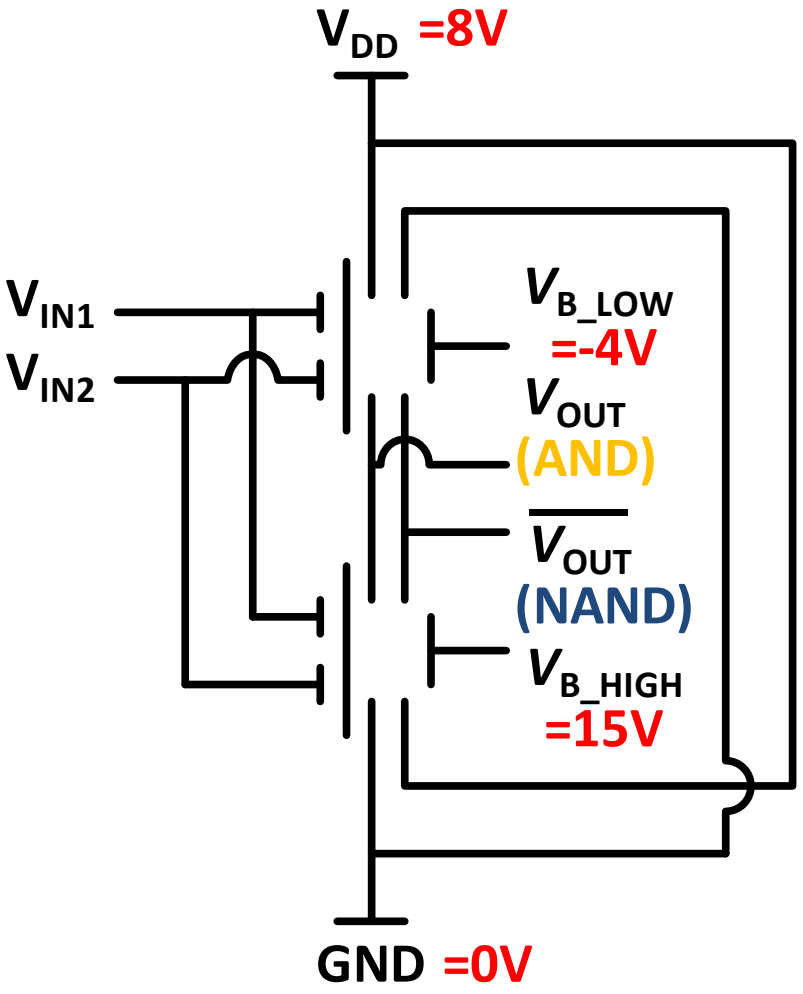


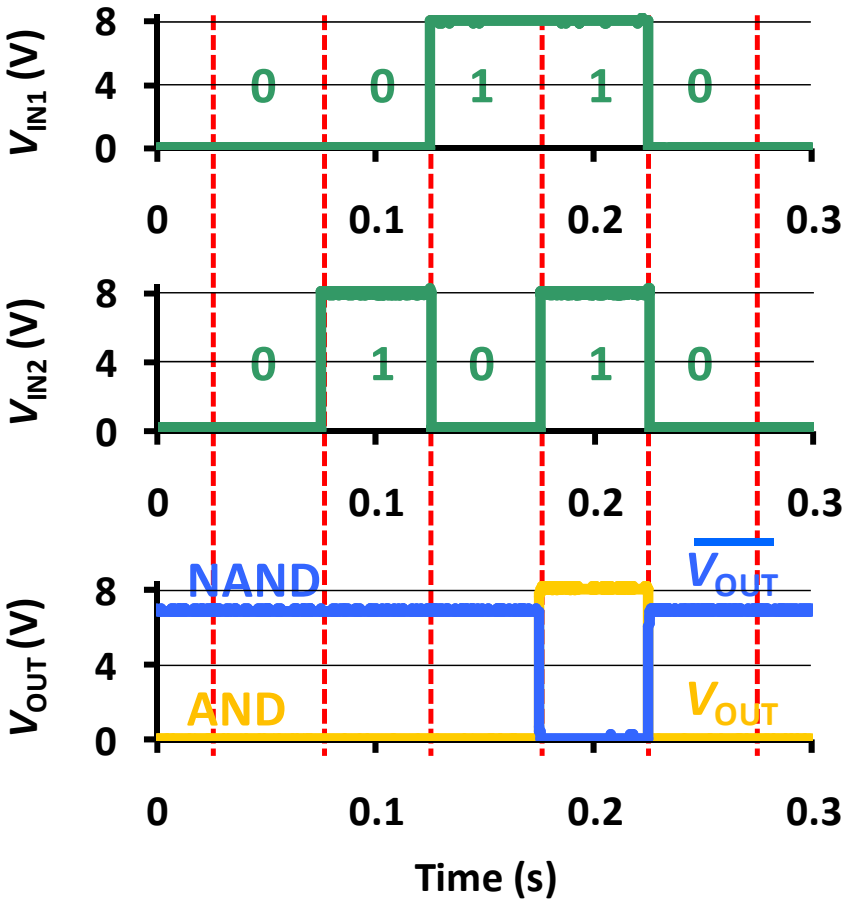


- "1"≡V_G
- Each gate has equal influence
- Depending on V_B, relay can be actuated using one or two gate electrodes

Dual-Gate Relay Circuit: AND/NAND

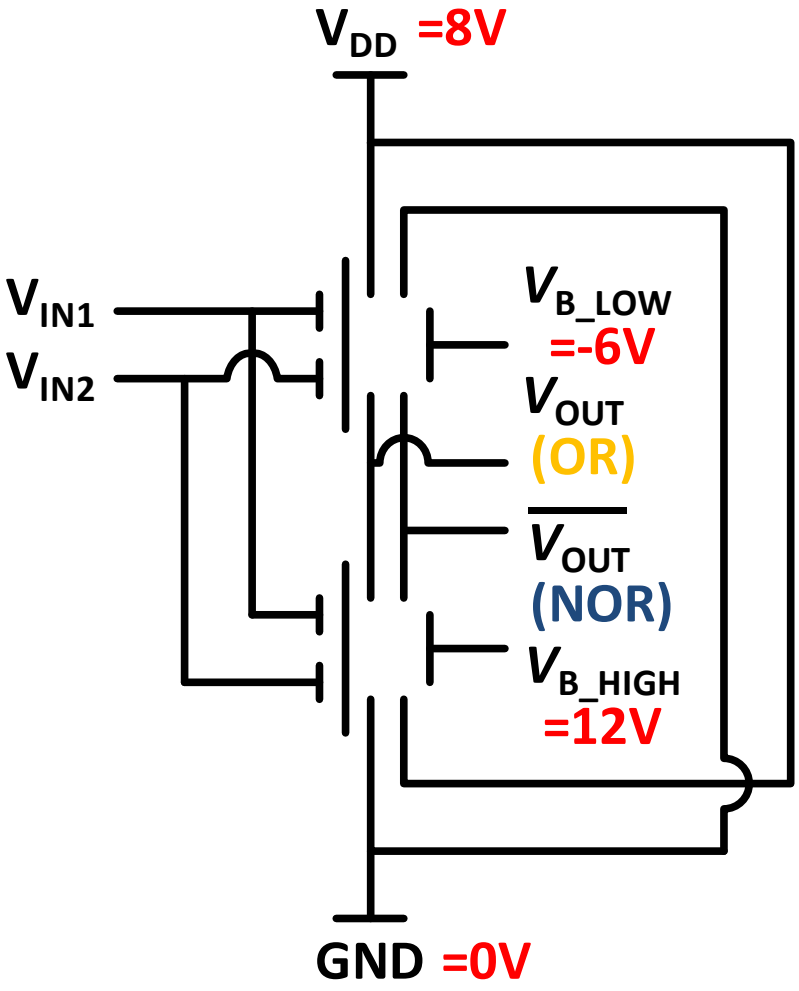
R. Nathanael *et al.*, *VLSI-TSA* 2012

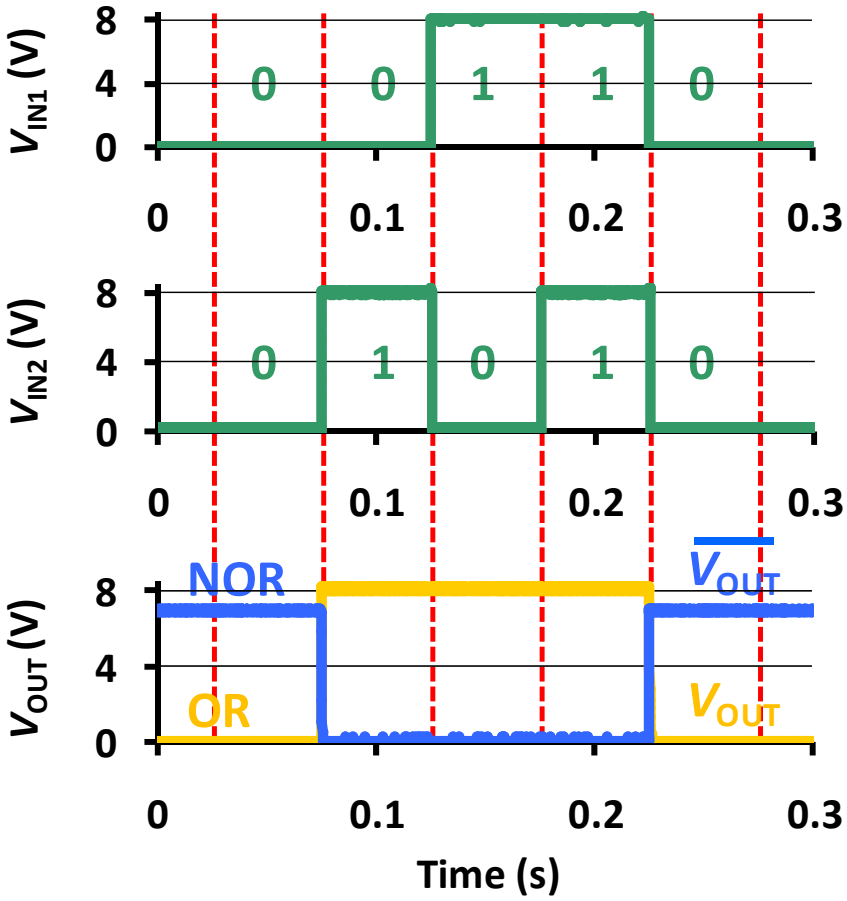




Dual-Gate Relay Circuit: OR/NOR

R. Nathanael *et al.*, *VLSI-TSA* 2012



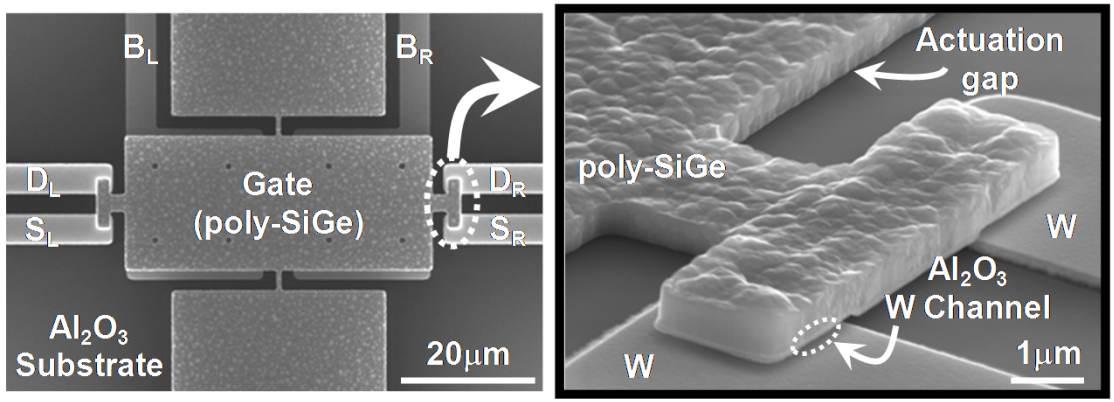


See-Saw (Active Turn-Off) Relay

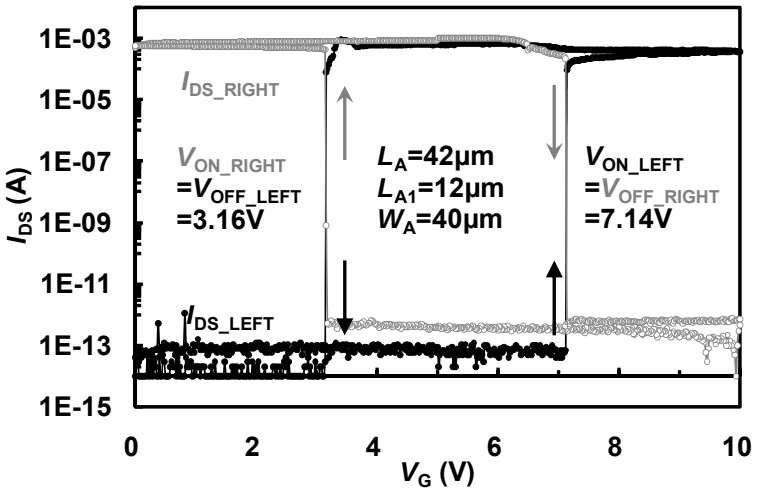
J. Jeon *et al.*, *IEEE Electron Device Letters,* Vol. 31, No. 4, pp. 371-373, 2010

- **Perfectly complementary switching , symmetric about $V_{DD}/2$**

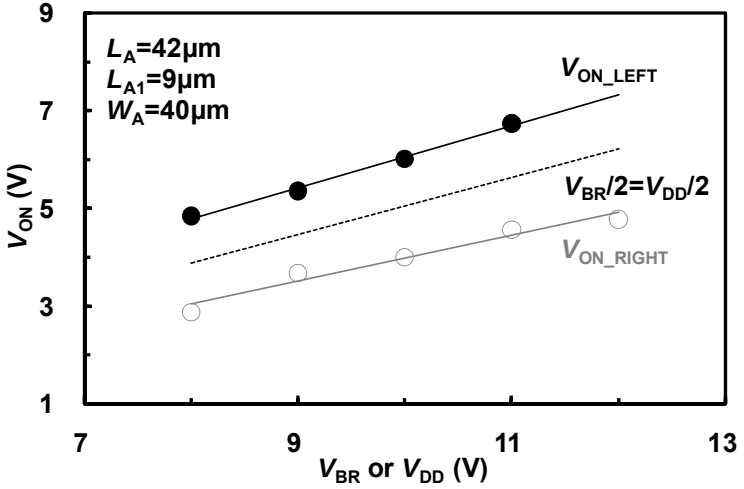
Scanning Electron Micrographs:



I_D-V_G characteristics



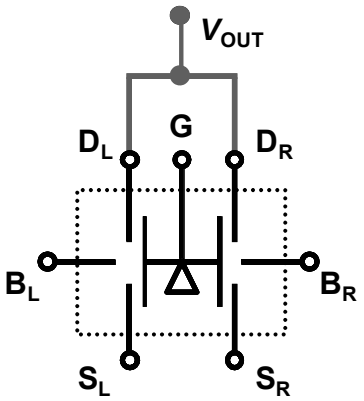
Switching Voltages *vs.* V_{DD}



See-Saw Relay Logic Gates

J. Jeon *et al., IEEE/ASME Journal of MicroElectroMechanical Systems*, Vol. 19, No. 4, pp. 1012-1014, 2010

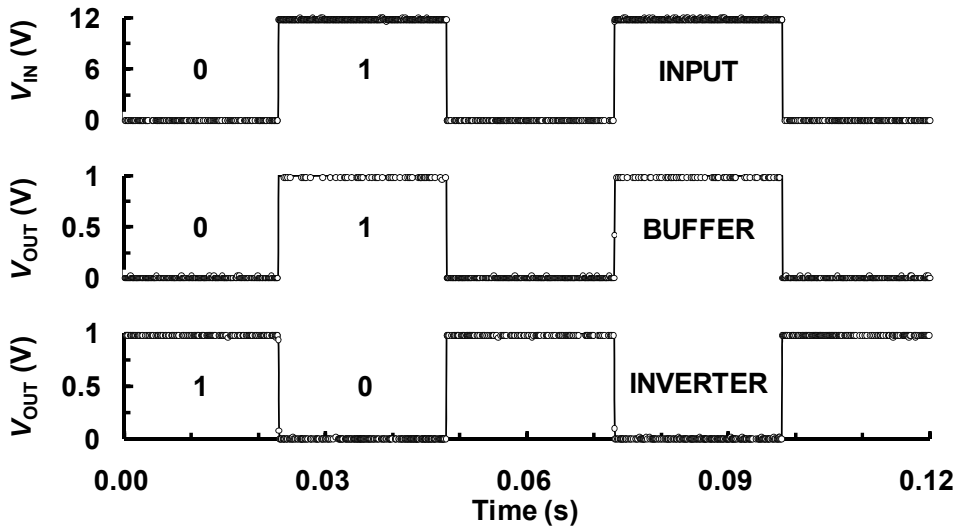
Circuit Symbol



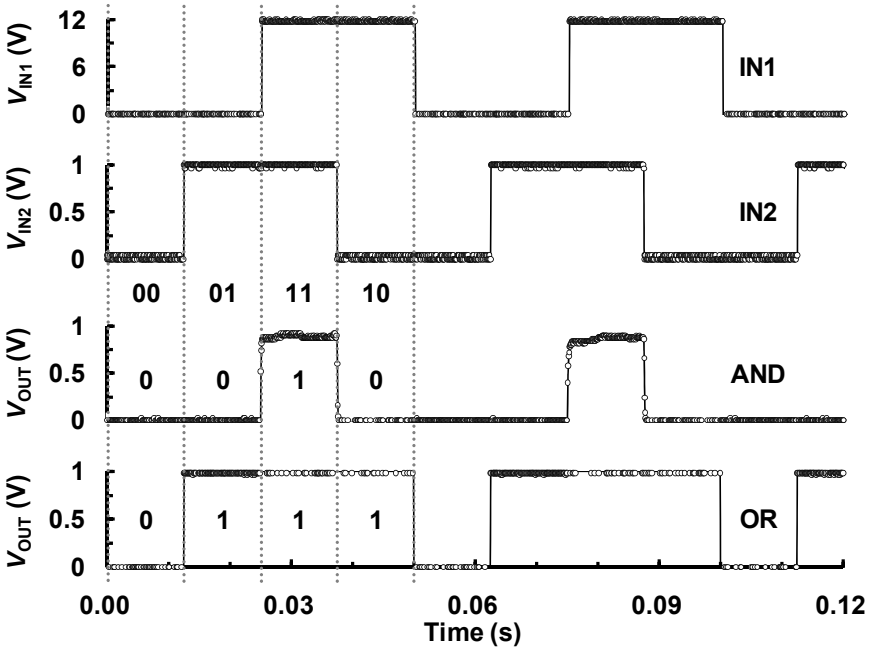
Relay Configurations

Function	V_G	V_{BL}	V_{SL}	V_{BR}	V_{SR}
BUFFER	V_{IN}	LO	HI	HI	LO
INVERTER	V_{IN}	LO	LO	HI	HI
AND	V_{IN1}	LO	V_{IN2}	HI	LO
OR	V_{IN1}	LO	HI	HI	V_{IN2}

Demonstrated Single-Input Operations



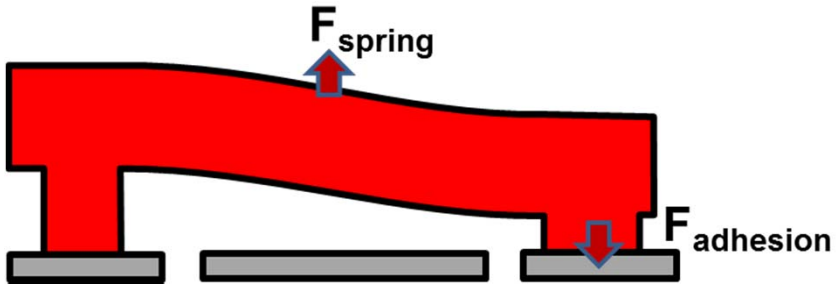
Demonstrated Dual-Input Operations



Stiction: Relay Scaling Limiter (?)

In order for a conventional electrostatic switch to turn off properly,

$F_{spring} > F_{adhesion}$



$$F_{adhesion} = \frac{H_c}{6\pi g^3} A_c$$

H_c = Hamaker constant [zJ]

g = separation between contacting surfaces [nm]

A_c = real contact area [nm^2]

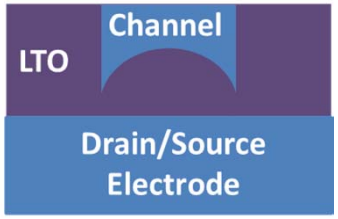
To turn on the relay: electrostatic force $F_{elec} > F_{spring} > F_{adhesion}$

→ Limits scaling of actuation area *A* and/or V_{PI}

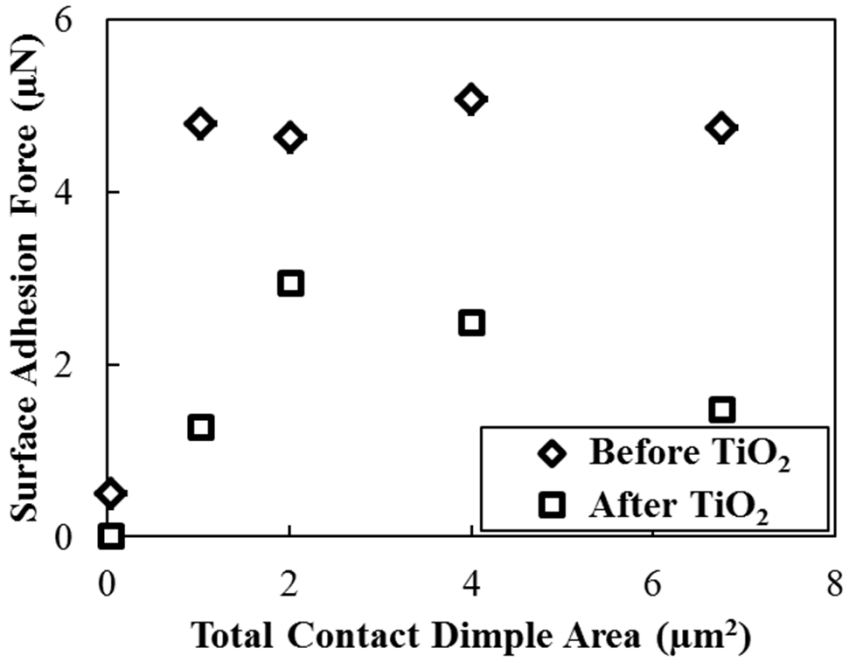
Contact Adhesive Force Scaling

J. Yaung *et al.*, *IEEE/ASME Journal of Microelectromechanical Systems*, Vol. 23, pp. 198-203, 2014

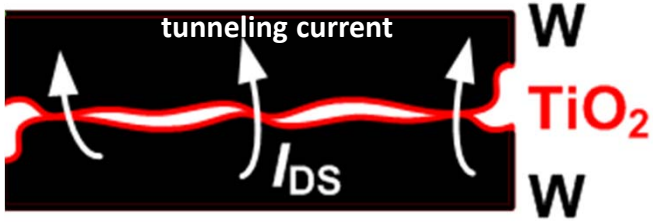
Schematic cross-section of contact dimple:



- **Model indicates that adhesion is due to van der Waals force**
  - **F_A should scale with area, 0.02 nN/nm² for W-W contact**



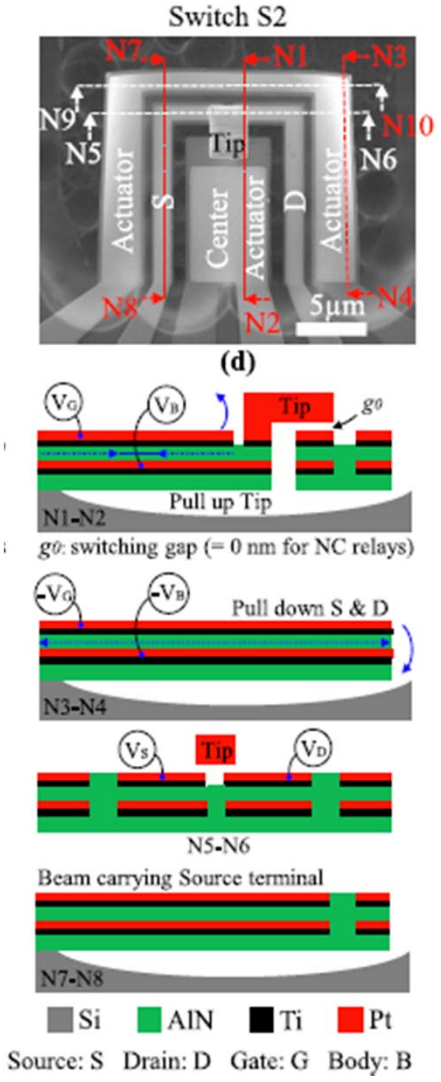
- **Adhesive force is lowered by TiO_2 coating**



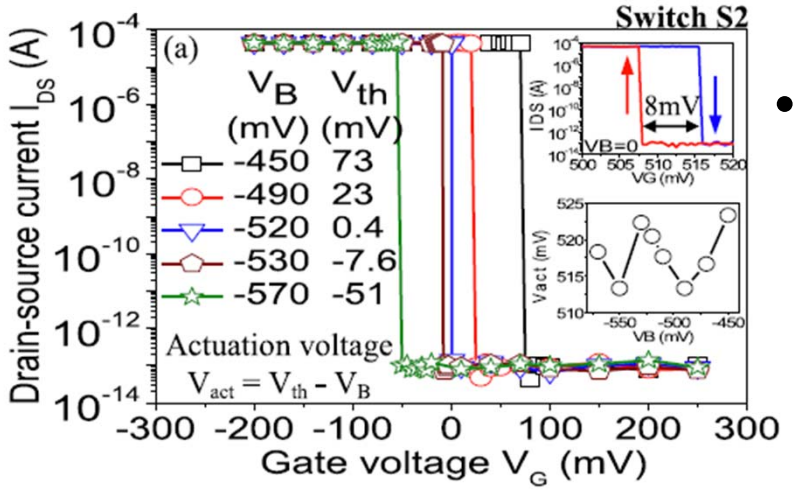
10 mV Micromechanical Switch Operation

U. Zaghloul *et al.*, *IEEE Electron Device Letters* Vol. 35, pp. 669-671, June 2014

4-T piezoelectric relay

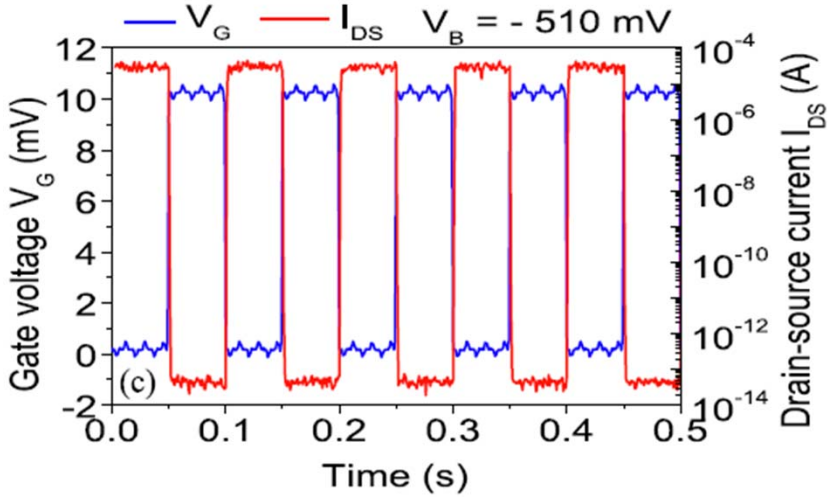


I-V Characteristics



- **Small hysteresis is indicative of low surface adhesion**

Input/Output Waveforms



- **~23 aJ projected switching energy for 5 mV operation**

Non-Volatile Memory Technologies

ITRS (Table ERD3), 2011 Edition

		Baseline Technologies		Prototypical technologies		
		Flash				
		NOR Embedded	NAND Stand-alone	FeRAM	STT-MRAM	PCM
Storage Mechanism		Charge trapped in floating gate or in gate insulator		Remnant polarization on a ferroelectric capacitor	Magnetization of ferromagnetic layer	Reversibly changing amorphous and crystalline phases
Cell Elements		1T		1T1C	1(2)T1R	1T(D)1R
Feature size F, nm	**2011**	90	22	180	65	45
	2024	25	8	65	16	8
Cell Area	**2011**	10 F^2	4 F^2	22F^2	20F^2	4F^2
	2024	10 F^2	4 F^2	12F^2	8F^2	4F^2
Read Time	**2011**	15 ns	0.1ms	40 ns	35 ns	12 ns
	2024	8 ns	0.1ms	<20 ns	<10 ns	< 10 ns
W/E Time	**2011**	1µs/10ms	1/0.1 ms	65 ns	35 ns	100 ns
	2024	1µs/10ms	1/0.1 ms	<10 ns	<1 ns	<50 ns
Retention Time	**2011**	10 y	10 y	10 y	>10 y	>10 y
	2024	10 y	10 y	10 y	>10 y	>10 y
Write Cycles	**2011**	1E5	1E4	1E14	>1E12	1E9
	2024	1E5	5E3	>1E15	>1E15	1E9
Write Operating Voltage (V)	**2011**	10	15	1.3-3.3	1.8	3
	2024	9	15	0.7–1.5	<1	<3
Read Operating Voltage (V)	**2011**	1.8	1.8	1.3–3.3	1.8	1.2
	2024	1	1	0.7–1.5	<1	<1
Write Energy (J/bit)	**2011**	1E-10	>2E-16	3E-14	2.5E-12	6E-12
	2024	1E-11	>2E-17	7E-15	1.5E-13	~1E-15

In contrast to logic switches, NVM devices can have:

- **Long write/erase times (>1 us)**
- **Modest endurance (< 10^6 cycles)**
- **Large operating voltages (>1 V)**

Outline

- Introduction
- Nanomechanical switches for computing
- **Nanomechanical memory**
  - Early designs
  - Recent design for cross-point array architecture
- Summary

First MEMS NVM Cell

B. Halg, *IEEE Trans. Electron Devices*, Vol. 37, pp. 2230-2236, 1990

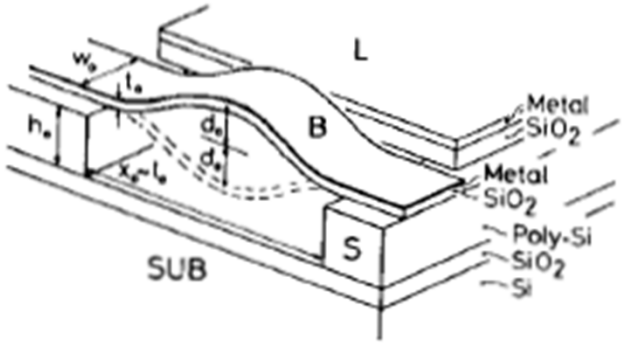


Fig. 1. Schematic drawing of a micro-electro-mechanical nonvolatile memory cell based on a bistable bridge (*B*) on a spacer (*S*) on the substrate (*SUB*) with lateral electrodes (*L*). The materials used are indicated, and the symbols for the dimensions are defined.

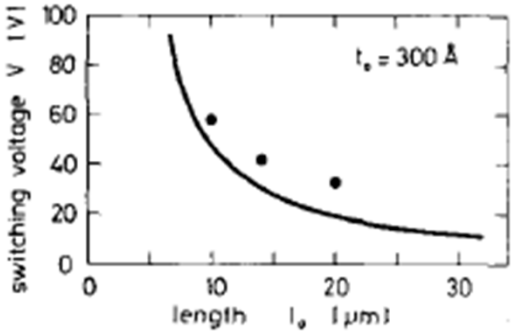


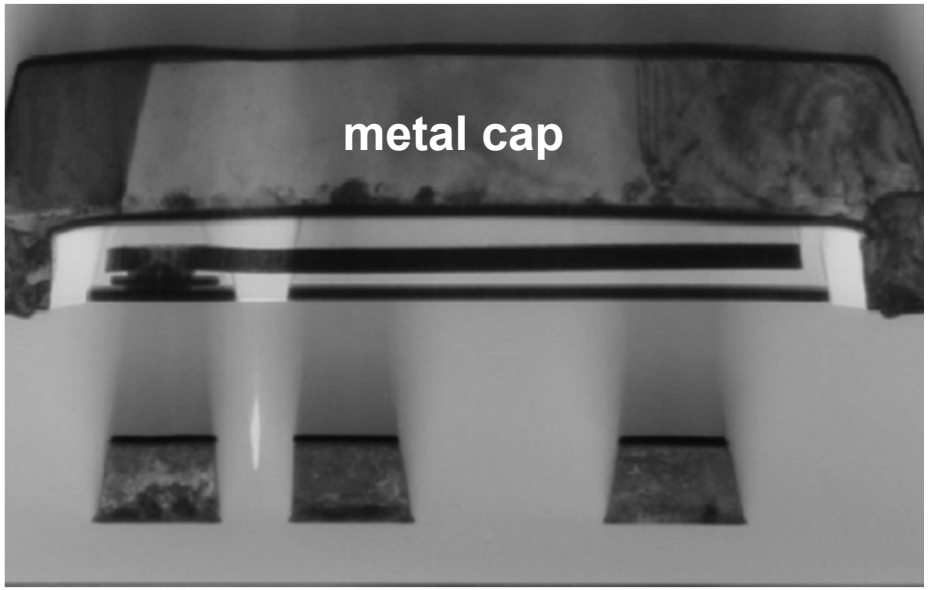
Fig. 6. Experimentally observed and calculated switching voltages V as a function of the length l_0 of a 300-Å-thick bridge.

- **Bistable buckled beam**
  - Switched with electrostatic force
  - Immune to radiation, shock
- **Too large (>100um^2) for reasonable storage capacities…**

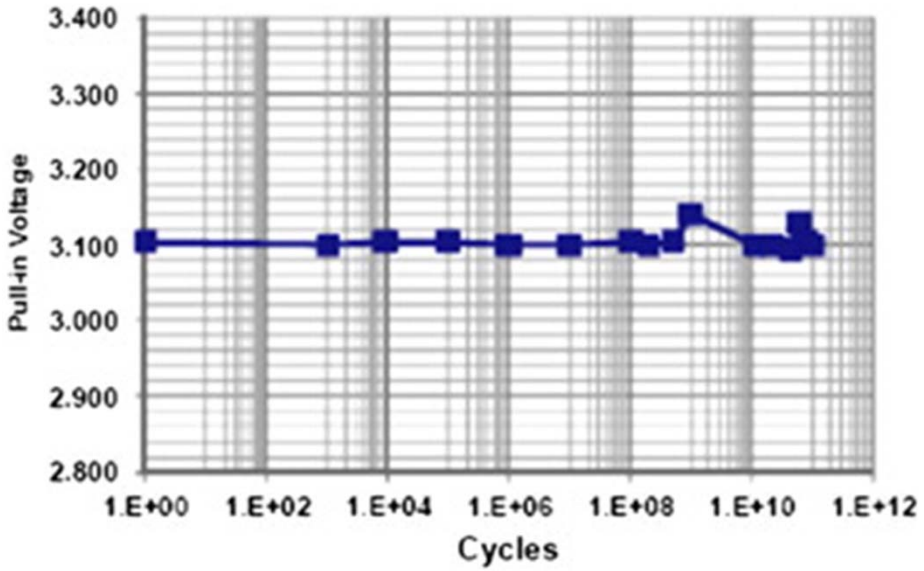
Nanomech™ Technology

R. Gaddi *et al*. (Cavendish Kinetics), *Microelectronics Reliability* Vol. 50, pp. 1593-1598, 2010

TEM cross-section



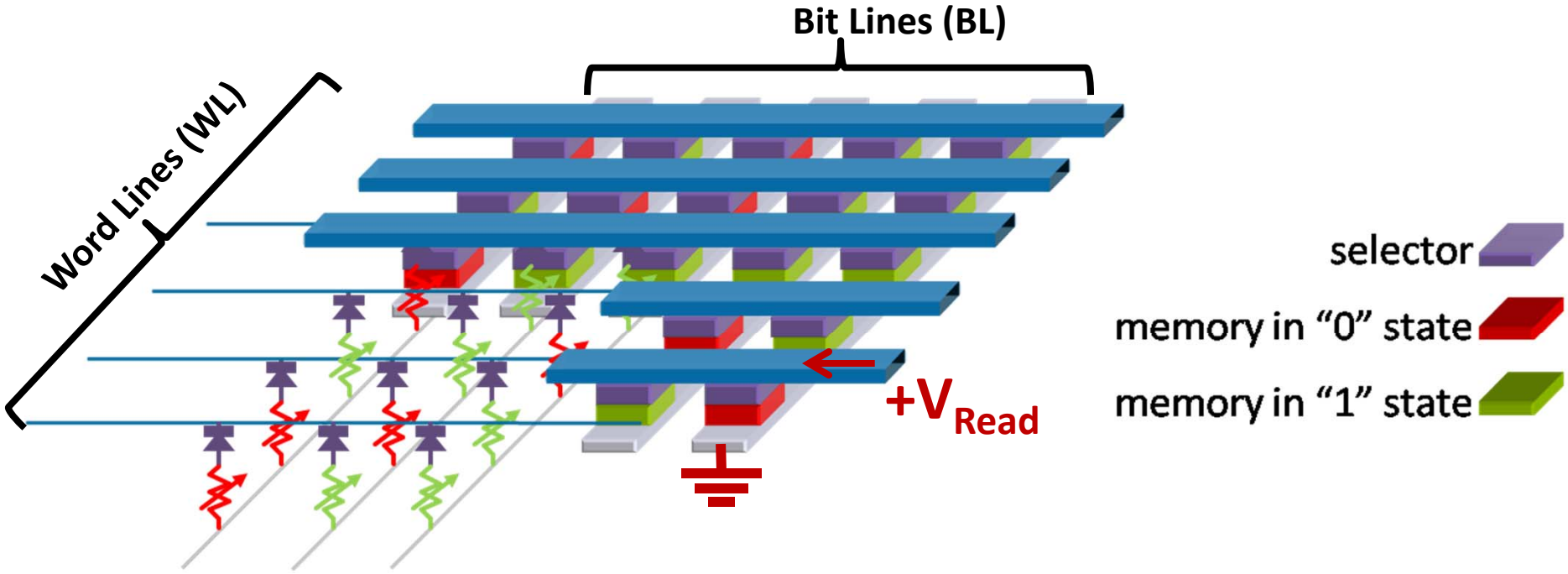
Endurance test results



- **The beam can be pulled out of contact by biasing the cap.**
- **A select device (*e.g.* a transistor) is needed for each MEM switch in the memory array.**

Cross-Point Array Architecture

- **Most compact architecture ($4F^2$ cell size)**
- **Requires selector device at each cross-point to reduce "sneak" leakage current during a read operation**
  - *e.g.* 2-terminal diode

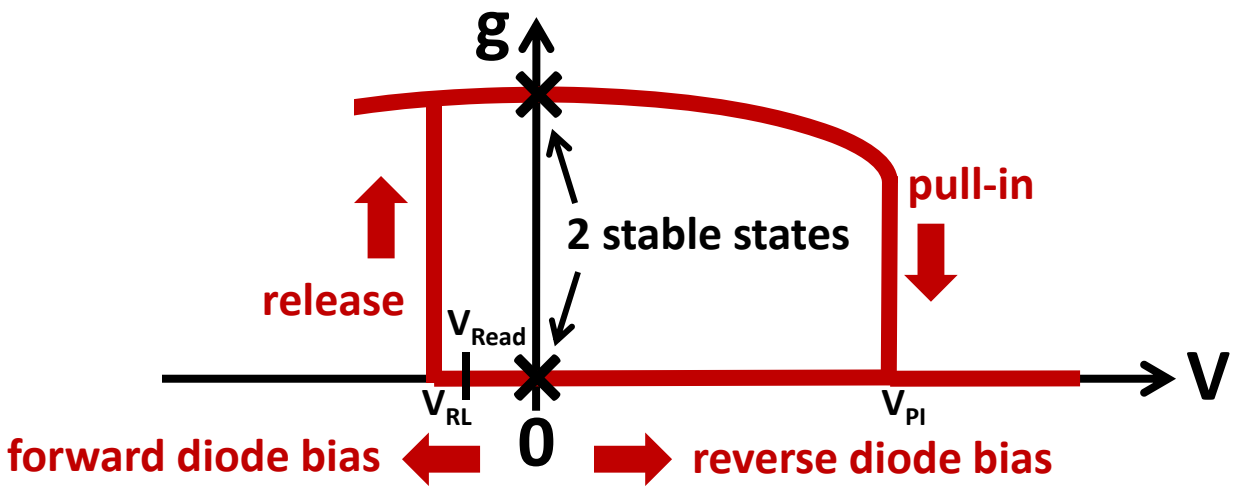


http://www.smartplanet.com/blog/thinking-tech/what-might-replace-flash-memory/943

Electro-Mechanical Diode NVM Cell

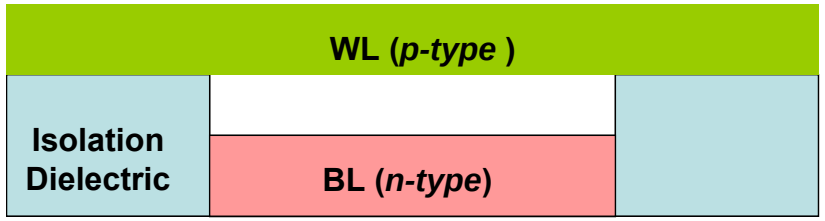
W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012

- **Achieve bi-stable operation of an electrostatic gap-closing actuator by leveraging the built-in electric field of a diode:**

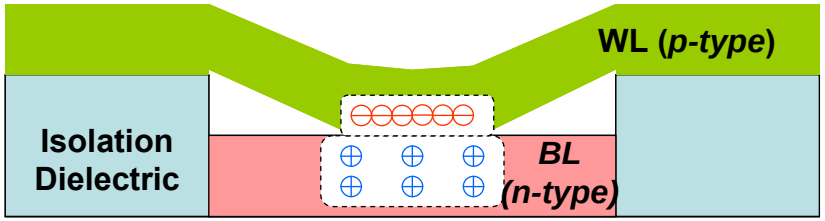


CROSS-SECTIONAL ILLUSTRATIONS

Reset State



Set State



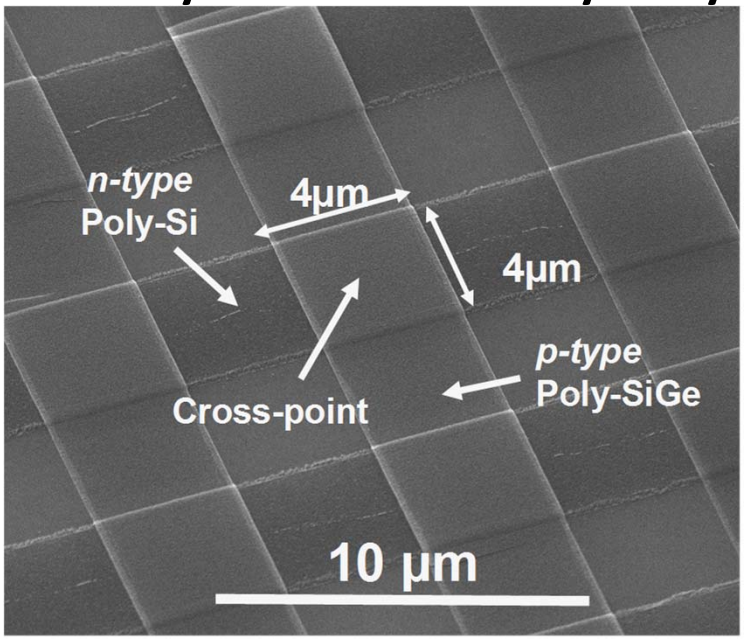
$F_{adhesion} + F_{elec} > F_{spring}$

First Prototype MEM Diode

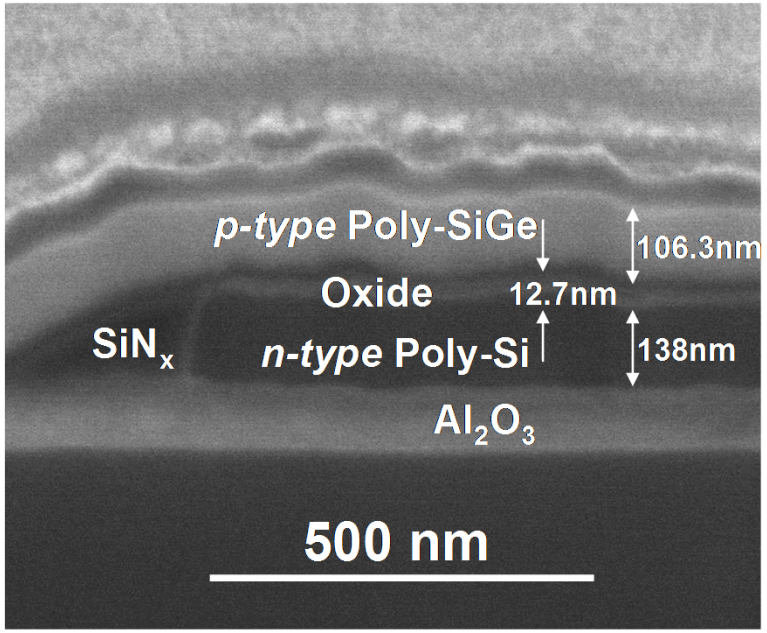
W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012

- **Cross-point arrays of MEM diodes were fabricated using conventional planar processing techniques.**
  - The WL (100-nm p-type poly-$Si_{0.4}Ge_{0.6}$) is supported by SiN_x spacers formed along the sidewalls of the BL (100 nm n-type poly-Si).
  - The air-gap (~13 nm thick) between the WL and BL is formed by selectively removing a sacrificial layer of LTO using HF vapor.

Bird's-eye view of memory array

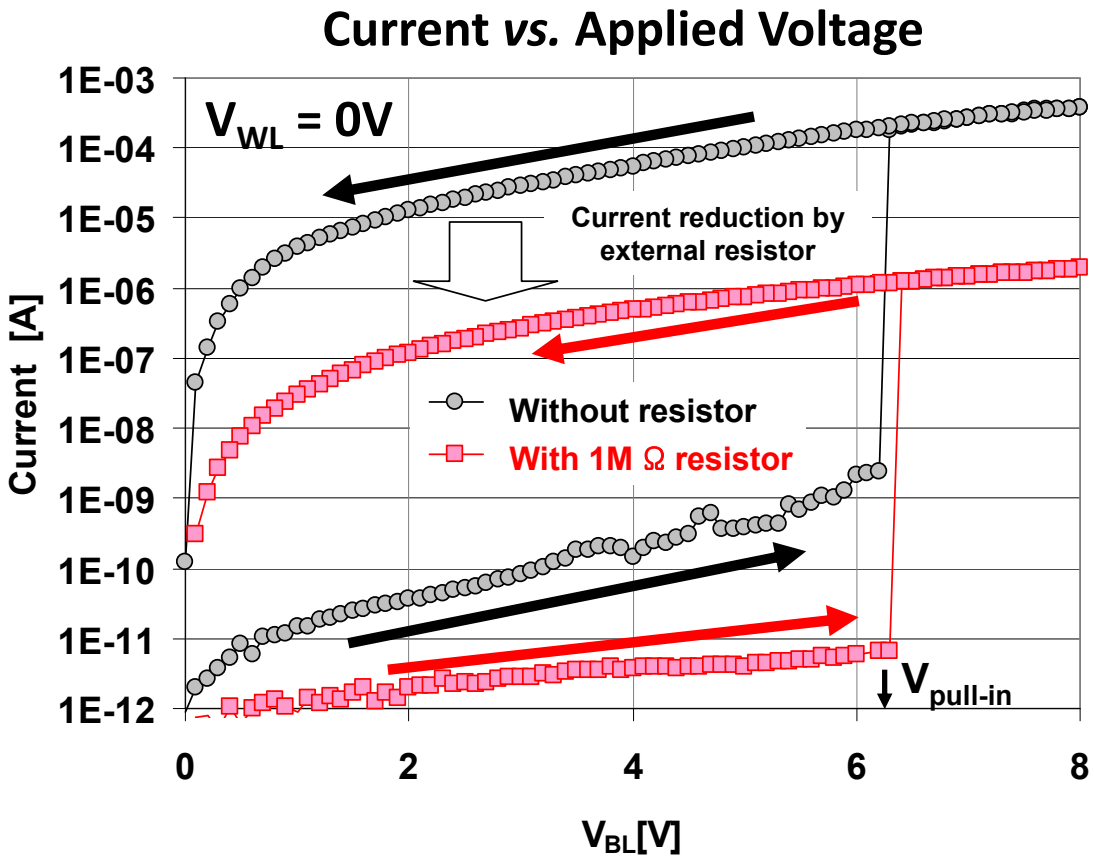


Cross-sectional view of a bit-cell



Set Operation

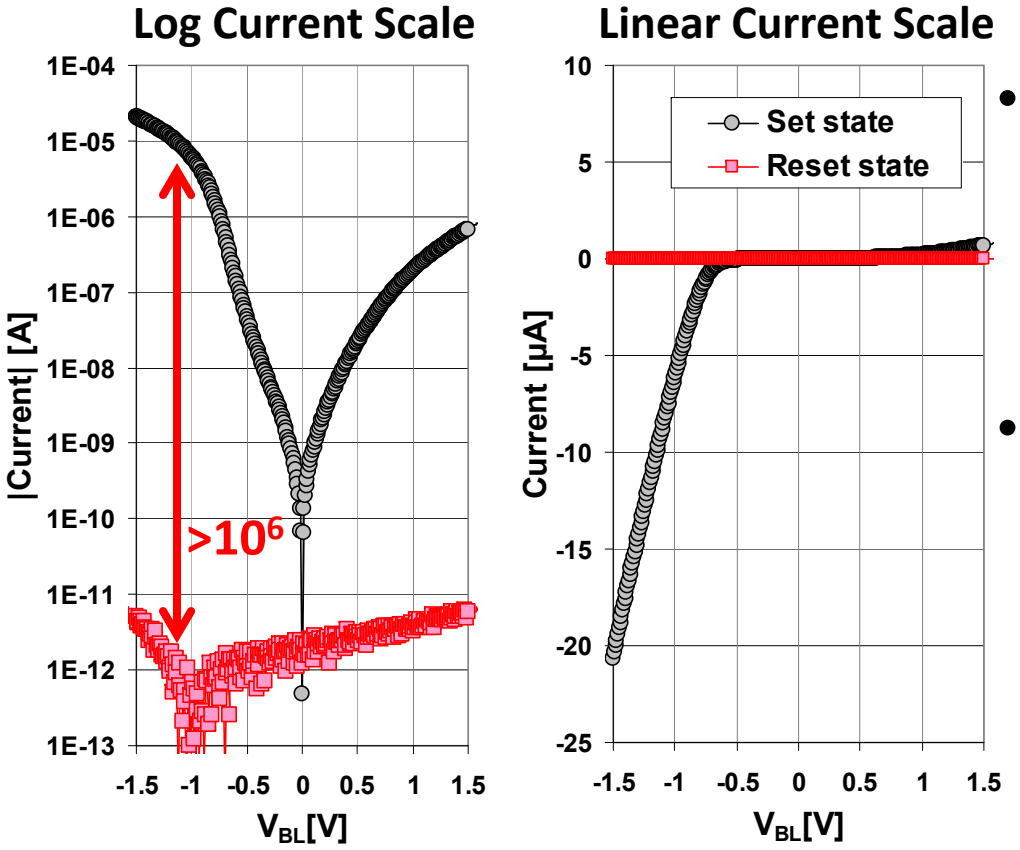
W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012



- **A sudden increase in current is seen at the voltage when the WL is pulled in to the BL.**
  - $V_{Set} \cong 6$ V, $t_{Set} \cong 2$ us
- **Since it is an applied voltage (not current) that is required to actuate the WL, the Set current can be lowered by inserting a current-limiting resistor.**

I-V Characteristics

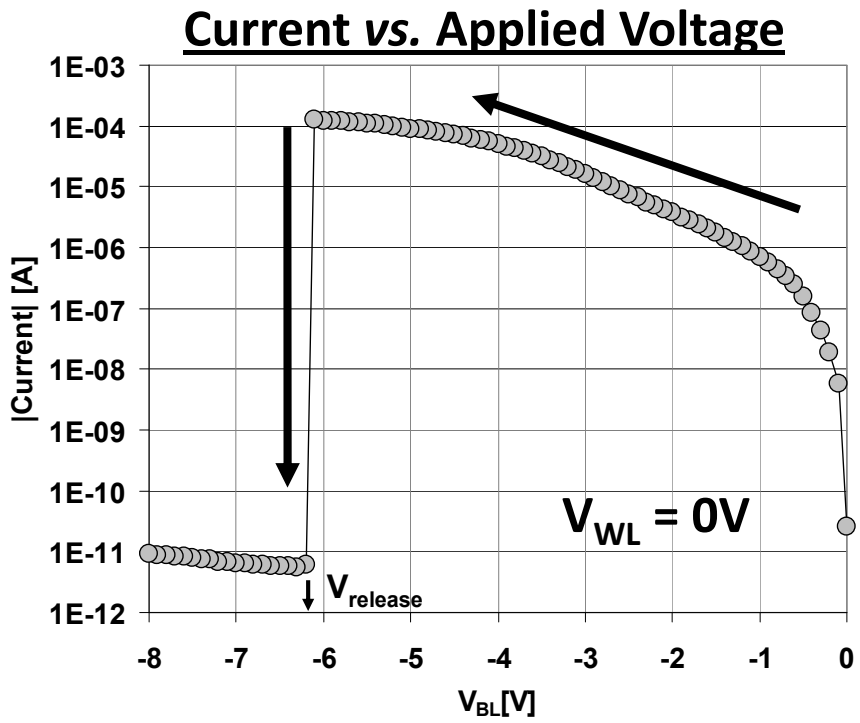
W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012



- **Set/Reset current ratio > 10^6**
  - Leakage through SiN_x spacers can be reduced with process improvements.
- **For V_{Read} = 1.2 V, the ratio of Set cell current to sneak path leakage current is ~100 for the prototype device**
  - This rectification ratio can be increased with process improvements.

Reset Operation

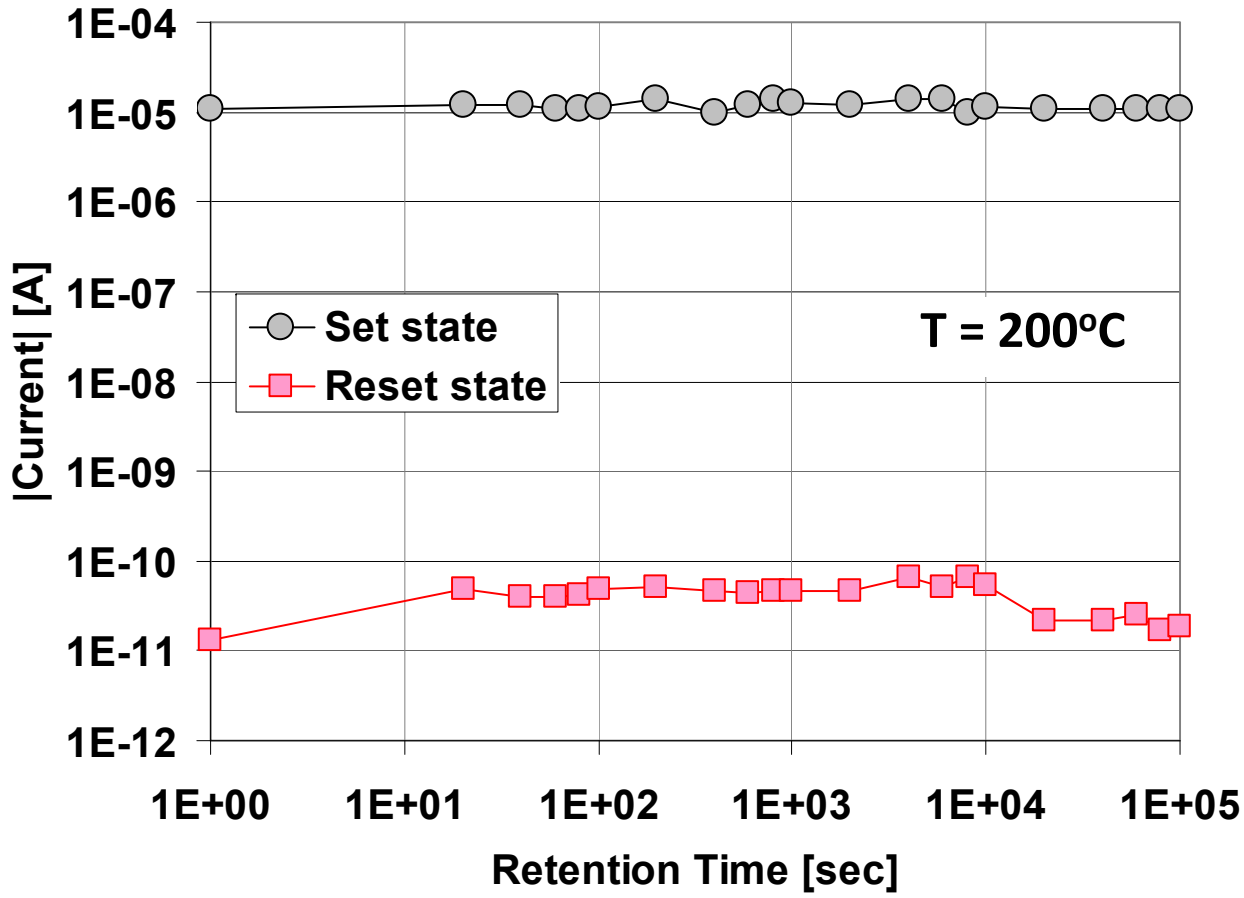
W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012



- **To Reset a memory cell, a voltage pulse is applied to counteract the built-in field of the p-n diode.**
  - forward bias → current flow
- **A sudden decrease in current is seen at the voltage when the WL comes out of contact with the BL.**
  - $V_{Reset} \cong$ -6 V, $t_{Reset} \cong$ 100 ms

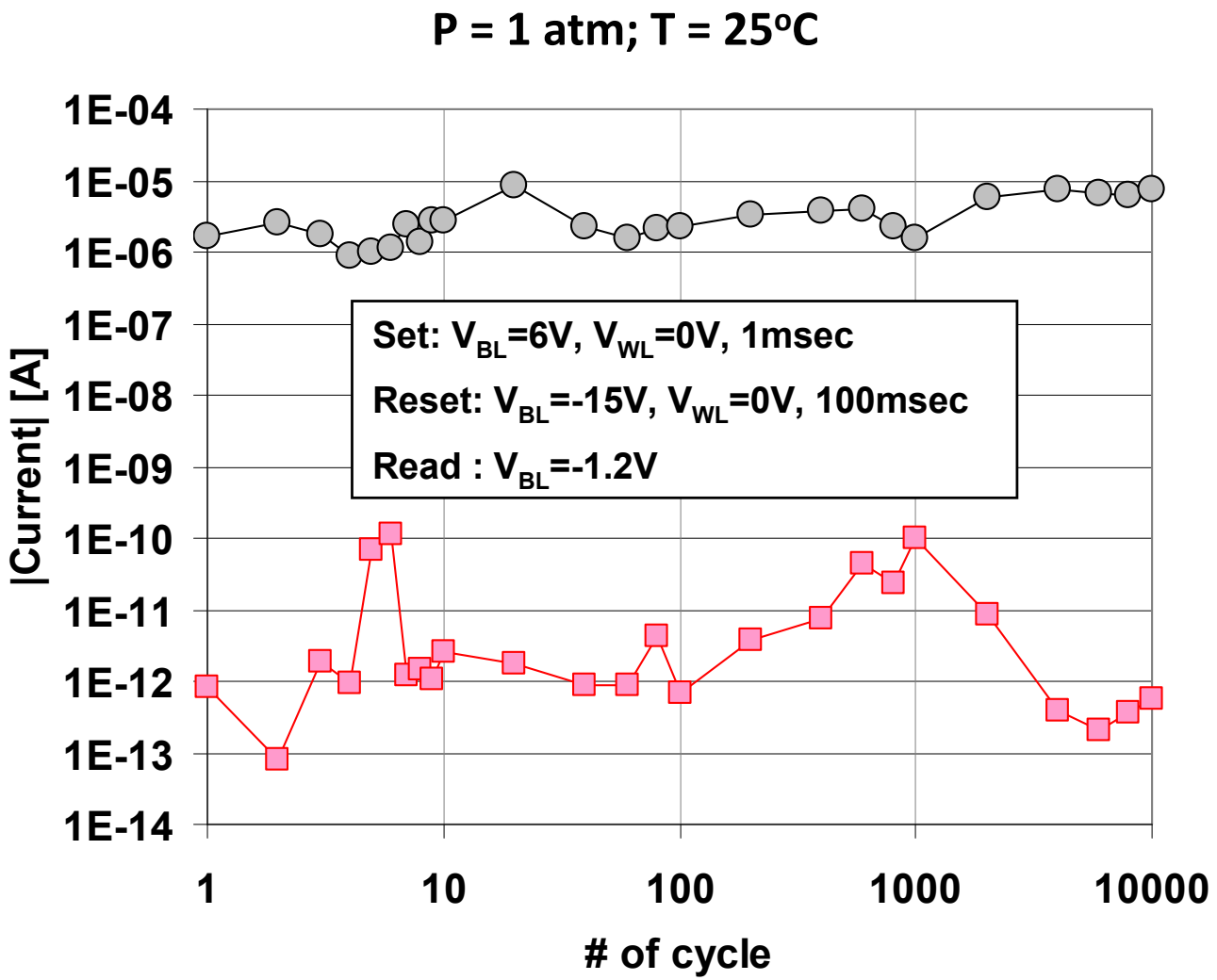
Retention Behavior

W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012



Endurance Characteristics

W. Kwon *et al*. (UC Berkeley), *IEEE Electron Device Letters*, Vol. 33, pp. 131-133, 2012



Scaled NVM Technology Comparison

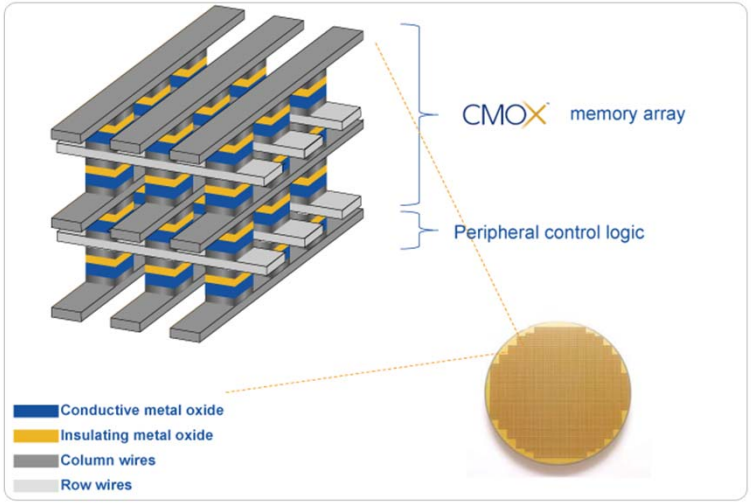
W. Kwon *et al*. (UC Berkeley), *2012 International Memory Workshop*

Technology	NAND Flash	PCM	STT-MRAM	Redox RRAM	Electro-mechanical diode
Cell Size	2.5 F^2	6 F^2	20-40 F^2	5-8 F^2	4-6 F^2
Scaling Limit	16 nm	5-10 nm	7-10 nm	5-10 nm	5 nm W x 20 nm L
Storage Mechanism	F-N Tunneling	Phase change by Joule heating	Electron spin torque transfer	Ion transport and redox reaction	Mechanical gap closing actuation
Write/Erase Voltage	18-20 V	< 3 V	< 1.8 V	< 0.5 V	< 3 V
Write time	>10 us	50-120 ns	< 100 ns	< 5 ns	< 1 ns
Endurance	10^4 - 10^5	10^{15}	10^{12}	10^{16}	$>10^{10}$
Retention	10 yrs	10 yrs	10 yrs	10 yrs	> 10 yrs @ 200 ℃
Ease of Integration	10 Masks	2-3 Masks to BEOL	3-4 Masks to BEOL	2-3 Masks to BEOL	2 Masks
Write Energy per Bit	> 1 fJ	< 2 pJ	< 4 pJ	1 fJ	< 0.1 fJ

http://www.itrs.net/Links/2010ITRS/2010Update/ToPost/ERD_ERM_2010FINALReportMemoryAssessment_ITRS.pdf

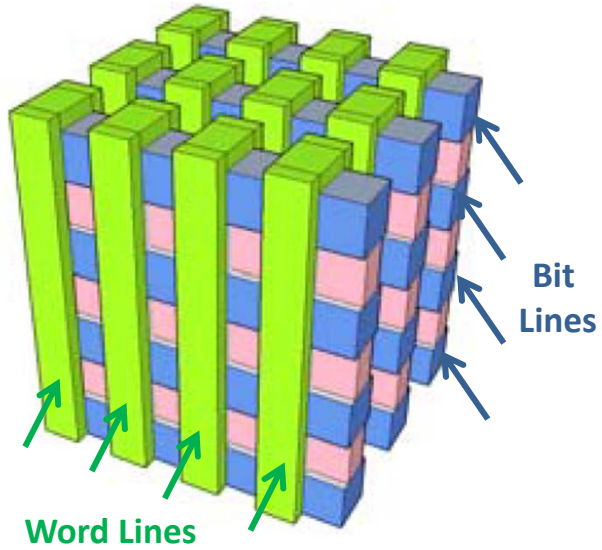
- **NEMory technology potentially offers the best performance and lowest energy consumption!**

3-D Integration



Unity Semiconductor Corp.

- **Conventional cross-point memory array technologies require 2 lithography steps per memory layer**



W. Kwon *et al*. PhD thesis, UC Berkeley

- **NEMory technology requires only 2 lithography steps to define the 3-D memory array**
  - built-in redundancy (2 WL/cell)
  - allows for longer beam length

Outline

- Introduction
- Nanomechanical switches for computing
- Nanomechanical memory
- **Summary**

Summary

- **Electronic devices which enable more energy-efficient computing and information storage, at ever lower cost per function, will be required to realize the vision of ambient intelligence.**
- **Mechanical devices show promise in this regard:**
  - ✓ **Ideal switching behavior**
  - ✓ **Simple fabrication process (lower cost)**
  - ✓ **Enhanced device functionality**
  - ✓ **Adequate reliability**

Contact adhesive forces must be well controlled in order to fully realize this promise.

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  @ UCLA: Kevin Dwan, Cheng C. Wang, Mingzhe Jiang
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