FinFET
History, Fundamentals and Future

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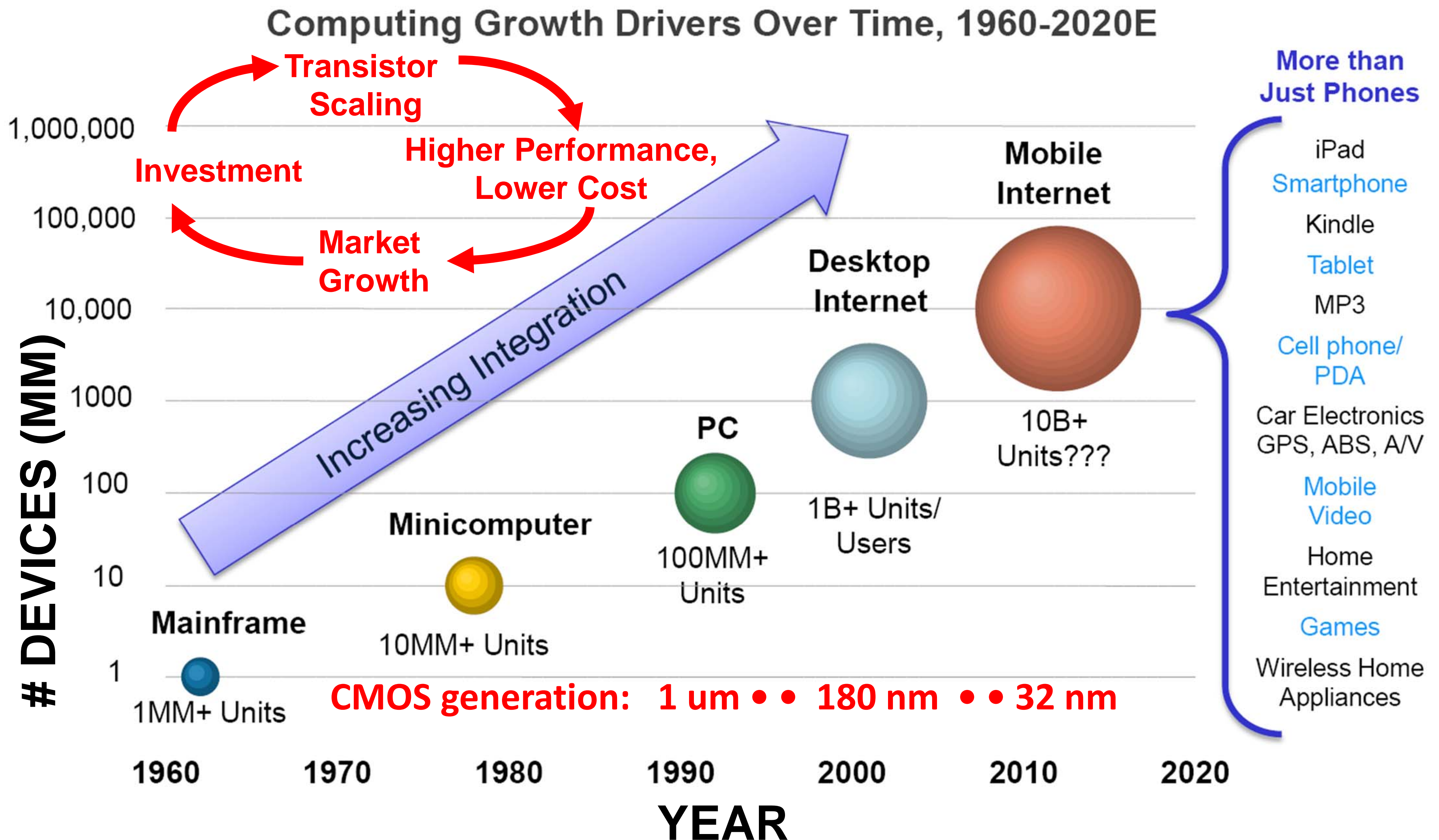
June 11, 2012

Impact of Moore's Law



Source: ITU, Mark Lipacis, Morgan Stanley Research

http://www.morganstanley.com/institutional/techresearch/pdfs/2SETUP_12142009_RI.pdf

1996: The Call from DARPA

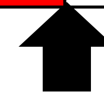
- **0.25 μm CMOS technology was state-of-the-art**
- **DARPA Advanced Microelectronics (AME) Program Broad Agency Announcement for 25 nm CMOS technology**

1998 International Technology Roadmap for Semiconductors (ITRS)

	1999	2002	2005	2008	2011	2014	2017	2020
Technology Node	180 nm	130 nm	100 nm	70 nm	50 nm	35 nm	25 nm	18 nm
Gate Oxide Thickness, T_{OX} (nm)	1.9-2.5	1.5-1.9	1.0-1.5	0.8-1.2	0.6-0.8	0.5-0.6		
Drive Current, I_{DSAT}								

Solutions being pursued

No known solutions

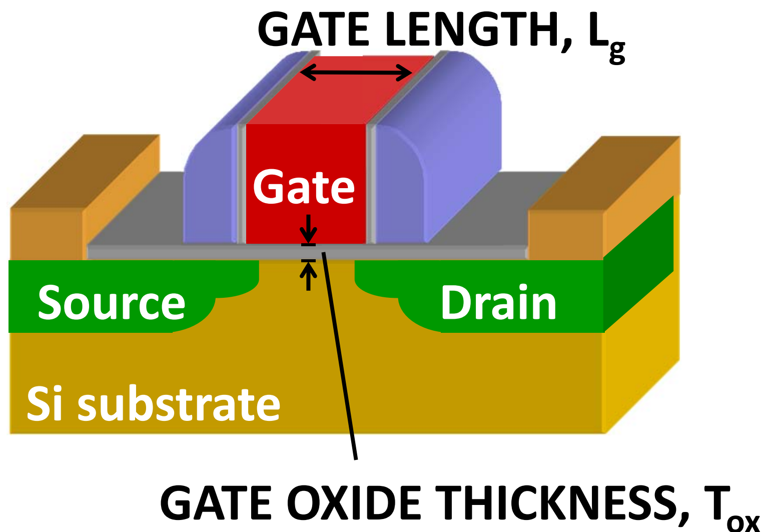


End of Roadmap

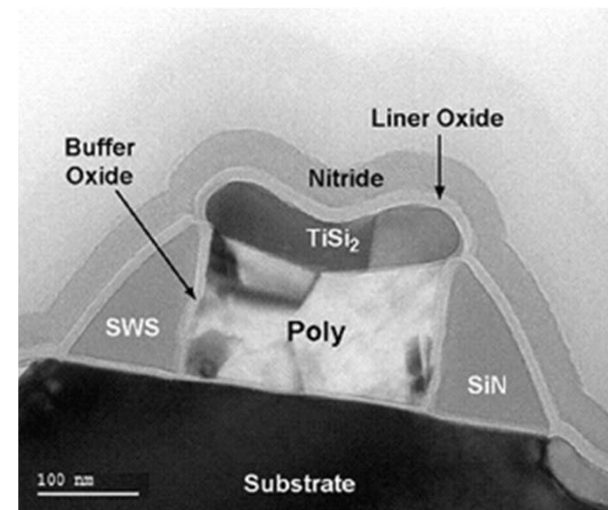
→ **UC-Berkeley project "Novel Fabrication, Device Structures, and Physics of 25 nm FETs for Terabit-Scale Electronics"**
- **June 1997 through July 2001**

MOSFET Fundamentals

<u>M</u>etal <u>O</u>xide <u>S</u>emiconductor <u>F</u>ield-<u>E</u>ffect <u>T</u>ransistor:



0.25 micron MOSFET XTEM

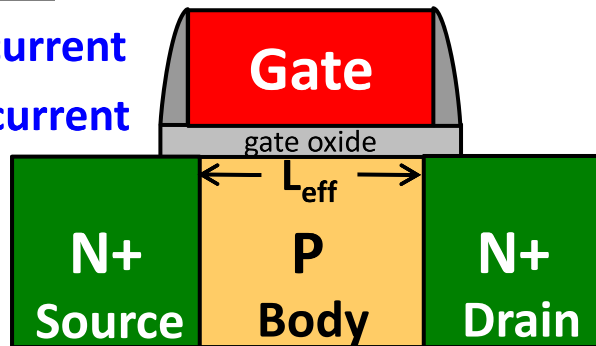


http://www.eetimes.com/design/automotive-design/4003940/LCD-driver-highly-integrated

MOSFET Operation: Gate Control

Desired characteristics:
- High ON current
- Low OFF current

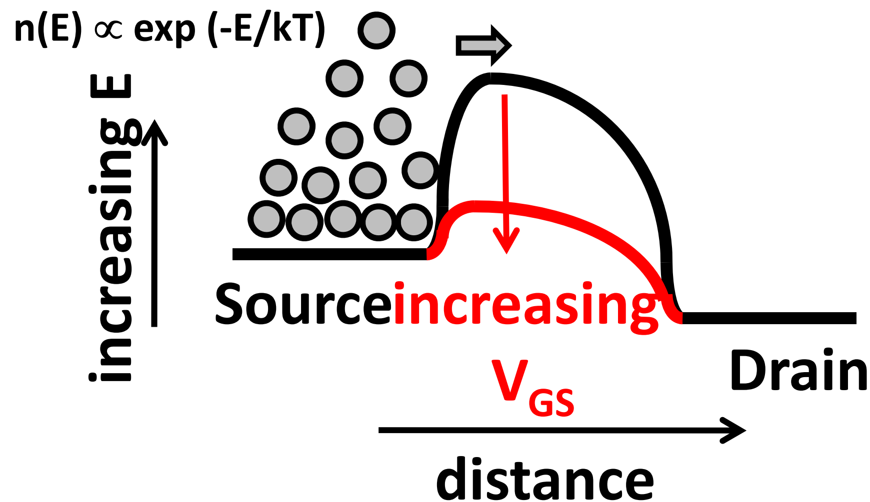
N-channel MOSFET cross-section

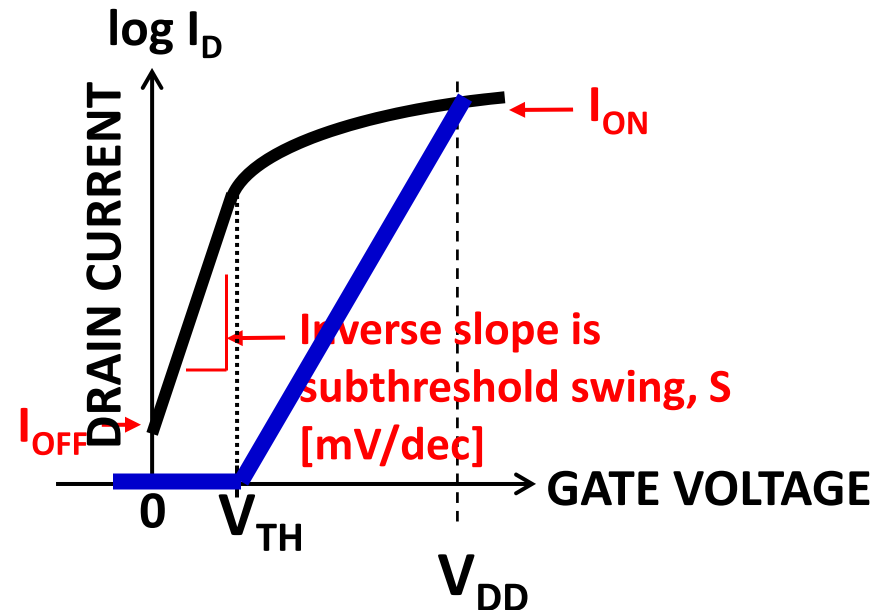


- Current between Source and Drain is controlled by the Gate voltage.
- "N-channel" & "P-channel" MOSFETs operate in a complementary manner

"CMOS" = Complementary MOS

Electron Energy Band Profile

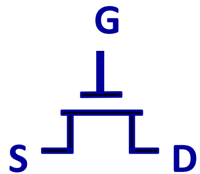




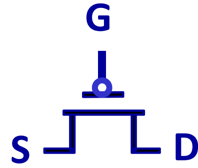
CMOS Devices and Circuits

CIRCUIT SYMBOLS

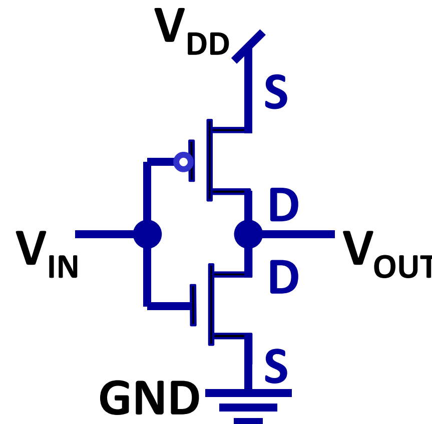
N-channel MOSFET

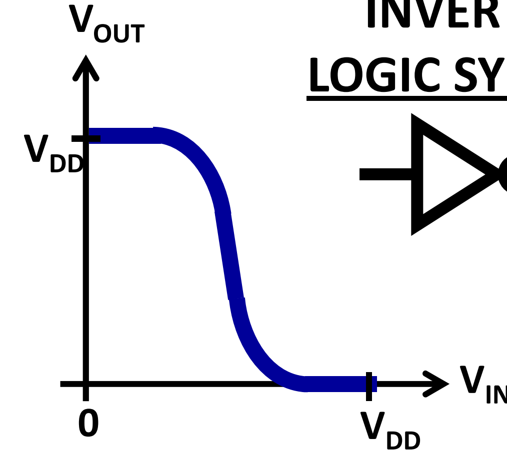


P-channel MOSFET

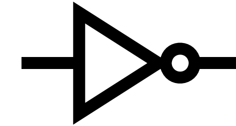


CMOS INVERTER CIRCUIT

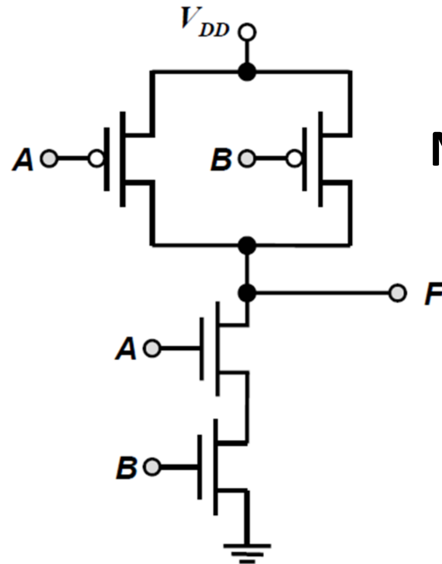




INVERTER LOGIC SYMBOL



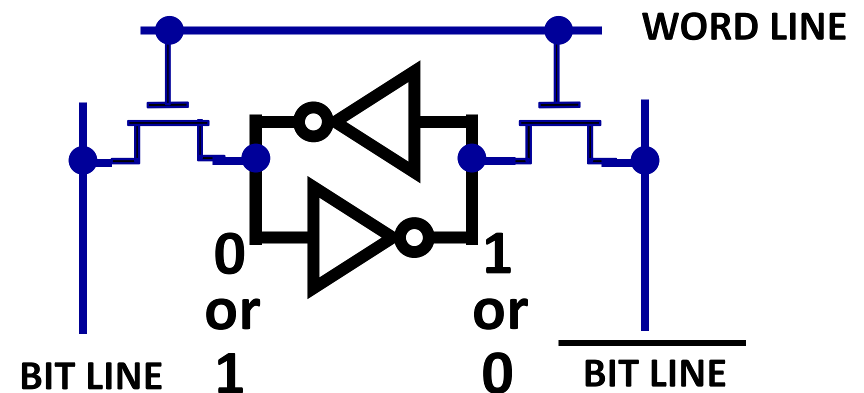
CMOS NAND GATE



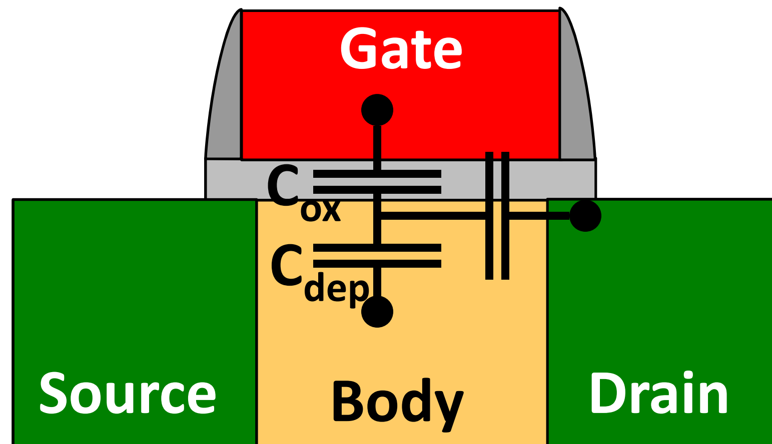
NOT AND (NAND) TRUTH TABLE

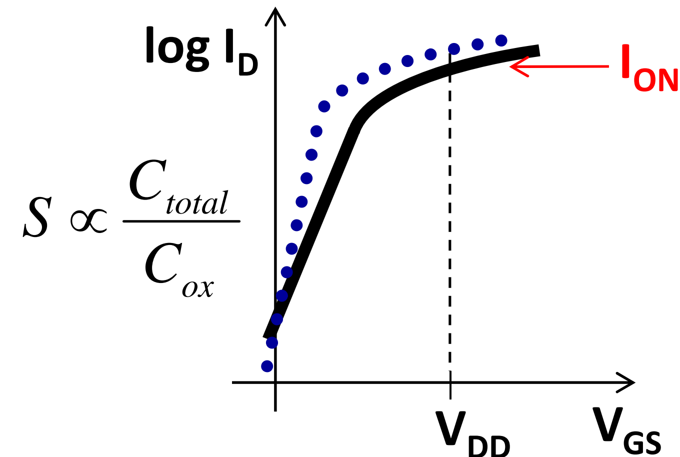
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

STATIC MEMORY (SRAM) CELL



Improving the ON/OFF Current Ratio

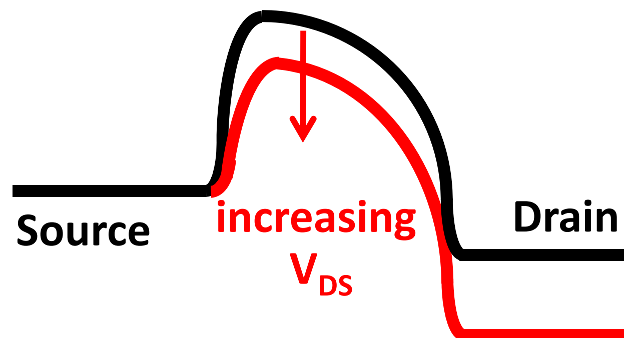


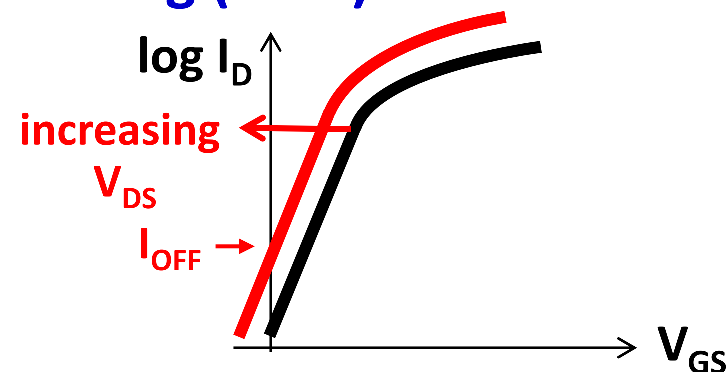


- **The greater the capacitive coupling between Gate and channel, the better control the Gate has over the channel potential.**

  →higher I_{ON}/I_{OFF} for fixed V_{DD}, or lower V_{DD} to achieve target I_{ON}/I_{OFF}

  →reduced drain-induced barrier lowering (DIBL):





MOSFET in ON State ($V_{GS} > V_{TH}$)

width, velocity, inversion-layer charge density

$$I_D = W \times v \times Q_{inv}$$

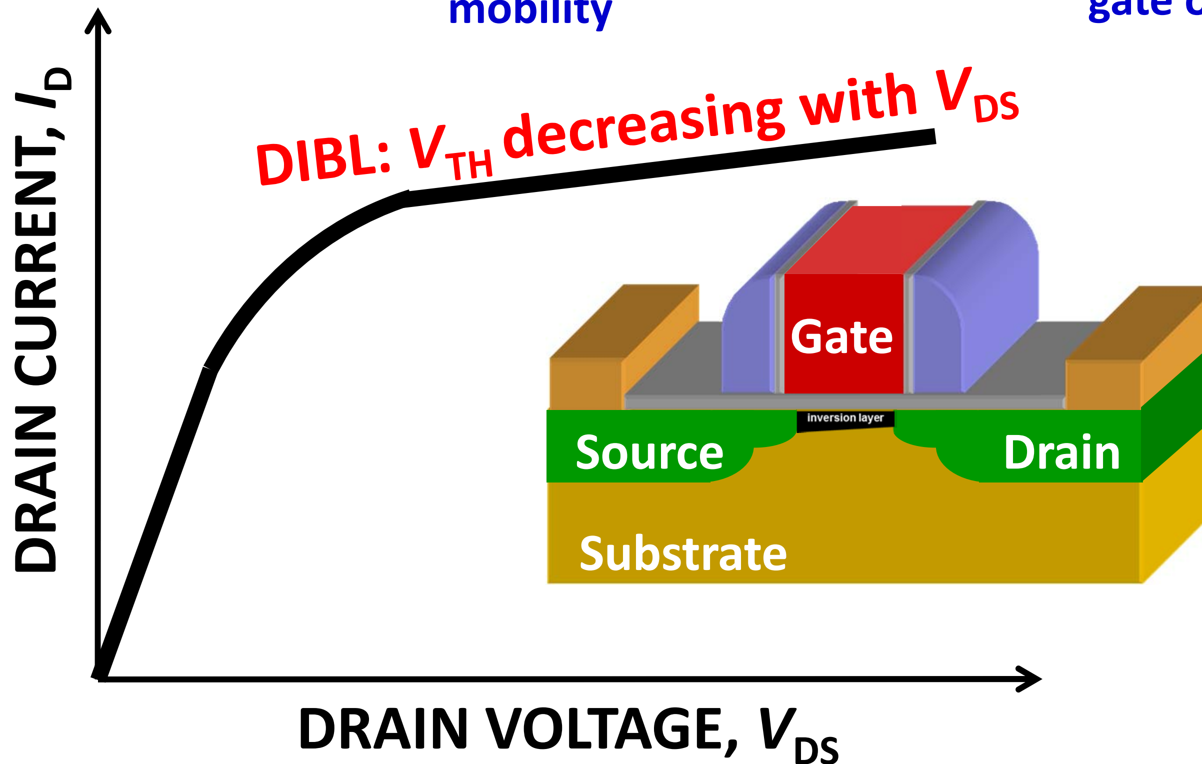
$$v \propto \mu_{eff}$$

mobility

gate-oxide capacitance

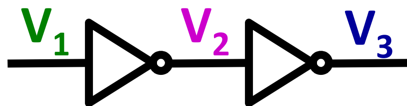
$$Q_{inv} \propto C_{ox} (V_{GS} - V_{TH})^{\eta}$$

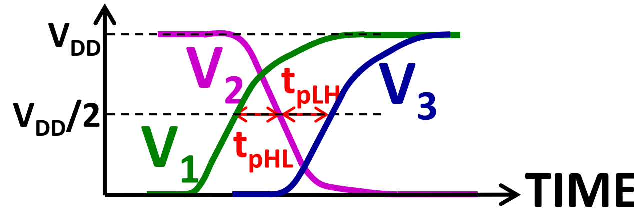
gate overdrive



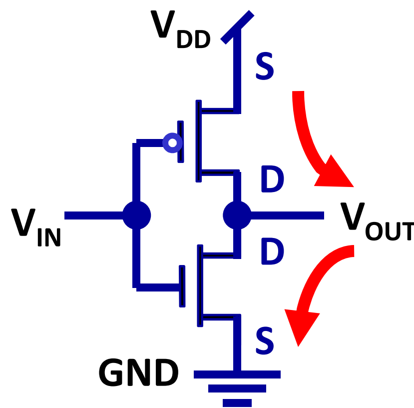
Effective Drive Current (I_{EFF})

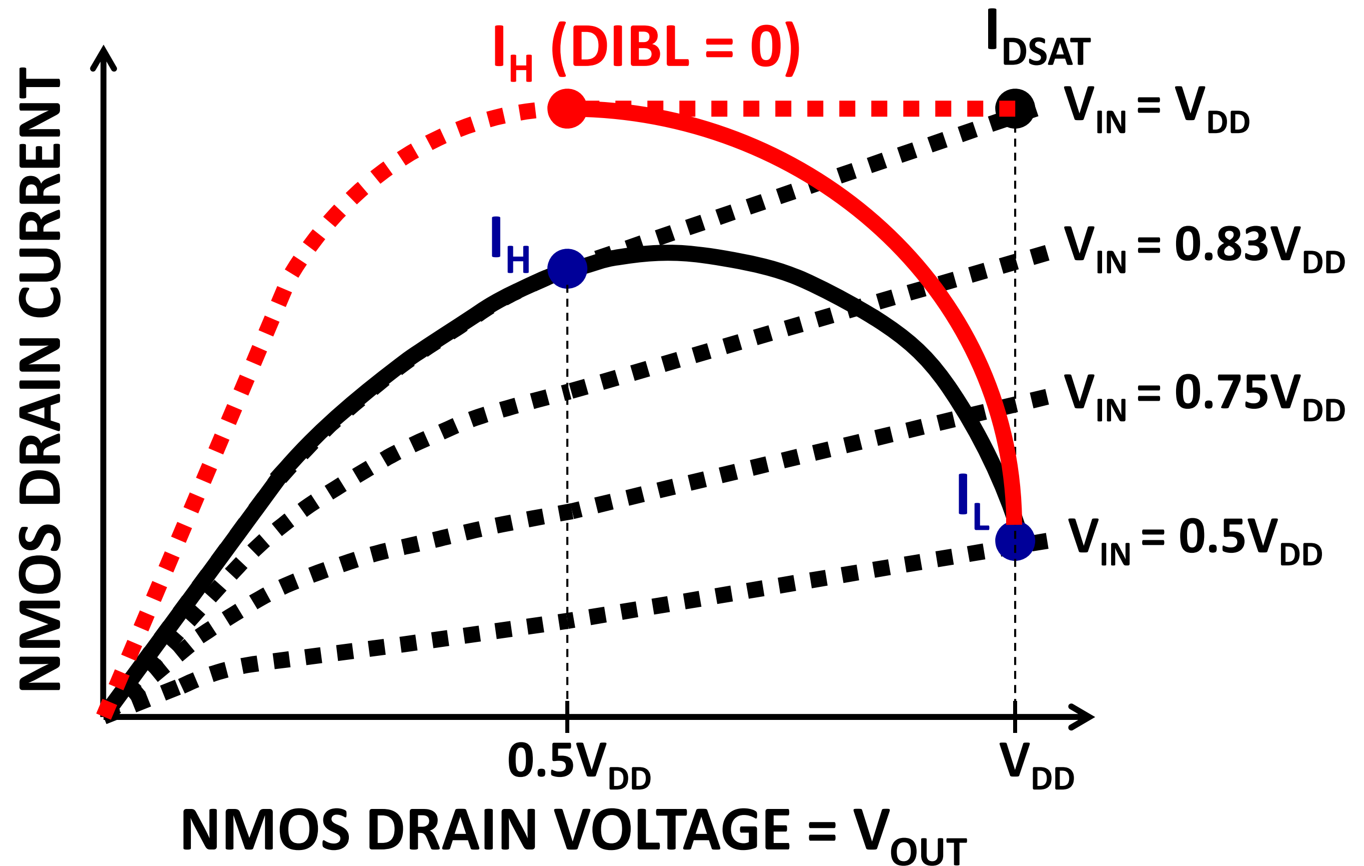
CMOS inverter chain:





$$I_{EFF} = \frac{I_H + I_L}{2}$$





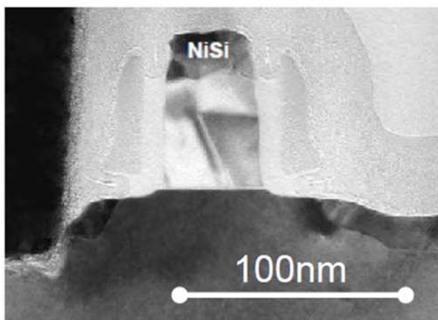
M. H. Na *et al.* (IBM), *IEDM Technical Digest*, pp. 121-124, 2002

CMOS Technology Scaling

XTEM images with the same scale

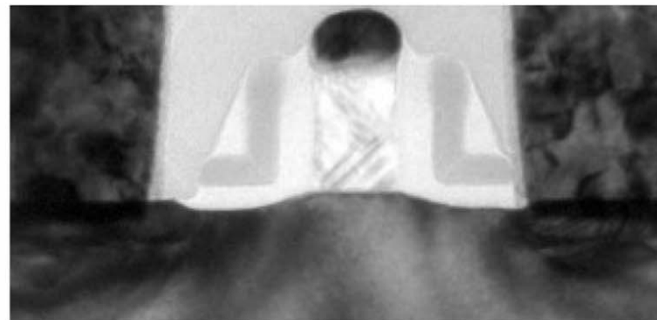
courtesy V. Moroz (Synopsys, Inc.)

90 nm node



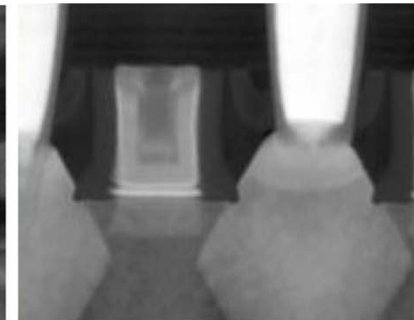
T. Ghani *et al.*, *IEDM* 2003

65 nm node



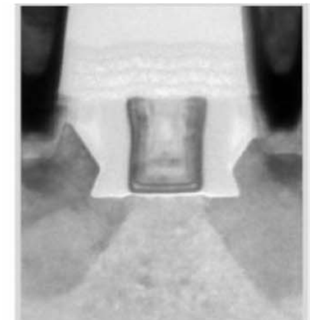
(after S. Tyagi *et al.*, *IEDM* 2005)

45 nm node



K. Mistry *et al.*, *IEDM* 2007

32 nm node



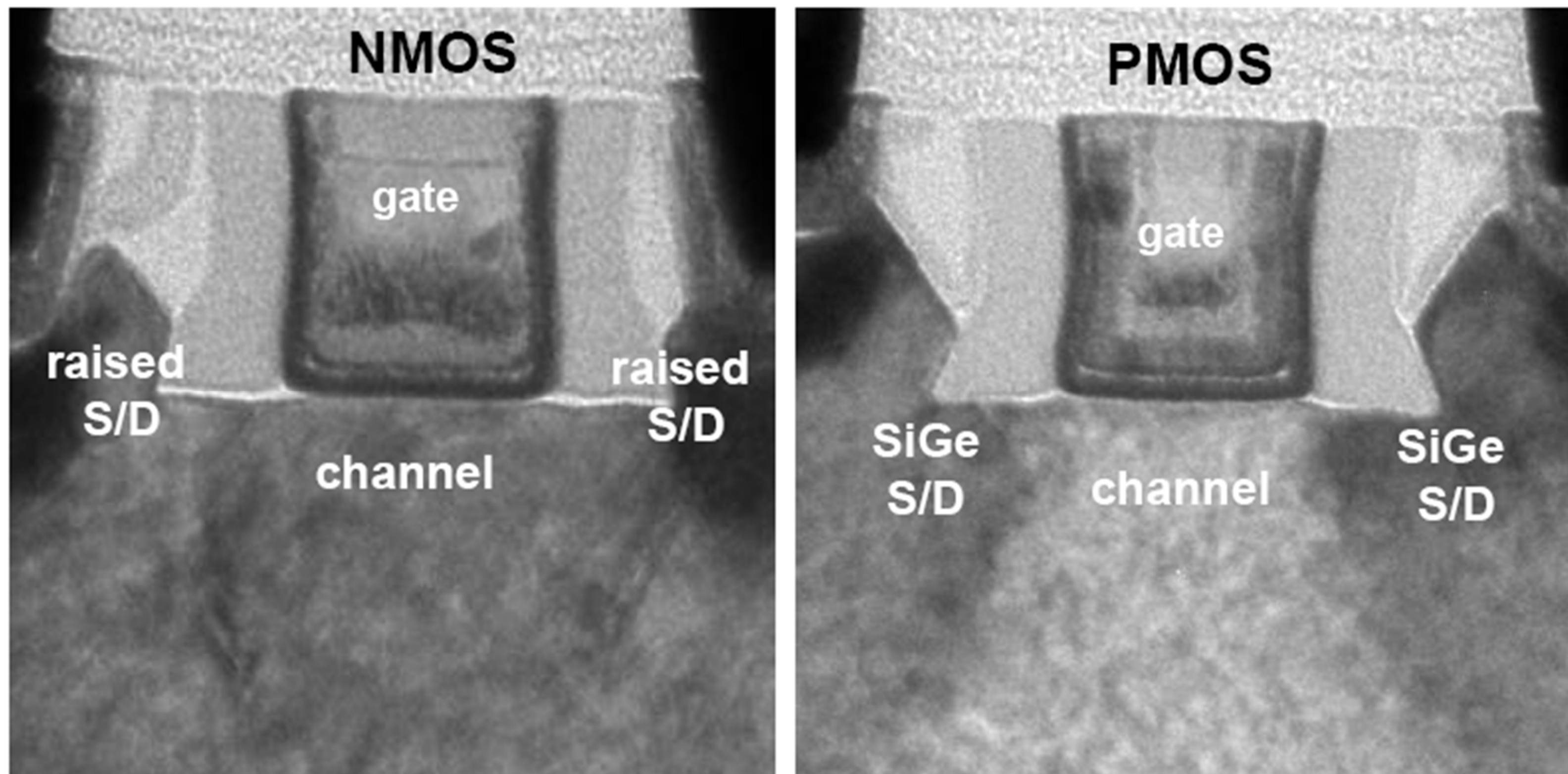
P. Packan *et al.*, *IEDM* 2009

- **Gate length has not scaled proportionately with device pitch (0.7x per generation) in recent generations.**
  - **Transistor performance has been boosted by other means.**

MOSFET Performance Boosters

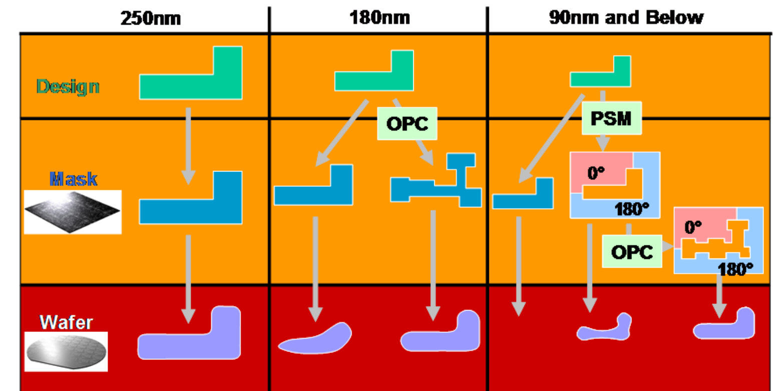
- **Strained channel regions → $\mu_{eff}\uparrow$**
- **High-k gate dielectric and metal gate electrodes → $C_{ox}\uparrow$**

Cross-sectional TEM views of Intel's 32 nm CMOS devices



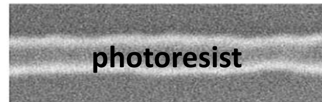
Process-Induced Variations

- **Sub-wavelength lithography:**
  - Resolution enhancement techniques are costly and increase process sensitivity

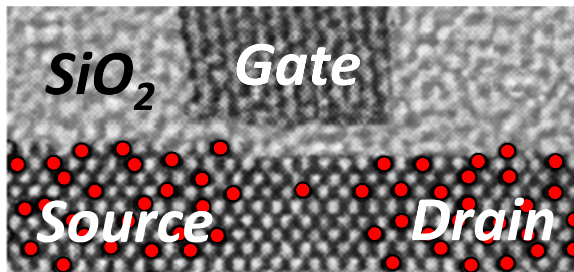


courtesy Mike Rieger (Synopsys, Inc.)

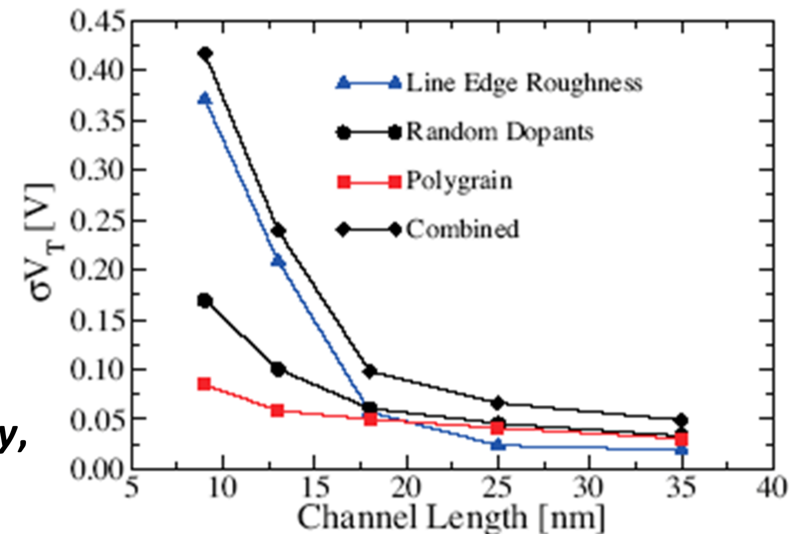
- **Gate line-edge roughness:**



- **Random dopant fluctuations (RDF):**
  - Atomistic effects become significant in nanoscale FETs



A. Brown *et al.*, *IEEE Trans. Nanotechnology*, p. 195, 2002



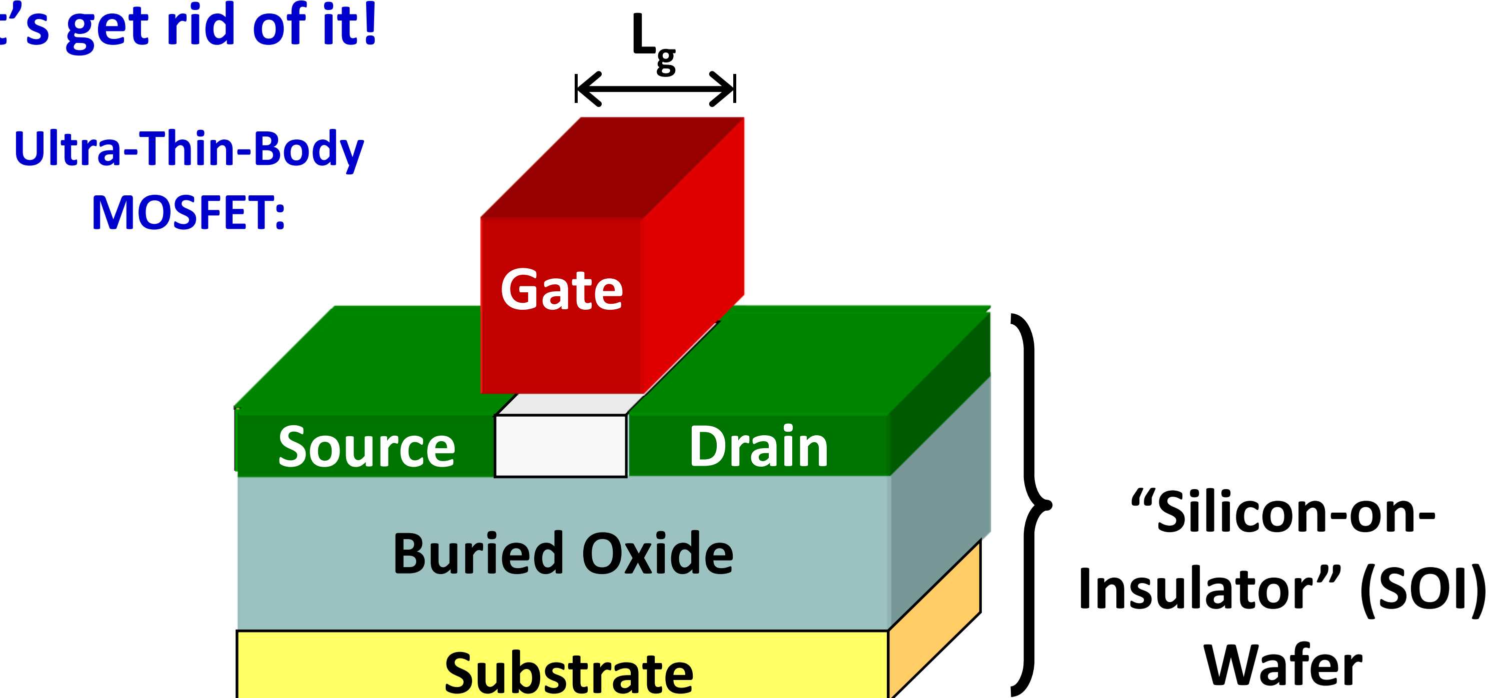
A. Asenov, *Symp. VLSI Tech. Dig.*, p. 86, 2007

A Journey Back through Time…

Why New Transistor Structures?

- Off-state leakage (I_{OFF}) must be suppressed as L_g is scaled down
  - allows for reductions in V_{TH} and hence V_{DD}
- Leakage occurs in the region away from the channel surface

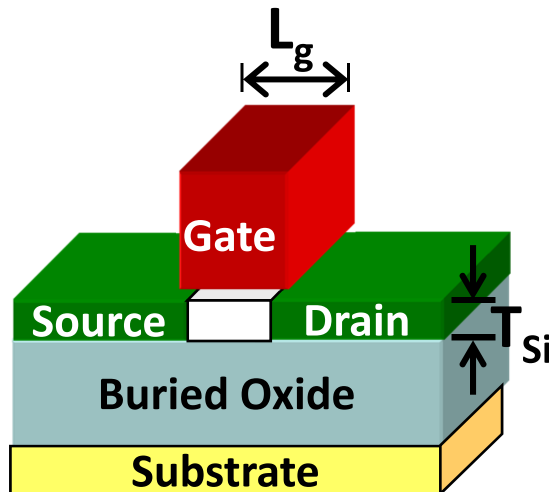
→ Let's get rid of it!



Thin-Body MOSFETs

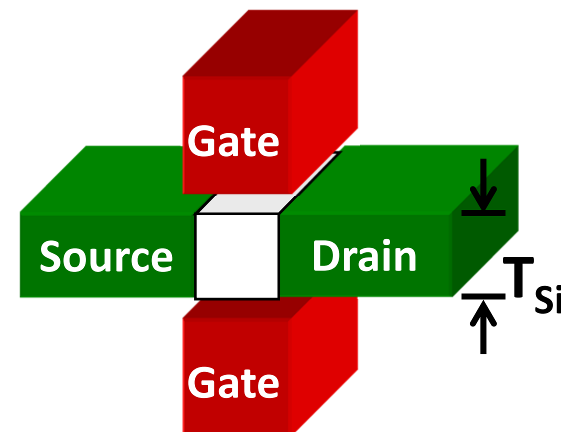
- I_{OFF} is suppressed by using an adequately thin body region.
  - Body doping can be eliminated
    → higher drive current due to higher carrier mobility
    → Reduced impact of random dopant fluctuations (RDF)

Ultra-Thin Body (UTB)



$T_{Si} < (1/4) \times L_g$

Double-Gate (DG)

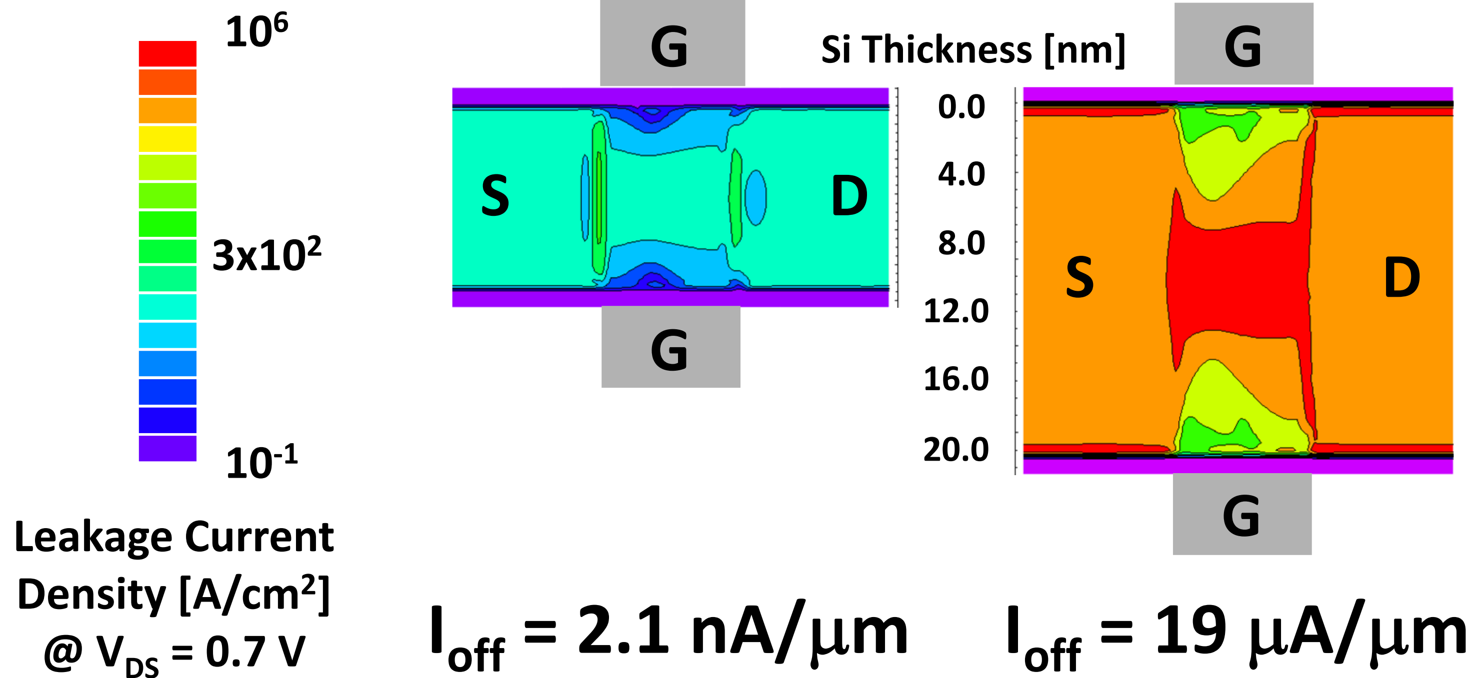


$T_{Si} < (2/3) \times L_g$

B. Yu *et al.*, *ISDRS* 1997   R.-H. Yan *et al.*, *IEEE TED* 1992

Effect of T_{Si} on Leakage

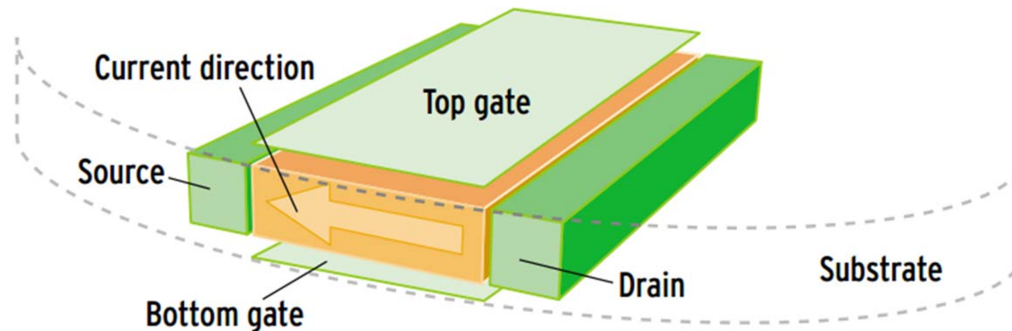
L_g = 25 nm; $T_{ox,eq}$ = 12Å



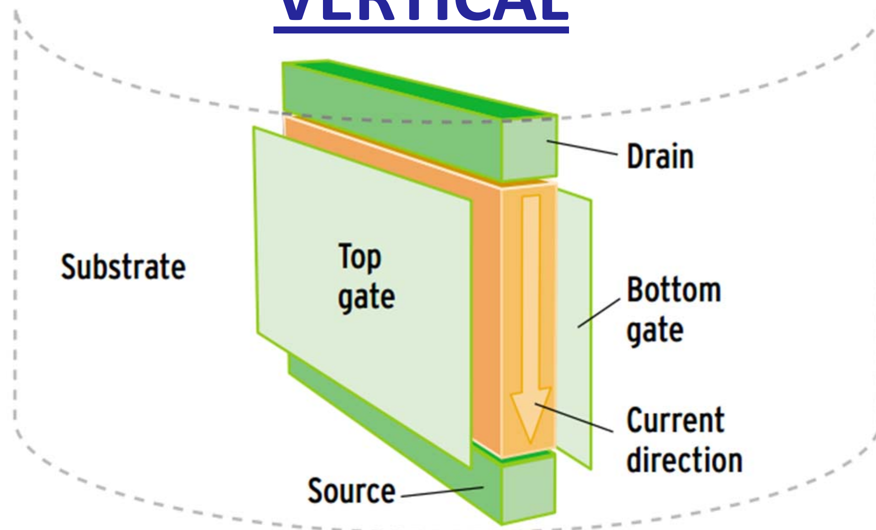
I_{off} = 2.1 nA/μm I_{off} = 19 μA/μm

Double-Gate MOSFET Structures

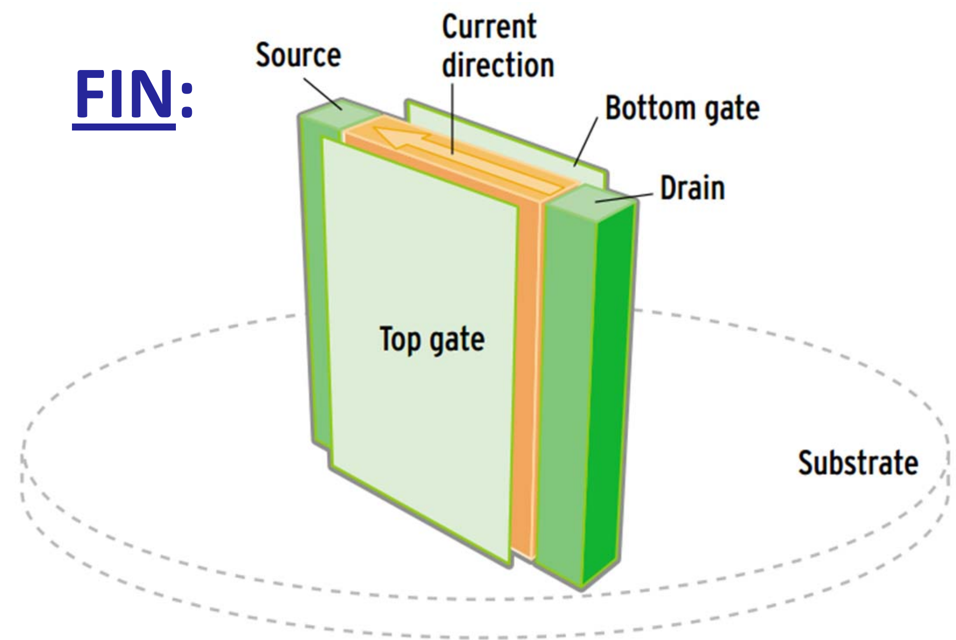
PLANAR:



VERTICAL



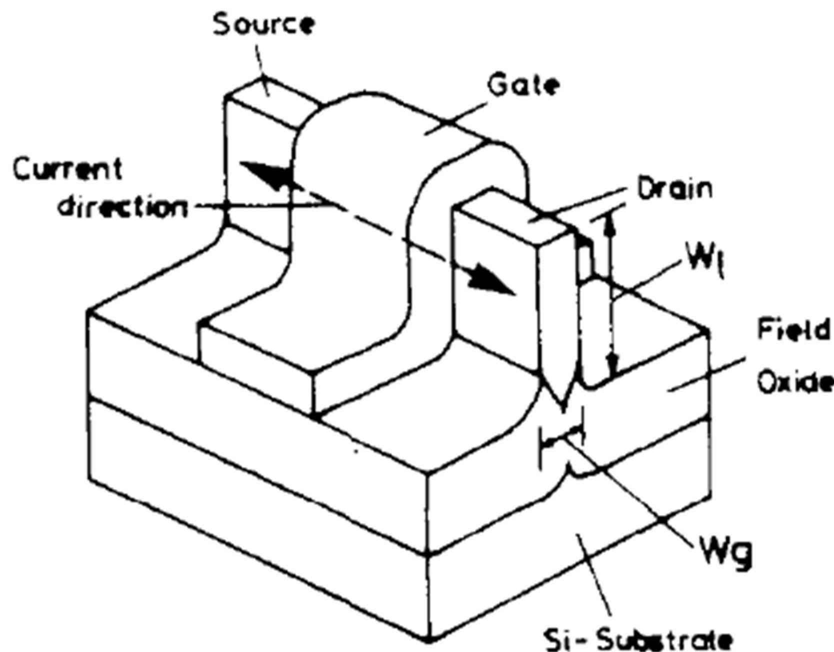
FIN:

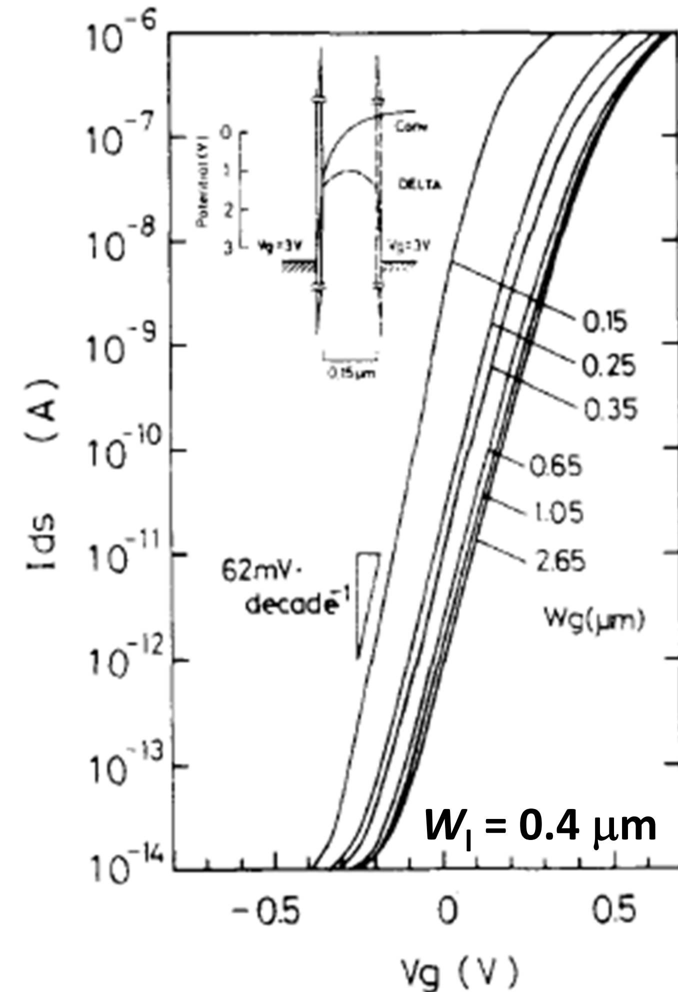


L. Geppert, *IEEE Spectrum*, October 2002

DELTA MOSFET

D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda (Hitachi Central Research Laboratory),
"A fully depleted lean-channel transistor (DELTA) – a novel vertical ultrathin SOI MOSFET,"
IEEE Electron Device Letters Vol. 11, pp. 36-39, 1990

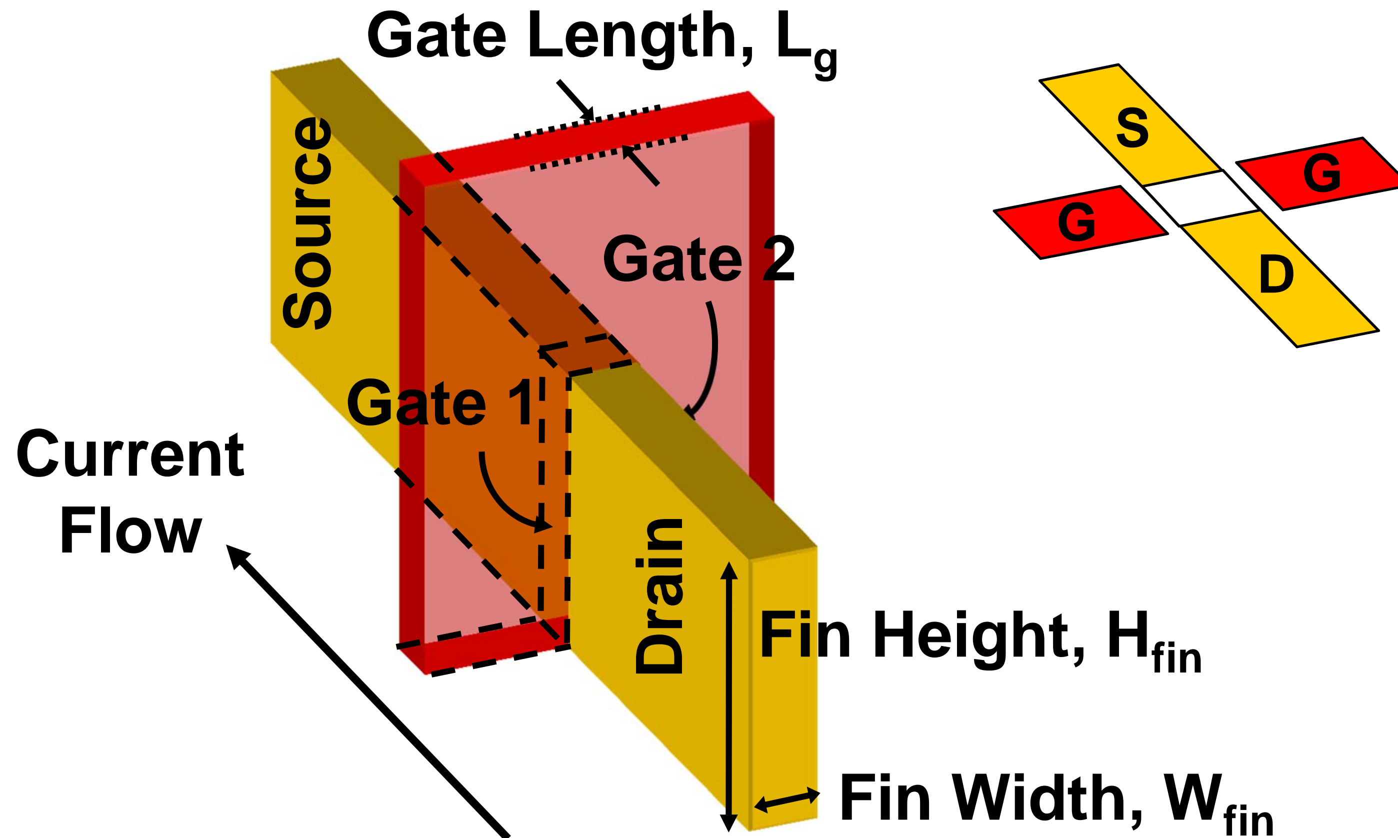




- **Improved gate control observed for W_g < 0.3 μm**
  - **L_{eff}= 0.57 μm**

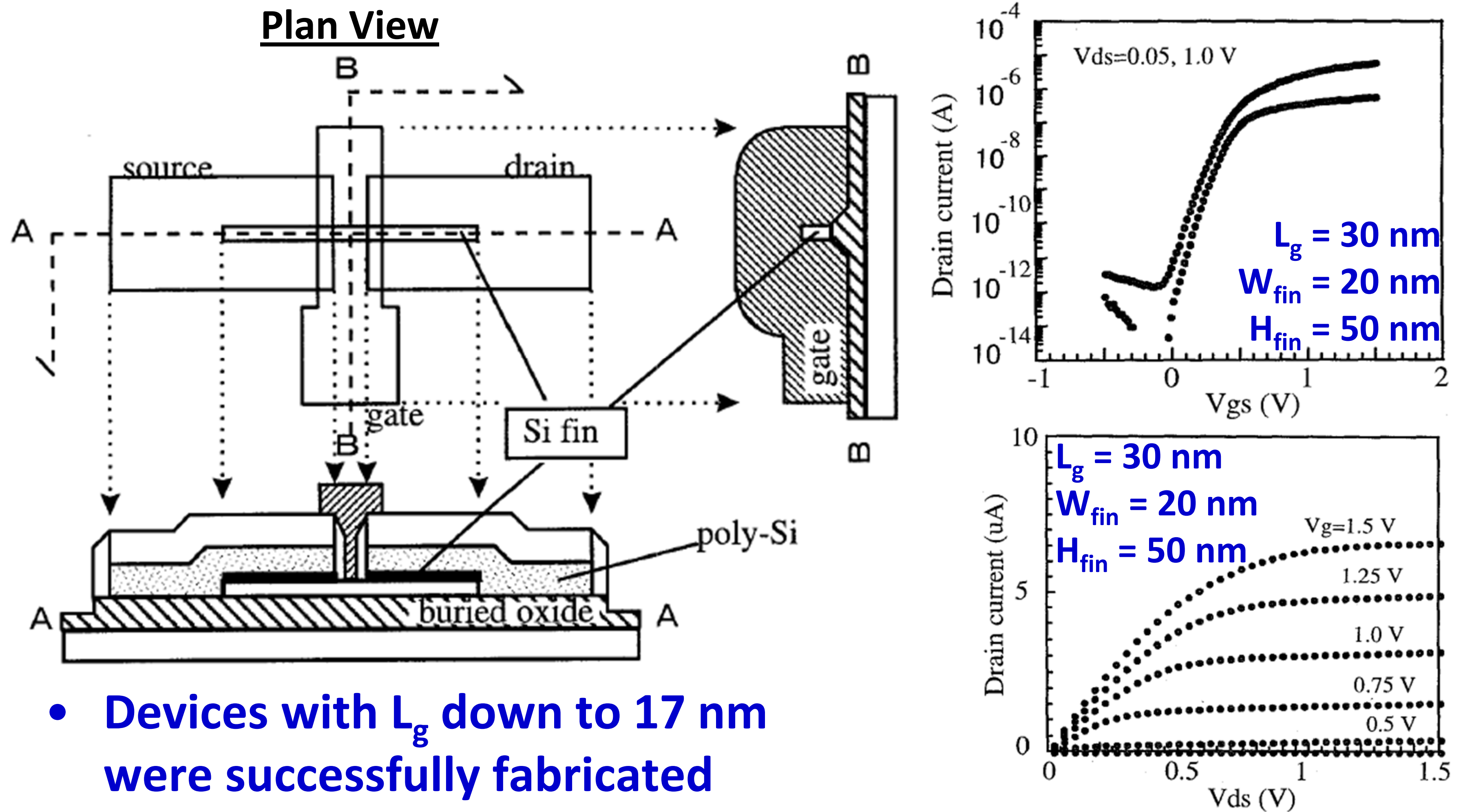
Double-Gate FinFET

- Self-aligned gates straddle narrow silicon fin
- Current flows parallel to wafer surface



1998: First N-channel FinFETs

D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, and C. Hu,
"A folded-channel MOSFET for deep-sub-tenth micron era,"
IEEE International Electron Devices Meeting Technical Digest, pp. 1032-1034, 1998



- **Devices with L_g down to 17 nm were successfully fabricated**

1999: First P-channel FinFETs

X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," *IEEE International Electron Devices Meeting Technical Digest*, pp. 67-70, 1999

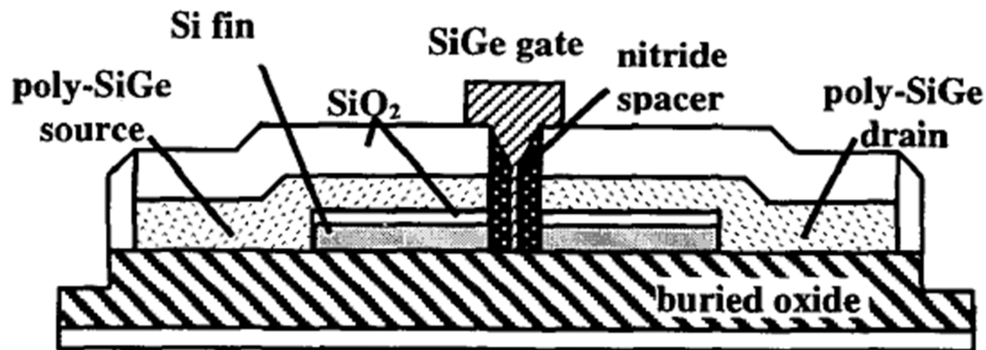
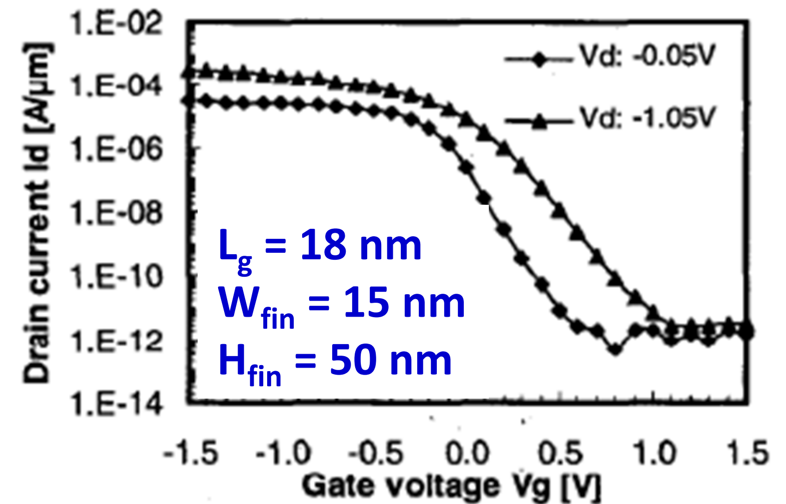
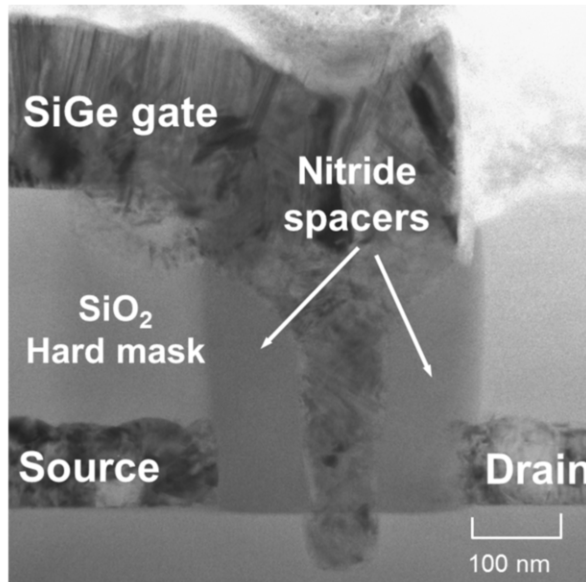
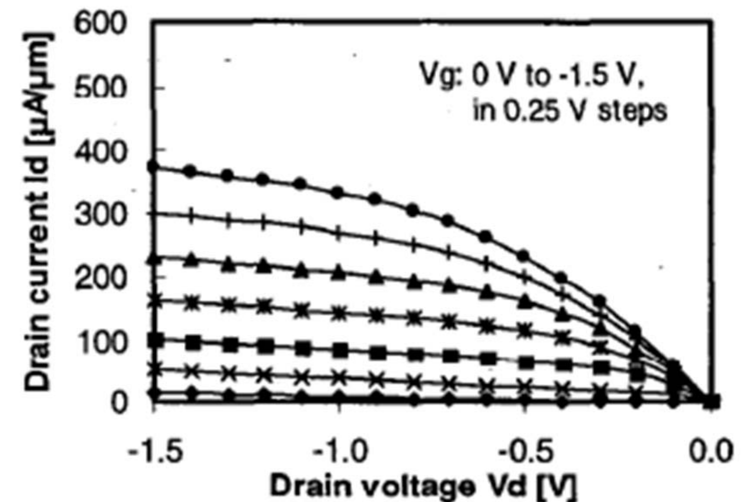


Figure 1: Schematic drawing of FinFET





Transmission Electron Micrograph



2000: Vested Interest from Industry

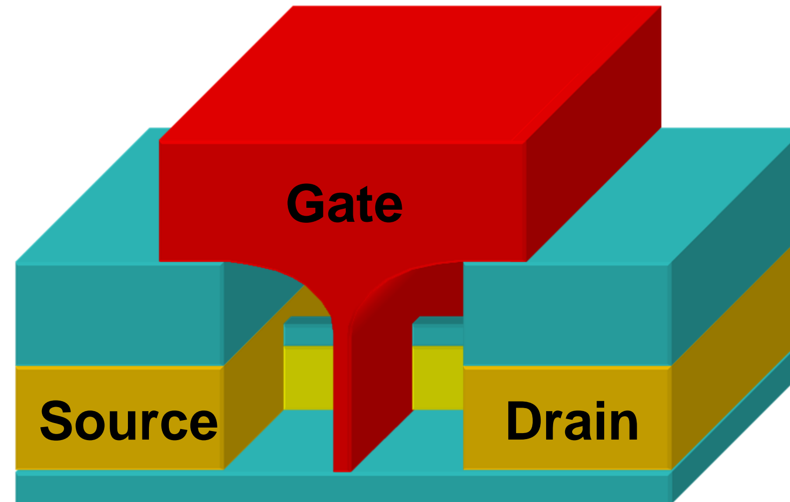
- **Semiconductor Research Corporation (SRC) & AMD fund project:**
  - **Development of a FinFET process flow compatible with a conventional planar CMOS process**
  - **Demonstration of the compatibility of the FinFET structure with a production environment**

  (October 2000 through September 2003)

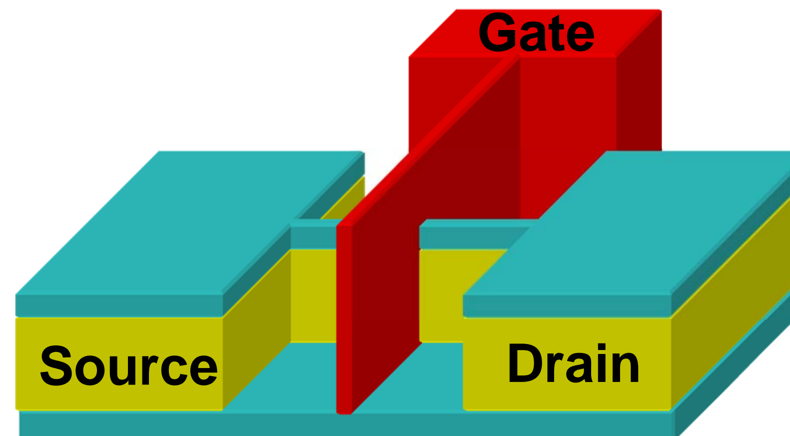
- **DARPA/SRC Focus Center Research Program funds projects:**
  - **Approaches for enhancing FinFET performance**
    (MSD Center, April 2001 through August 2003)
  - **FinFET-based circuit design**
    (C2S2 Center, August 2003 through July 2006)

FinFET Structures

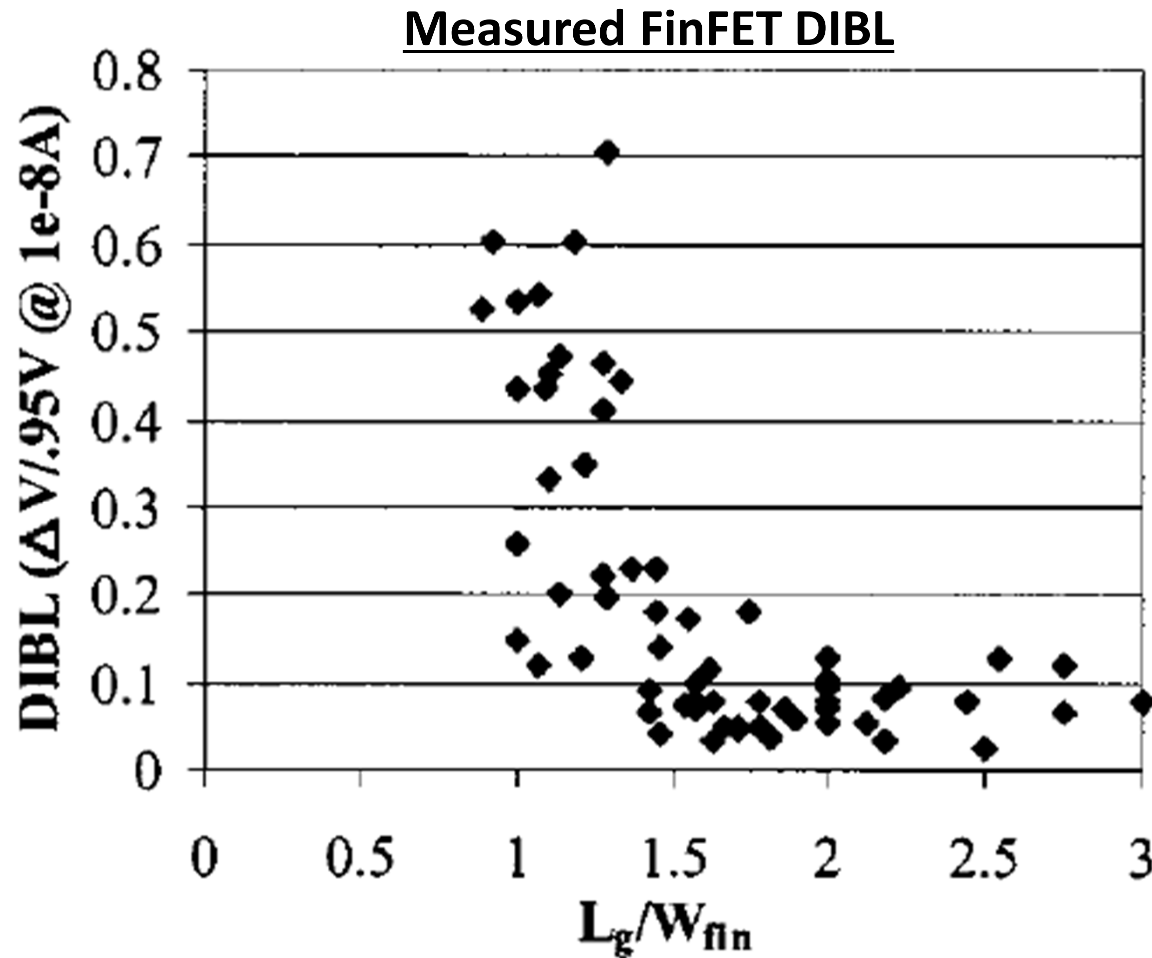
<u>Original</u>:
Gate-last process flow



<u>Improved</u>:
Gate-first process flow



Fin Width Requirement



- **To adequately suppress DIBL, $L_g/W_{fin} > 1.5$**

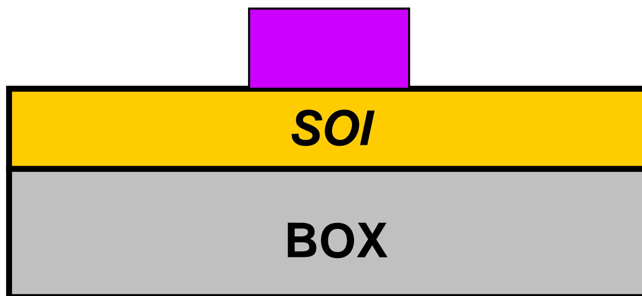
→ Challenge for lithography!

Sub-Lithographic Fin Patterning

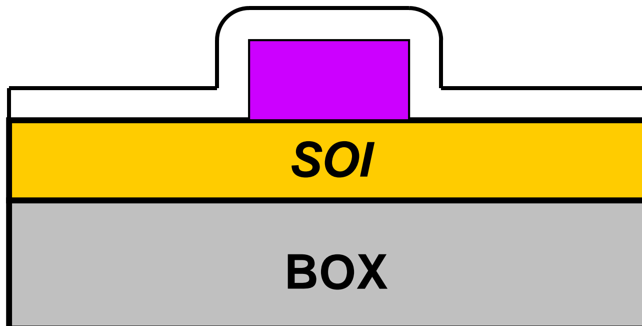
Spacer Lithography

a.k.a. Sidewall Image Transfer (SIT) and Self-Aligned Double Patterning (SADP)

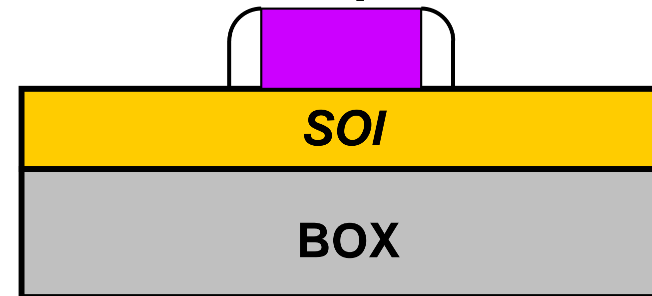
1. Deposit & pattern sacrificial layer



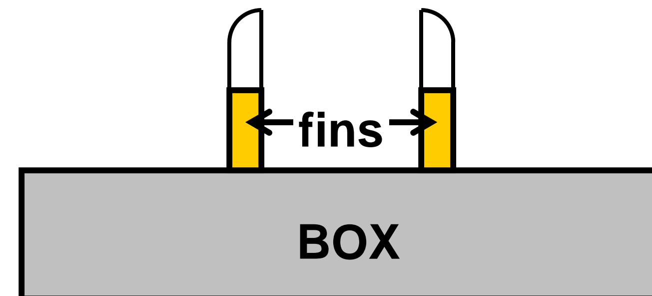
2. Deposit mask layer (SiO_2 or Si_3N_4)



3. Etch back mask layer to form "spacers"



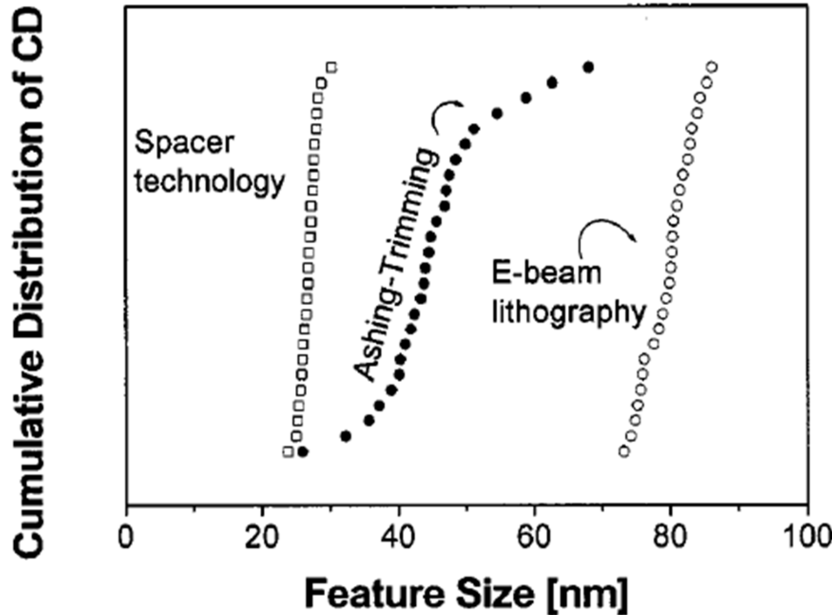
4. Remove sacrificial layer; etch SOI layer to form fins



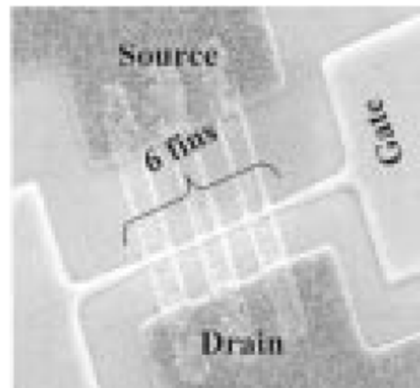
Note that fin pitch is 1/2× that of patterned layer

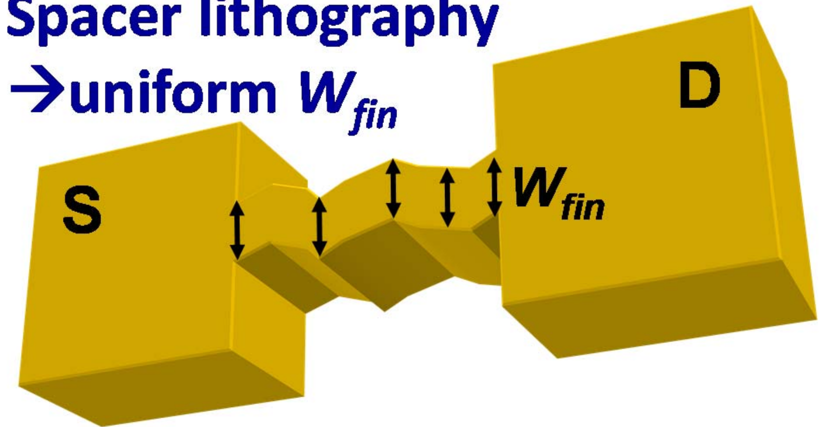
Benefits of Spacer Lithography

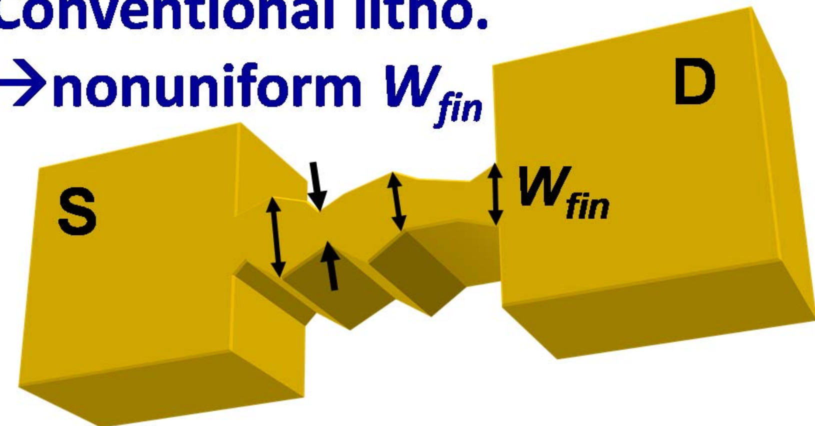
- Spacer litho. provides for better CD control and uniform fin width



SEM image of FinFET with spacer-defined fins:







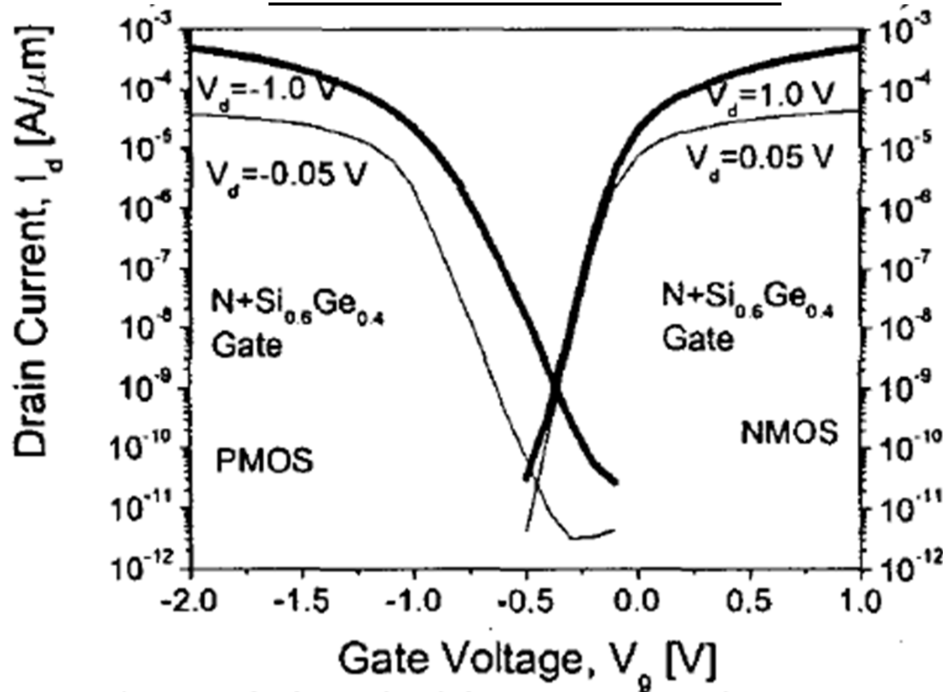
Y.-K. Choi *et al*. (UC-Berkeley), *IEEE Trans. Electron Devices*, Vol. 49, pp. 436-441, 2002

Spacer-Defined FinFETs

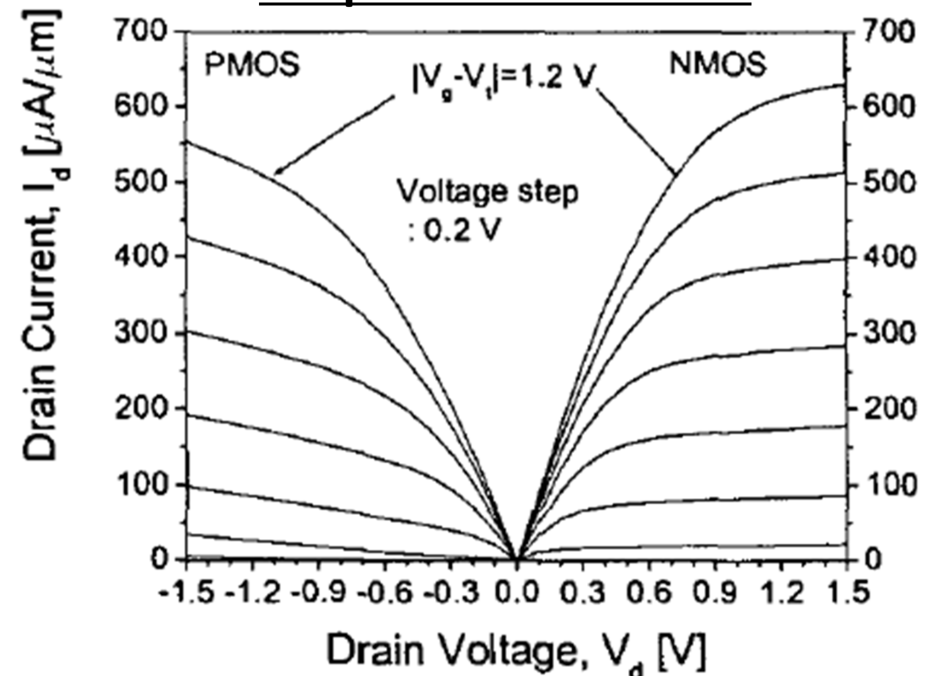
Y.-K. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "Sub-20nm CMOS FinFET technologies," *IEEE International Electron Devices Meeting Technical Digest*, pp. 421-424, 2001

L_g = 60 nm, W_{fin} = 40 nm

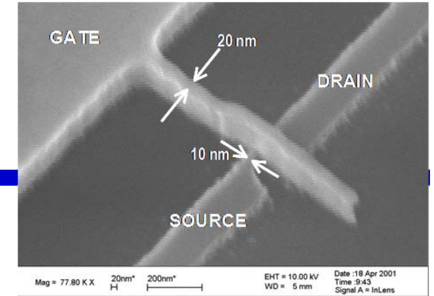
<u>Transfer Characteristics</u>



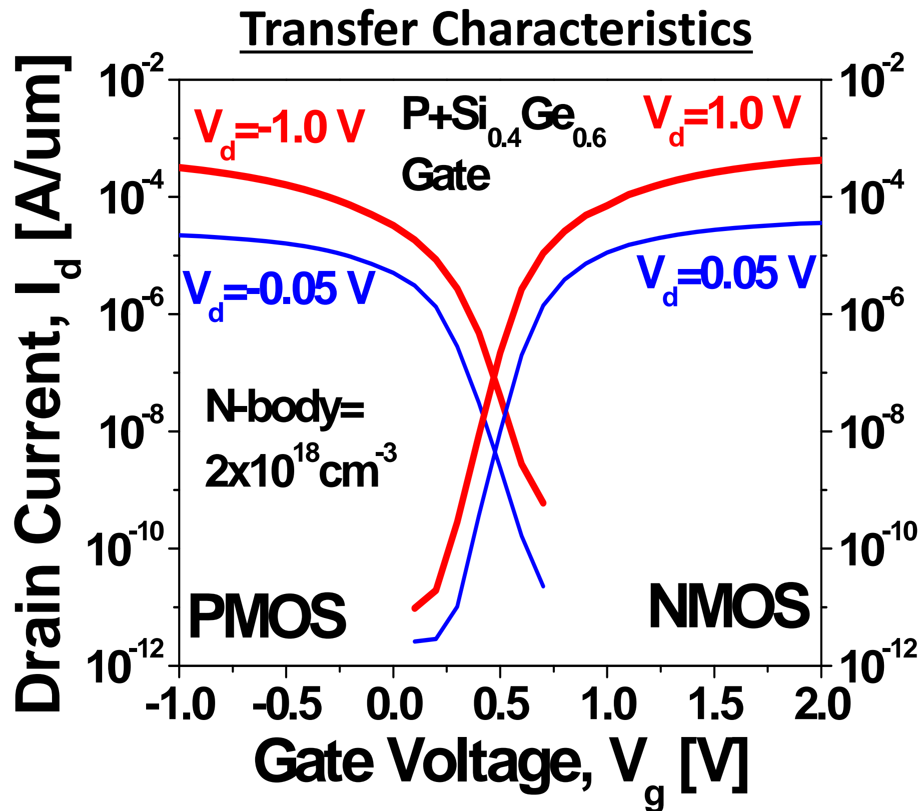
<u>Output Characteristics</u>

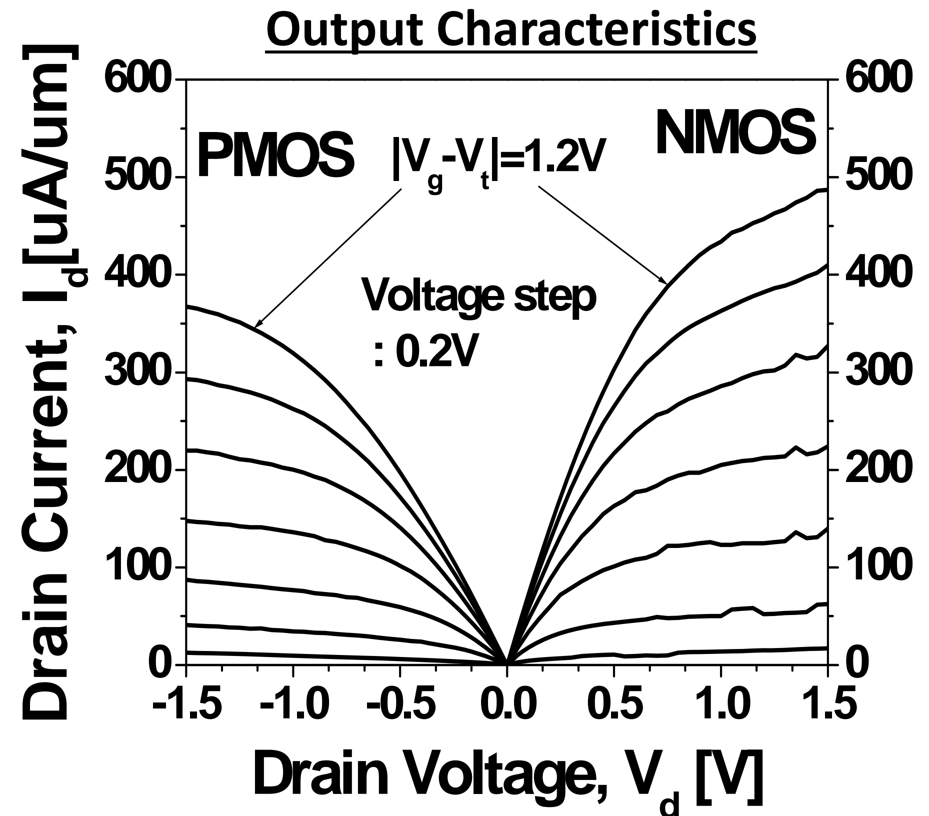


2001: 15 nm FinFETs



Y.-K. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T.-J. King, J. Bokor, C. Hu,
"Sub-20nm CMOS FinFET technologies,"
IEEE International Electron Devices Meeting Technical Digest, pp. 421-424, 2001

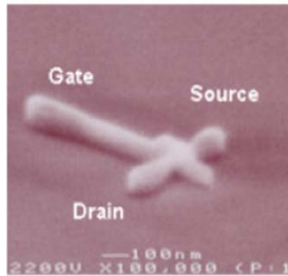




W_{fin} = 10 nm; T_{ox} = 2.1 nm

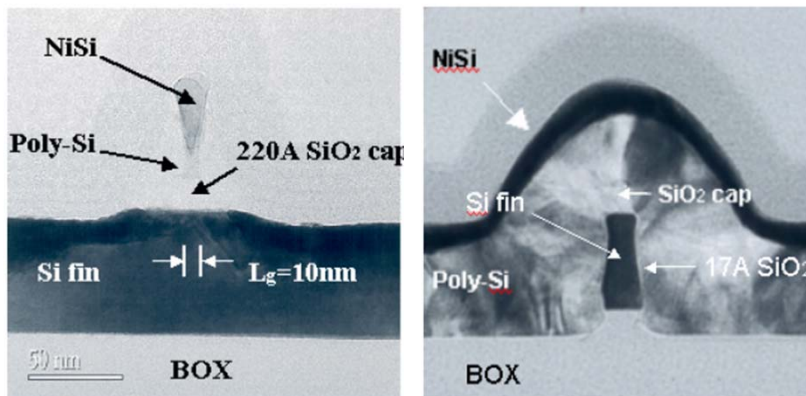
2002: 10 nm FinFETs

SEM image:



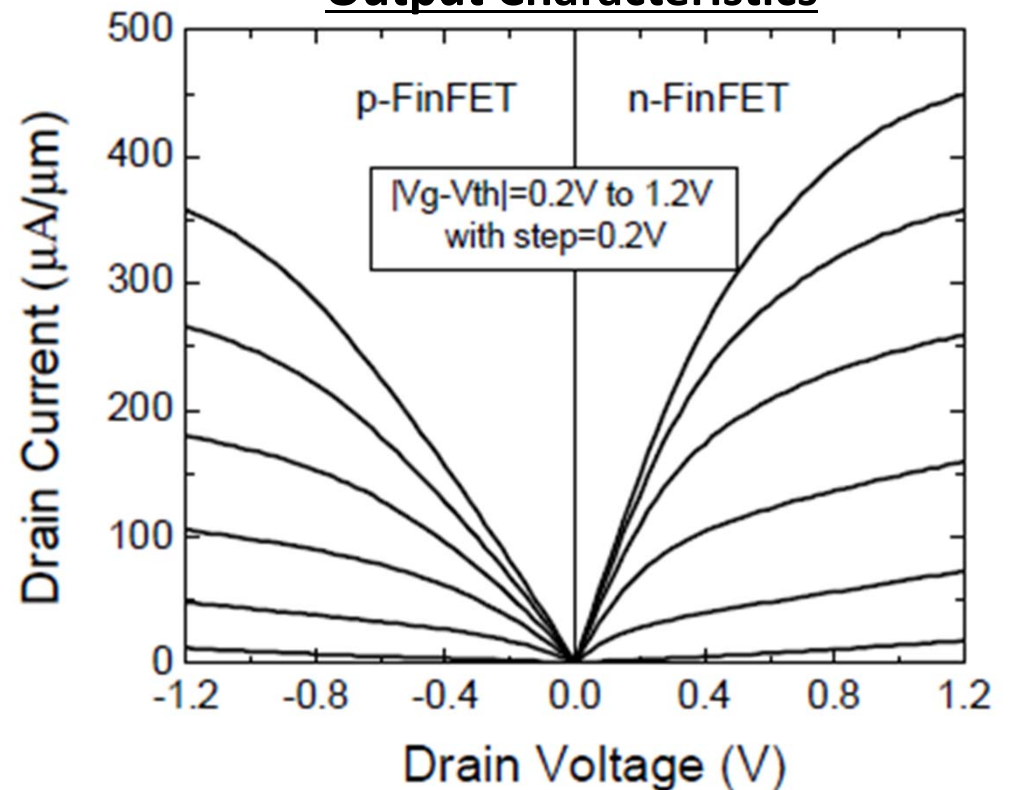
B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Hu, T.-J. King, J. Bokor, M.-R. Lin, and D. Kyser, "FinFET scaling to 10nm gate length," *International Electron Devices Meeting Technical Digest*, pp. 251-254, 2002

TEM images

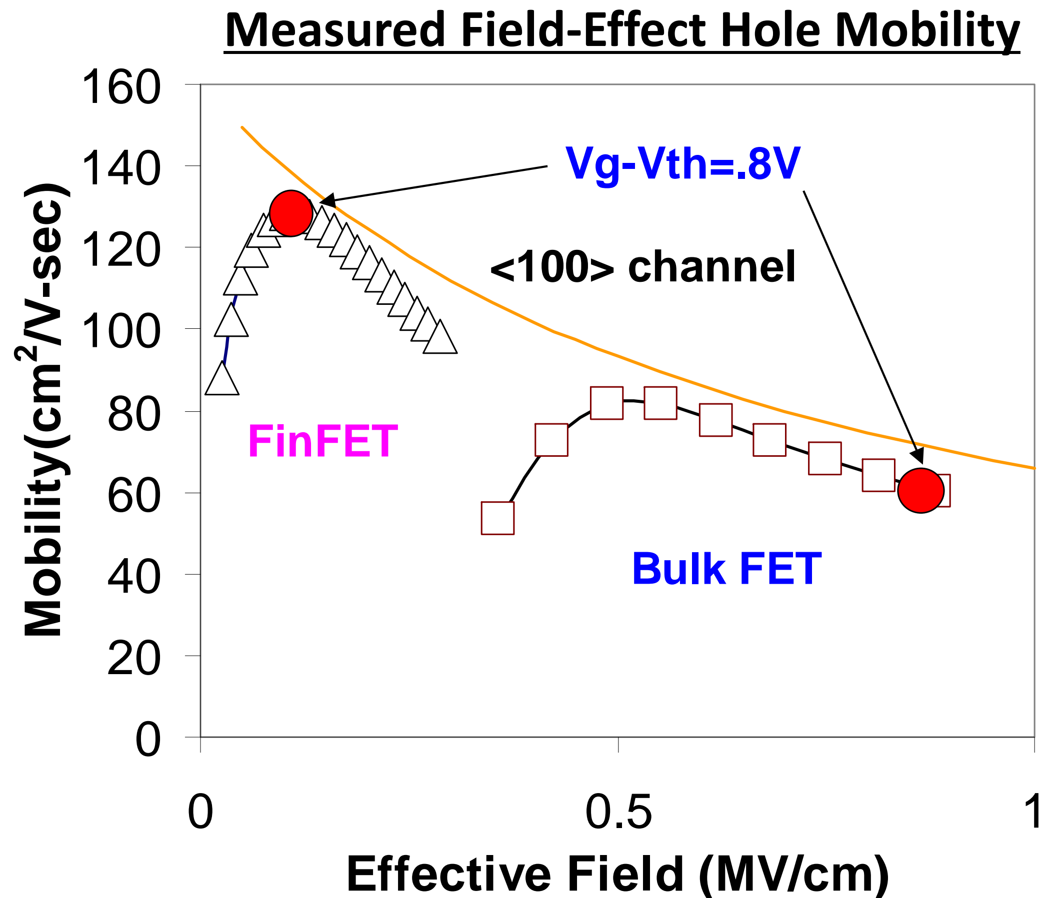


- **These devices were fabricated at AMD, using optical lithography.**

Output Characteristics



Hole Mobility Comparison

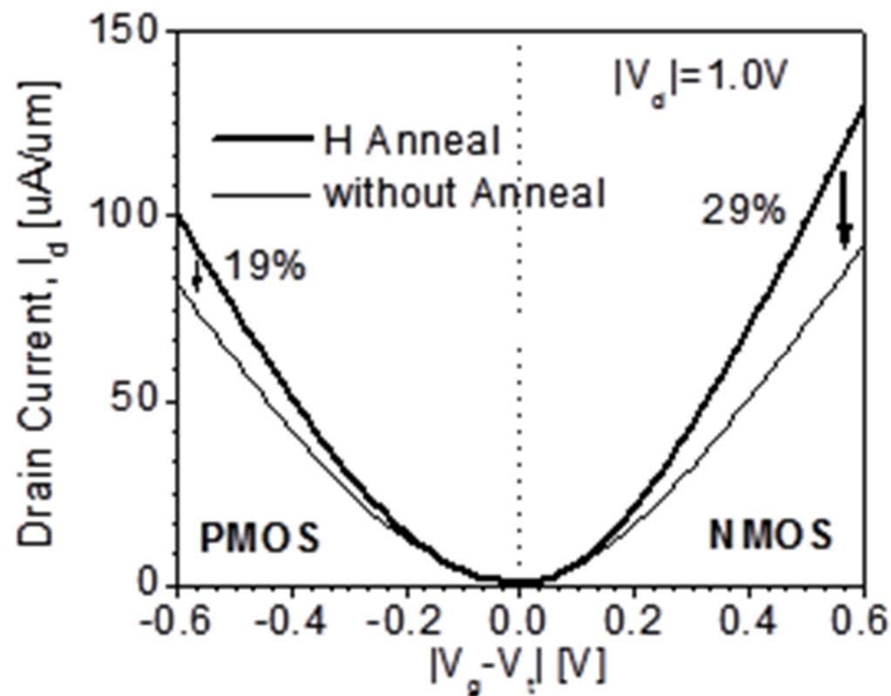


- **DG FET has higher hole mobility due to lower transverse electric field**
- **For the same gate overdrive, hole mobility in DG-FinFET is 2× that in a control bulk FET**

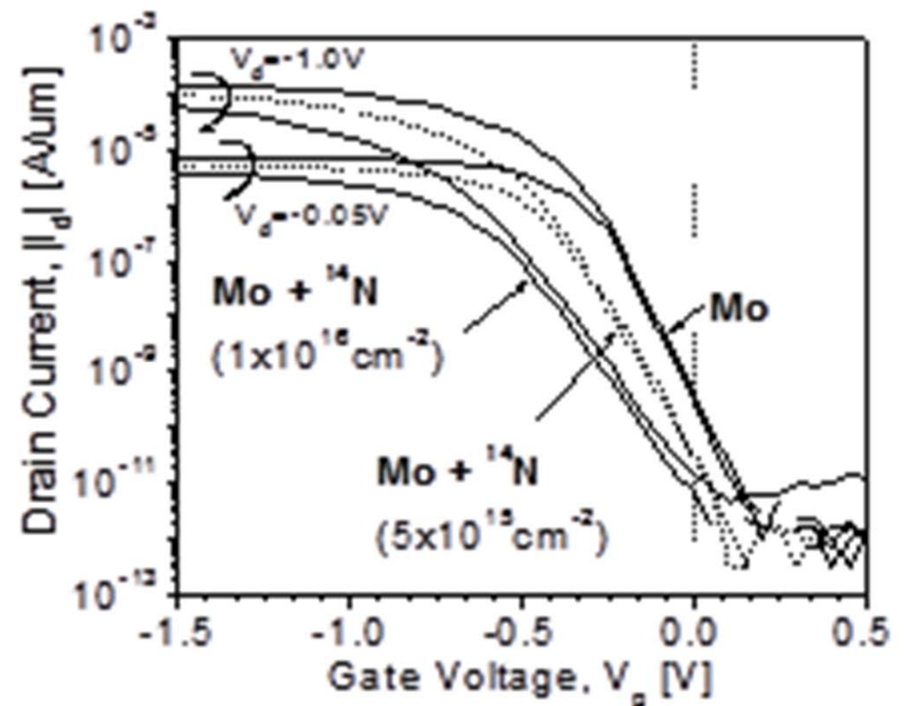
FinFET Process Refinements

Y.-K. Choi, L. Chang, P. Ranade, J. Lee, D. Ha, S. Balasubramanian, A. Agarwal, T.-J. King, and J. Bokor, "FinFET process refinements for improved mobility and gate work function engineering," *IEEE International Electron Devices Meeting Technical Digest*, pp. 259-262, 2002

Fin-sidewall smoothening for improved carrier mobilities

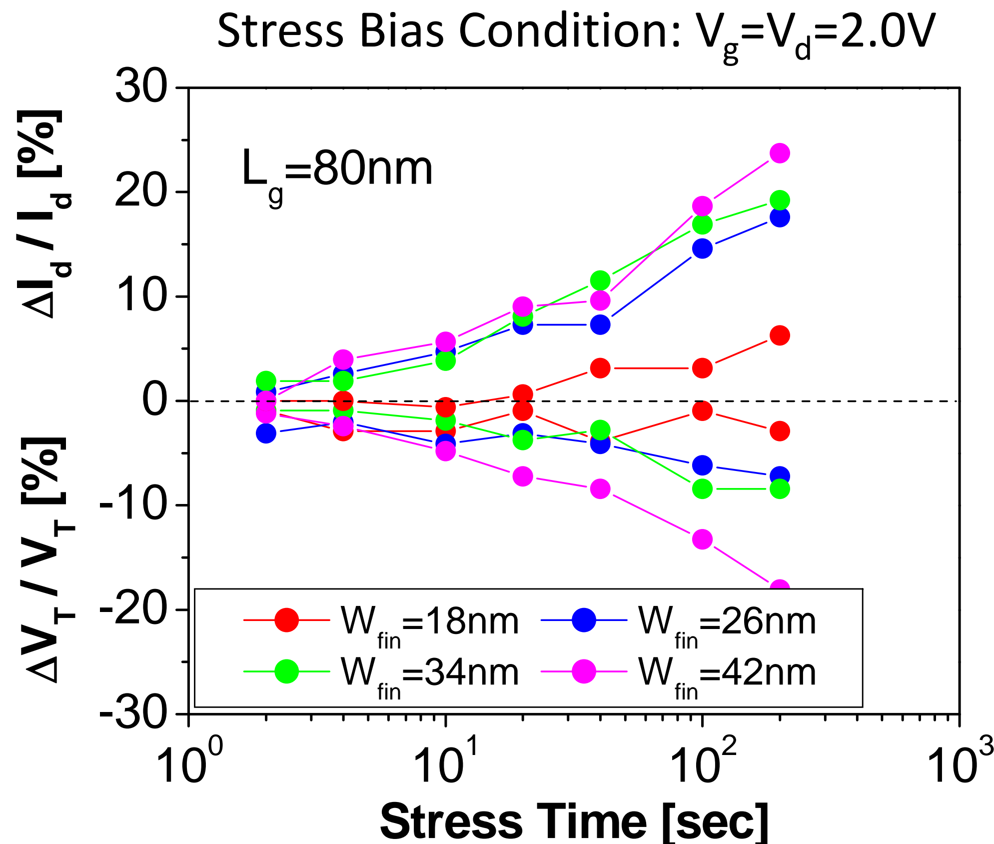


Gate work function tuning for V_{TH} adjustment



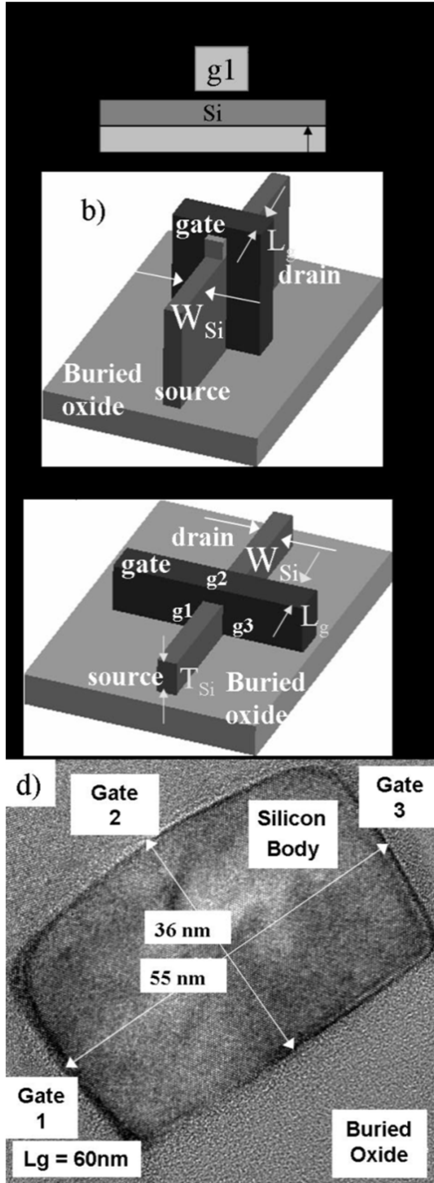
FinFET Reliability

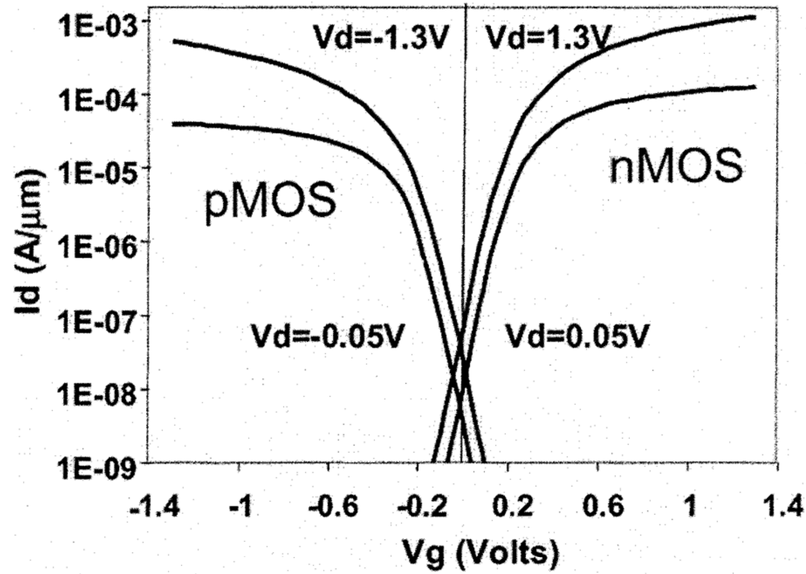
Y.-K. Choi, D. Ha, J. Bokor, and T.-J. King, "Reliability study of CMOS FinFETs," *IEEE International Electron Devices Meeting Technical Digest*, pp. 177-180, 2003

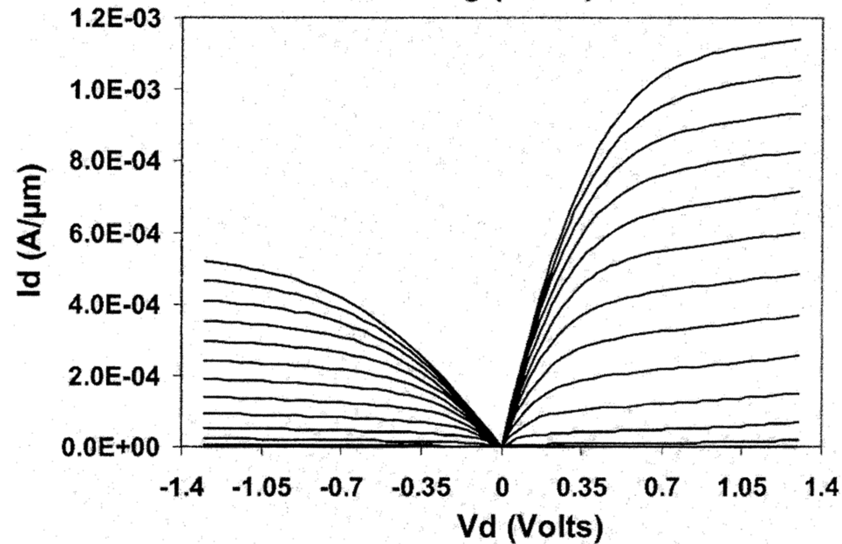


- **Narrower fin → improved hot-carrier (HC) immunity**
- **HC lifetime and oxide Q_{BD} are also improved by smoothening the Si fin sidewall surfaces** (by H_2 annealing)

Tri-Gate FET



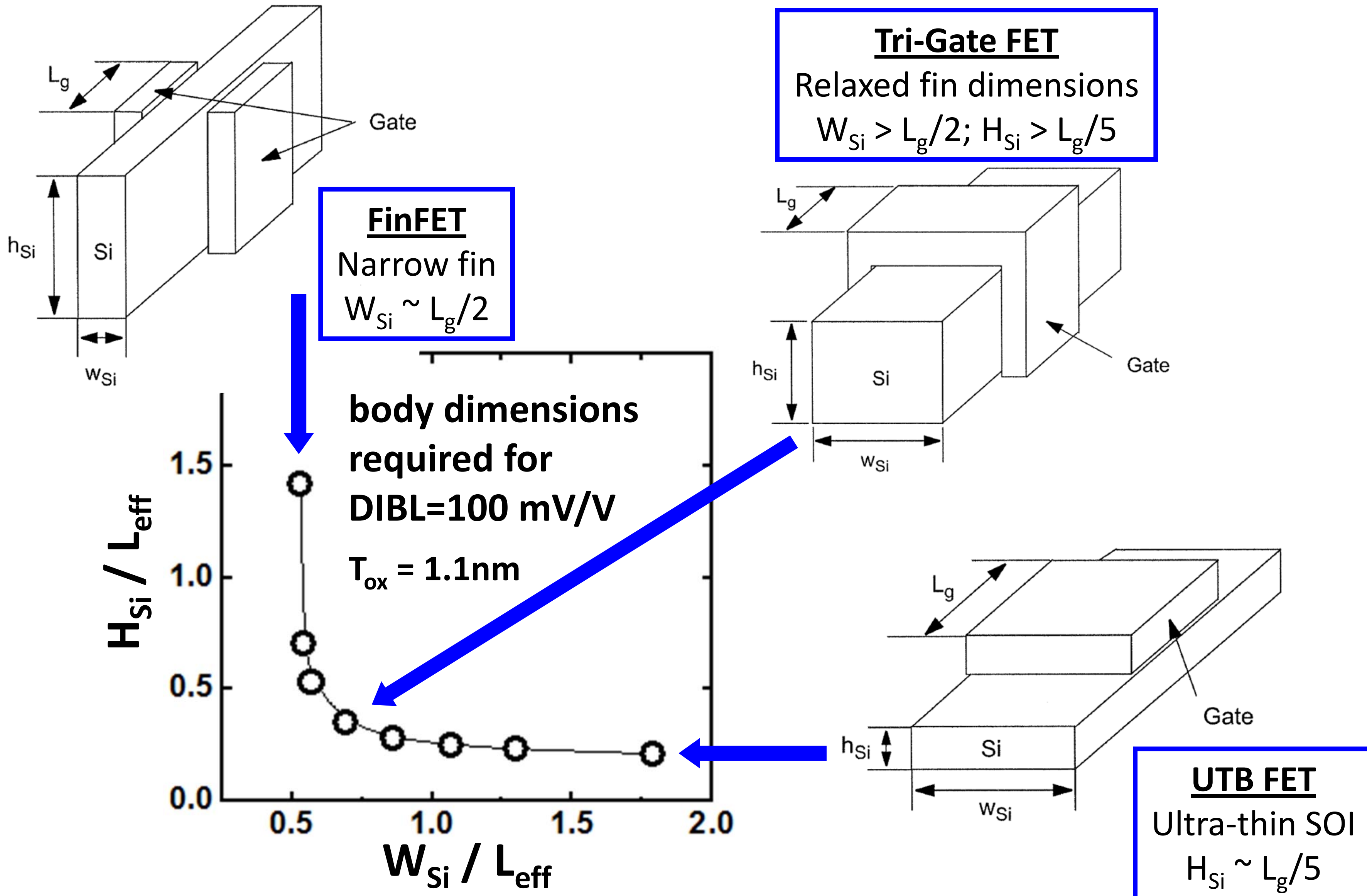




L_g = 60 nm
W_{fin} = 55 nm
H_{fin} = 36 nm

B. Doyle *et al.* (Intel), *IEEE Electron Device Letters*, Vol. 24, pp. 263-265, 2003

SOI Multi-Gate MOSFET Designs

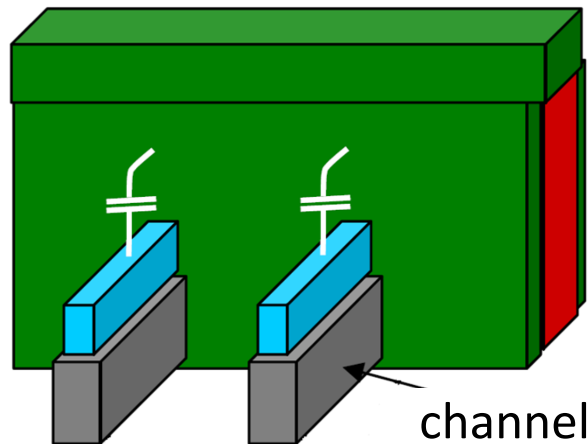


after Yang and Fossum, *IEEE Trans. Electron Devices*, Vol. 52, pp. 1159-1164, 2005

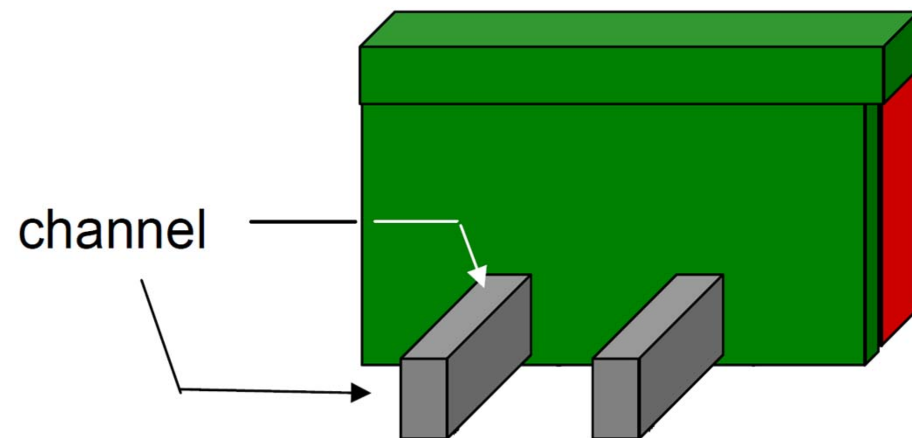
Double-Gate *vs.* Tri-Gate FET

- **The Double-Gate FET does not require a highly selective gate etch, due to the protective dielectric hard mask.**
- **Additional gate fringing capacitance is less of an issue for the Tri-Gate FET, since the top fin surface contributes to current conduction in the ON state.**

Double-Gate FET

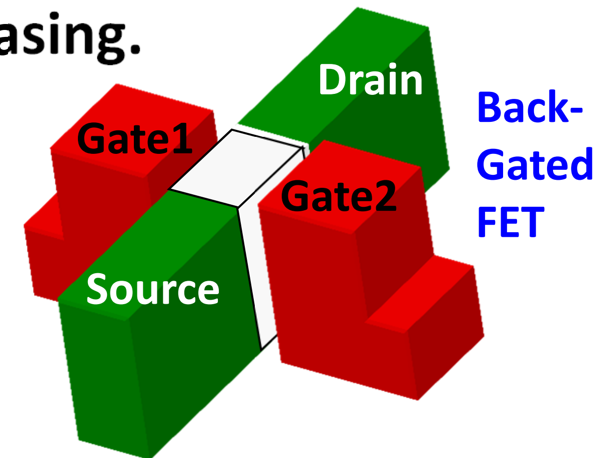


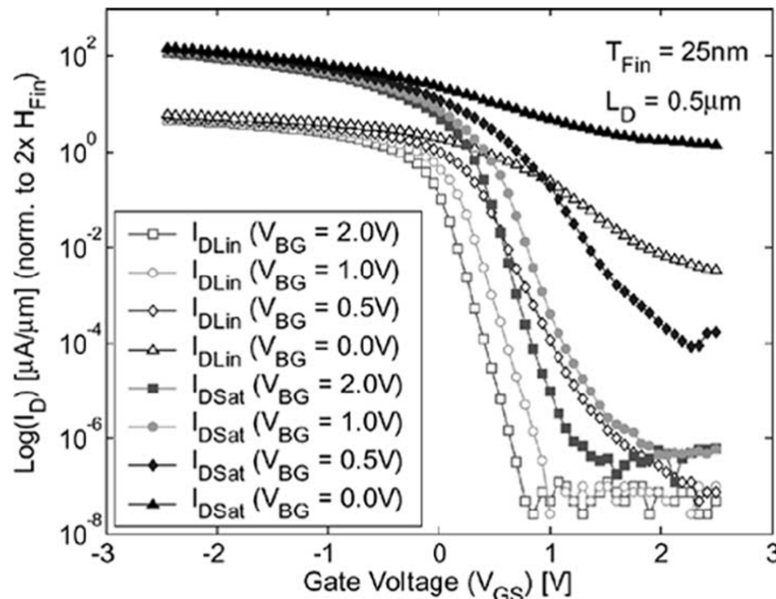
Tri-Gate FET



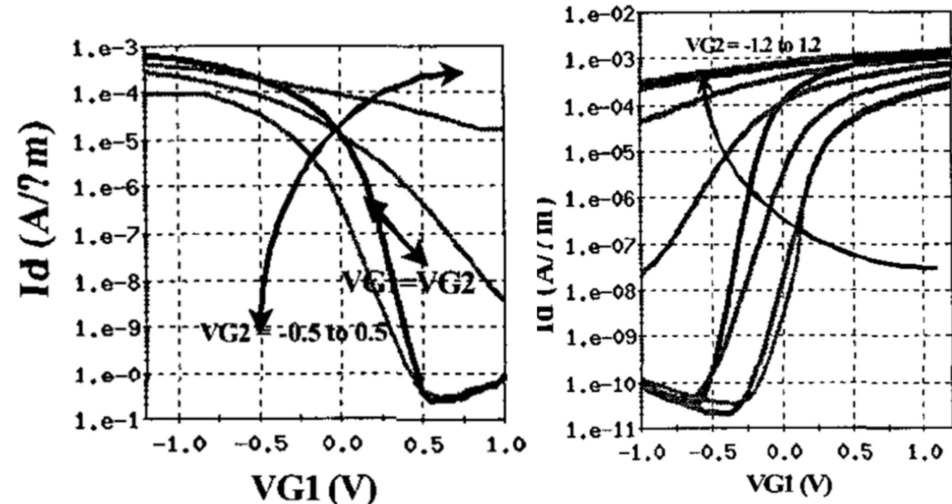
Independent Gate Operation

- The gate electrodes of a double-gate FET can be isolated by a masked etch, to allow for separate biasing.
  - One gate is used for switching.
  - The other gate is used for V_{TH} control.





D. M. Fried *et al*. (Cornell U.), *IEEE Electron Device Letters*, Vol. 25, *pp*. 199-201, 2004



L. Mathew *et al.* (Freescale Semiconductor), *2004 IEEE International SOI Conference*

Bulk FinFET

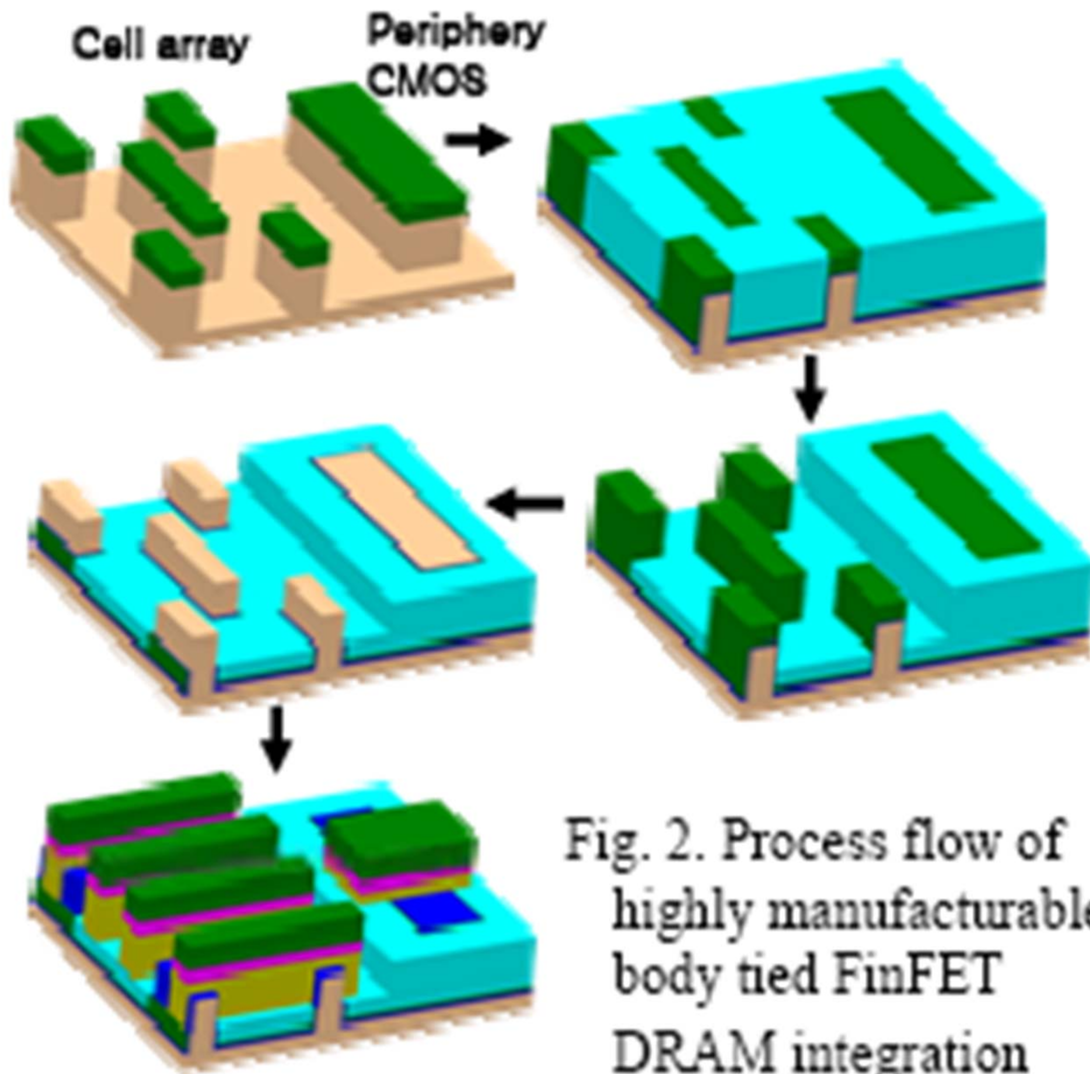


Fig. 2. Process flow of highly manufacturable body tied FinFET DRAM integration

- FinFETs can be made on bulk-Si wafers
  - ✓ lower cost
  - ✓ improved thermal conduction

  with super-steep retrograde well (SSRW) or "punch-through stopper" at the base of the fins

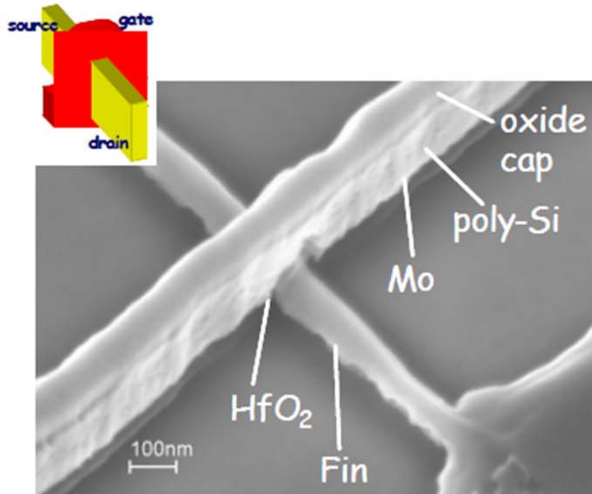
- 90 nm L_g FinFETs demonstrated
  - W_{fin} = 80 nm
  - H_{fin} = 100 nm

  DIBL = 25 mV

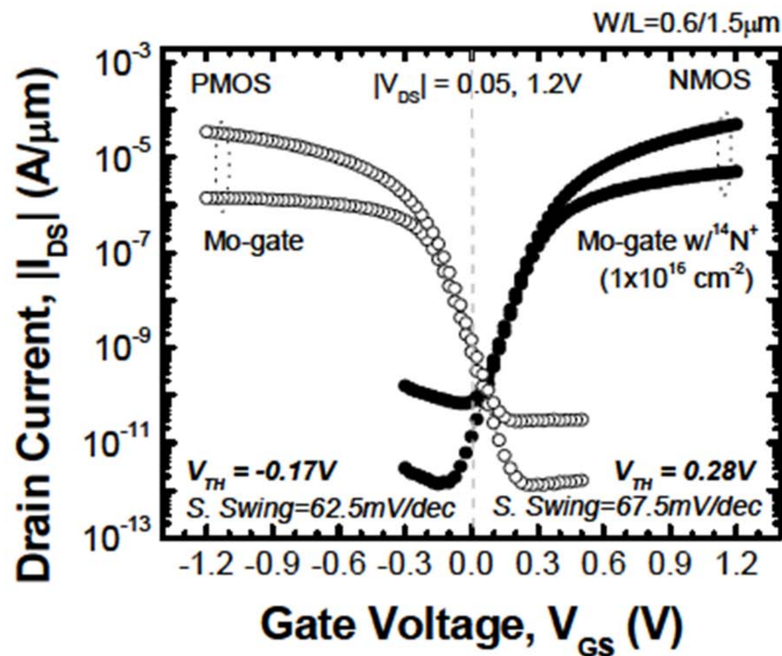
Bulk *vs.* SOI FinFET

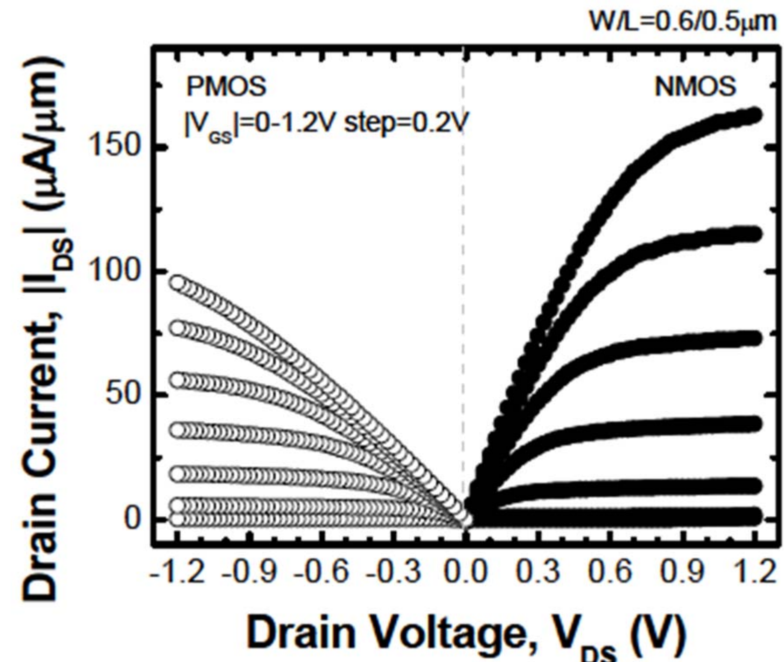
Item	Comment	Bulk FINFET (compared to SOI FinFET)
Density	Well Contact	-
Parasitic Cap	Impact of PTS	-
Performance/ Variability	Performance tradeoff to overcome variability	- -
Leakage & HVT capability	Impact of PTS implant in bulk FIN	-
Non FIN structure compatibility (passives, etc)		+
s/d stressor	eSiGe, eSiC	++
Gate stressor, liner stressor		**Similar**
Channel stressor	SiGe pFET; SSOI Si nFET, III-V nFET	+/-
SRAM Vt Variation		- -

2004: High-k/Metal Gate FinFET



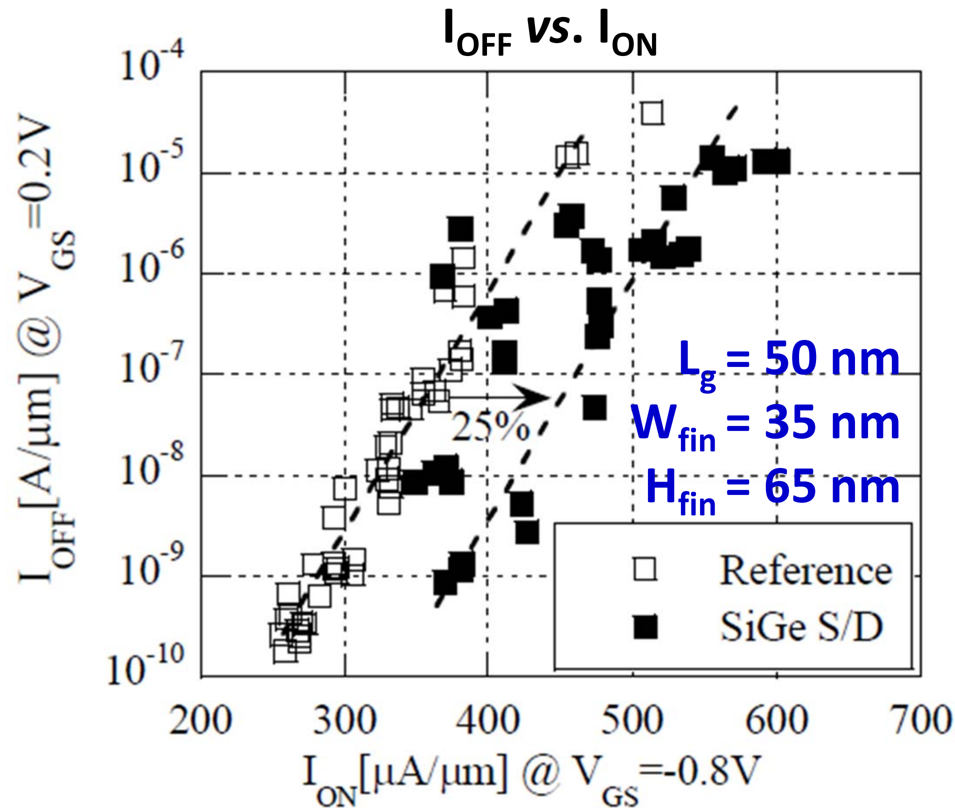
D. Ha, H. Takeuchi, Y.-K. Choi, T.-J. King, W. Bai, D.-L. Kwong, A. Agarwal, and M. Ameen, "Molybdenum-gate HfO_2 CMOS FinFET technology," *IEEE International Electron Devices Meeting Technical Digest*, pp. 643-646, 2004





I_{DSAT} Boost with Embedded-SiGe S/D

Process flow:

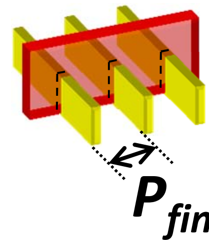


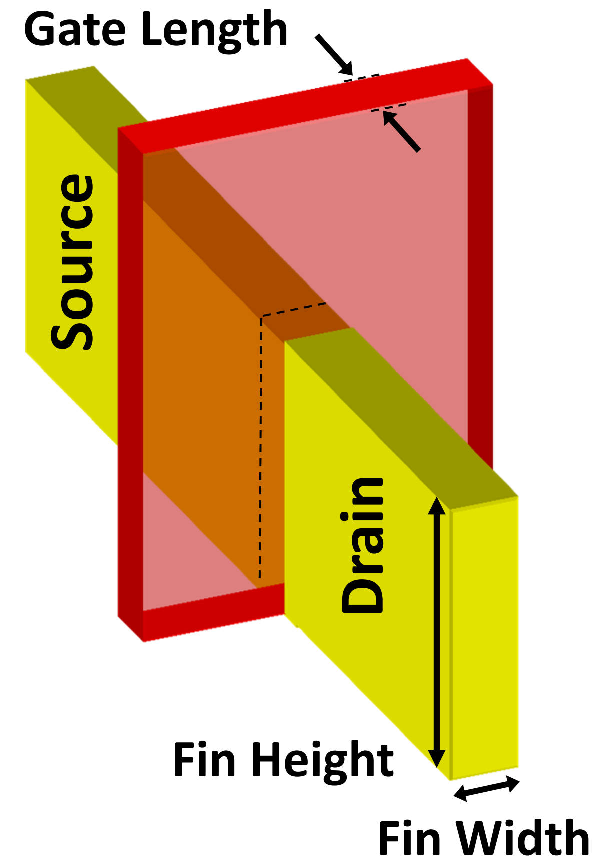
- **25% improvement in I_{DSAT} is achieved with silicon-germanium source/drain, due in part to reduced parasitic resistance**

P. Verheyen *et al.* (IMEC), *Symposium on VLSI Technology Digest*, pp. 194-195, 2005

Fin Design Considerations

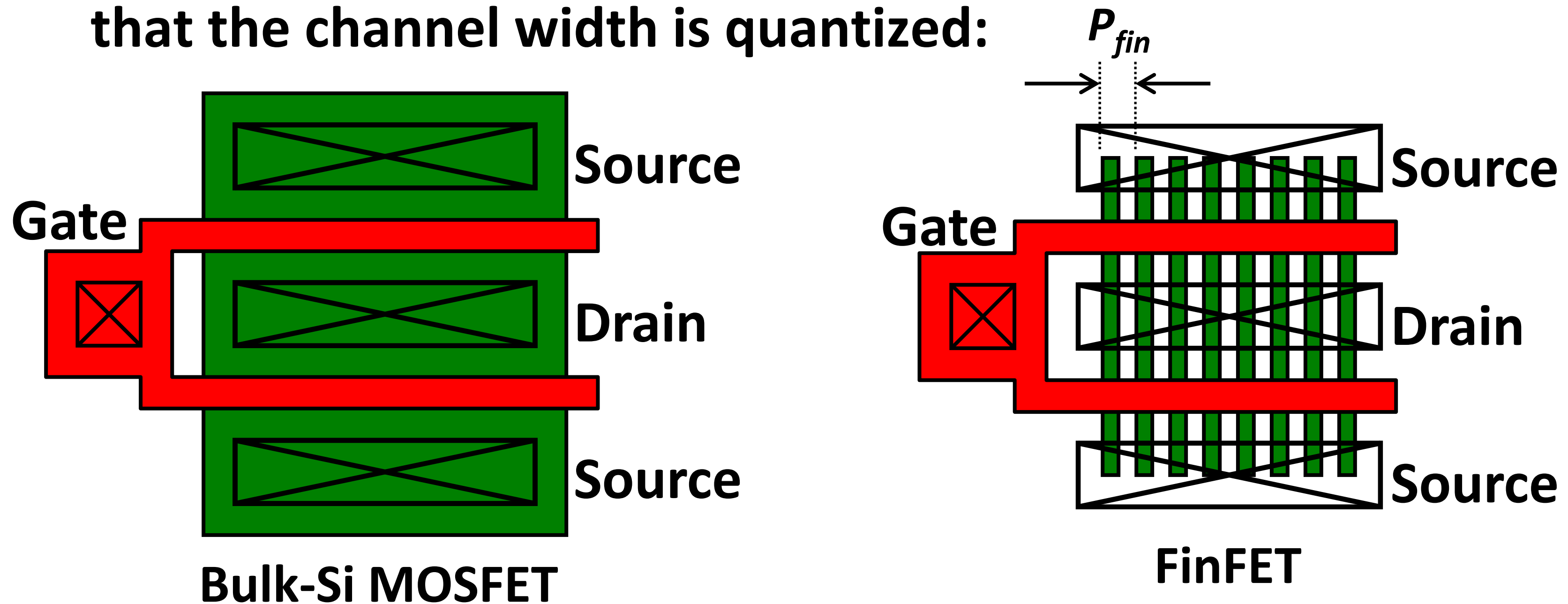
- **Fin Width**
  - Determines DIBL
- **Fin Height**
  - Limited by etch technology
  - Tradeoff: layout efficiency *vs.* design flexibility
- **Fin Pitch**
  - Determines layout area
  - Limits S/D implant tilt angle
  - Tradeoff: performance *vs.* layout efficiency





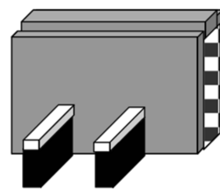
FinFET Layout

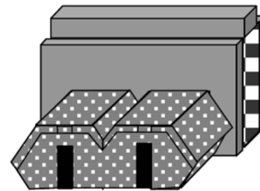
- Layout is similar to that of conventional MOSFET, except that the channel width is quantized:



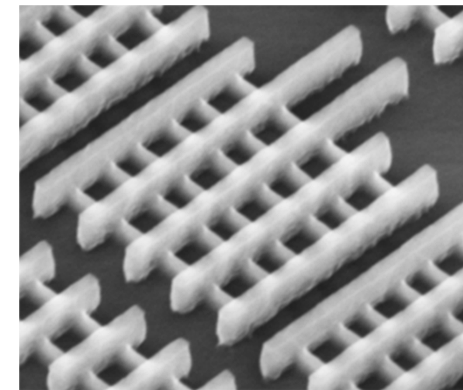
The S/D fins can be merged by selective epitaxy:

Poly Si
SOI
Epi Si
SiN
Silicide
SiO2



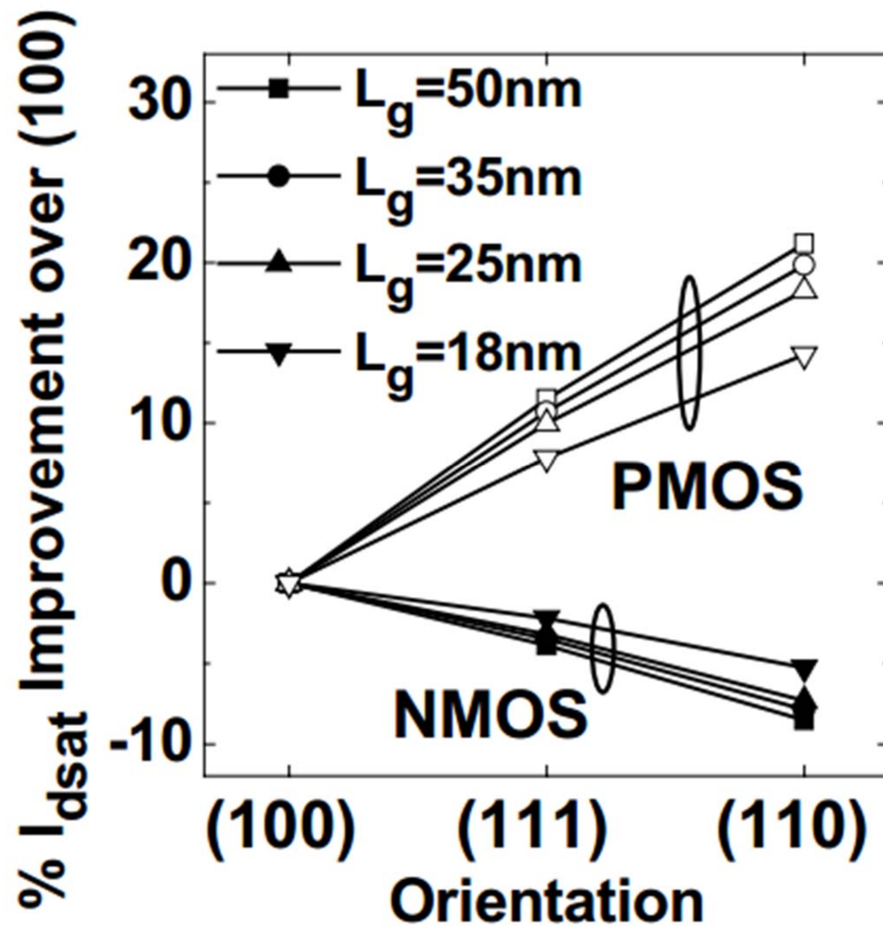


M. Guillorn *et al*. (IBM), *Symp. VLSI Technology* 2008

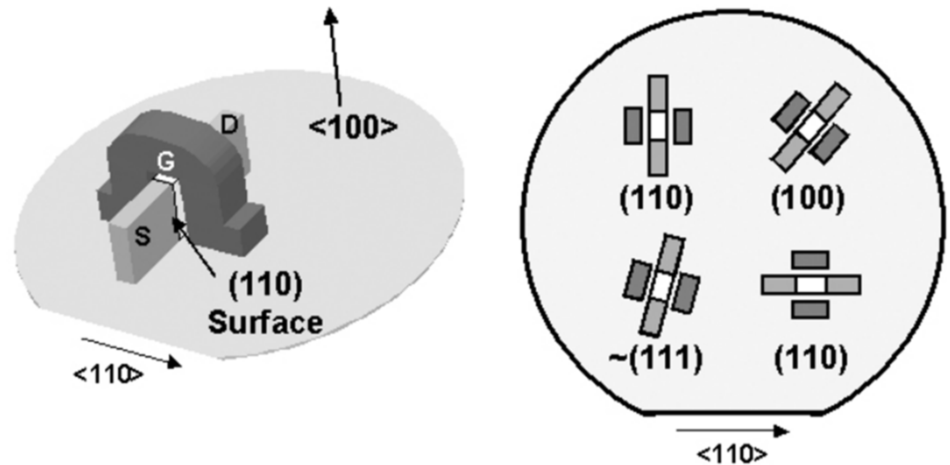


Intel Corp.

Impact of Fin Layout Orientation



(Series resistance is more significant at shorter L_g.)

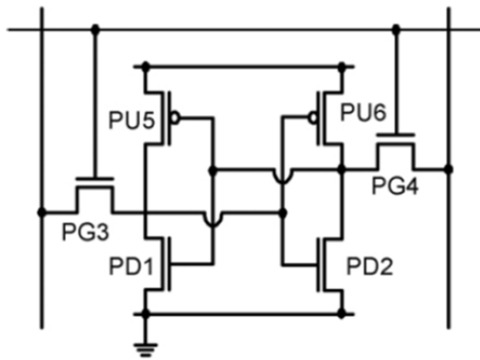


- If the fin is oriented || or ⊥ to the wafer flat, the channel surfaces lie along (110) planes.
  - lower electron mobility
  - higher hole mobility
- If the fin is oriented 45° to the wafer flat, the channel surfaces lie along (100) planes.

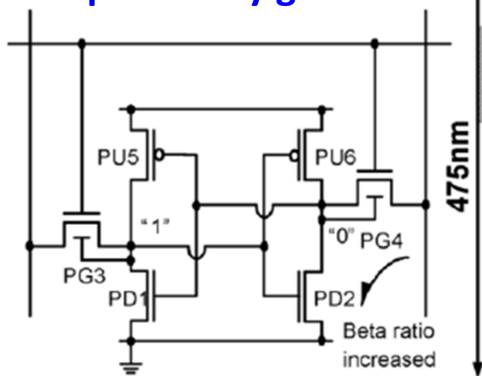
FinFET-Based SRAM Design

__Best Paper Award__: Z. Guo, S. Balasubramanian, R. Zlatanovici, T.-J. King, and B. Nikolic, "FinFET-based SRAM design," *Int'l Symposium on Low Power Electronics and Design*, pp. 2-7, 2005

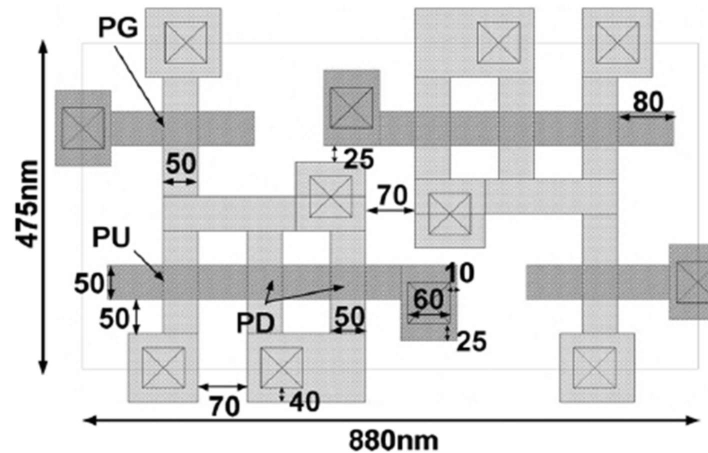
__6-T SRAM Cell Designs__

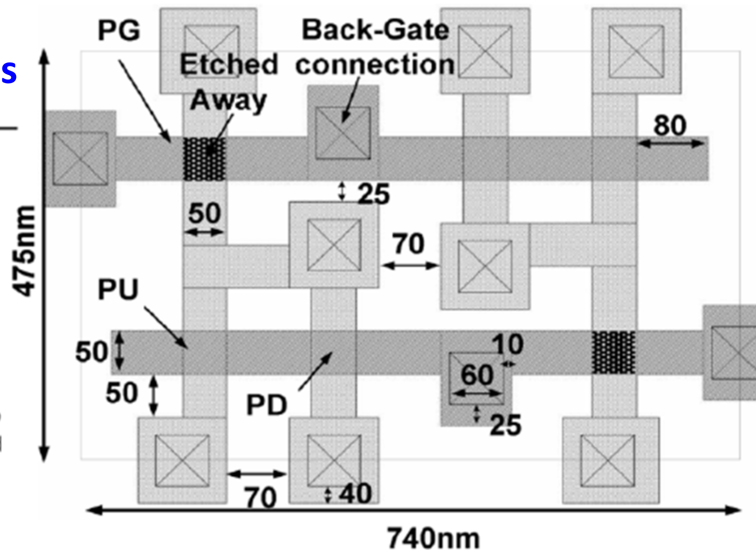


Reduced cell area with independently gated PGs

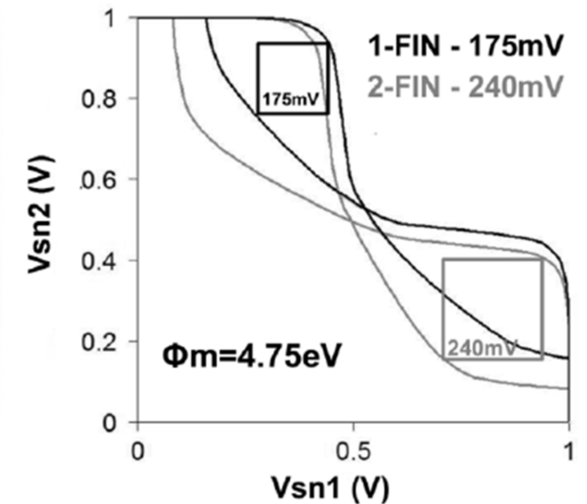


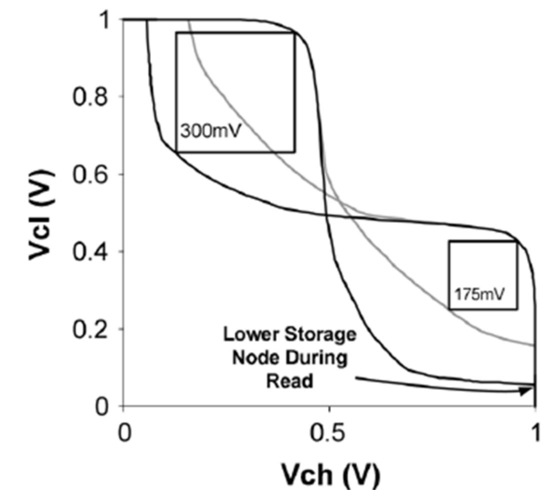
__Cell Layouts__





__Butterfly Curves__

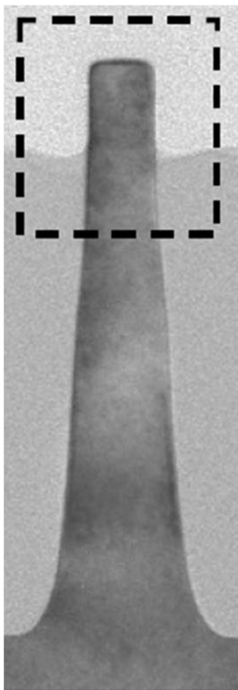




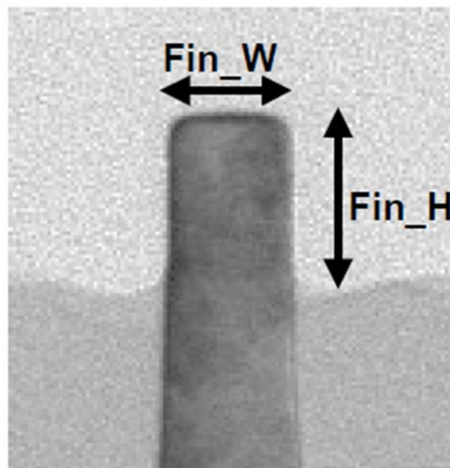
State-of-the-Art FinFETs

22nm/20nm high-performance CMOS technology

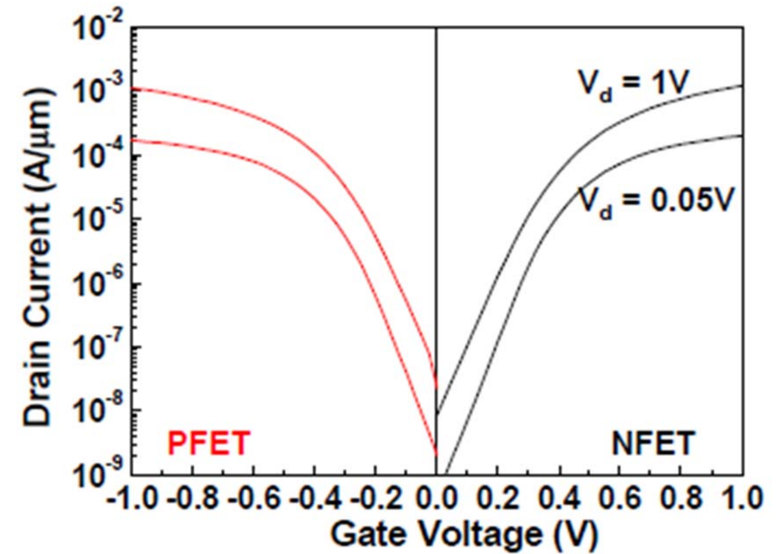
- L_g = 25 nm

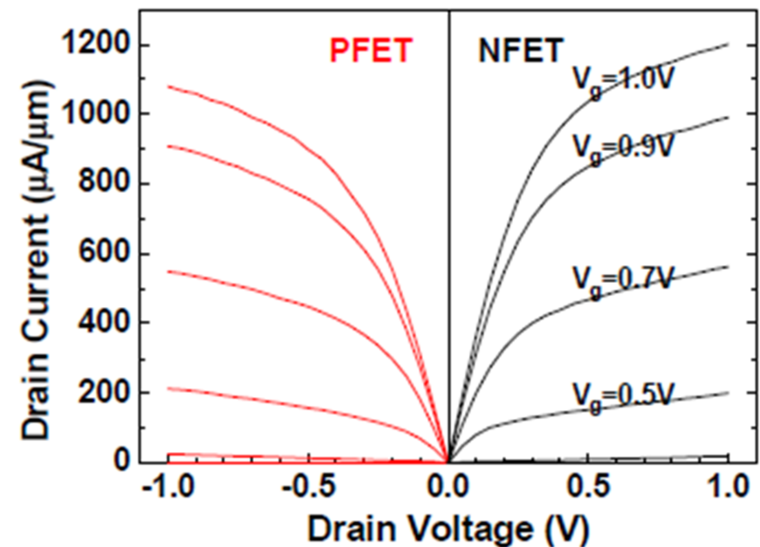


XTEM Images of Fin



Weff = 2 x Fin_H + Fin_W

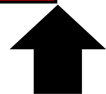




Looking to the Future…

2010 International Technology Roadmap for Semiconductors (ITRS)

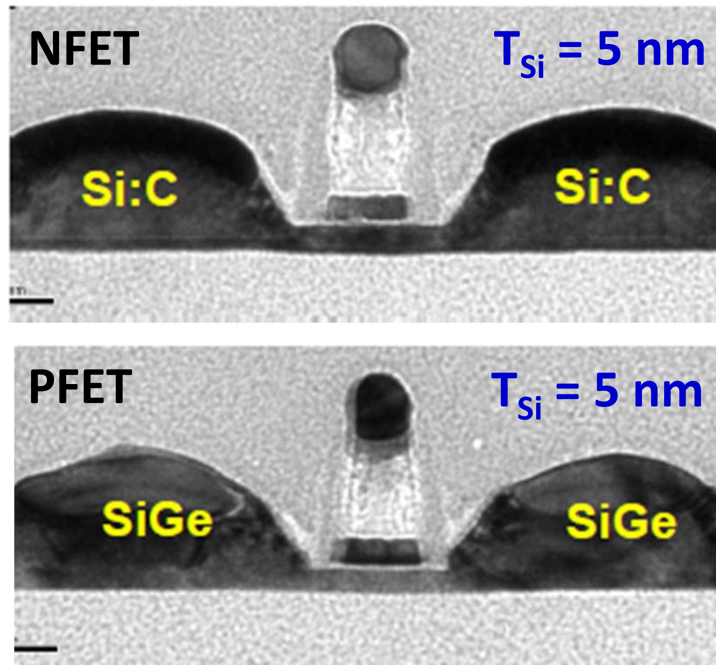
	2012	2014	2016	2018	2020	2022	2024
Gate Length	24 nm	18 nm	15 nm	13 nm	11 nm	10 nm	7 nm
Gate Oxide Thickness, T_{OX} (nm)							
Drive Current, I_{DSAT}							



End of Roadmap
(always ~15 yrs away!)

FinFET *vs.* UTBB SOI MOSFET

Cross-sectional TEM views of 25 nm UTB SOI devices



K. Cheng *et al.* (IBM), *Symposium on VLSI Technology Digest*, pp. 128-129, 2011

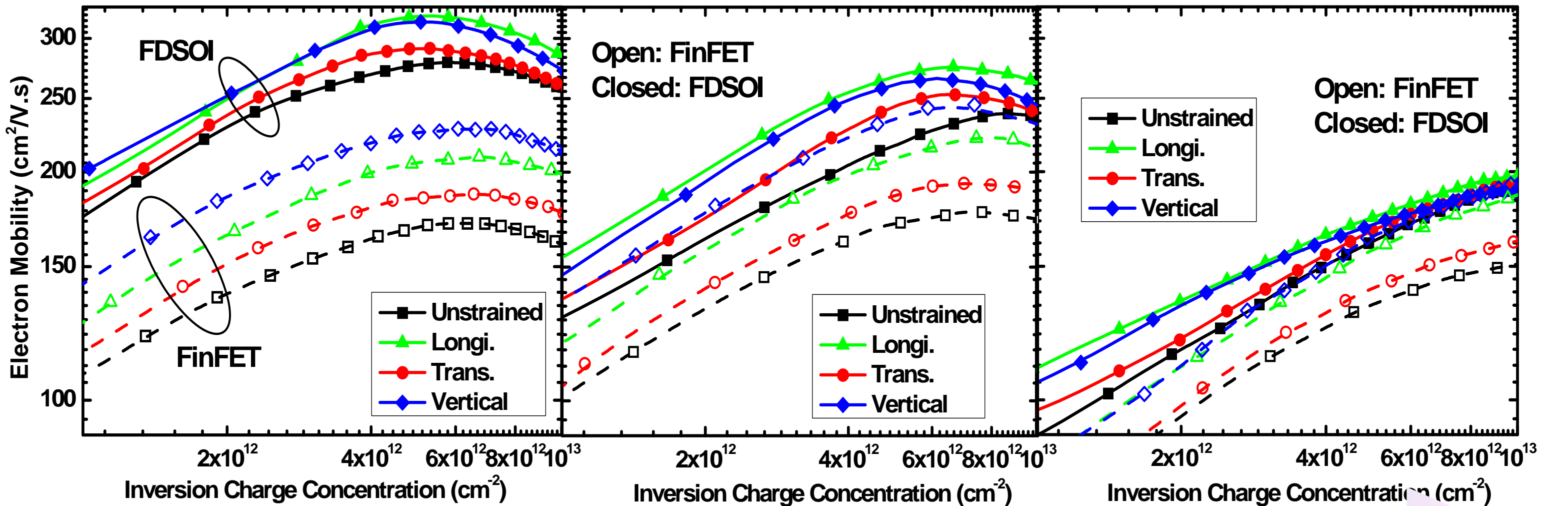
	20nm ETSOI	22nm Bulk finFET*
L_G (nm)	22	> 25
Pitch (nm)	80-100	100
I_{OFF} (nA/ µm)	1	1
NFET I_{on} (µA/µm)	920	960
PFET I_{on} (µA/µm)	880	850

B. Doris (IBM), *2011 IEEE International SOI Conference*

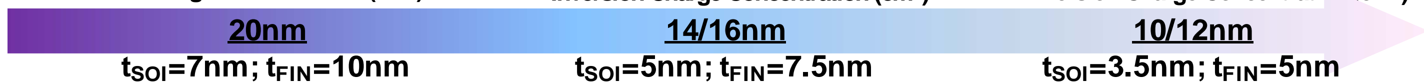
*C.C. Wu *et al.* (TSMC), *IEDM* 2010

Projections for FinFET *vs.* UTBB SOI MOSFETs

NMOS:
Electron Mobility

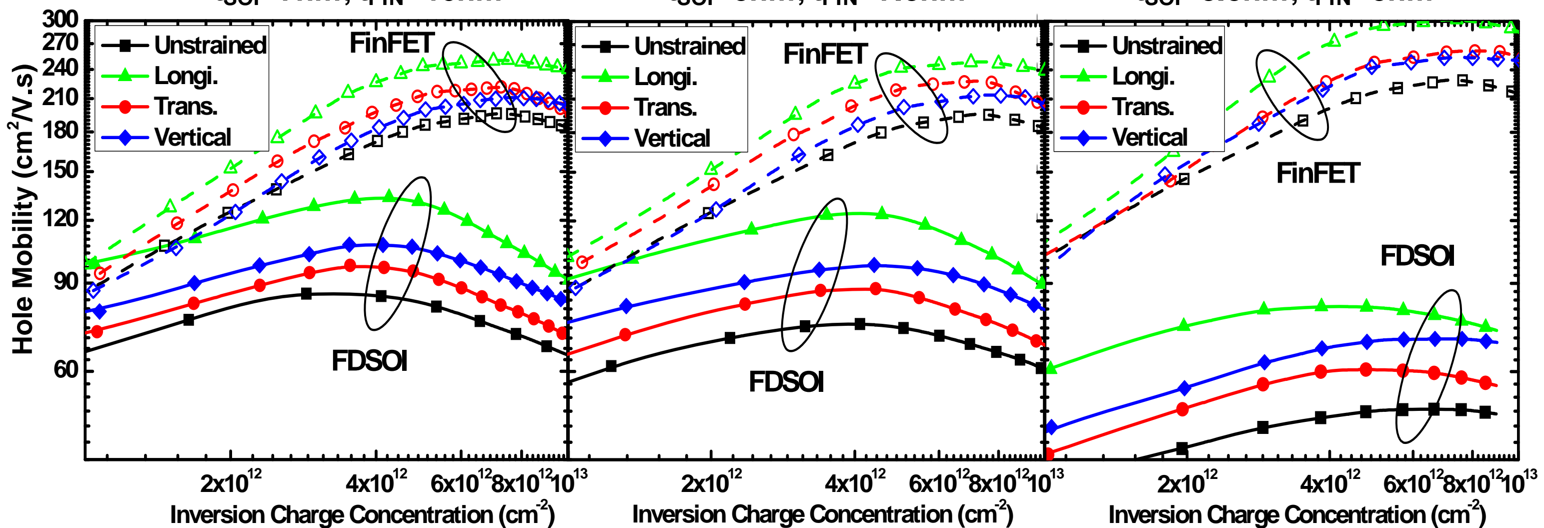


Technology Node:



t_{SOI}=7nm; t_{FIN}=10nm t_{SOI}=5nm; t_{FIN}=7.5nm t_{SOI}=3.5nm; t_{FIN}=5nm

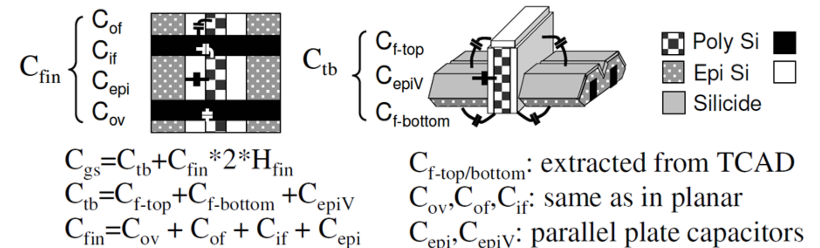
PMOS:
Hole Mobility



Remaining FinFET Challenges

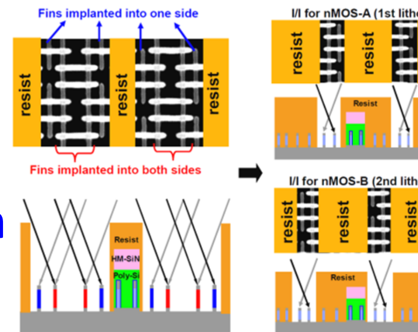
- V_{TH} adjustment
  - Requires gate work-function (WF) or L_{eff} tuning
  - Dynamic V_{TH} control is not possible for high-aspect-ratio multi-fin devices
- Fringing capacitance between gate and top/bottom of S/D
  - Mitigated by minimizing fin pitch and using via-contacted, merged S/D

    M. Guillorn, *Symp. VLSI Technology* 2008



- Parasitic resistance
  - Uniform S/D doping is difficult to achieve with conventional implantation

    H. Kawasaki, *IEDM* 2008

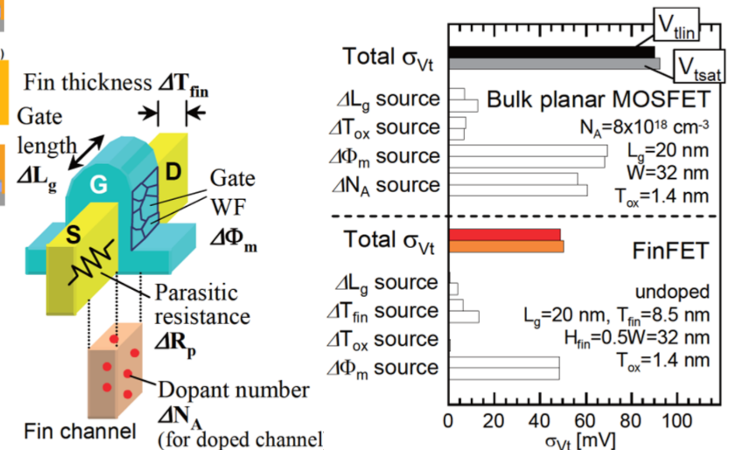


  - Conformal doping is needed

    e.g. Y. Sasaki, *IEDM* 2008

- Variability
  - Performance is very sensitive to fin width
  - WF variation dominant for undoped channel

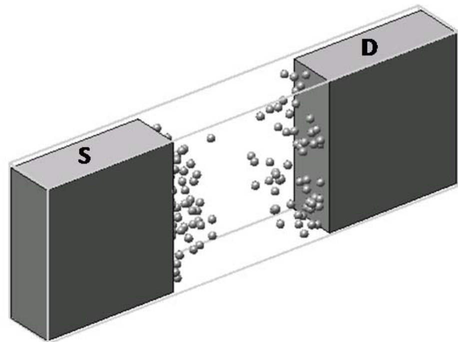
    T. Matsukawa, *Symp. VLSI Technology* 2008



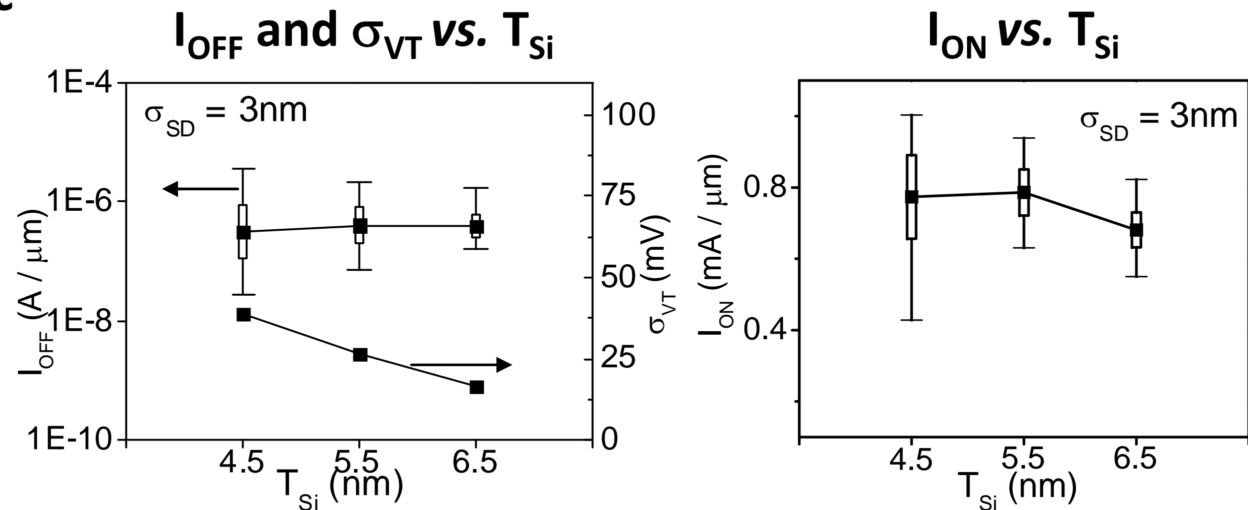
Random Dopant Fluctuation Effects

- **Channel/body doping can be eliminated to mitigate RDF effects.**
- **However, due to source/drain doping, a trade-off exists between performance & RDF tolerance for L_g < 10nm:**

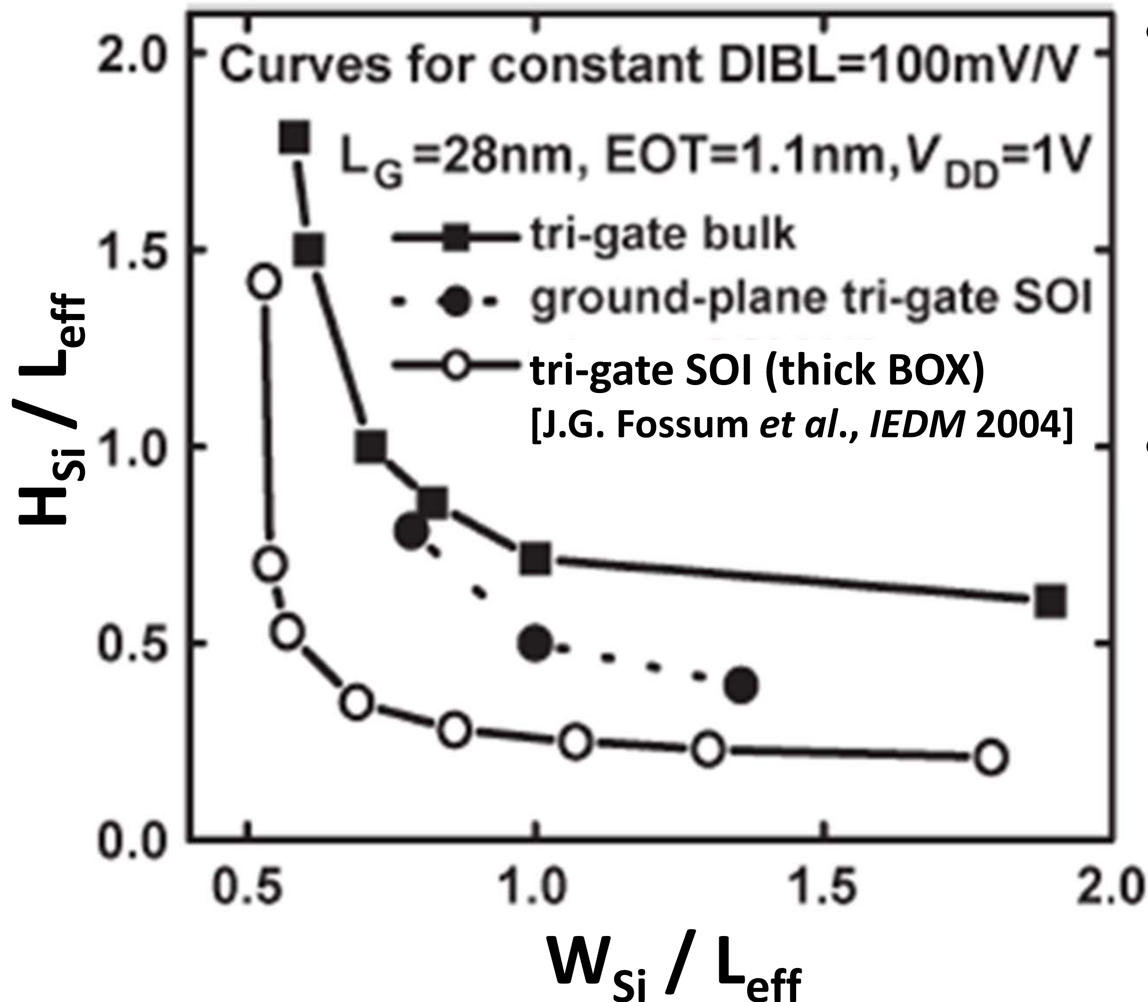
SOI FinFET w/ atomistic S/D gradient regions:



L_g = 9nm, EOT = 0.7nm



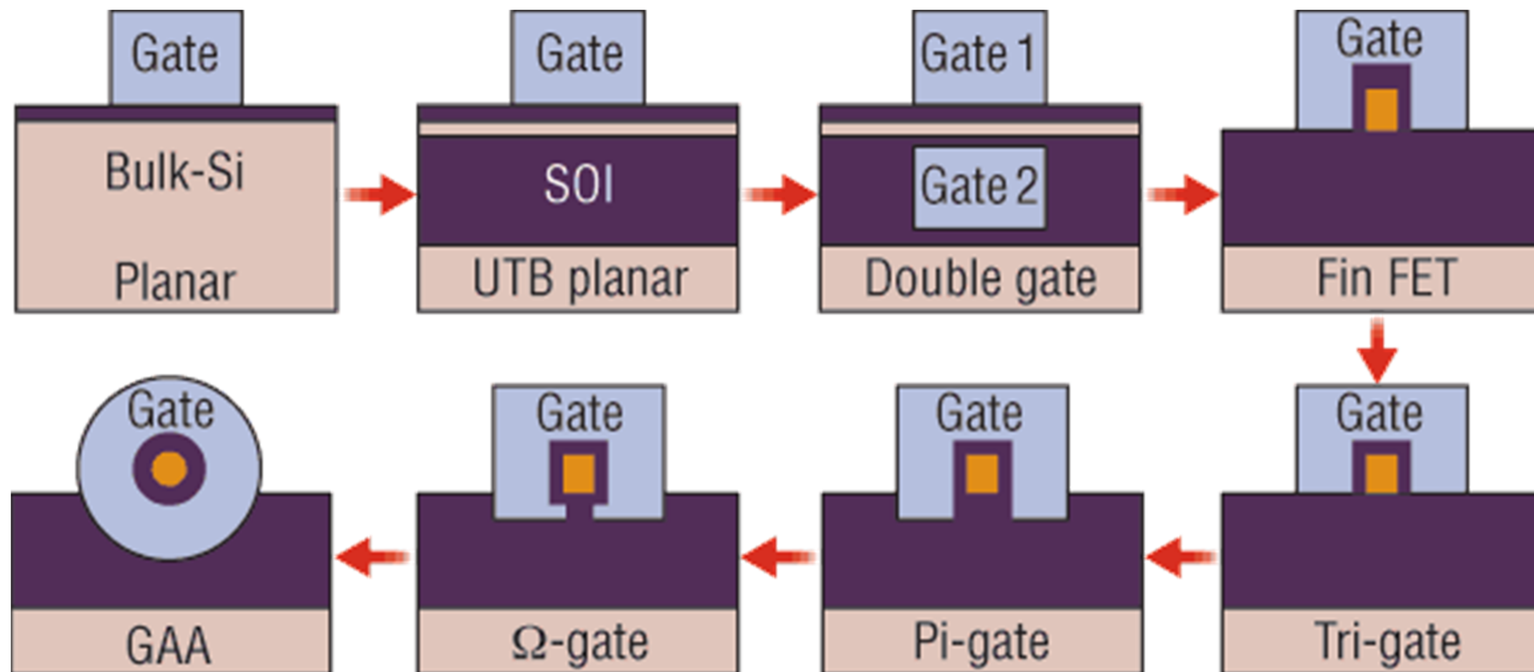
Bulk *vs*. SOI Multi-Gate FET Design



- To ease the fin width requirement, the fin height should be reduced.
- The bulk tri-gate design has the most relaxed body dimension requirements.
  - SSRW (at the base of the fin) improves electrostatic integrity

SOI MOSFET Evolution

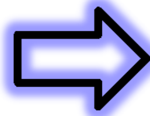
- **The Gate-All-Around (GAA) structure provides for the greatest capacitive coupling between the gate and the channel.**



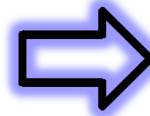
http://www.electroiq.com/content/eiq-2/en/articles/sst/print/volume-51/issue-5/features/nanotechnology/fully-gate-all-around-silicon-nanowire-cmos-devices.html

Scaling to the End of the Roadmap

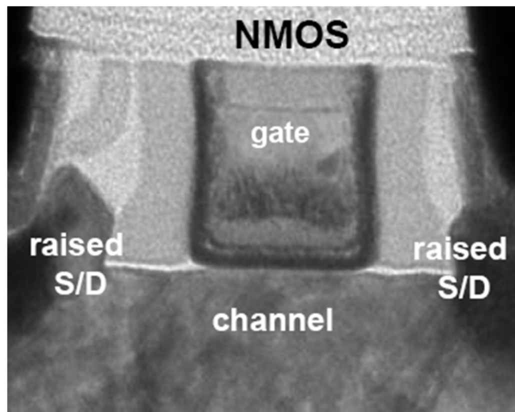
32 nm
planar

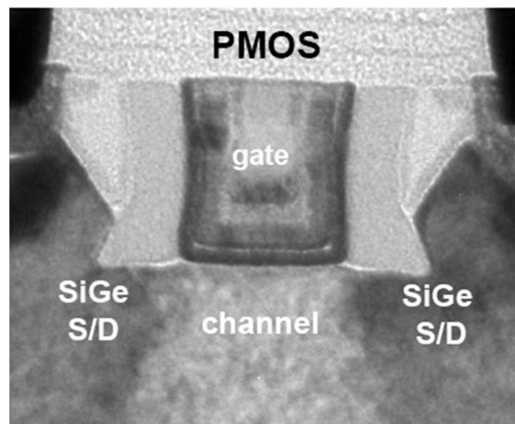


22 nm
multi-gate
segmented channel



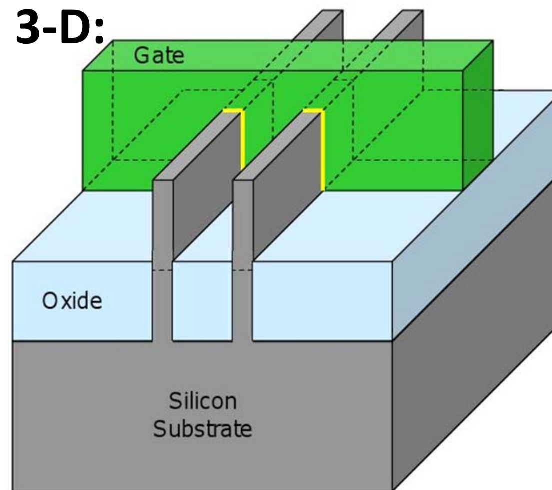
beyond 10 nm
stacked nanowires





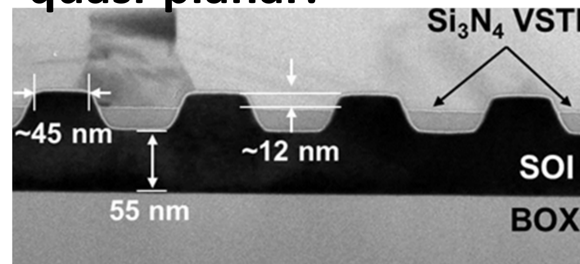
P. Packan *et al*. (Intel), *IEDM* 2009

3-D:

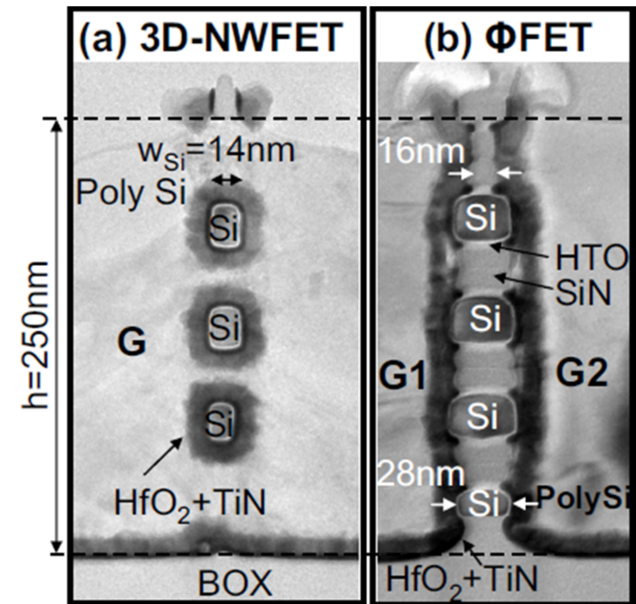


Intel Corp.

quasi-planar:



B. Ho (UCB), *ISDRS* 2011



C. Dupré *et al*. (CEA-LETI) *IEDM* 2008

Stacked gate-all-around (GAA) FETs achieve the highest layout efficiency.

Summary

- **The FinFET was originally developed for manufacture of self-aligned double-gate MOSFETs, to address the need for improved gate control to suppress I_{OFF}, DIBL and process-induced variability for L_g < 25nm.**
  - **Tri-Gate and Bulk variations of the FinFET have been developed to improve manufacturability and cost.**
  - **It has taken ~10 years to bring “3-D” transistors into volume production.**
- **Multi-gate MOSFETs provide a pathway to achieving lower power and/or improved performance.**
  - **Further evolution of the MOSFET to a stacked-channel structure may occur by the end of the roadmap.**

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- **UC Berkeley Microfabrication Laboratory**
  (birthplace of the FinFET)