Bulk CMOS Scaling to the End of the Roadmap

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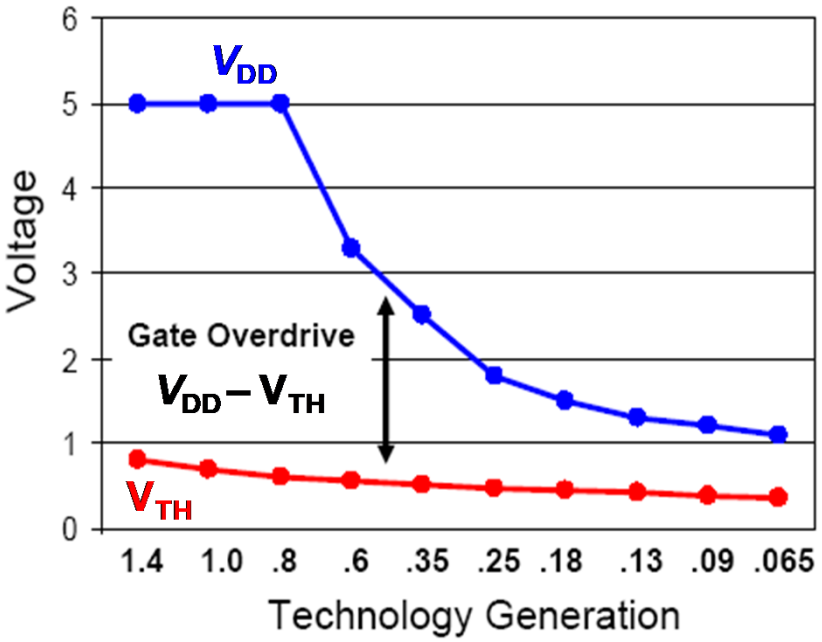
Symposium on VLSI Circuits Short Course

The CMOS Power Crisis

- As transistor density has increased, the supply voltage (V_{DD}) has not decreased proportionately.

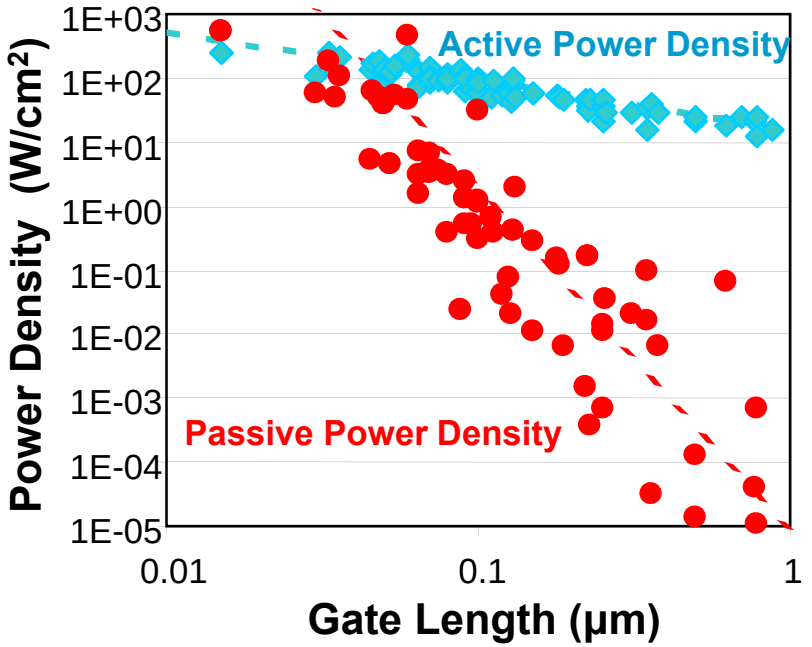
  → Power density now constrains CMOS chip design!

CMOS Voltage Scaling



Source: P. Packan (Intel), 2007 IEDM Short Course

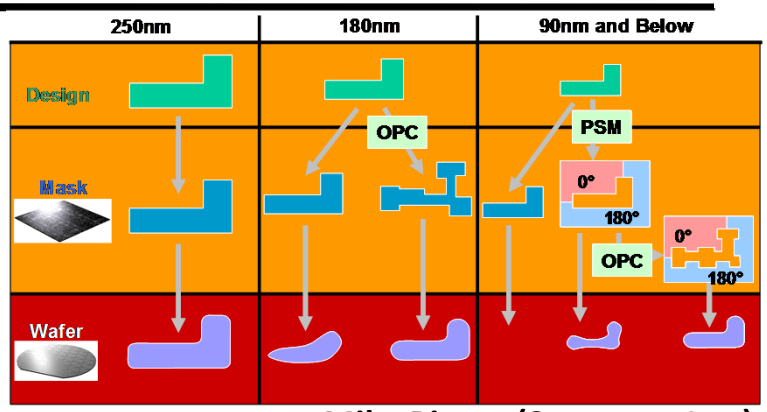
Power Density vs. Gate Length



Source: B. Meyerson (IBM) Semico Conf., January 2004

Sources of Variability

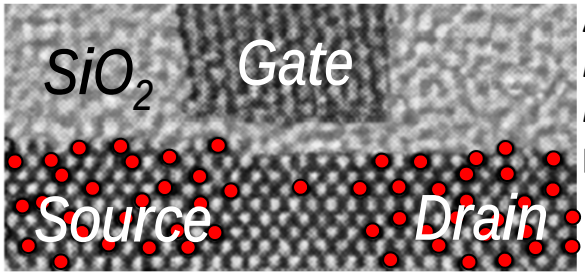
- **Sub-wavelength lithography:**
  - **Resolution enhancement techniques are costly and increase process sensitivity**



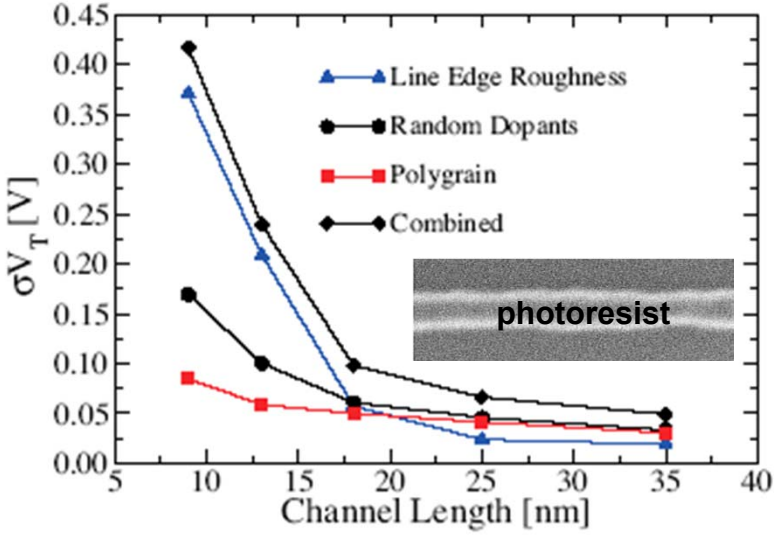
courtesy Mike Rieger (Synopsys, Inc.)

- **Layout-dependent transistor performance:**
  - **Process-induced stress is dependent on layout**

- **Random dopant fluctuations (RDF):**
  - **Atomistic effects become significant in nanoscale FETs**

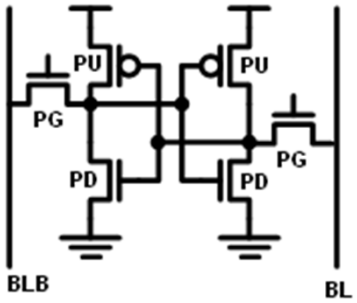


A. Brown *et al.*, *IEEE Trans. Nanotechnology*, p. 195, 2002



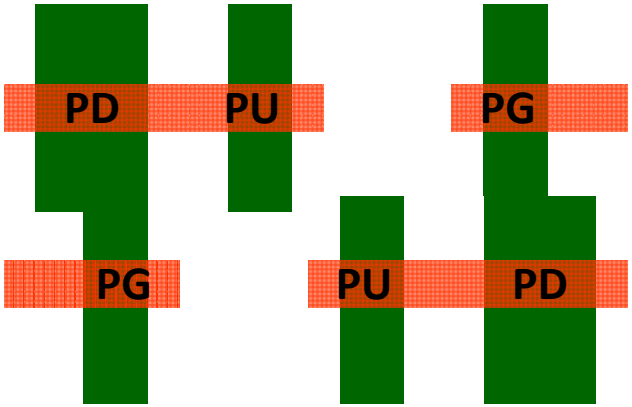
A. Asenov, *Symp. VLSI Tech. Dig.*, p. 86, 2007

6-T SRAM Cell

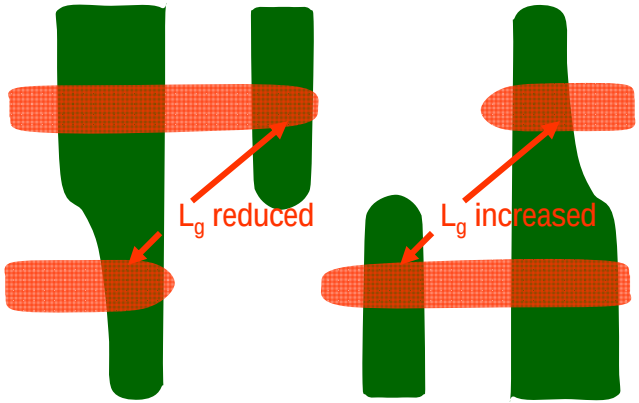


Impact of Misalignment

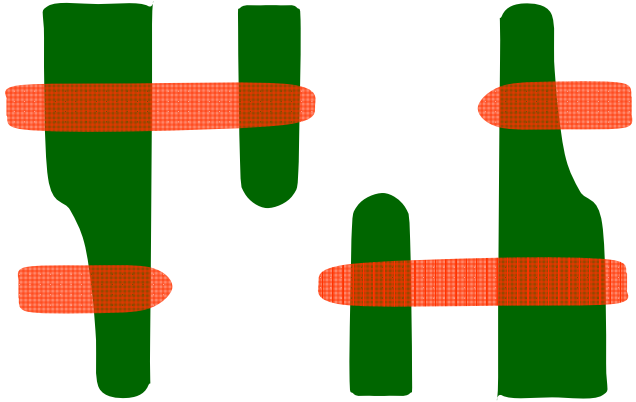
Desired layout
(6-T SRAM cell)



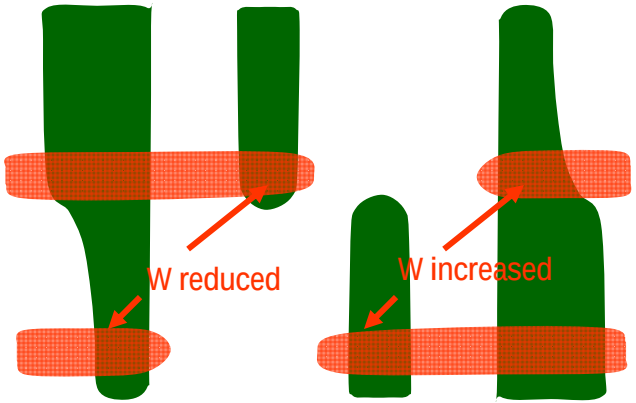
Actual layout w/ lateral misalignment
(gate length variations)



Actual layout
(corner rounding)

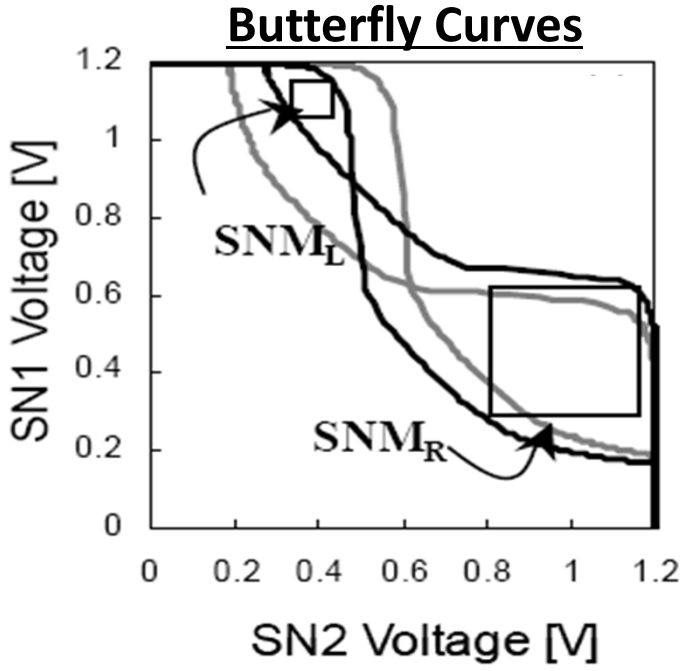


Actual layout w/ vertical misalignment
(channel width variations due to active jogs)



Impact of Variability on SRAM

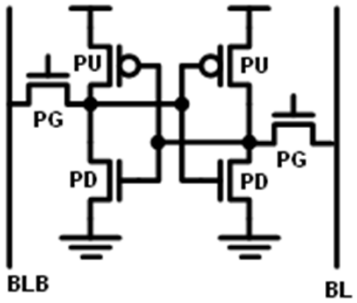
- V_{TH} mismatch results in reduced static noise margin.
  → lowers cell yield, and limits V_{DD} scaling



Y. Tsukamoto (Renesas) *et al.*, *Proc. IEEE/ACM ICCAD*, p. 398, 2005

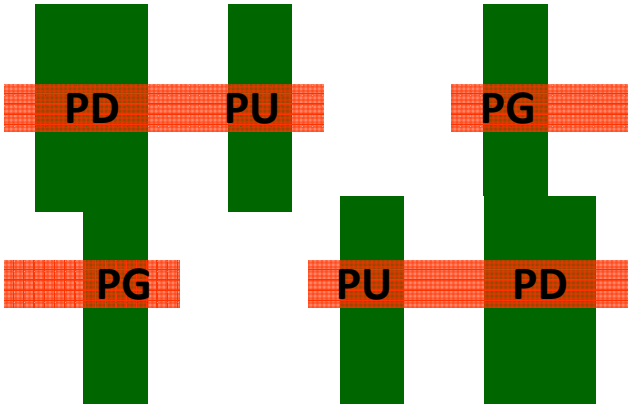
→ Immunity to short-channel effects (SCE) and narrow-width effects as well as RDF effects is needed to achieve high SRAM cell yield.

6-T SRAM Cell

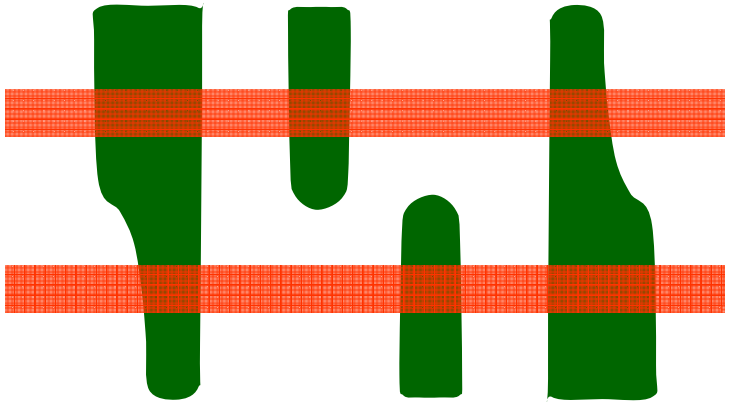


Double Patterning of Gate

Desired layout
(6-T SRAM cell)

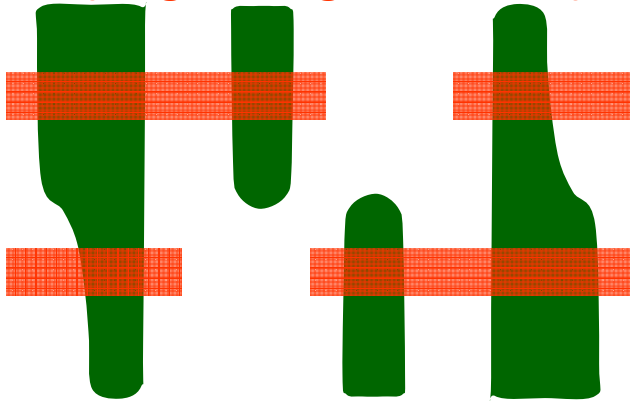


Actual layout after 1st gate patterning



Actual layout after active patterning

Actual layout after 2nd gate patterning
(no gate length variation)

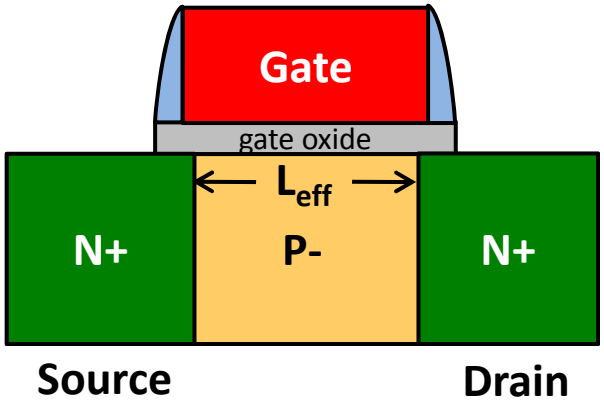


Outline

- Review: MOSFET Basics
- The Road Behind: CMOS Technology Advancement
- The Narrow Road Ahead: Thin-Body MOSFETs
- An Alternative Route: Planar Bulk MOSFET Evolution
- Summary

MOSFET Operation: Gate Control

Schematic Cross Section

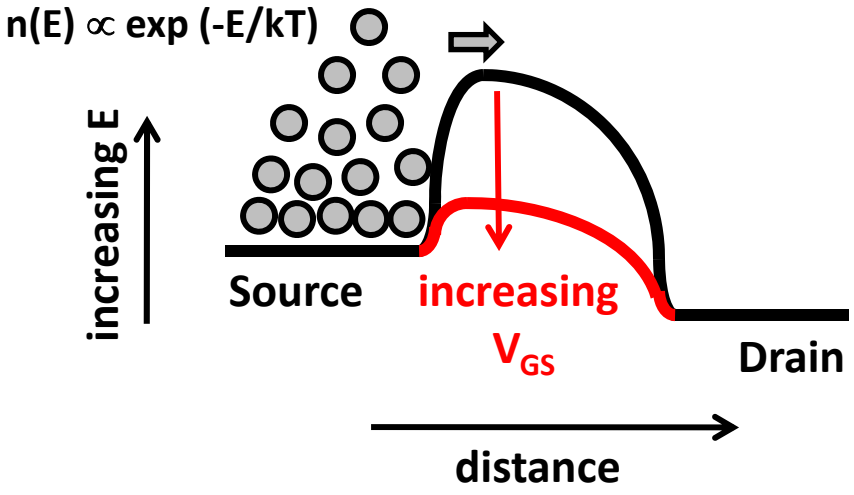


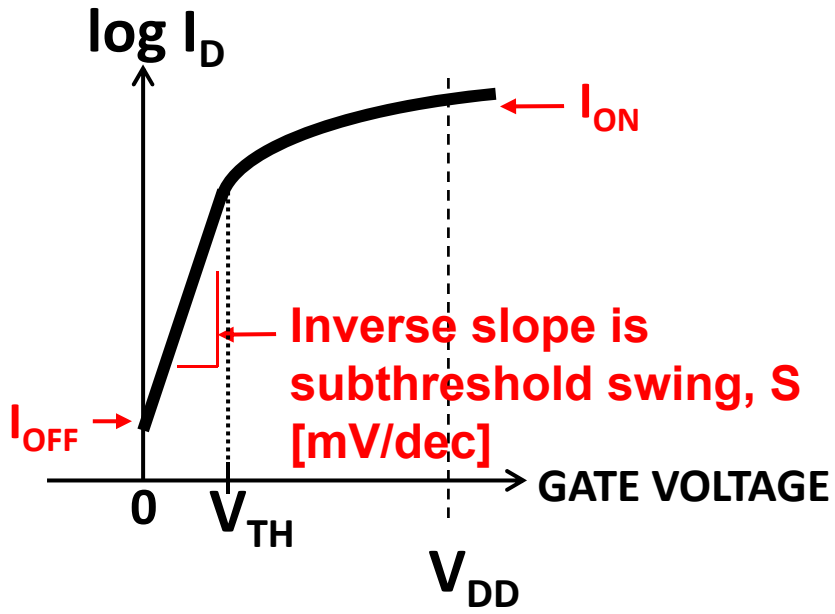
Current flowing between Source and Drain is controlled by the Gate voltage.

Desired characteristics:

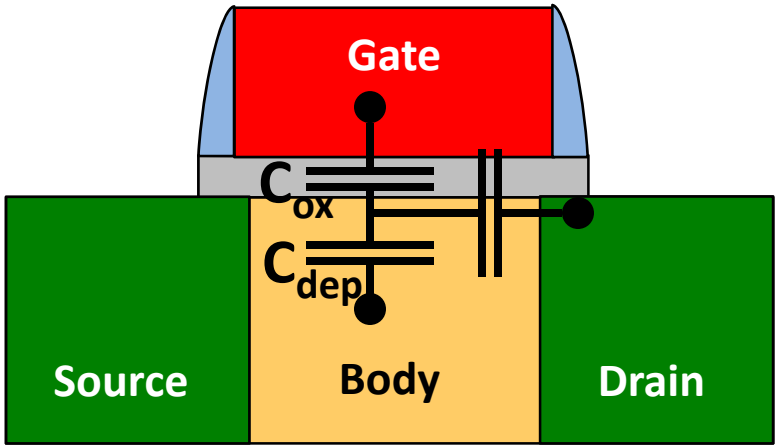
- High ON current
- Low OFF current

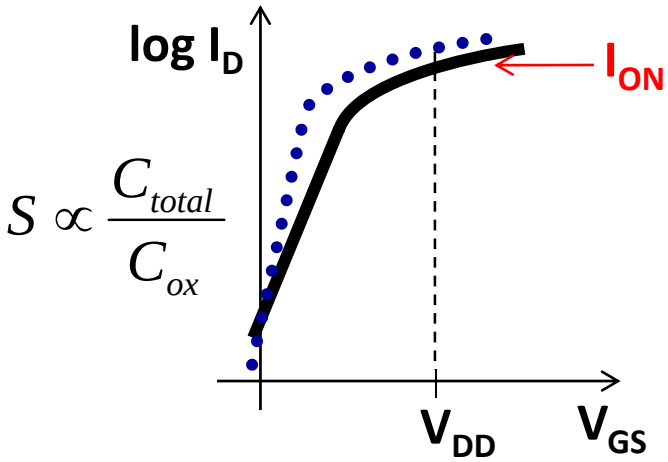
Electron Energy Band Profile





Improving I_{ON}/I_{OFF}

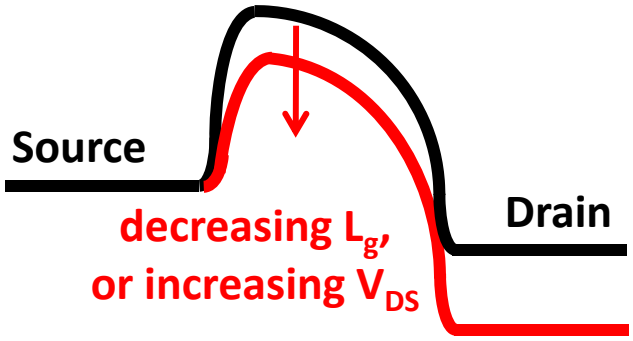


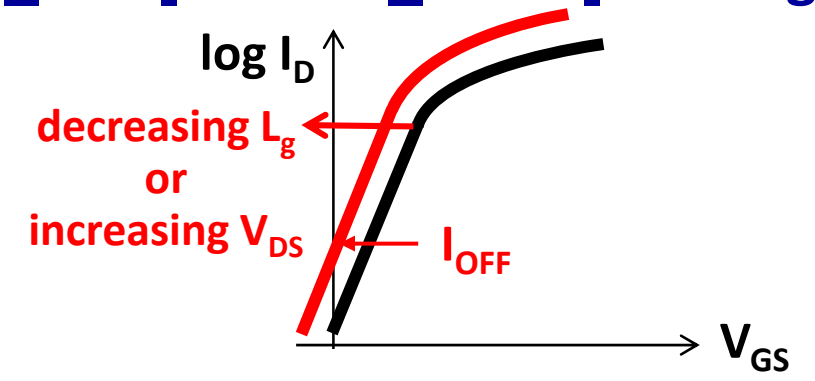


- **The greater the capacitive coupling between Gate and channel, the better control the Gate has over the channel potential.**

  →higher I_{ON}/I_{OFF} for fixed V_{DD}, or lower V_{DD} to achieve target I_{ON}/I_{OFF}

  →reduced short-channel effect and drain-induced barrier lowering:

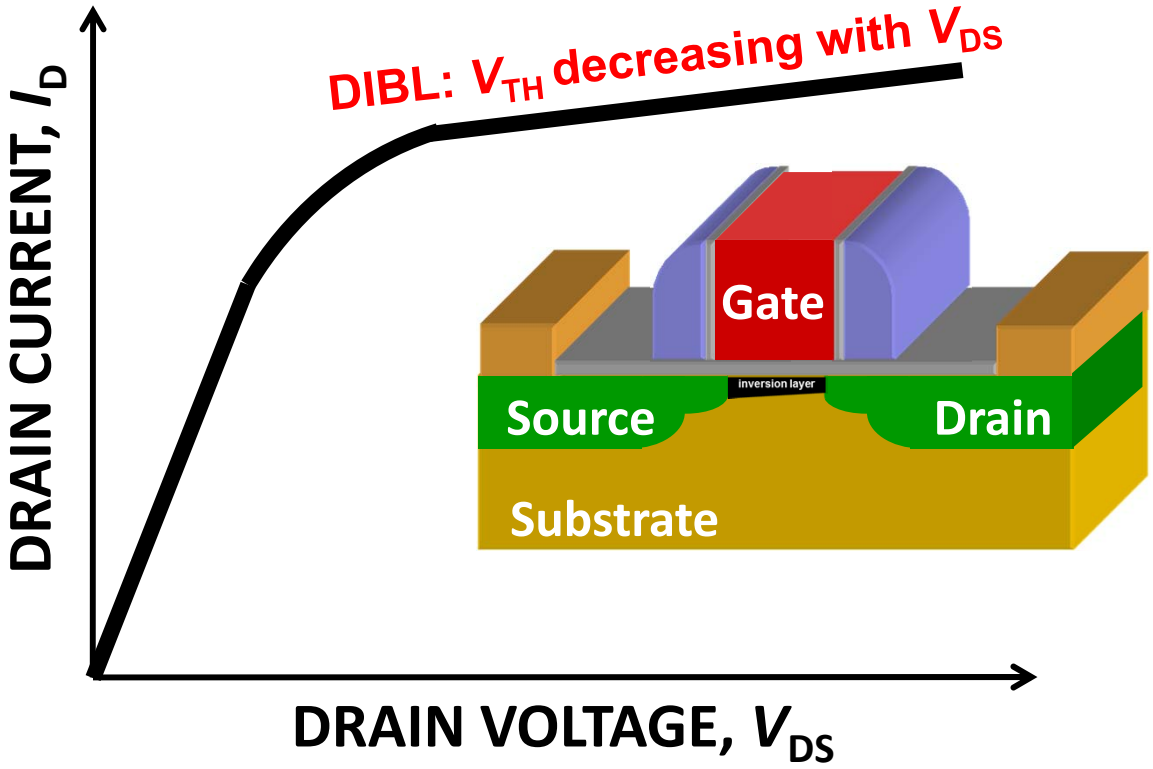




MOSFET in ON State ($V_{GS} > V_{TH}$)

$$I_D = W \cdot v \cdot Q_{inv}$$

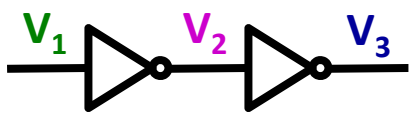
$$v \propto \mu_{eff} \qquad Q_{inv} \propto C_{ox}(V_{GS} - V_{TH})^{\eta}$$

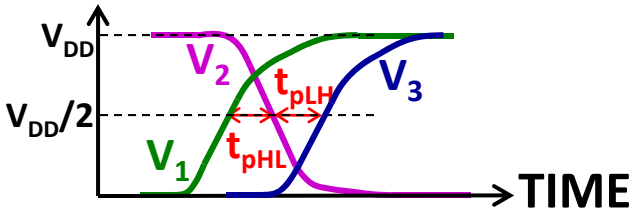


Effective Drive Current (I_{EFF})

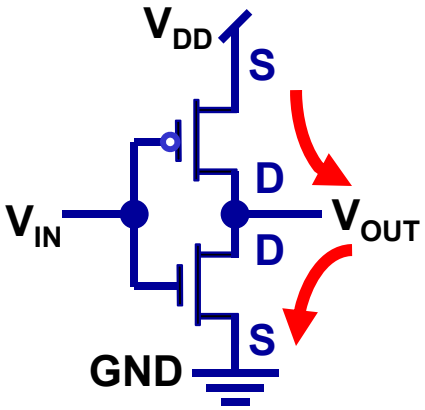
M. H. Na *et al.*, *IEDM Technical Digest*, pp. 121-124, 2002

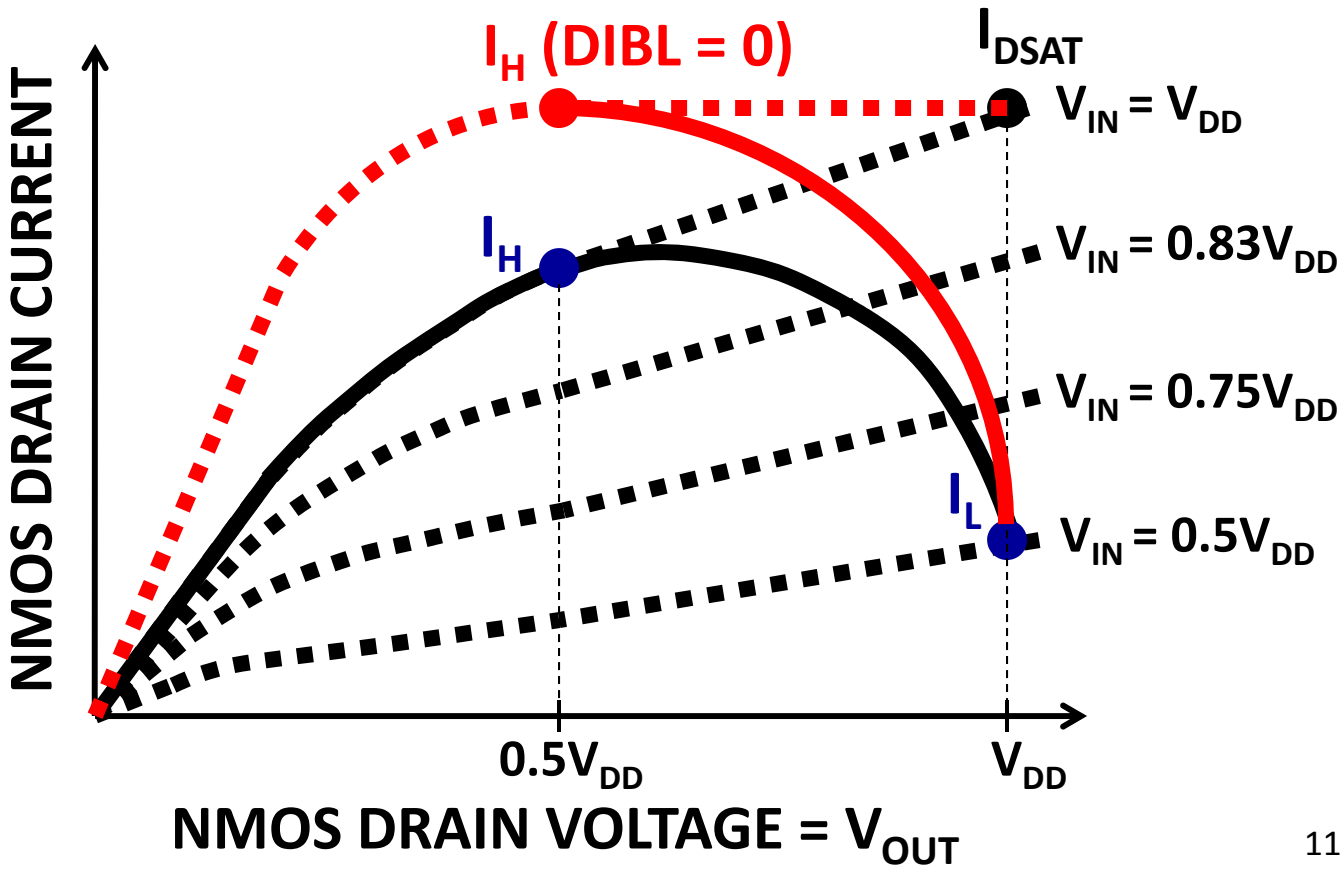
CMOS inverter chain:





$$I_{EFF} = \frac{I_H + I_L}{2}$$





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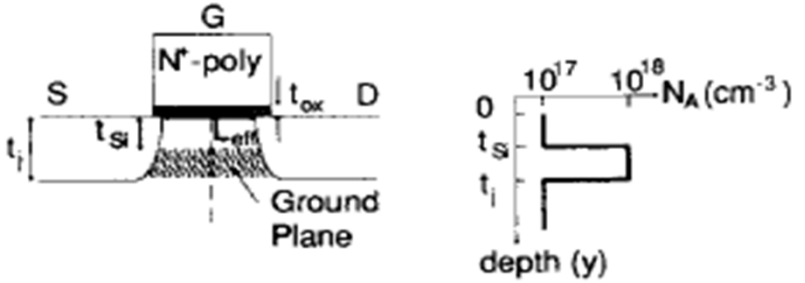
Optimizing Bulk MOSFET Performance

- **To maximize I_{ON}, heavy doping near the surface of the channel region should be avoided.**

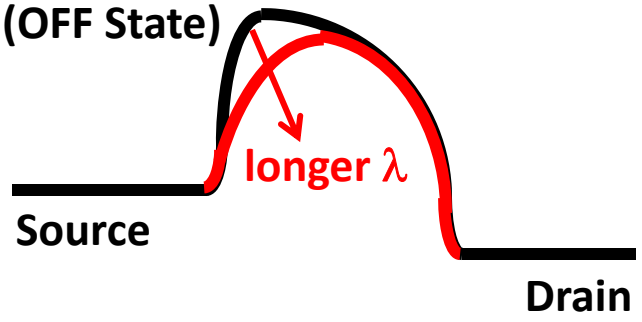
  → **Use a steep retrograde channel doping profile to suppress I_{OFF}**



R.-H. Yan *et al.*,
IEEE Trans. Electron Devices,
Vol. 39, pp. 1704-1710, 1992.

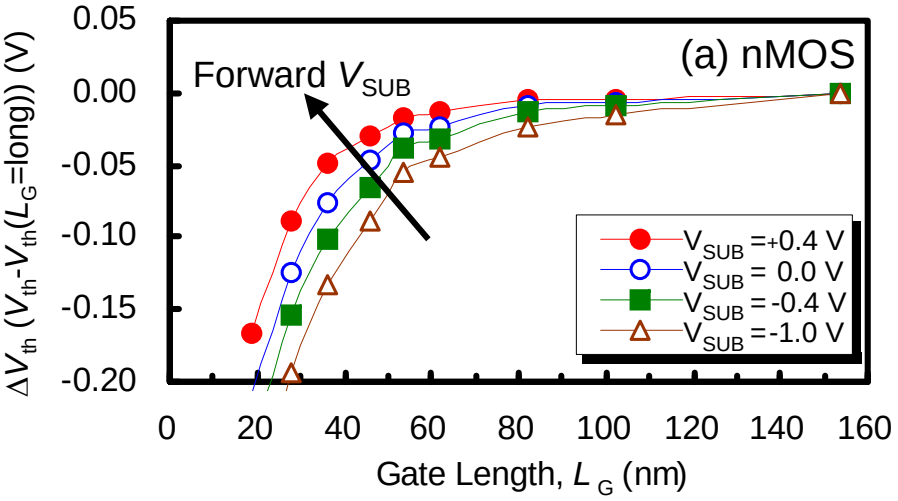
Fig. 6. The Pulse-Shaped Doped structure. (a) Cross-section view of the structure. (b) Vertical doping profile. The example used in Fig. 7 has L_{eff} = 0.1 μm, t_{ox} = 40 Å, t_{Si} = 250 Å, t_j = 500 Å, and the doping profile shown in Fig. 6(b).

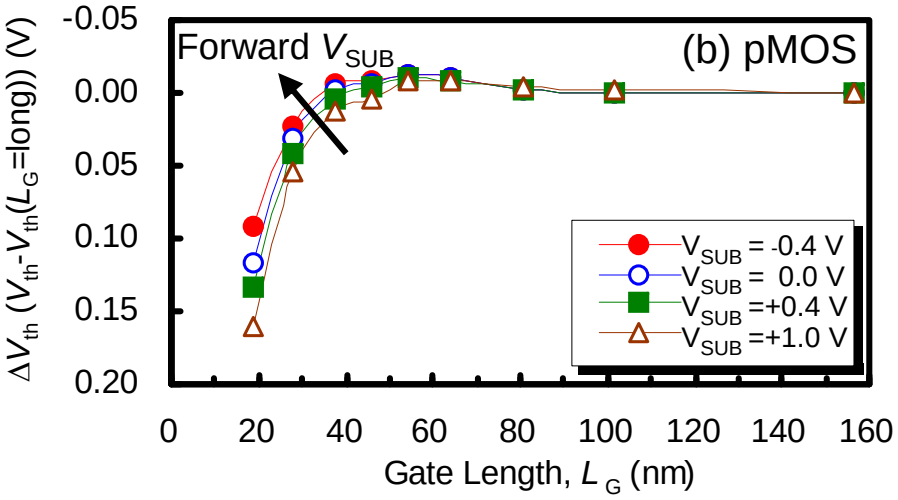
Energy Band Profile:
(OFF State)



Structure:	Double-Gate FET	Ground-Plane FET
Scale length:	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{Si} t_{ox}}$	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} \frac{t_{Si} t_{ox}}{1+\left(\varepsilon_{Si} t_{ox} / \varepsilon_{ox} t_{Si}\right)}}$

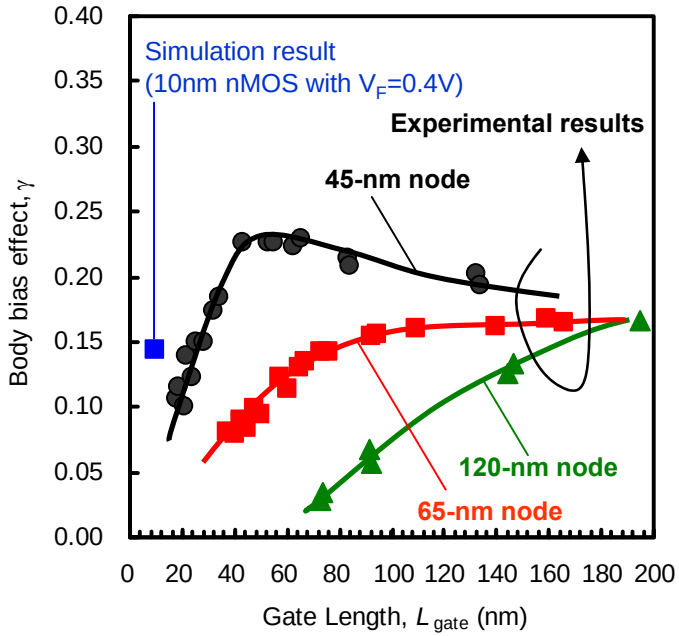
Reduced SCE with Body Biasing





A. Hokazono *et al.*, *IEEE Trans. Electron Devices*, Vol. 55, pp. 2657-2664, 2008

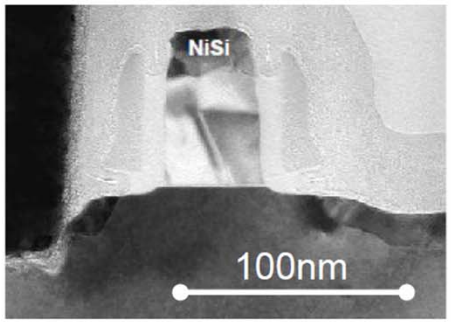
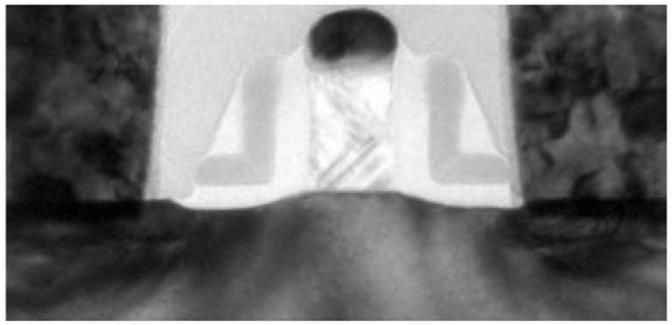
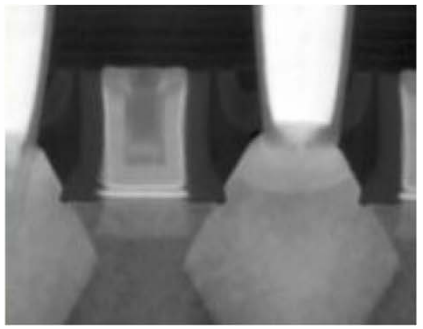
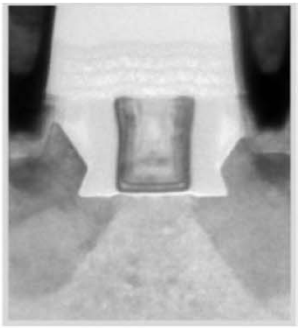
- **Forward body biasing reduces depletion depth and thereby improves MOSFET scalability**
- **Body effect factor is improved with steep retrograde doping:**



CMOS Technology Scaling

XTEM images with the same scale

courtesy V. Moroz (Synopsys, Inc.)

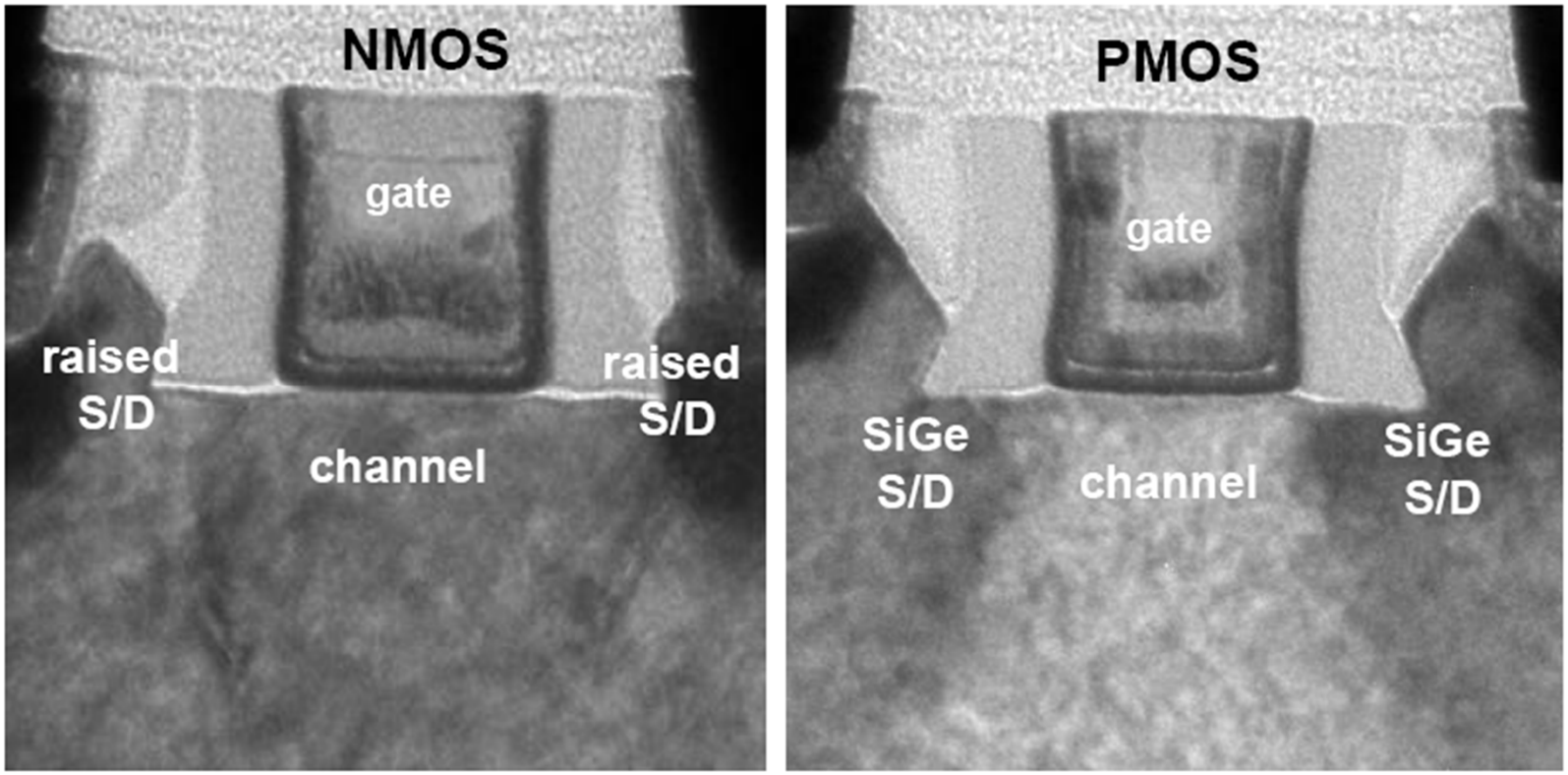
90 nm node	65 nm node	45 nm node	32 nm node
			
T. Ghani *et al.*, *IEDM* 2003	(after S. Tyagi *et al.*, *IEDM* 2005)	K. Mistry *et al.*, *IEDM* 2007	P. Packan *et al.*, *IEDM* 2009

- **Gate length has not scaled proportionately with device pitch (0.7x per generation) in recent generations.**
  - **Transistor performance has been boosted by other means.**

MOSFET Performance Boosters

- Strained channel regions → $\mu_{eff}\uparrow$
- High-k gate dielectric and metal gate electrodes → $C_{ox}\uparrow$

Cross-sectional TEM views of Intel's 32nm CMOS devices



P. Packan *et al.*, *IEDM Technical Digest*, pp. 659-662, 2009

Carrier Confinement w/o Doping

R. J. Mears *et al*. (Mears Technologies), *2012 Silicon Nanoelectronics Workshop* (Paper 3-5)

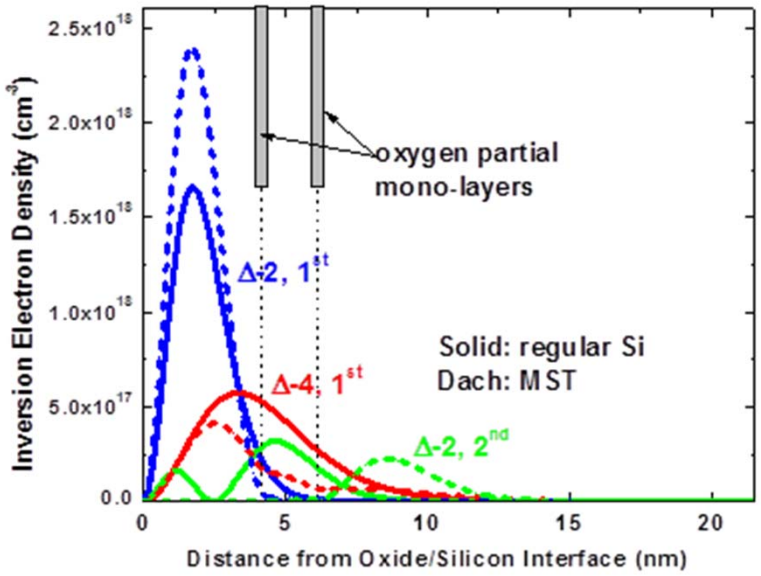
- **Inversion charge is confined to be near the surface, by inserting O partial mono-layers within the channel region**

  → relaxes requirement for thin t_{Si}

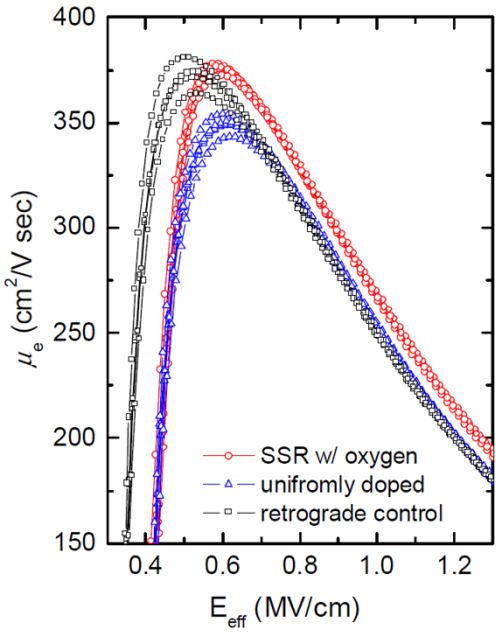
- **Separation of carrier sub-bands reduces inter-band scattering**

  → carrier mobility is enhanced

Inversion-charge density profile



Effective electron mobility



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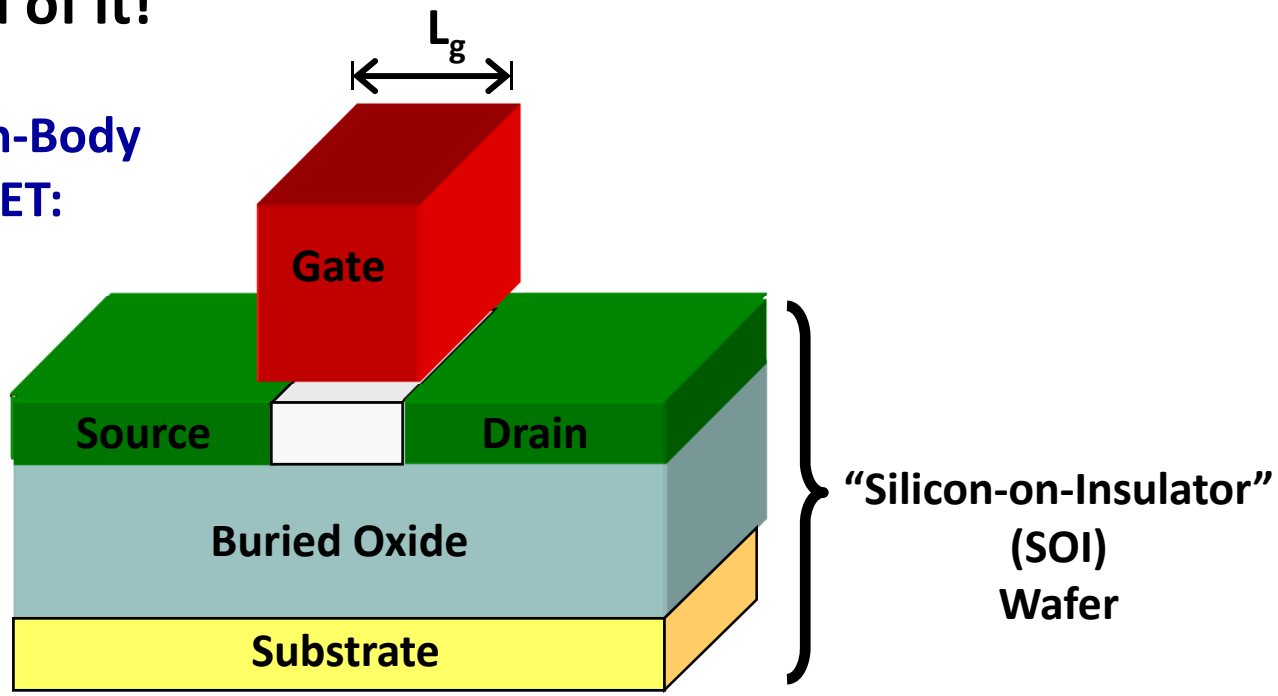
Why New Transistor Structures?

- Off-state leakage (I_{OFF}) must be suppressed as L_g is scaled down
  - allows for reductions in V_{TH} and hence V_{DD}
- Leakage occurs in the region away from the channel surface

→ Let's get rid of it!

Ultra-Thin-Body MOSFET:



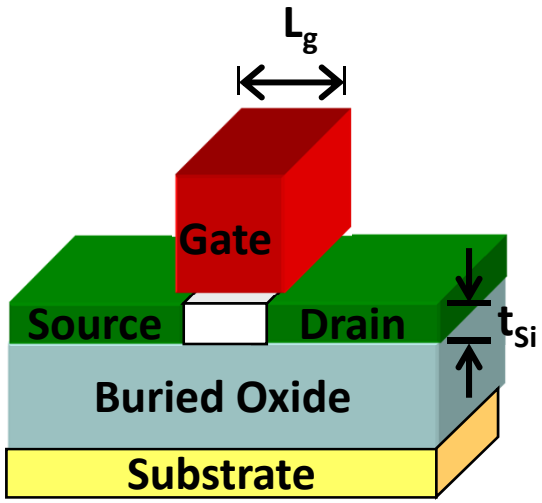
Thin-Body MOSFETs

- I_{OFF} is suppressed by using an adequately thin body region.
  - Channel/body doping can be eliminated

    → higher drive current (I_{ON}) due to higher carrier mobility

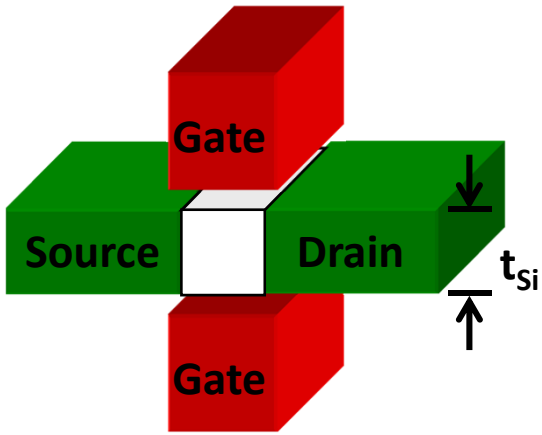
    → Reduced impact of random dopant fluctuations (RDF)

Ultra-Thin Body (UTB)



$t_{Si} < (1/4) \times L_g$

Double-Gate (DG)

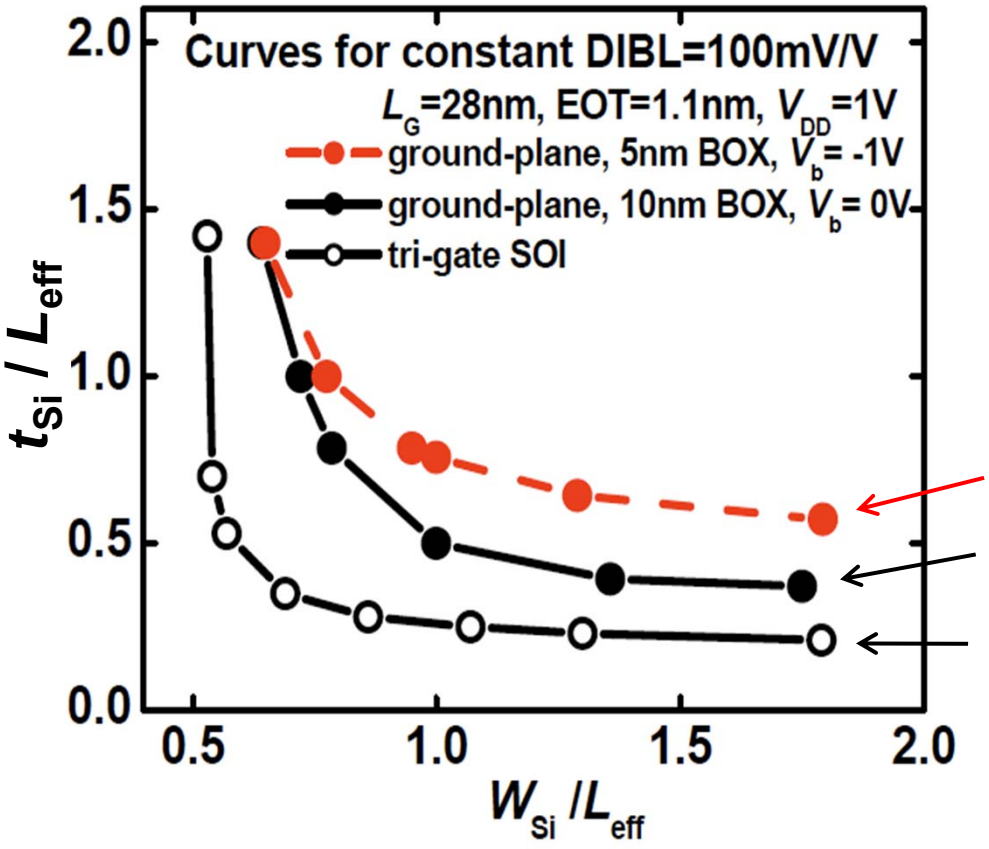


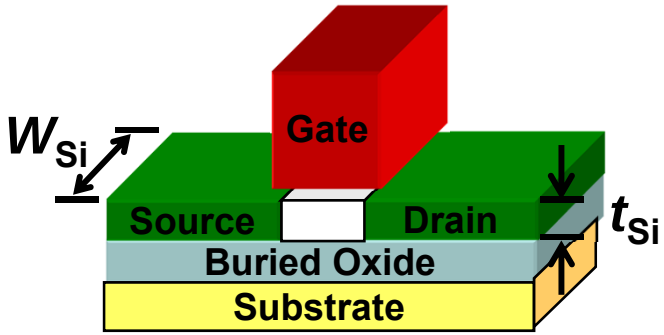
$t_{Si} < (2/3) \times L_g$

Relaxing the Body Thinness Requirement

Adapted from X. Sun *et al.*, *IEEE Electron Device Letters,* Vol. 29, pp. 491-493, 2008

- Thinner BOX → reduced drain-induced barrier lowering
- Reverse back biasing → further reduction of SCE





T_{BOX} = 5nm, V_b = -1V (NMOS)

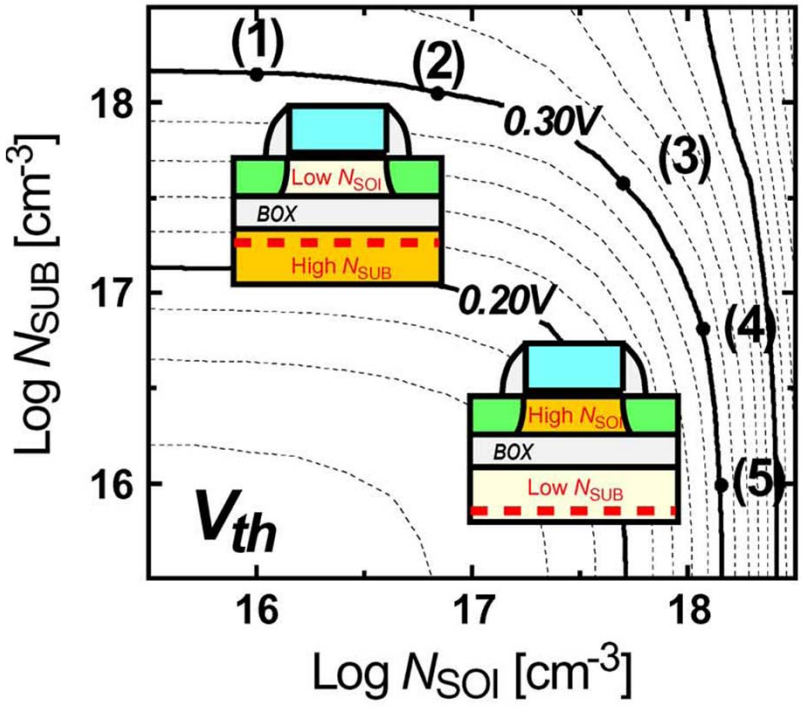
T_{BOX} = 10nm

T_{BOX} = ∞

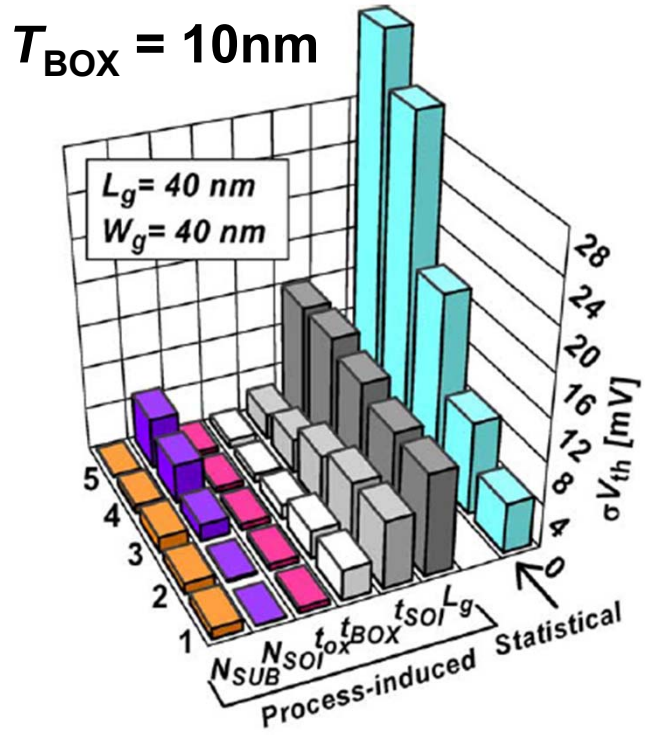
→ Thicker SOI can be used for back-gated FD-SOI MOSFETs

Threshold Voltage Adjustment

- V_{TH} can be adjusted via substrate doping, for reduced σ_{VTH}:



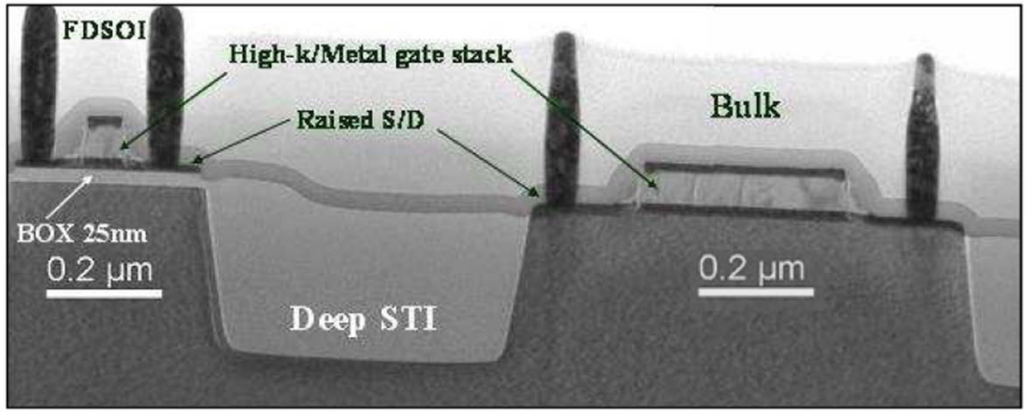
T. Ohtou *et al.*, *IEEE-EDL* 28, p. 740, 2007



- V_{TH} can be dynamically adjusted via back-biasing.
  - Reverse back biasing (to increase V_{TH}) is beneficial for lowering SCE.

    S. Mukhopadhyay *et al.*, *IEEE-EDL* 27, p. 284, 2006

UTBB SOI FET Technology Challenges

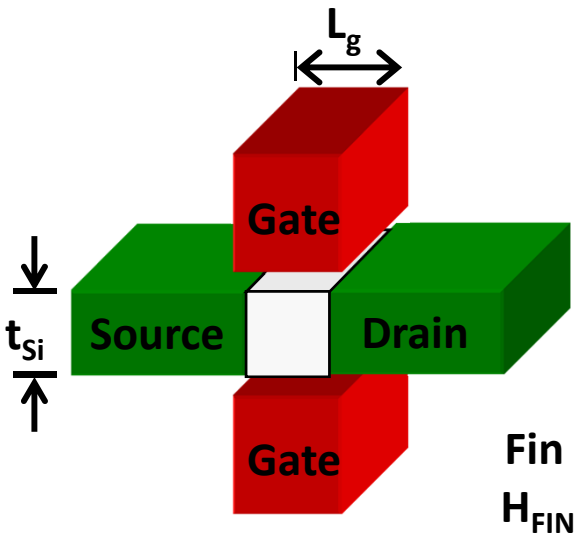


C. Fenouillet-Beranger *et al., IEDM 2009*

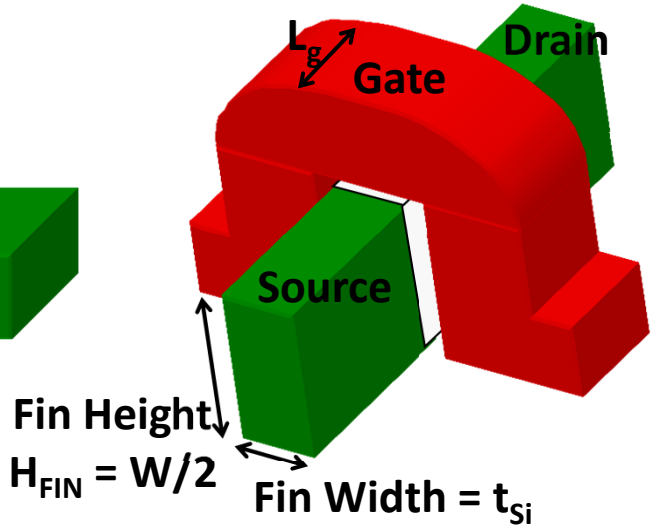
- **Higher substrate cost**
  - cannot be offset by simpler process, if thin-BOX and RBB are used
- **Mobility enhancement**
  - Embedded S/D stressors are not as effective as for bulk MOSFETs
  - Integration of advanced channel materials?
- **System-on-chip (SoC) requirements**
  - Implementation of multiple gate oxide thicknesses → STI recess → practical lower limit for T_{BOX}

Double-Gate "FinFET"

Planar DG-FET



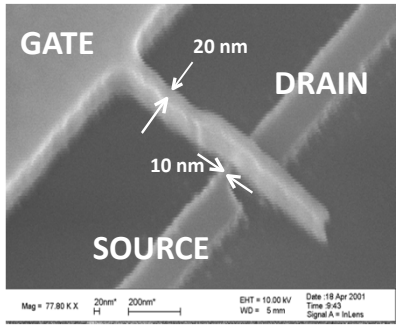
FinFET



D. Hisamoto *et al.*, *IEDM Technical Digest*, 1998

N. Lindert *et al.*, *IEEE Electron Device Letters*, p. 487, 2001

15nm L_g FinFET:

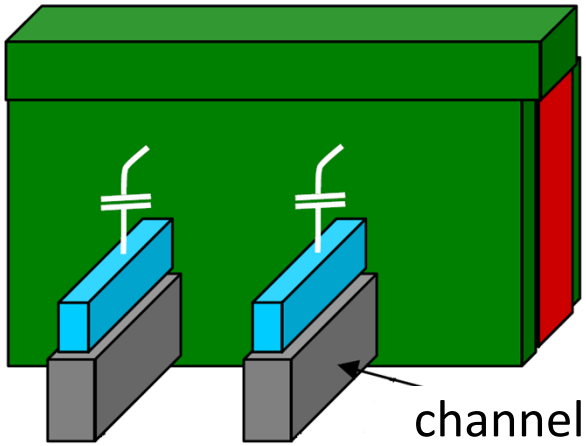


Y.-K. Choi *et al.*, *IEDM Technical Digest*, 2001

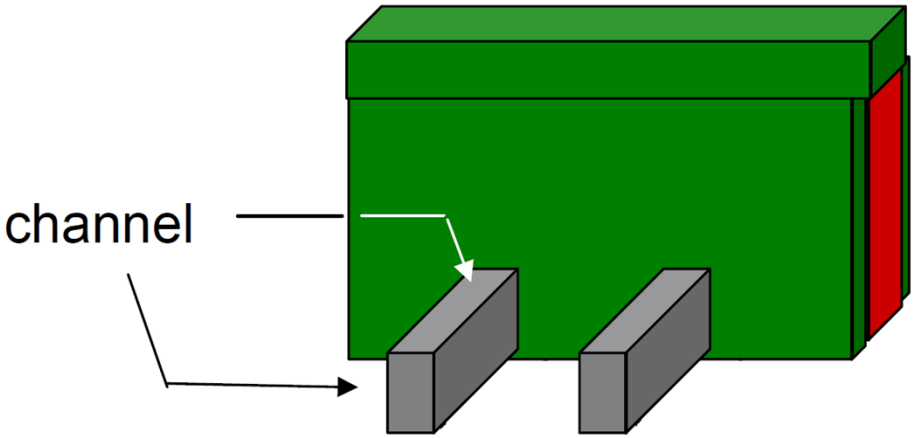
Double-Gate *vs.* Tri-Gate FET

- **The Double-Gate FET does not require a highly selective gate etch, due to the protective dielectric hard mask.**
- **Additional gate fringing capacitance is less of an issue for the Tri-Gate FET, since the top fin surface contributes to current conduction in the ON state.**

Double-Gate FET

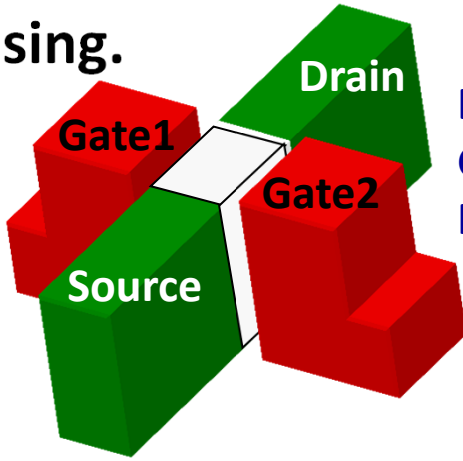


Tri-Gate FET

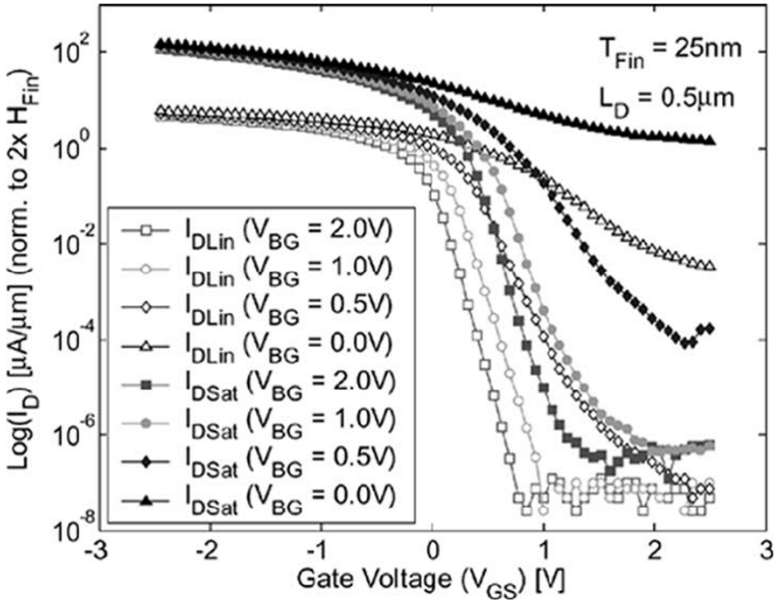


Independent Gate Operation

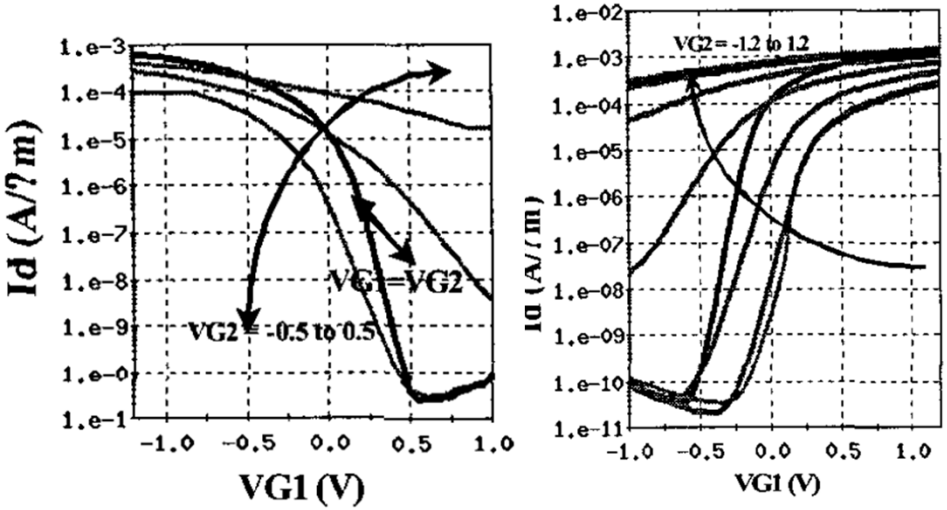
- The gate electrodes of a double-gate FET can be isolated by a masked etch, to allow for separate biasing.
  - One gate is used for switching.
  - The other gate is used for V_{TH} control.



Back-Gated FET



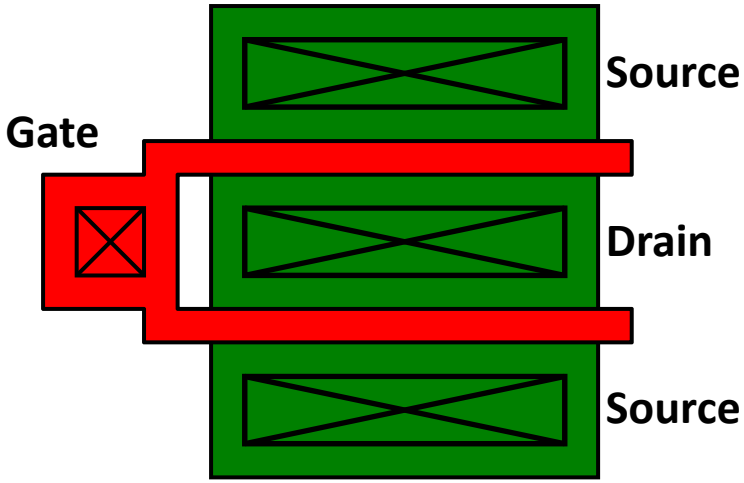
D. M. Fried *et al*. (Cornell U.),
IEEE Electron Device Letters,
Vol. 25, *pp.* 199-201, 2004



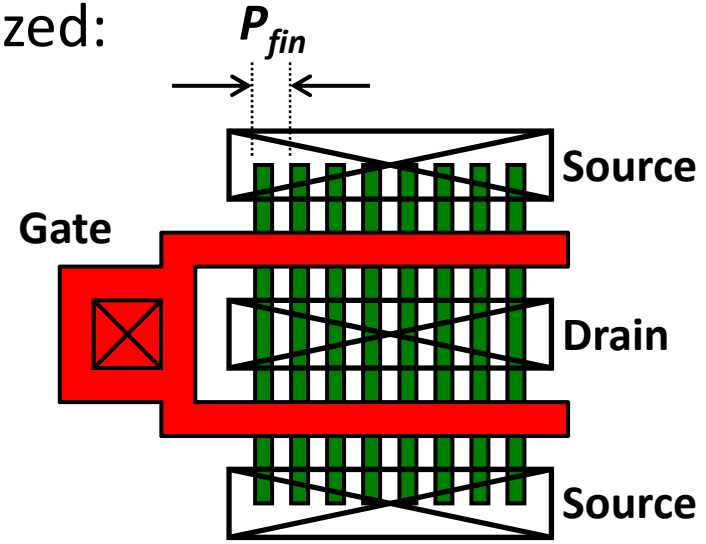
L. Mathew *et al.* (Freescale Semiconductor),
2004 IEEE International SOI Conference

FinFET Layout

- **Layout is similar to that of conventional MOSFET,** except that the channel width is quantized:

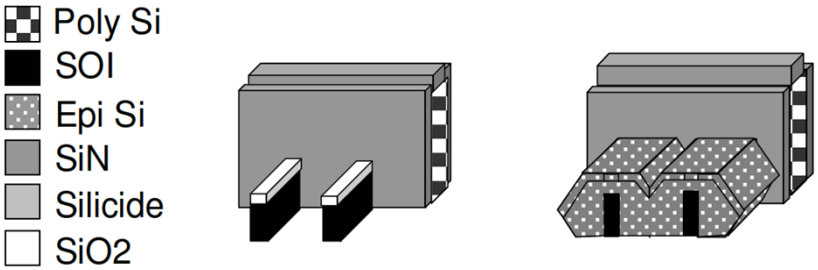


Bulk-Si MOSFET

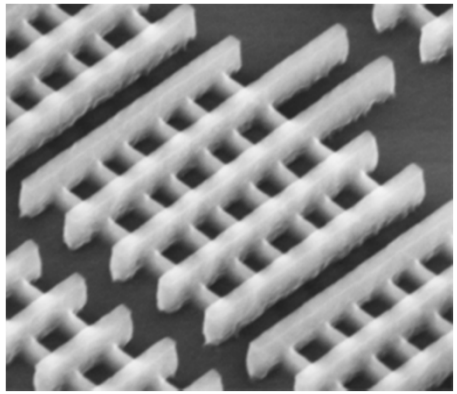


FinFET

The S/D fins can be merged by selective epitaxy:



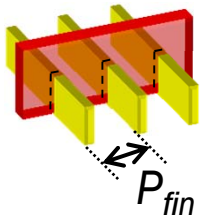
M. Guillorn *et al*. (IBM), *Symp. VLSI Technology* 2008

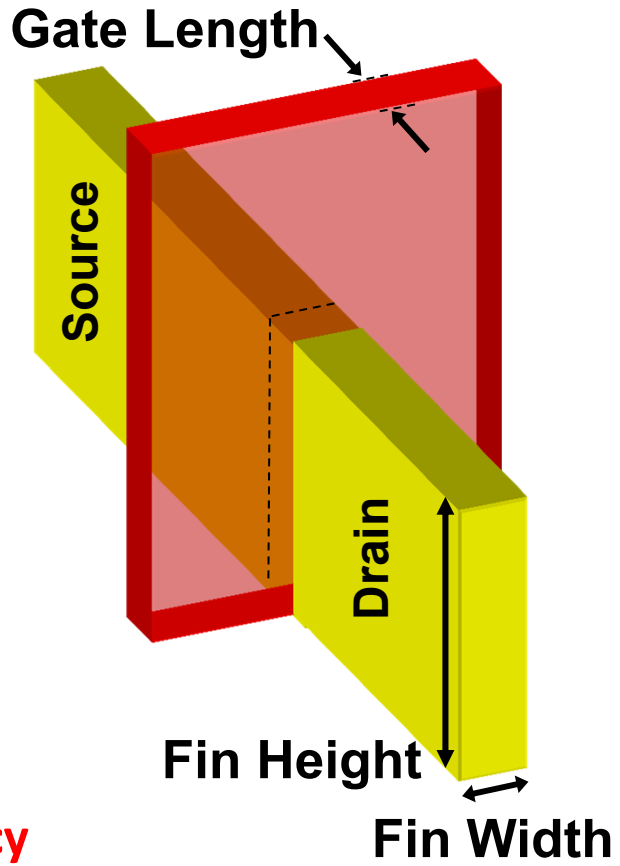


Intel Corp.

Fin Design Considerations

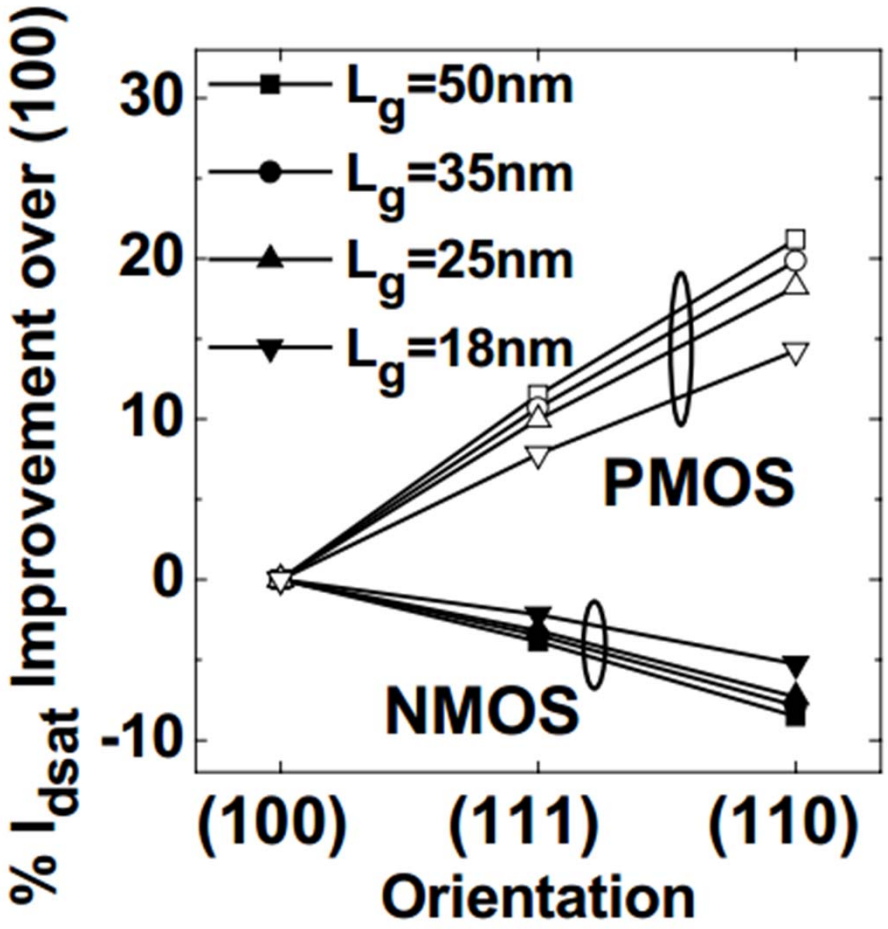
- **Fin Width**
  - Determines SCE
- **Fin Height**
  - Limited by etch technology
  - Tradeoff: layout efficiency *vs.* design flexibility
- **Fin Pitch**
  - Determines layout area
  - Limits S/D implant tilt angle
  - Tradeoff: performance *vs.* layout efficiency



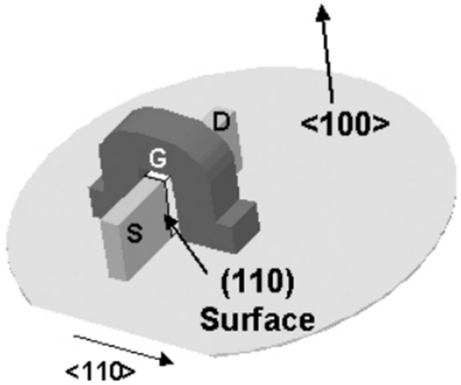


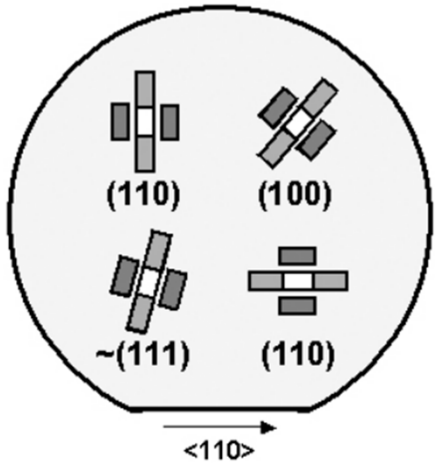
Impact of Fin Layout Orientation

L. Chang *et al.* (IBM), *SISPAD* 2004



(Series resistance is more significant at shorter L_g.)





- **If the fin is oriented || or ⊥ to the wafer flat, the channel surfaces lie along (110) planes.**
  - **Lower electron mobility**
  - **Higher hole mobility**
- **If the fin is oriented 45° to the wafer flat, the channel surfaces lie along (100) planes.**

Bulk FinFET

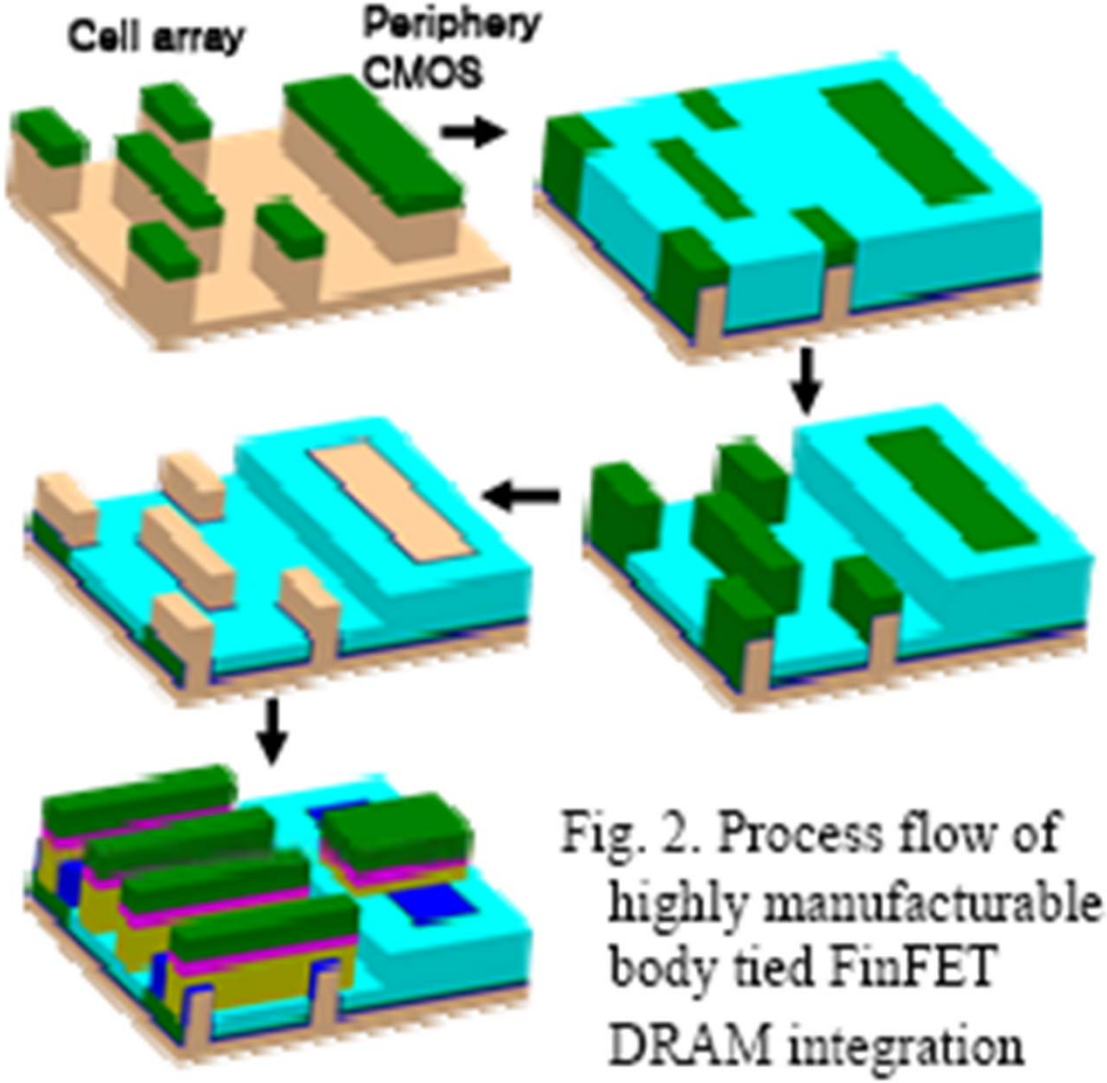


Fig. 2. Process flow of highly manufacturable body tied FinFET DRAM integration

- FinFETs can be made on bulk-Si wafers
  - ✓ lower cost
  - ✓ improved thermal conduction

  with super-steep retrograde well (SSRW) or "punch-through stopper" at the base of the fins
- 90 nm L_g FinFETs demonstrated
  - W_{fin} = 80 nm
  - H_{fin} = 100 nm

  DIBL = 25 mV

C.-H. Lee *et al.* (Samsung), *Symposium on VLSI Technology Digest,* pp. 130-131, 2004

Bulk *vs.* SOI FinFET

Item	Comment	Bulk FINFET (compared to SOI FinFET)
Density	Well Contact	-
Parasitic Cap	Impact of PTS	-
Performance/ Variability	Performance tradeoff to overcome variability	- -
Leakage & HVT capability	Impact of PTS implant in bulk FIN	-
Non FIN structure compatibility (passives, etc)		+
s/d stressor	eSiGe, eSiC	++
Gate stressor, liner stressor		**Similar**
Channel stressor	SiGe pFET; SSOI Si nFET, III-V nFET	+/-
SRAM Vt Variation		- -

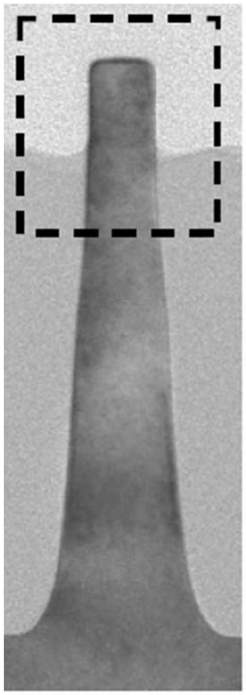
H. Bu (IBM), ***2011 IEEE International SOI Conference***

22nm FinFETs

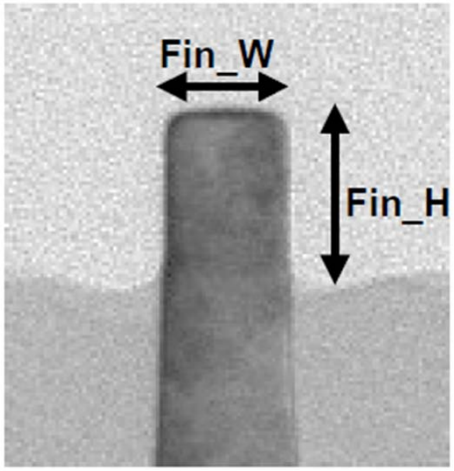
C.C. Wu *et al.* (TSMC), *IEEE International Electron Devices Meeting*, 2010

22nm/20nm high-performance CMOS technology

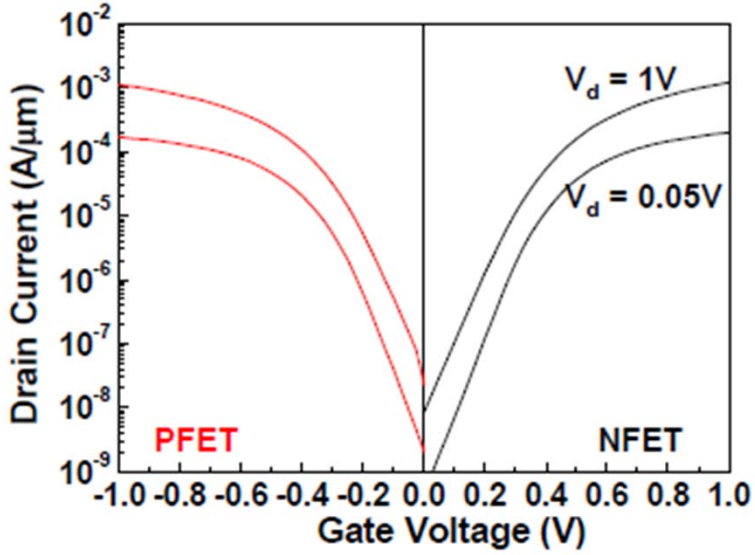
- L_g = 25 nm

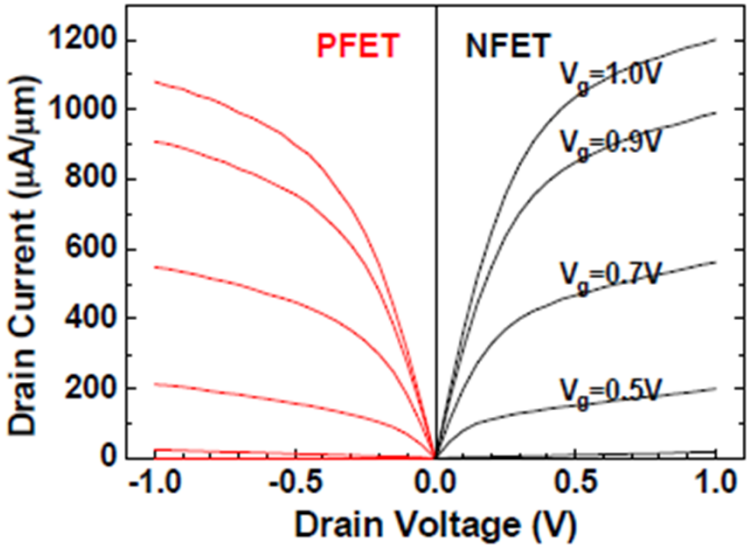


XTEM Images of Fin



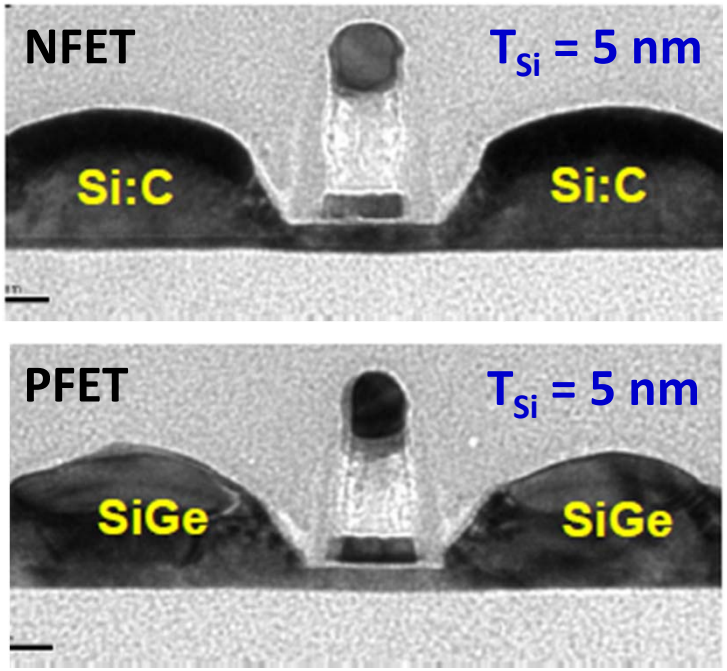
Weff = 2 x Fin_H + Fin_W





FinFET *vs.* UTBB SOI MOSFET

Cross-sectional TEM views of 25 nm UTB SOI devices



K. Cheng *et al.* (IBM), *Symposium on VLSI Technology Digest*, pp. 128-129, 2011

	20nm ETSOI	22nm Bulk finFET*
L_G (nm)	22	> 25
Pitch (nm)	80-100	100
I_{OFF} (nA/ μm)	1	1
NFET I_{on} (μA/μm)	920	960
PFET I_{on} (μA/μm)	880	850

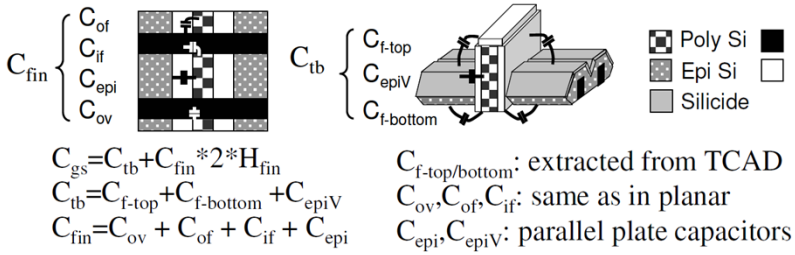
B. Doris (IBM), *2011 IEEE International SOI Conference*

*C.C. Wu *et al.* (TSMC), *IEDM* 2010

Remaining FinFET Challenges

- V_{TH} adjustment
  - Requires gate work-function (WF) or L_{eff} tuning
  - Dynamic V_{TH} control is not possible for high-aspect-ratio multi-fin devices
- Fringing capacitance between gate and top/bottom of S/D
  - Mitigated by minimizing fin pitch and using via-contacted, merged S/D

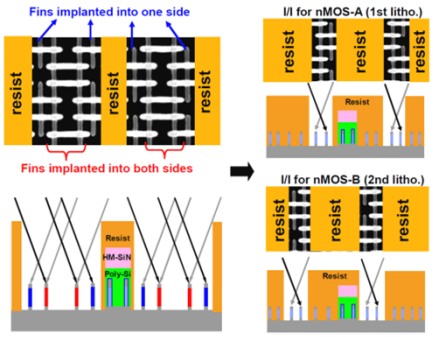
    M. Guillorn, *Symp. VLSI Technology* 2008



- Parasitic resistance
  - Uniform S/D doping is difficult to achieve with conventional implantation

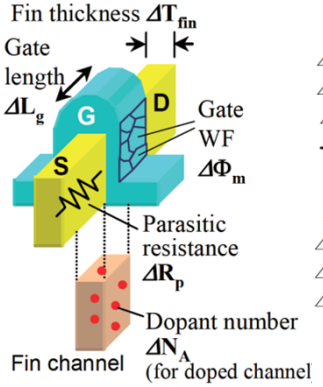
    H. Kawasaki, *IEDM* 2008
  - Conformal doping is needed

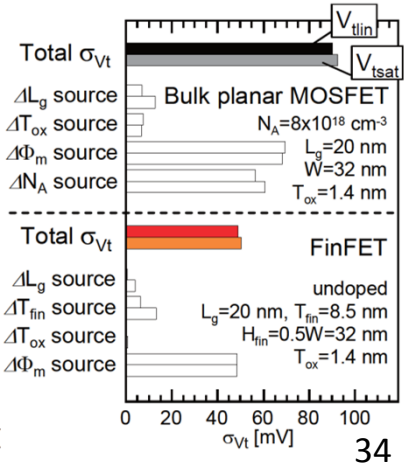
    e.g. Y. Sasaki, *IEDM* 2008



- Variability
  - Performance is very sensitive to fin width
  - WF variation dominant for undoped channel

    T. Matsukawa, *Symp. VLSI Technology* 2008



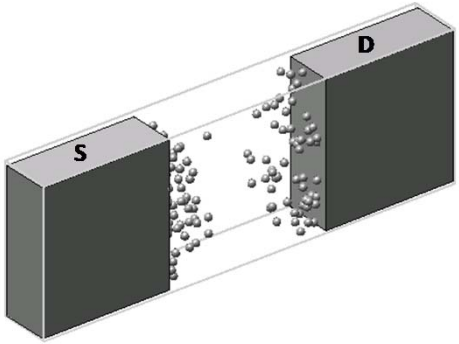


Impact of RDF on FinFETs

V. Varadarajan *et al.*, *Proc. IEEE Silicon Nanoelectronics Workshop*, pp. 137-138, 2006

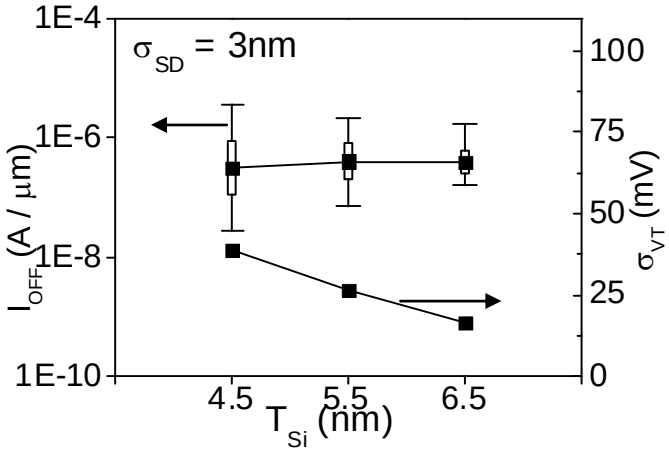
- **Channel/body doping can be eliminated in thin-body FETs such as the double-gate FinFET, to mitigate RDF effects.**
- **However, due to source/drain doping, a trade-off exists between performance & RDF tolerance for L_g < 10nm:**

FinFET with atomistic S/D gradient regions:

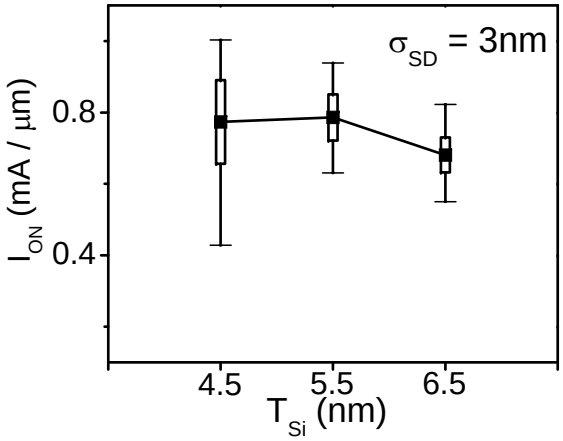


L_g = 9nm, EOT = 0.7nm

***I_{OFF}* and σ_{VT} *vs.* T_{Si}**



***I_{ON}* *vs.* T_{Si}**



Outline

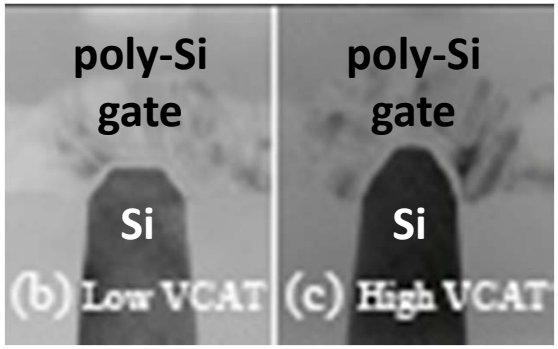
- Review: MOSFET Basics
- The Road Behind: CMOS Technology Advancement
- The Narrow Road Ahead: Thin-Body MOSFETs
- **An Alternative Route: Planar Bulk MOSFET Evolution**
- Summary

Quasi-Planar (QP) Bulk MOSFET

M. Kito *et al*. (Toshiba Corp.), *2005 Symp. VLSI Technology*

- The quasi-planar bulk FET structure is easily achieved by slightly recessing the isolation oxide, or by selective epitaxial growth, prior to gate-stack formation
  - Retrograde doping helps to suppress SCE, so that W_{Si} can be greater L_g
  - Body bias effect can be retained

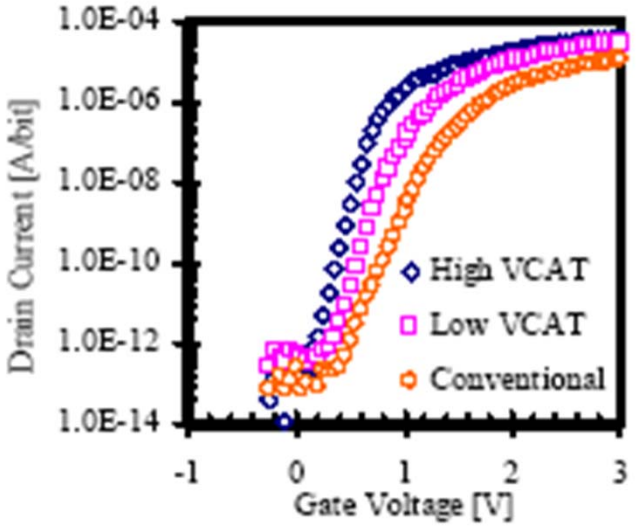
XTEM images



In contrast to the FinFET / MuGFET

- Superior electrostatic integrity is achieved with quasi-planar structure
  - →reduced impact of process-induced variations
  - →facilitates voltage scaling

Measured *I-V* Characteristics



Quasi-Planar 28nm CMOS Technology

C. Shin *et al.*, *2010 ESSDERC*

Experiment performed at UMC in early 28nm CMOS technology

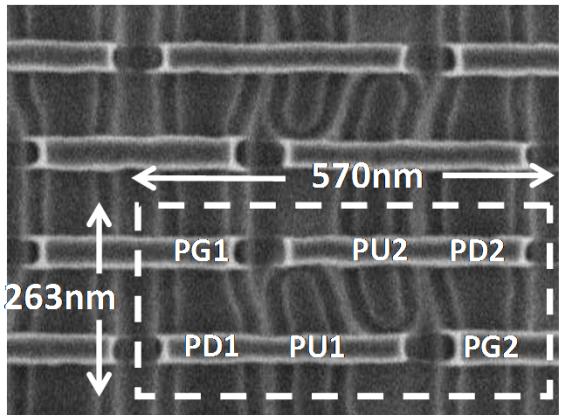
- **Individual logic transistors and 6T-SRAM arrays fabricated**
  - **~2500 cell per device-under-test (DUT)**
  - **Dual-stress liners for performance enhancement**

CMOS front-end-of-line steps

- STI Formation
- Well & V_T Implants
- ***STI Oxide Recess*** **0 or 15nm**
- Gate Ox./Poly Deposition
- Gate Patterning
- LDD & Pocket Implants
- Spacer & S/D Formation
- Activation Process
- Salicidation

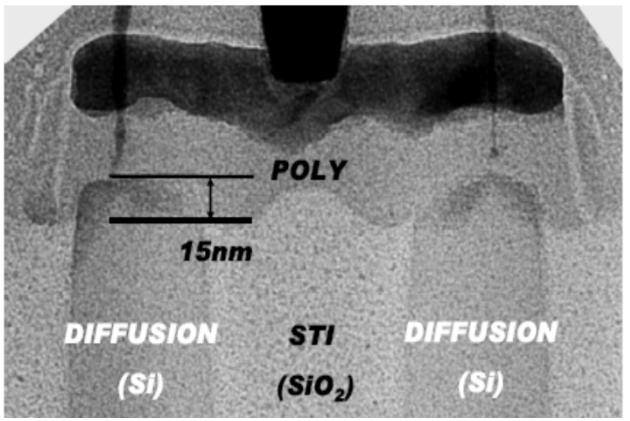
PKT dose split: Standard or Light

SRAM cell plan-view SEM



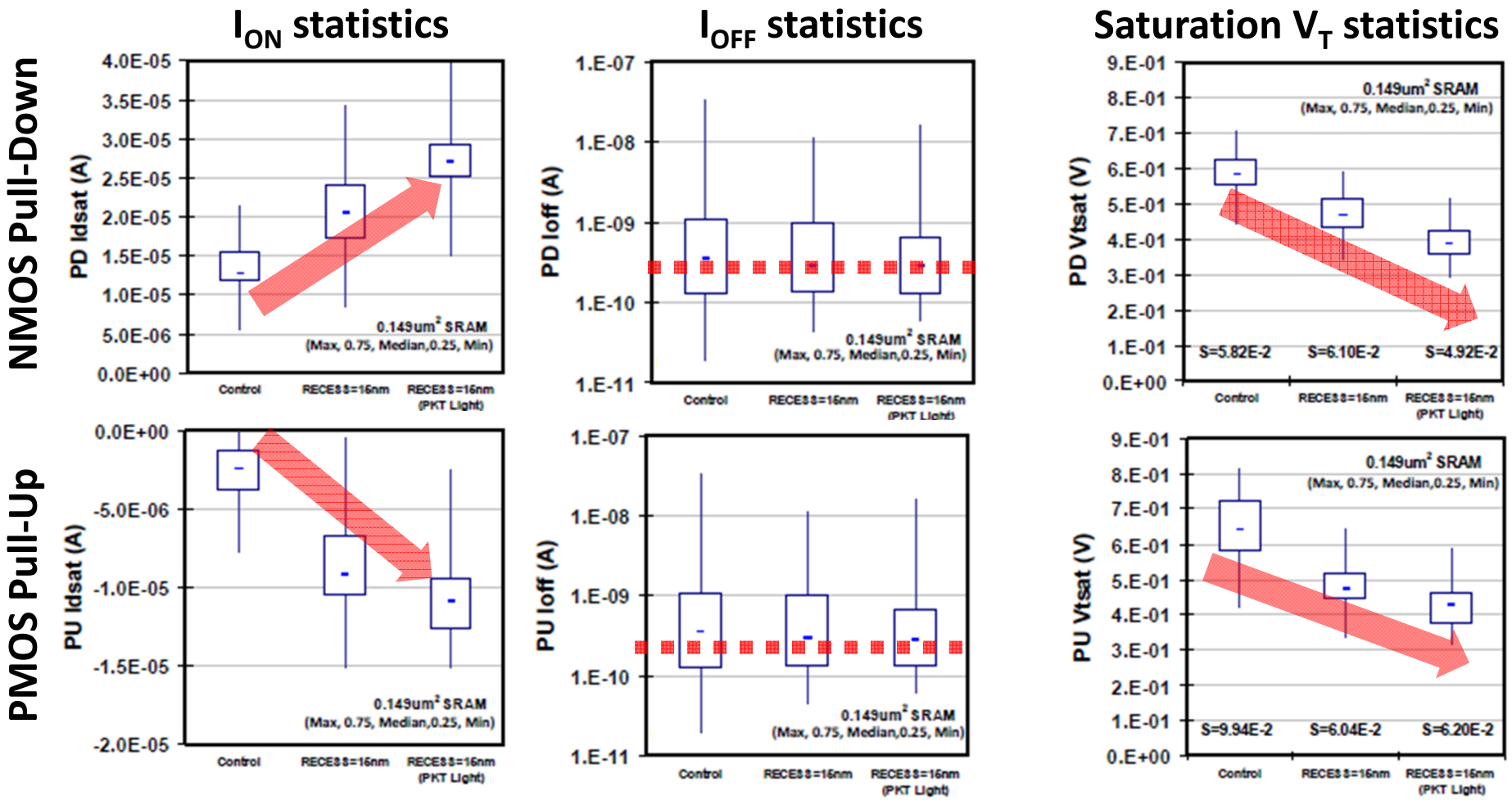
cell-area = 0.149 um^2

XTEM along gate electrode



Measured QP Bulk CMOS Results

C. Shin *et al.*, *2010 ESSDERC*



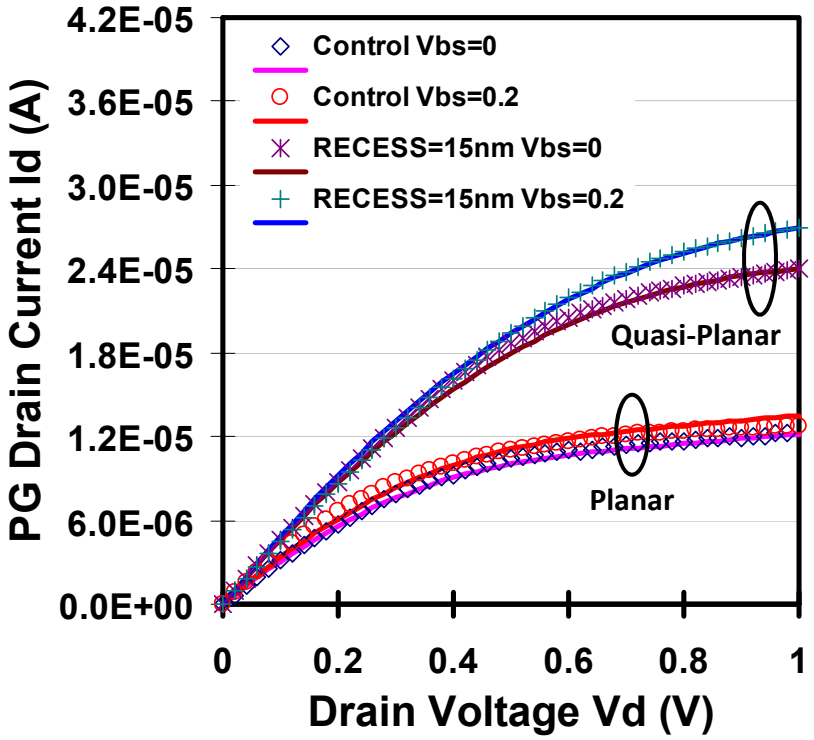
- Quasi-planar I_{ON} is higher, for comparable I_{OFF}
  - 2x increase for NMOS, 4x increase for PMOS
- Quasi-planar V_{TH} variation is lower

Body Bias Effect and Compact Model

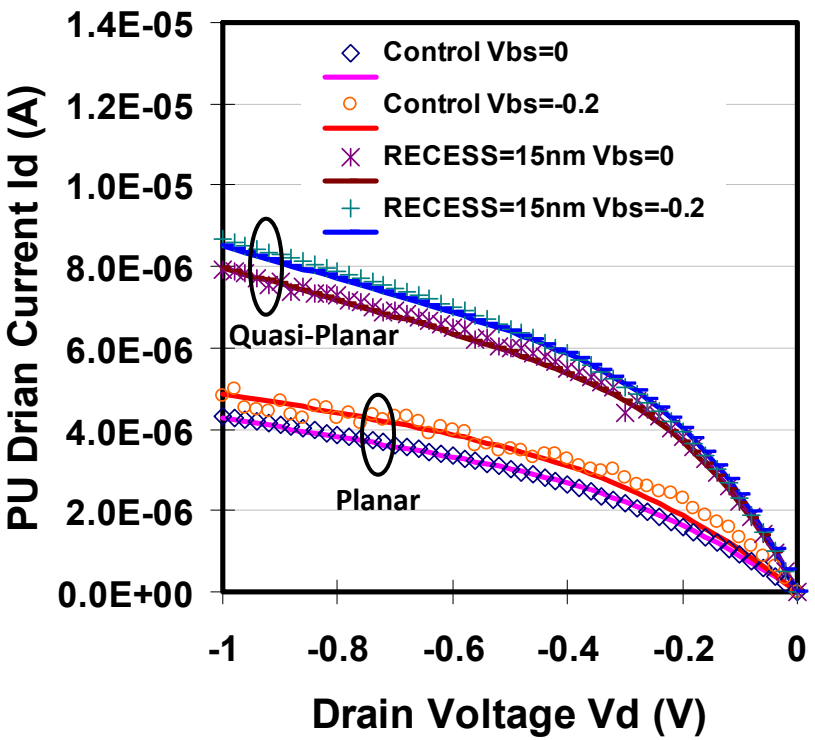
C. Shin *et al.*, *2010 ESSDERC*

- **The standard bulk MOSFET compact model can well predict quasi-planar MOSFET performance -- including body bias effect**

NMOS

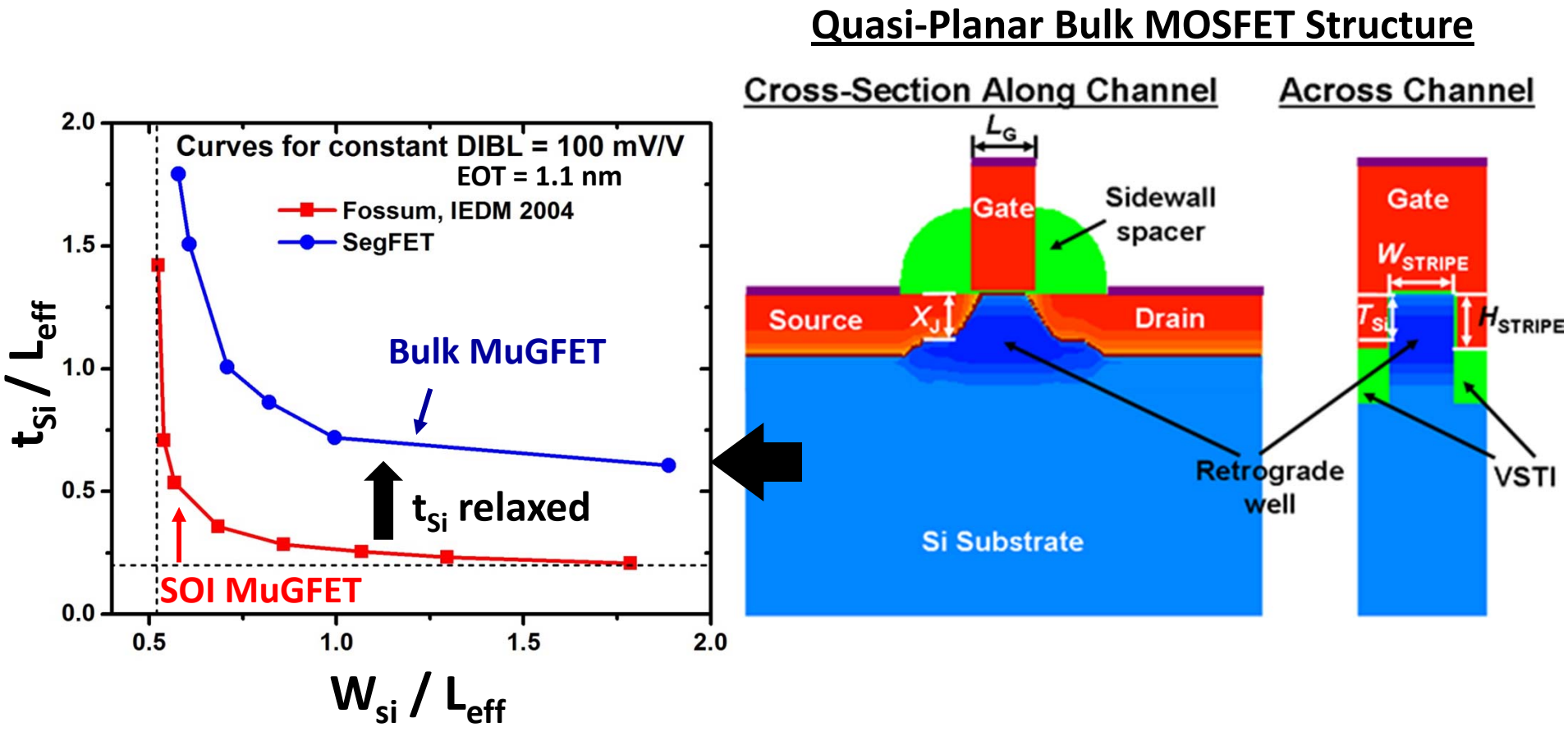


PMOS



Bulk vs. SOI Multi-Gate FET Designs

X. Sun *et al.*, *IEEE Electron Device Letters* Vol. 29, pp. 491-493, 2008



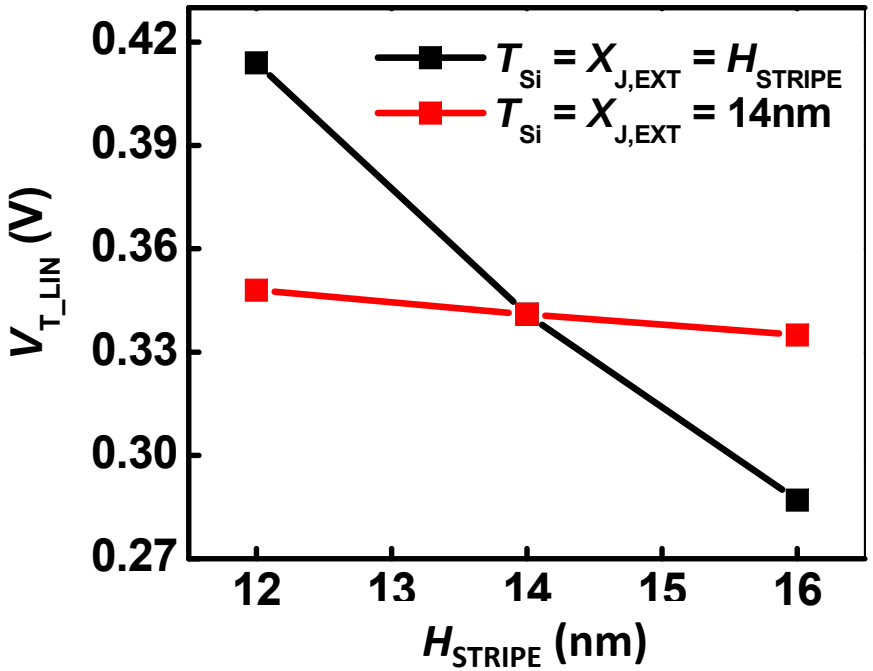
- Thin/narrow body requirement is relaxed with retrograde doping

  →The bulk MOSFET structure achieves better layout efficiency!

Simulated Impact of H_{STRIPE} Variation

3-D device simulation results, to be published by X. Sun *et al*.

L_G = 20nm, EOT = 0.9nm, W_{STRIPE} = 20nm

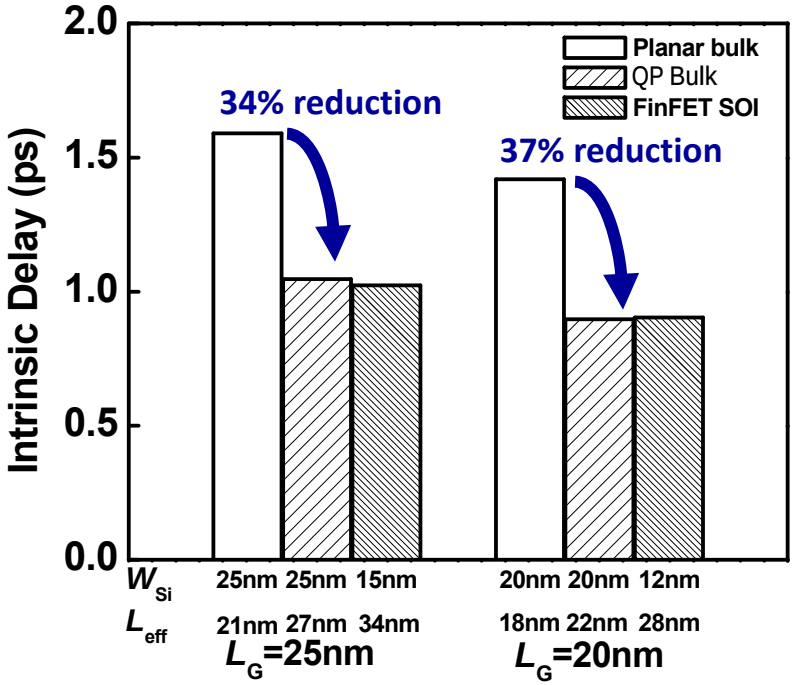


- If t_{Si} is fixed, V_T is not sensitive to H_{STRIPE} variation.

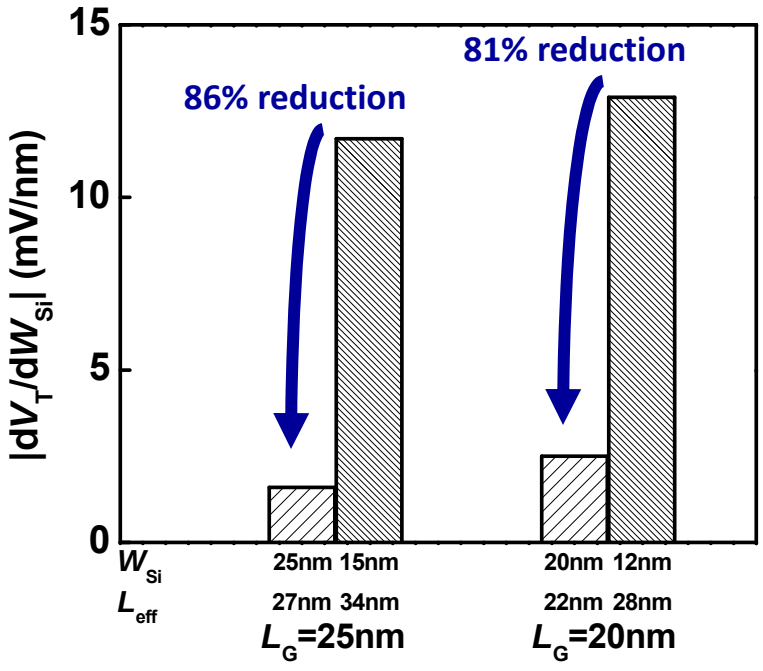
Performance Comparison with FinFET

- 3-D device simulations were performed for MOSFETs designed to achieve minimum intrinsic delay at a given I_{OFF} specification:
  - For L_G=25nm, I_{OFF}=8nA/μm
  - For L_G=20nm, I_{OFF}=18nA/μm

✓ The intrinsic delay advantage of the QP FET increases with scaling.



✓ The QP FET is less sensitive to W_{STRIPE} variation than the FinFET.



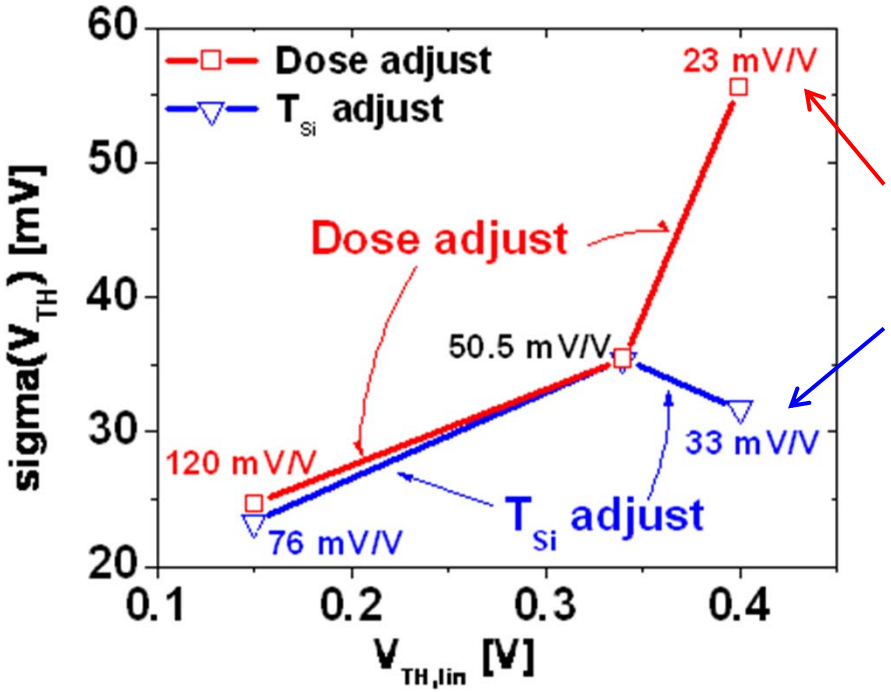
Xin Sun Ph.D. thesis, UC Berkeley, 2010

V_{TH} Adjustment Approaches

C. Shin *et al.*, *IEEE 2008 Silicon Nanoelectronics Workshop*

- V_{TH} of a quasi-planar bulk MOSFET can be adjusted by tuning either the dose (N_{peak}) or the depth (t_{Si}) of the retrograde doping.
  - 200 atomistic simulations were run for each nominal design.
- V_{TH} adjustment via t_{Si} tuning provides for less variation, and eliminates the trade-off with short-channel control.

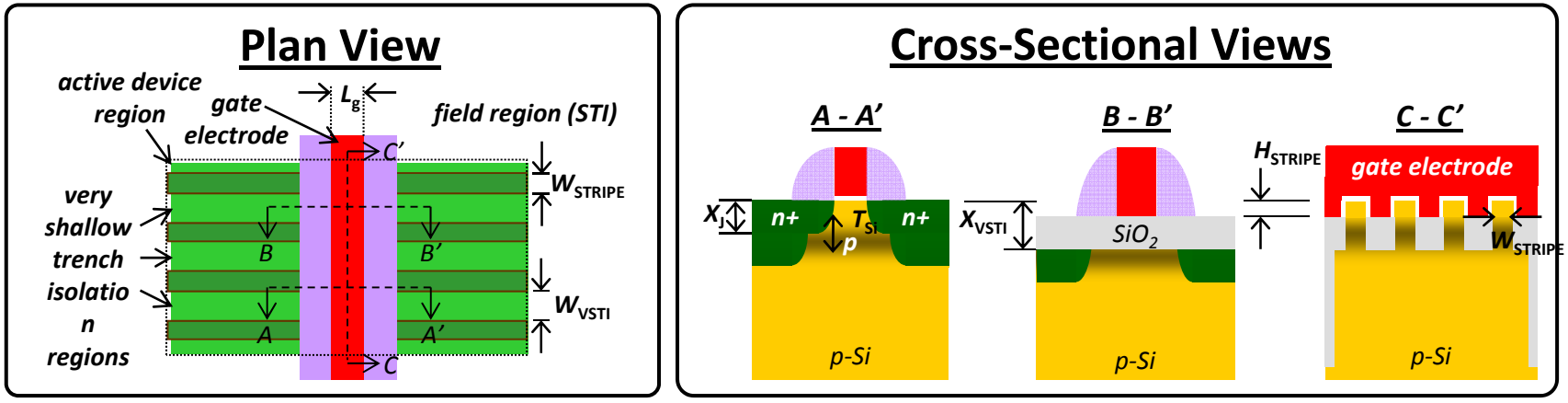
L_g = 20 nm
EOT = 0.9 nm
W_{STRIPE} = 20 nm
H_{STRIPE} = 14 nm
W_{eff} = 44 nm
t_{Si} = 14 nm
X_J = 14 nm



DIBL values for each design are indicated

Segmented-Channel MOSFET (SegFET)

- The channel is digitized into stripes of equal width, isolated by very shallow trench isolation (VSTI) oxide
  - The VSTI oxide is deeper than the source/drain extensions.
  - Device width is adjusted by adjusting the number of stripes.
  - Each stripe is a (quasi-planar) bulk MOSFET.
- The deep source/drain regions remain contiguous.

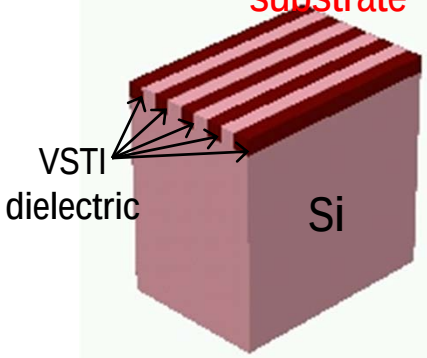


T.-J. King Liu and L. Chang, "Transistor Scaling to the Limit," in *Into the Nano Era*, H. Huff ed. (Springer), 2008.

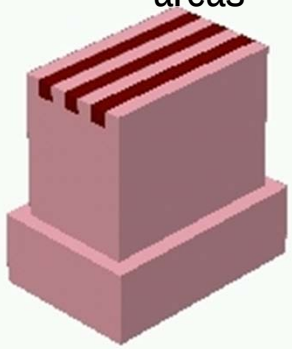
Segmented-Channel MOSFET Fabrication

T.-J. King and V. Moroz, U.S. Patent 7,265,008

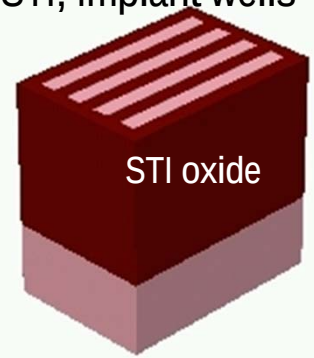
1. Start with corrugated substrate



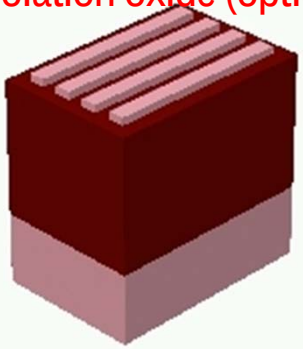
2. Define active areas



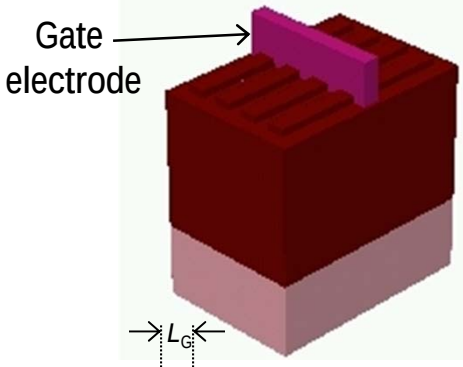
3. Fill trenches to form STI; Implant wells



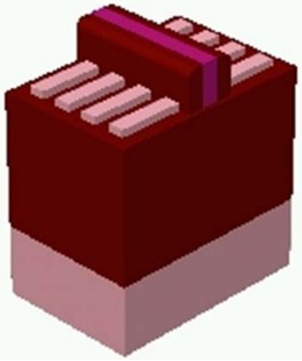
4. Slightly recess the isolation oxide (optional)



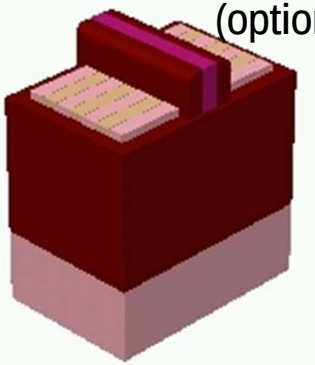
5. Implant channels; Form gate stack



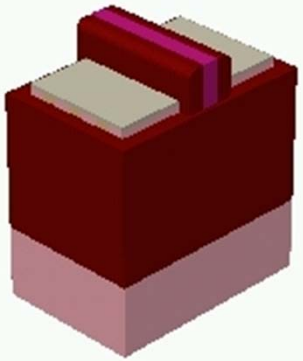
6. Form S/D extensions, then sidewall spacers

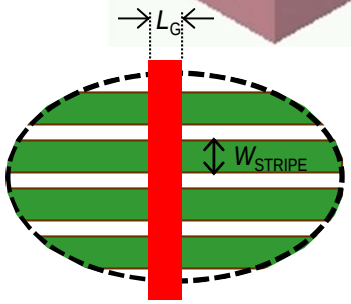


7. Embed/grow epitaxial material in S/D regions (optional)



8. Dope S/D regions; Form silicide





✓ **Precise control of channel width is achieved**

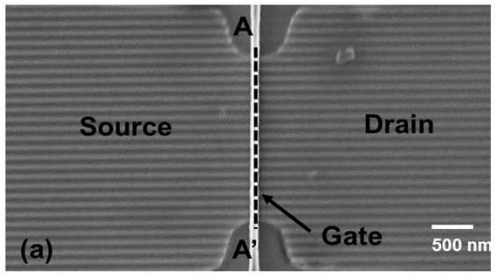
(Layout dependencies, sensitivity to misalignment are reduced)

→ **variation in MOSFET performance is reduced**

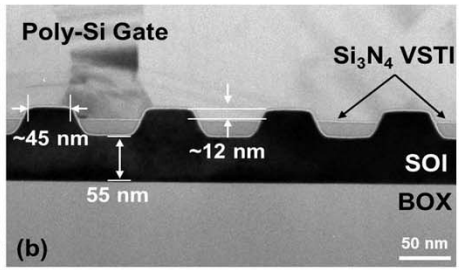
First Demonstration of SegFET

B. Ho *et al., International Semiconductor Device Research Conference* 2012

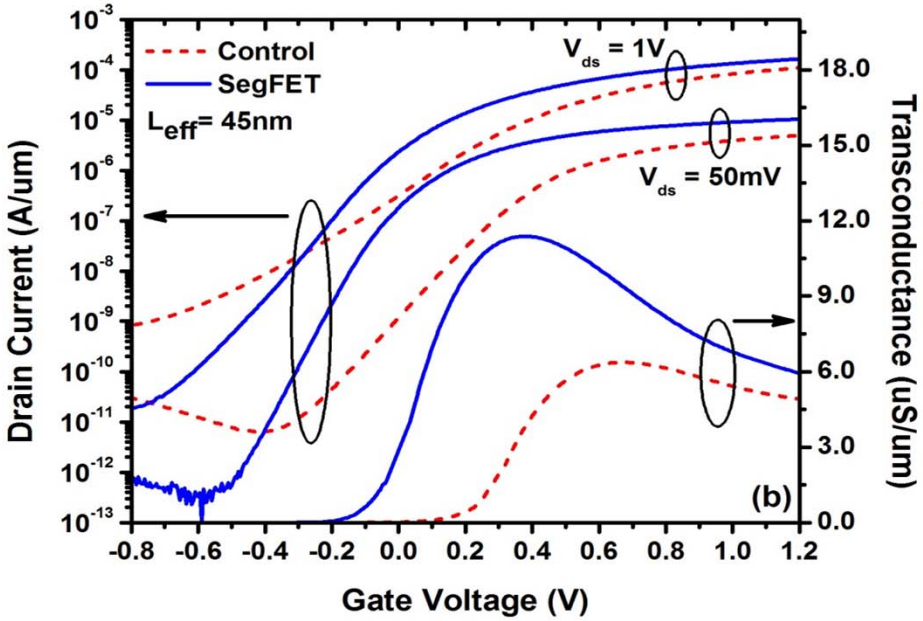
Plan-View SEM Image



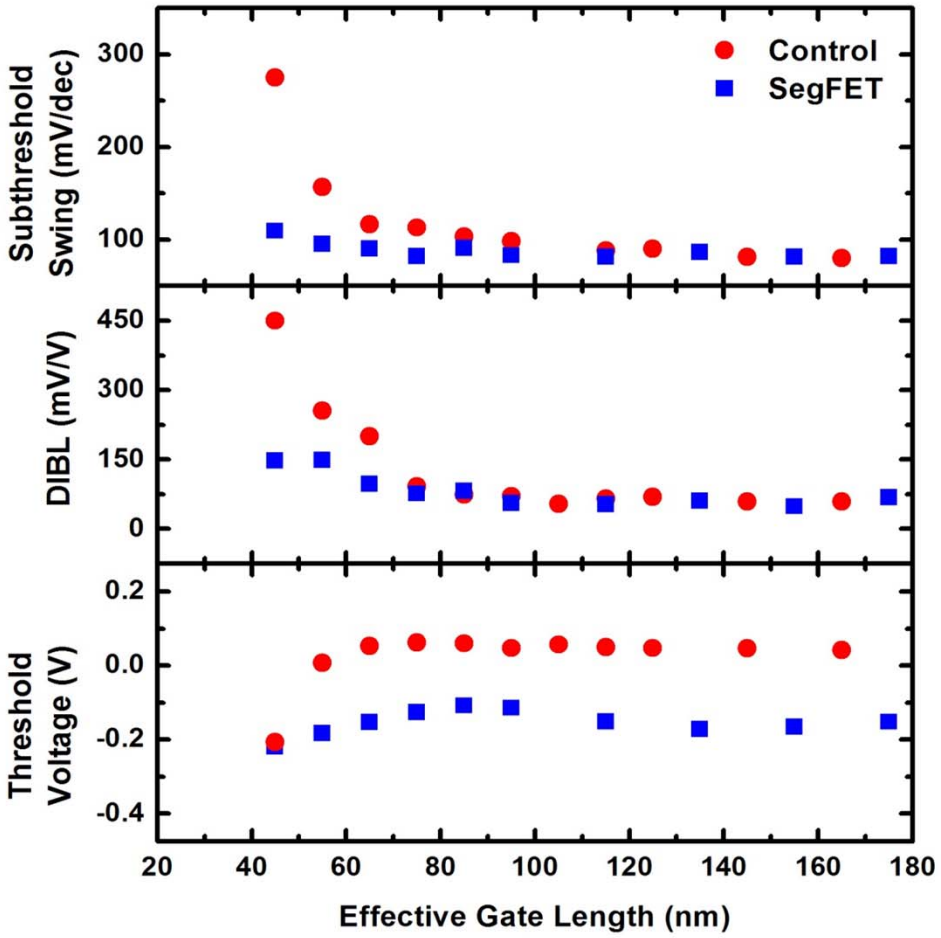
XTEM along A-A'



Measured I-V Characteristics



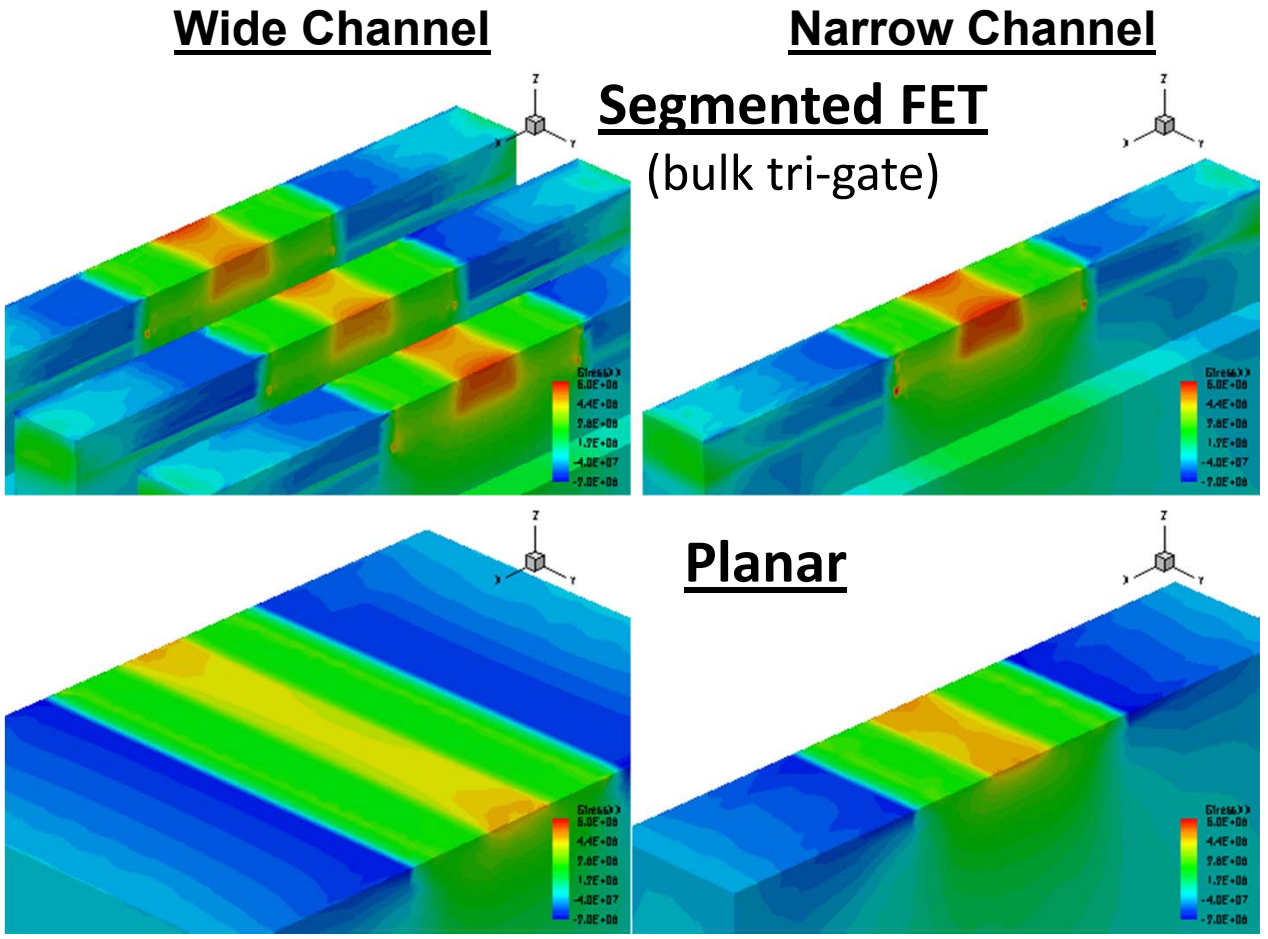
(Currents are normalized to layout width)



- **SegFETs have reduced SCE and comparable area efficiency as conventional planar MOSFETs.**

Impact of Channel Width on Strain Profile

Capping-layer-induced strain along the channel



Contact etch stop liner is assumed to be a 30nm-thick silicon nitride with 2GPa tensile stress

- SegFET parameters:
  W_{STRIPE} = 20nm
  $W_{SPACING}$ = 20nm
  H_{STRIPE} = 10nm

- L_G = 20nm
- EOT = 0.9nm
- T_{GATE} = 40nm
- L_{SPACER} = 20nm

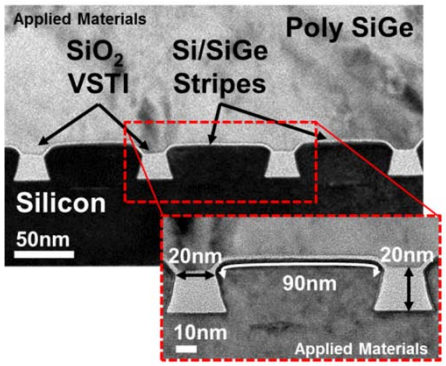
- **More stress is induced in SegFET → More mobility enhancement**
- **Reduced variation with W_{eff} for SegFET → Reduced μ_{eff} variation**

Xin Sun Ph.D. thesis, UC Berkeley, 2010

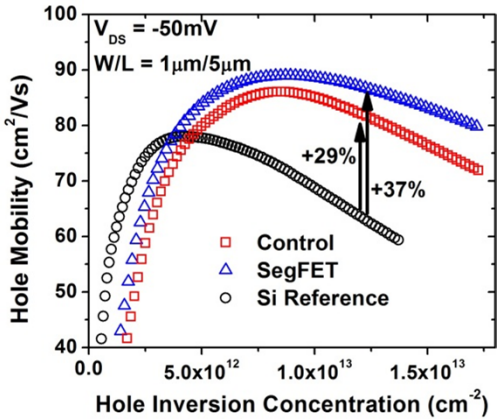
$Si_{1-x}Ge_x$ P-Channel SegFET

B. Ho *et al., Symp. VLSI Technology* 2012 (Paper 19.4)

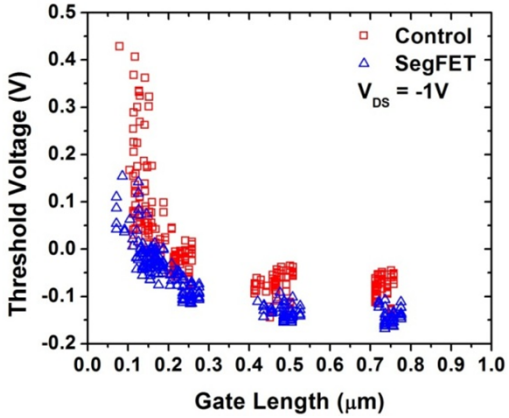
XTEM along Gate



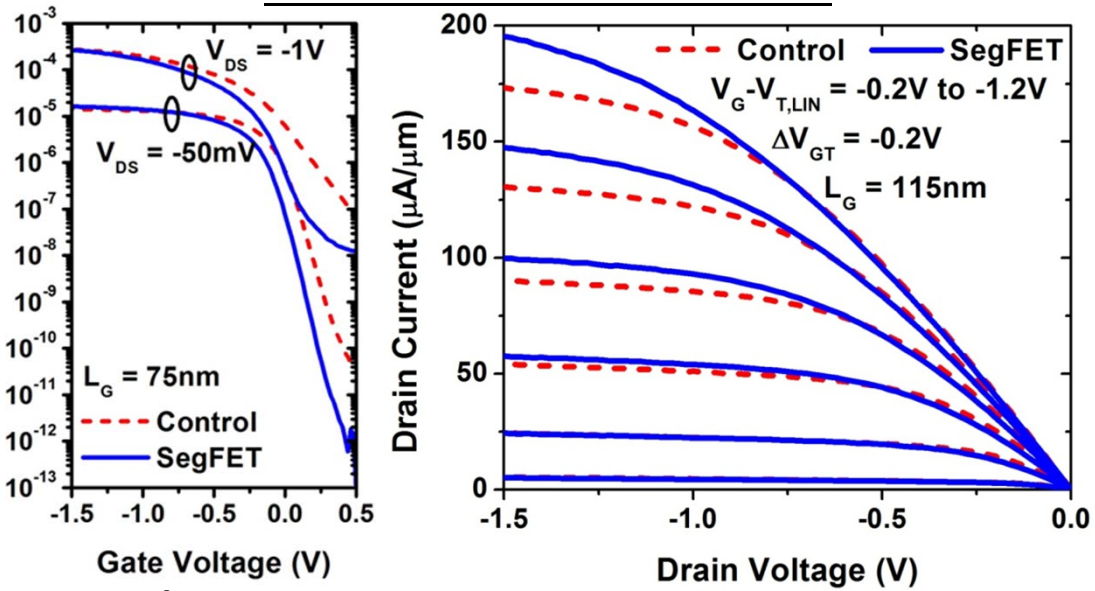
Hole Mobility



Short Channel Effect



Measured I-V Characteristics



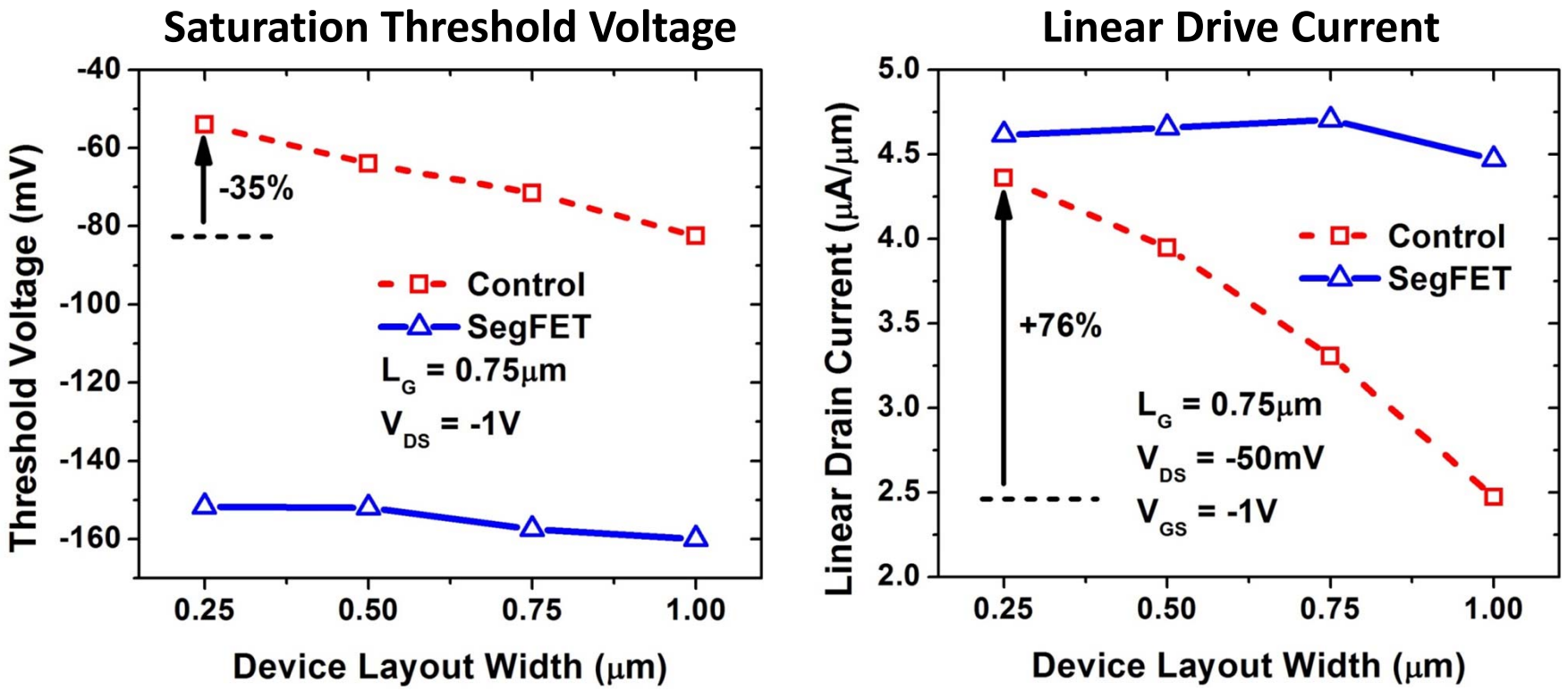
(Currents are normalized to layout width)

The SegFET exhibits

- **higher linear V_T** (due to reduced biaxial strain)
- **larger drive current per unit layout width**

Layout Width Dependence

B. Ho *et al., Symp. VLSI Technology* 2012



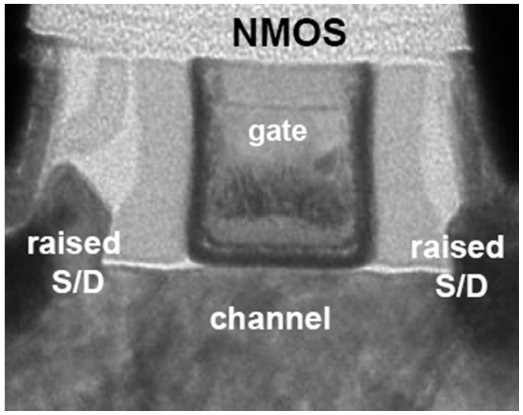
- **SegFETs show dramatically reduced narrow width effects.**

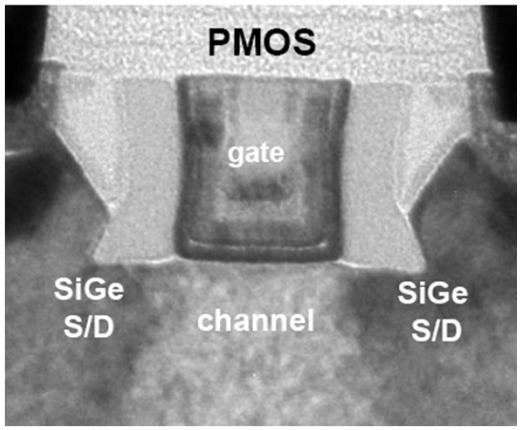
Outline

- Review: MOSFET Basics
- The Road Behind: CMOS Technology Advancement
- The Narrow Road Ahead: Thin-Body MOSFETs
- An Alternative Route: Planar Bulk MOSFET Evolution
- **Summary**

MOSFET Evolution

32 nm
planar

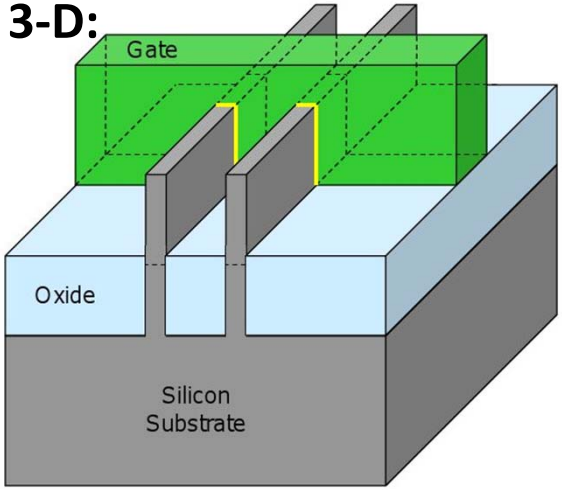




P. Packan *et al*. (Intel), *IEDM* 2009

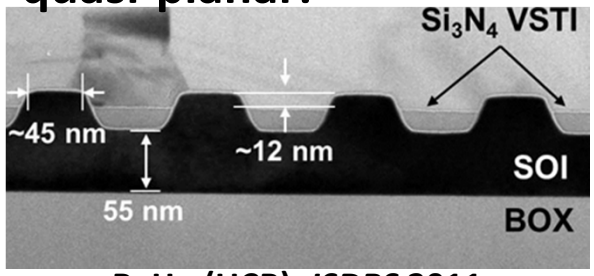
22 nm
multi-gate
segmented channel

3-D:



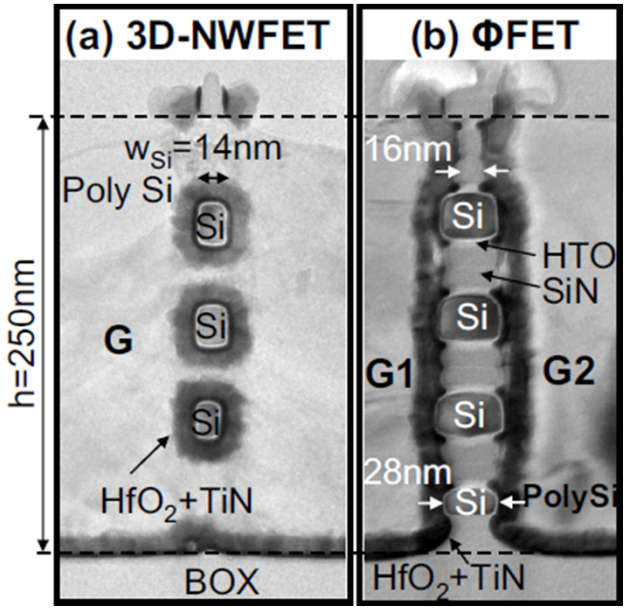
Intel Corp.

quasi-planar:



B. Ho (UCB), *ISDRS* 2011

beyond 10 nm
stacked nanowires?



C. Dupré *et al*. (CEA-LETI) *IEDM* 2008

Stacked gate-all-around (GAA) FETs achieve the highest layout efficiency.

Summary

- **Power density and variability now limit transistor scaling.**
  →Designs which achieve improved gate control are needed!
- **Thin-body MOSFET solutions are *revolutionary*, and introduce challenges for design and/or manufacturing.**
- **Quasi-planar bulk MOSFET (SegFET) technology offers an *evolutionary* (low-cost) pathway to lower V_{DD} and σ_{VTH}.**
  - **utilizes conventional (established) IC fabrication techniques**
  - **is compatible with all technologies developed for bulk CMOS**
- **Segmented-channel designs will be adopted at ≤22 nm**
  - **for lower power consumption and/or improved performance**

to enable bulk CMOS technology scaling to the end.

SegFET at a Glance

- **SegFET is a proven transistor design based on segmenting only the channel region of a standard planar MOSFET.**
- **Not a FinFET: nearly planar, *i.e.* no high-aspect-ratio fins**
  - **Uses same retrograde channel doping as a planar MOSFET to suppress the short-channel effect; allows body biasing to be used.**
- **Improves CMOS power *vs.* performance at present node; is superior to thin-body MOSFET structures for future nodes.**
- **Easiest and highest-performance approach to extend Moore's Law to the end of the technology roadmap (sub-10 nm CMOS)**
- **Inexpensive barrier to adoption**
  - **Requires one additional mask – which can be used for multiple designs**
  - **Uses existing device footprints and EDA tools**
  - **Requires no process-tool changes or new materials**

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- **Collaborators:**
  - X. Sun (now with IBM Microelectronics), C. Shin (now with U. Seoul), B. Ho (UCB)
  - V. Moroz and Q. Lu (Synopsys)
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