Segmented-Channel $Si_{1-x}Ge_x$/Si pMOSFET for Improved I_{ON} and Reduced Variability

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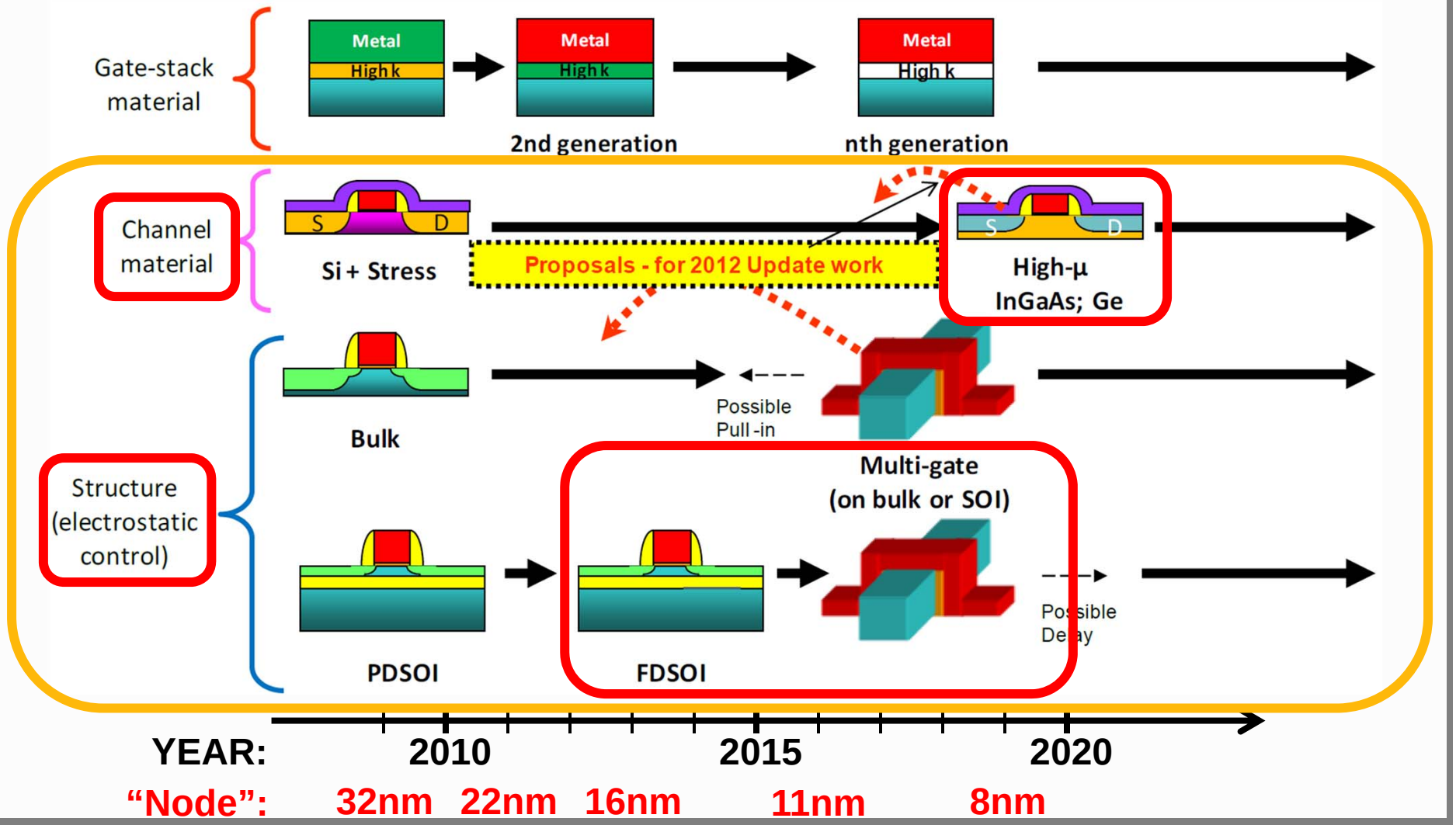
Outline

- ***Introduction***
  - Why silicon-germanium (**$Si_{1-x}Ge_x$**) ?
  - Segmented-channel MOSFET (**SegFET**) design
- Device Fabrication
  - Corrugated substrate
  - p-channel MOSFETs
- Results and Discussion
- Conclusion

Motivation

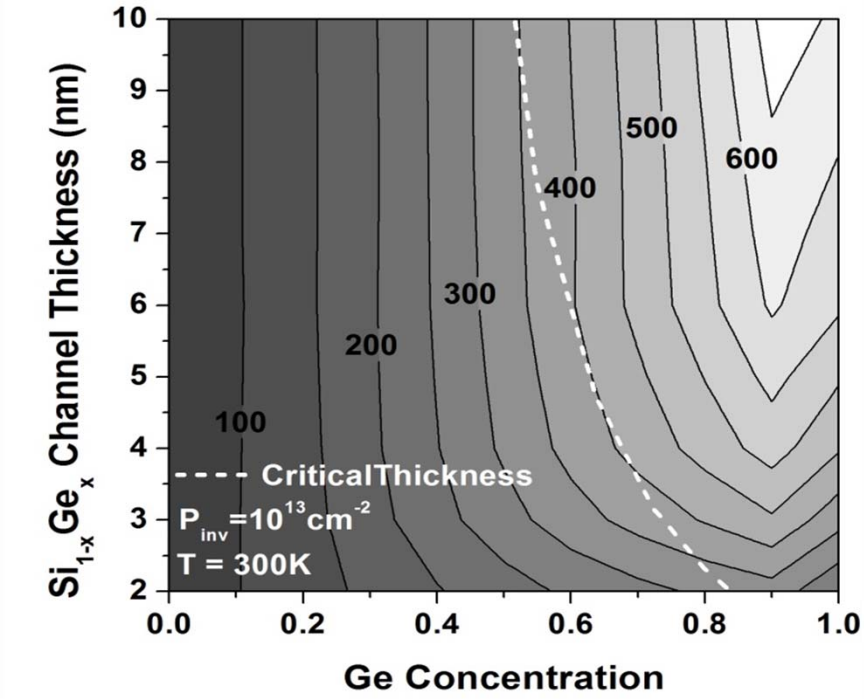
- New FET materials & structures are needed to continue scaling.



Why $Si_{1-x}Ge_x$?

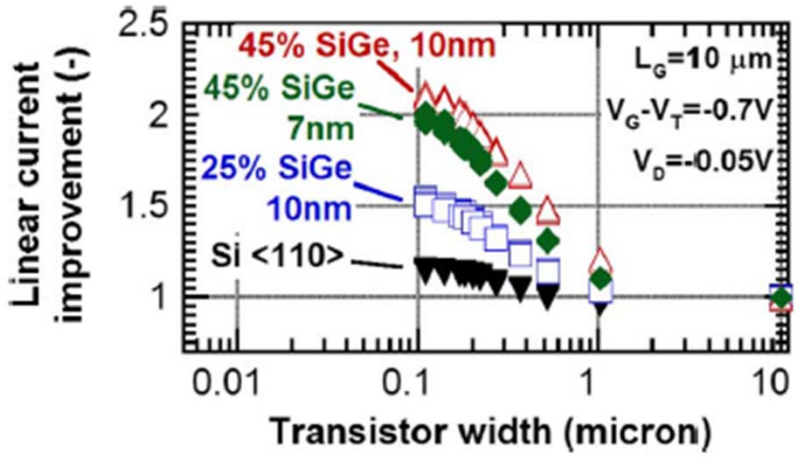
- Enhanced hole mobility …but significant width dependence

$Si/Si_{1-x}Ge_x/Si$ pMOSFET inversion-layer hole mobility



B. Ho *et al., IEEE Trans. Electron Devices,* **May 2012**

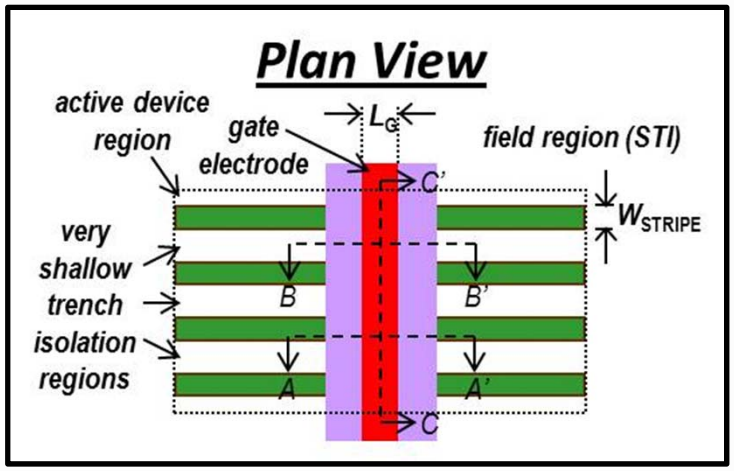
$Si/Si_{1-x}Ge_x/Si$ pMOSFET width dependence

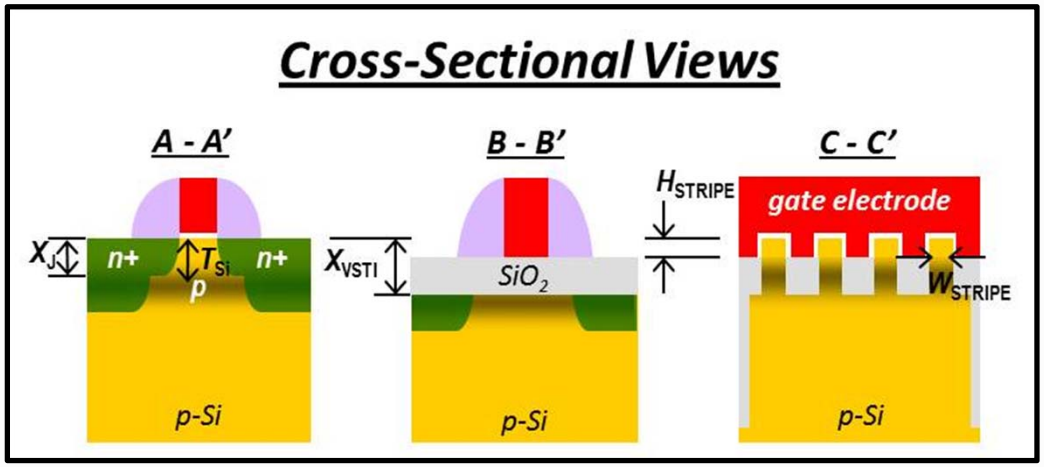


G. Eneman *et al., IEEE Trans. Electron Devices,* **August 2011**

Segmented Channel MOSFET (SegFET)

- Channel comprises parallel stripes of equal width, isolated by very shallow trench isolation (**VSTI**).
  - VSTI is much shallower than the STI between transistors
    → Source/drain regions are contiguous!
- Electrostatic control is enhanced by fringing E-fields; also, the channel stripes can be slightly elevated above the VSTI so that the gate stack wraps their top portions.

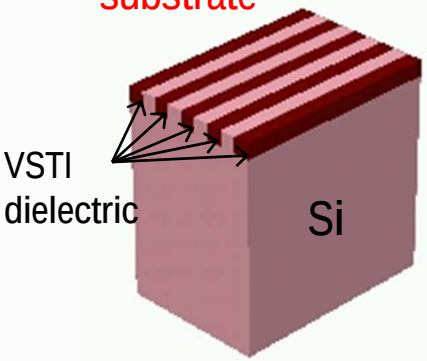




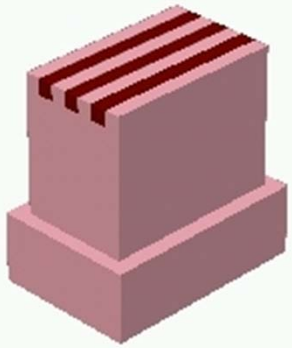
SegFET Fabrication

- Conventional CMOS process starting w/ corrugated substrate
  - Geometrically regular pattern → uniform stripe width

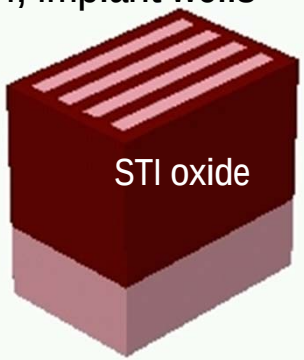
1. Start with corrugated substrate



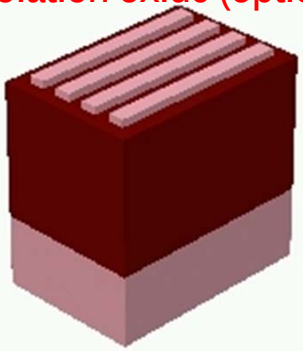
2. Define active areas



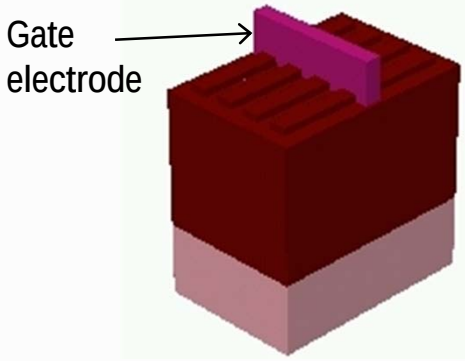
3. Fill trenches to form STI; Implant wells



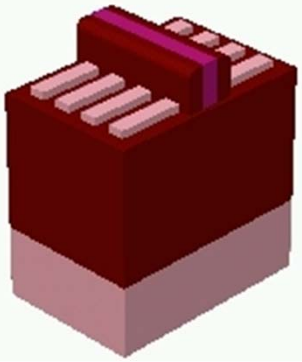
4. Slightly recess the isolation oxide (optional)



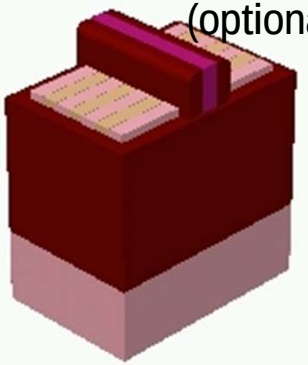
5. Implant channels; Form gate stack



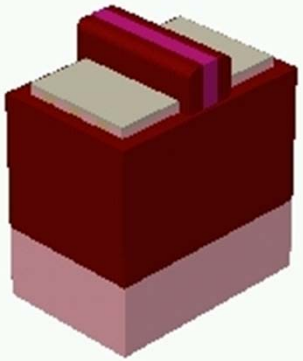
6. Form S/D extensions, then sidewall spacers



7. Embed/grow epitaxial material in S/D regions (optional)



8. Dope S/D regions; Form silicide



This Work

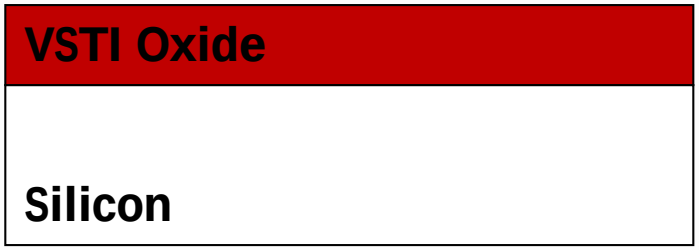
- Fabrication of segmented *vs*. conventional (non-segmented) $Si_{1-x}Ge_x$/Si pMOSFETs using the same process flow
  i.e., corrugated substrate *vs.* non-corrugated substrate
- Comparison of MOSFET drive current per unit layout width
  i.e., layout area efficiency
- Comparison of active area width dependence

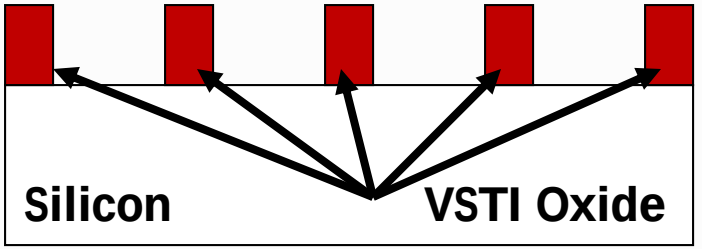
Outline

- Introduction
  - Why silicon-germanium (**$Si_{1-x}Ge_x$**) ?
  - Segmented-channel MOSFET (**SegFET**) design
- ***Device Fabrication***
  - Corrugated substrate
  - p-channel MOSFETs
- Results and Discussion
- Conclusion

Corrugated Substrate Fabrication

- Start with Si wafer substrate
- Deposit/grow VSTI oxide layer
  - 20 nm SiO_2
- Pattern VSTI layer to form 30 nm/70 nm lines/spaces (double patterning)



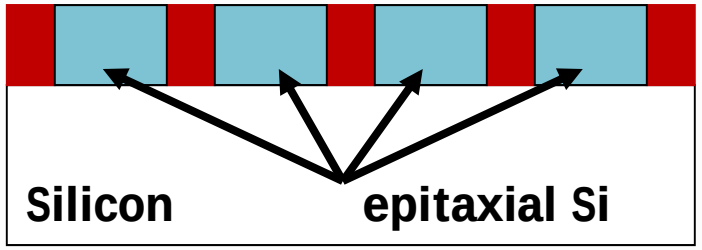


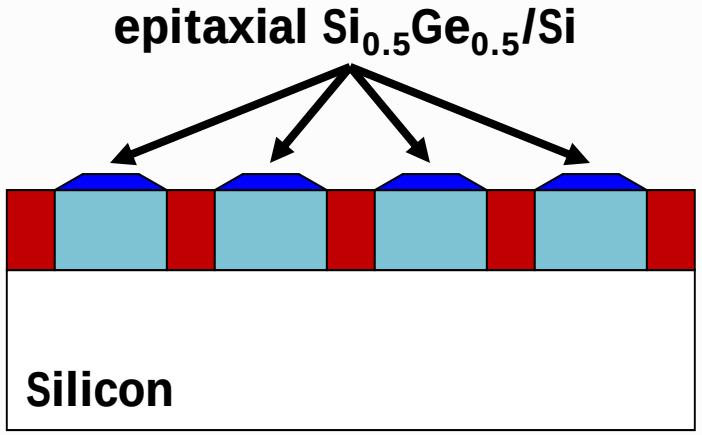
Corrugated Substrate Fabrication (cont'd)

Selectively grow silicon epitaxially, to fill trenches
- 20 nm Si

Selectively grow segmented channel regions
- 2 nm $Si_{0.5}Ge_{0.5}$
- 3 nm Si cap

pMOSFET Device Fabrication

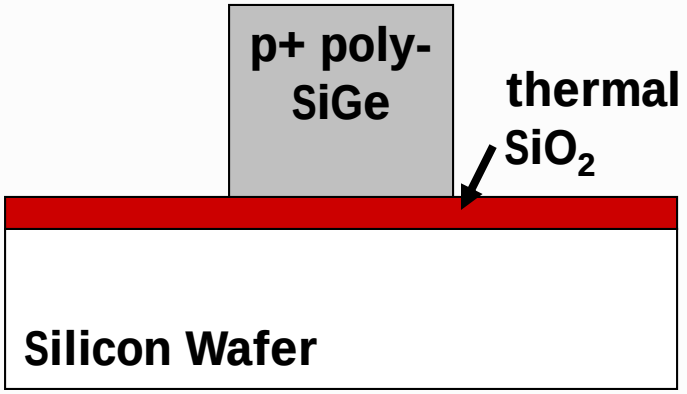


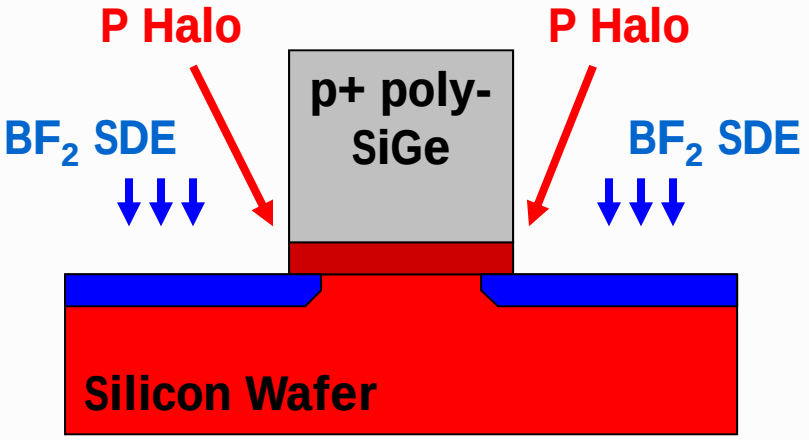


Note: Same epi growth done on planar (un-corrugated) substrates for planar control devices

p-channel MOSFET Fabrication

- Active area patterning
- Thermal oxidation (750^{O}C)
- Poly-SiGe deposition (p+)
- Gate patterning (L_G down to ~50 nm)
- Poly reoxidation
- Halo and source/drain extension implants (P, BF_2)

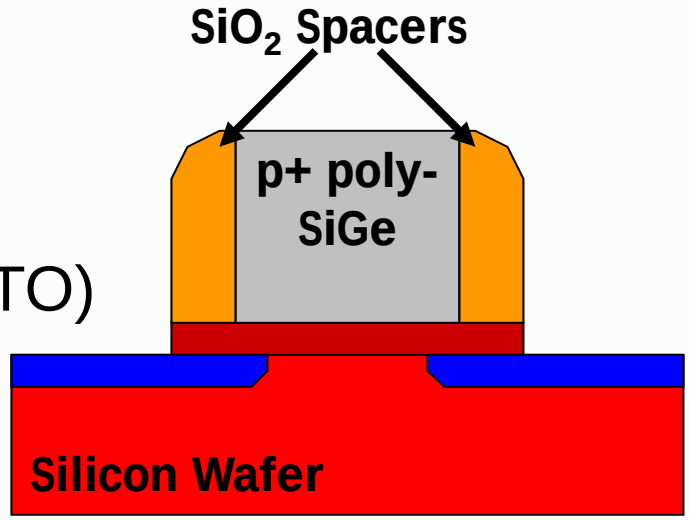


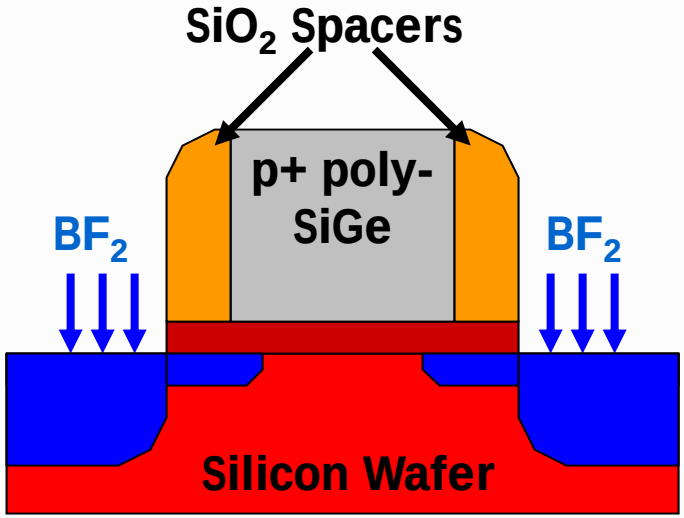


p-channel MOSFET Fabrication (cont'd)

- Spacer formation (LTO)
- Source/drain implant (BF_2)
- Passivation layer deposition (LTO)
- Thermal anneal (900^{O}C RTA)
- Contact hole formation
- Metal deposition (Al / 2% Si)
- Forming gas anneal (400^{O}C)

Note: No silicide, high-k/metal gate, or strain techniques used to boost MOSFET performance





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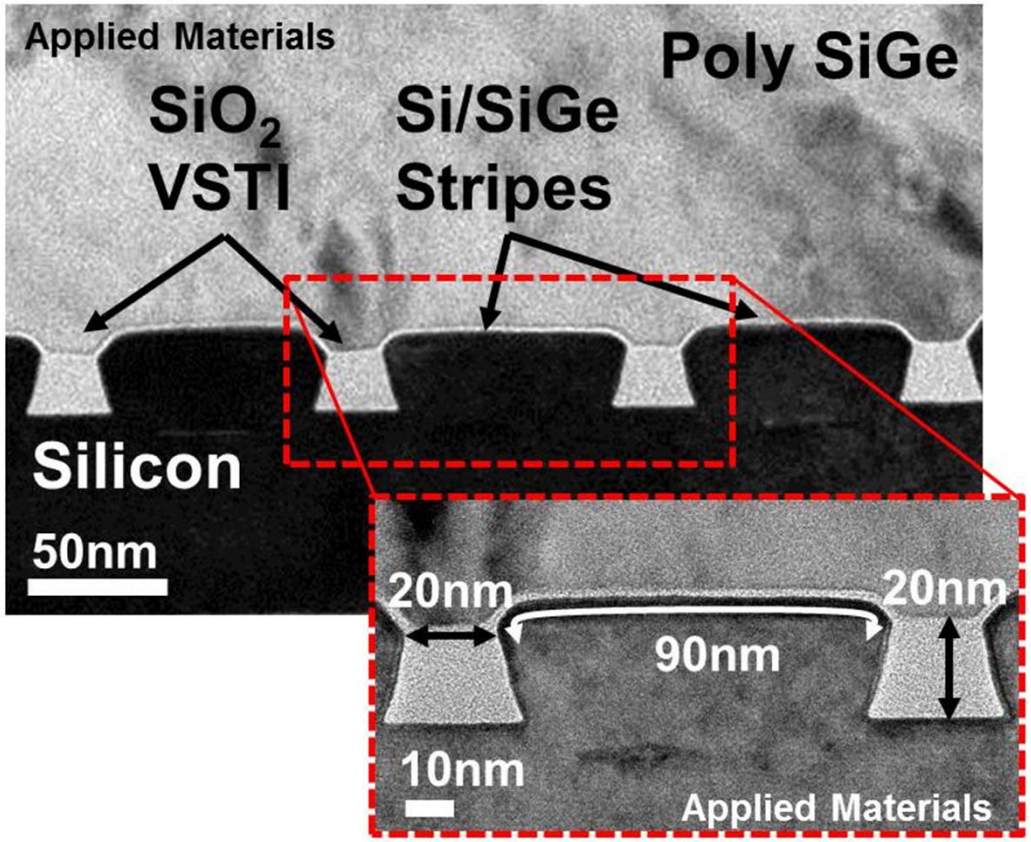
SegFET X-TEM Analysis

Cross-section along Gate electrode



- Stripe width ~ 80 nm
  - pitch = 100 nm
- Channel regions are elevated ~5 nm above VSTI

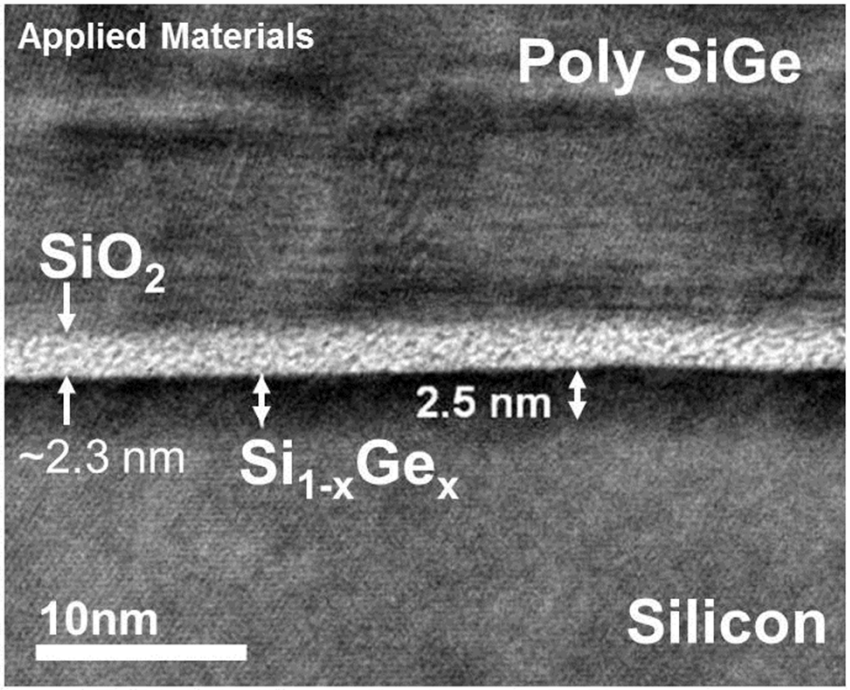
  → 90 nm effective channel width (W_{EFF}) per stripe

  → 10% lower W_{EFF} per unit layout width than non-segmented channel control device

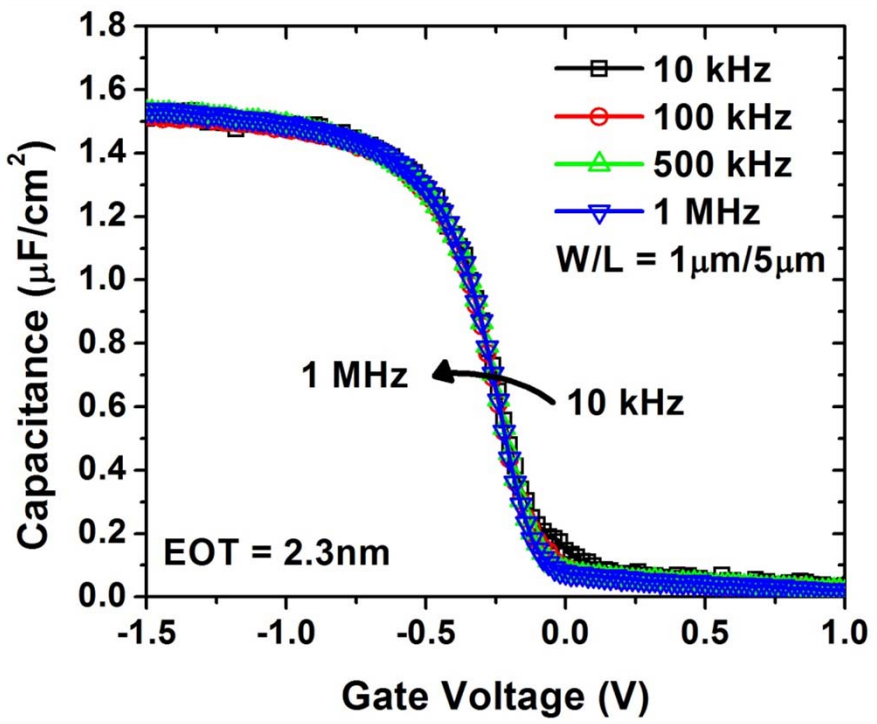
Gate Stack Characterization

- $Si_{1-x}Ge_x$ channel layer is ~2.5 nm thick.
  → Si cap layer was consumed during device fabrication.
- *C-V* indicates high-quality gate dielectric interface.

X-TEM of Gate Stack



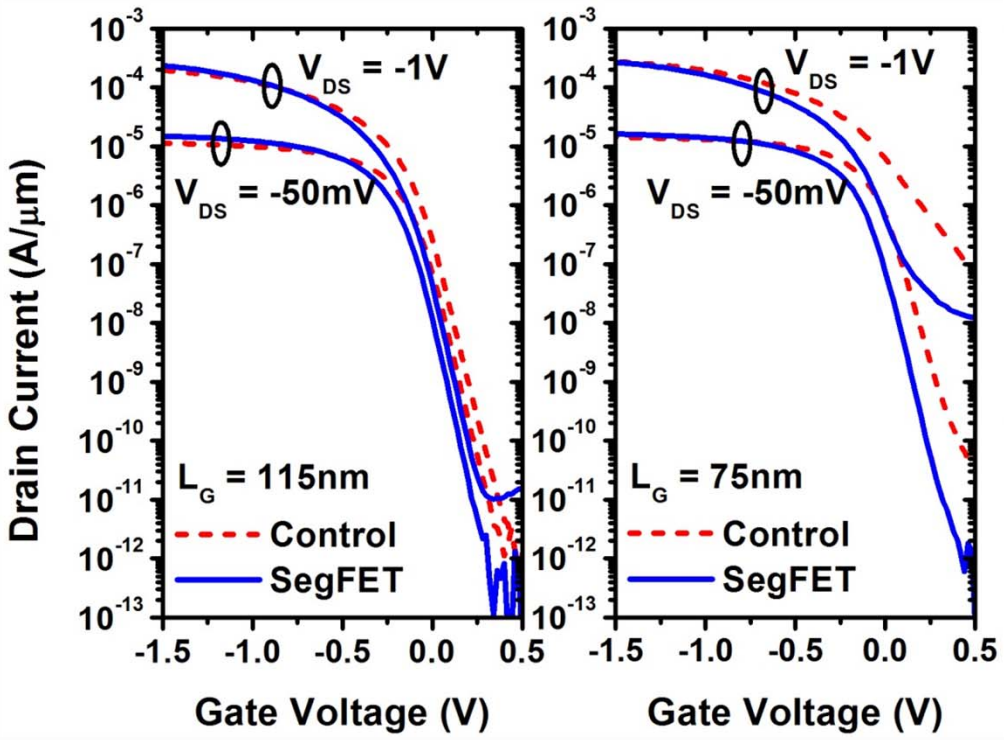
SegFET Gate Capacitance



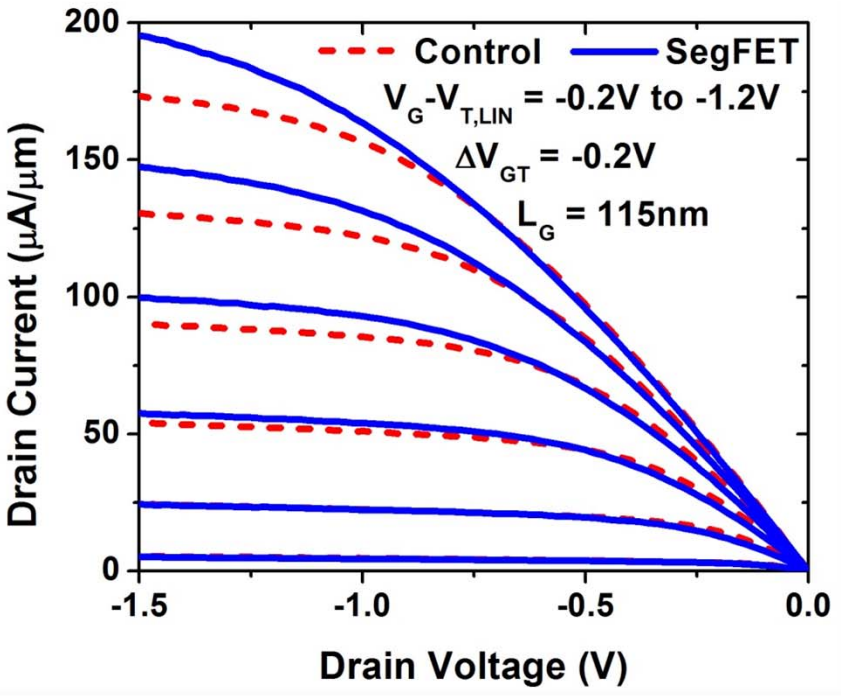
Measured Current per Unit Layout Width

- SegFET has higher linear V_T than control device.
  - possibly due to reduced biaxial (more uniaxial) strain
- SegFET has better layout area efficiency (same V_{GT}).

Transfer Characteristics

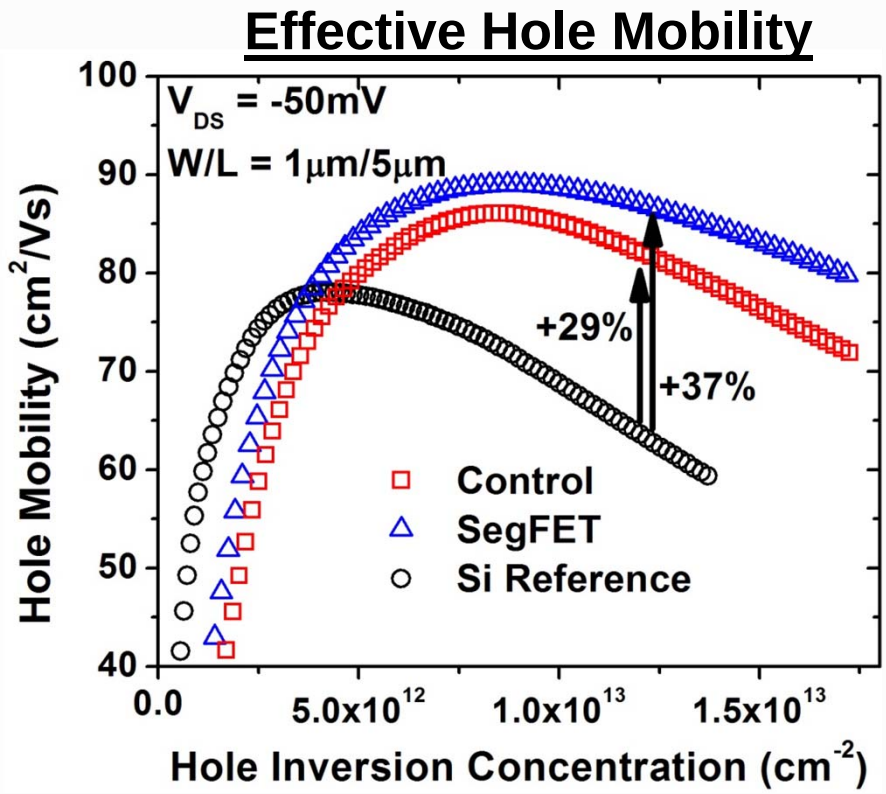


Output Characteristics



Transconductance and Mobility

- Higher effective hole mobility is seen in the SegFET, especially at higher inversion charge concentration.
  - due to different channel strain and lower transverse E-field

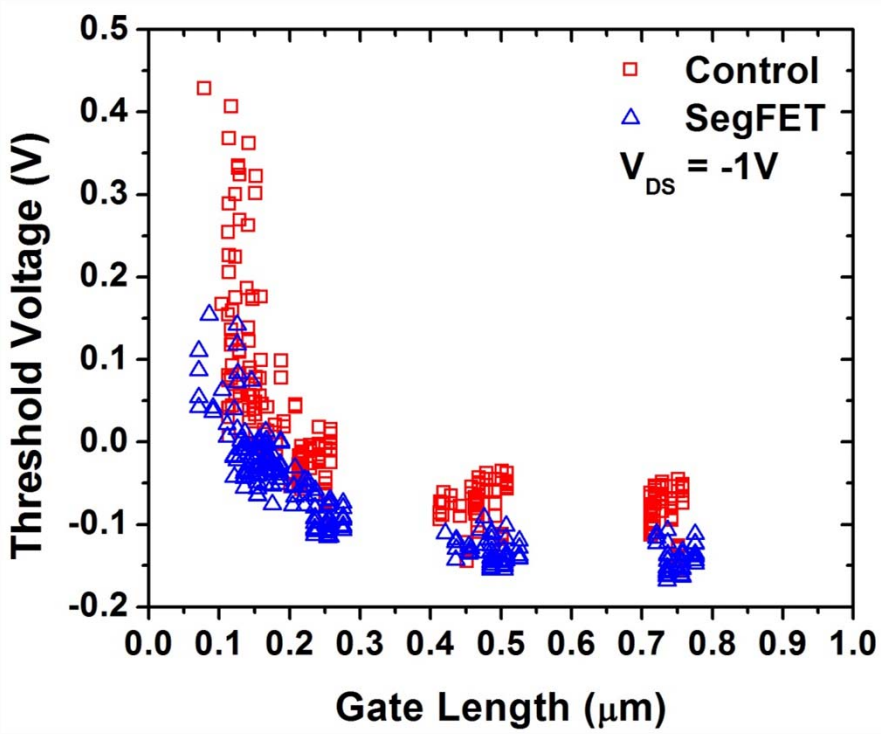


Comparison of Short-Channel Effects

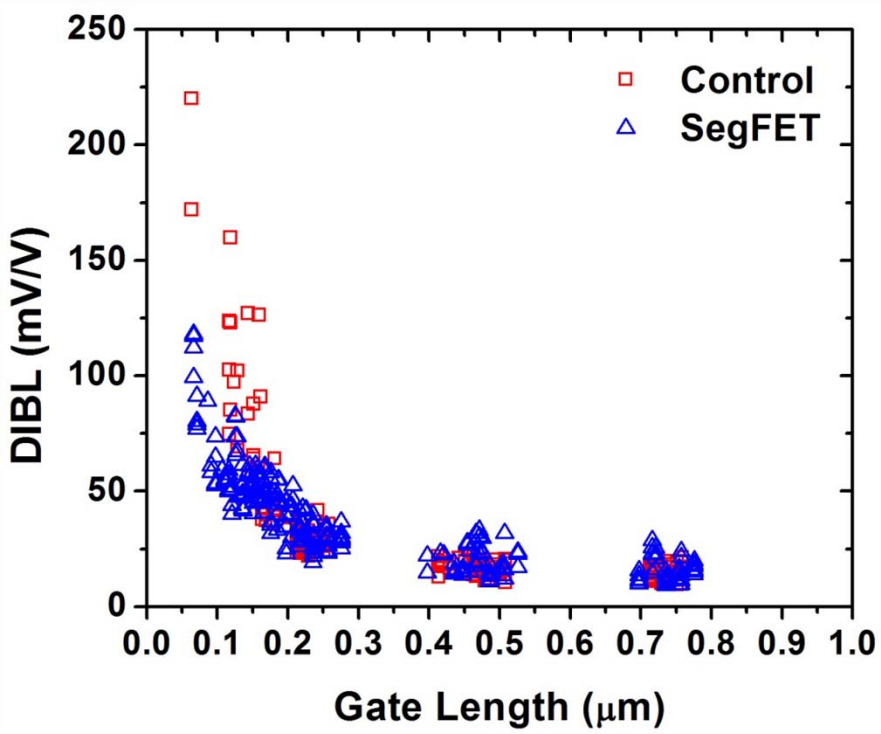
- Short-channel effects are mitigated in SegFETs

  …and can be better suppressed by recessing the VSTI oxide and/or reducing W_{STRIPE} to improve gate control

Saturation Threshold Voltage

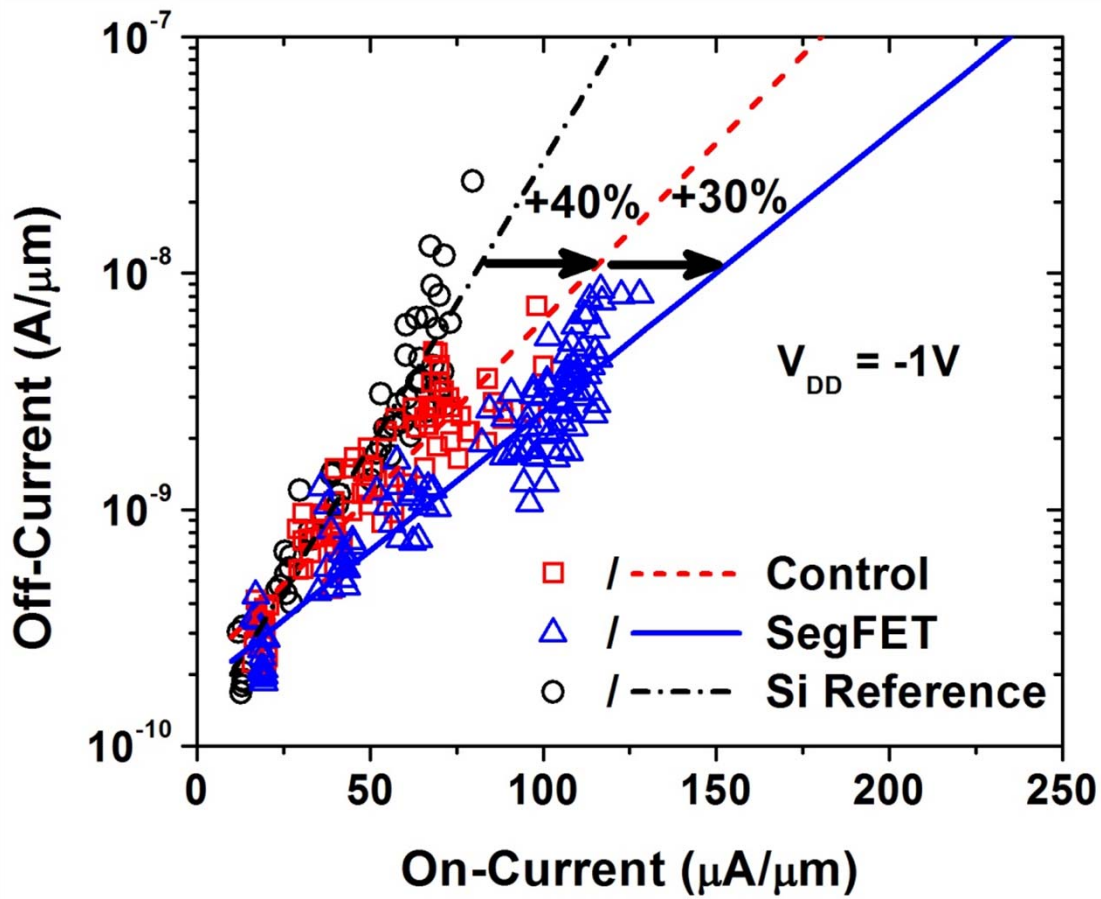


Drain-Induced Barrier Lowering



I_{OFF} *vs.* I_{ON} (normalized to layout width)

- SegFETs achieve 30% higher I_{ON} (I_{OFF} = 10nA/um)
  - higher hole mobility, lower R_{SD}, reduced short-channel effects

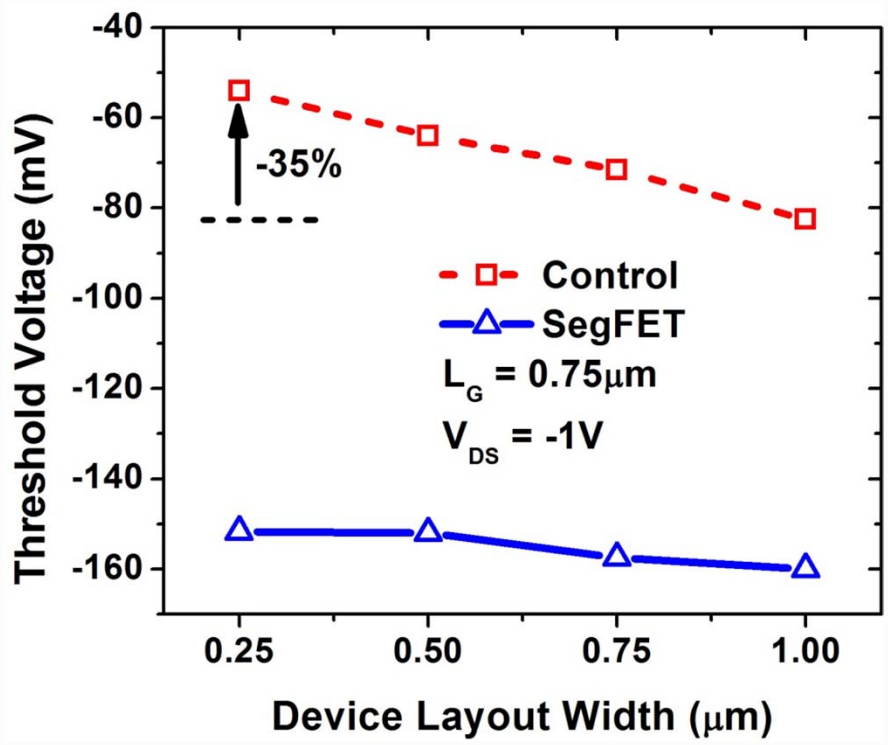


Active Area Width (W) Dependence

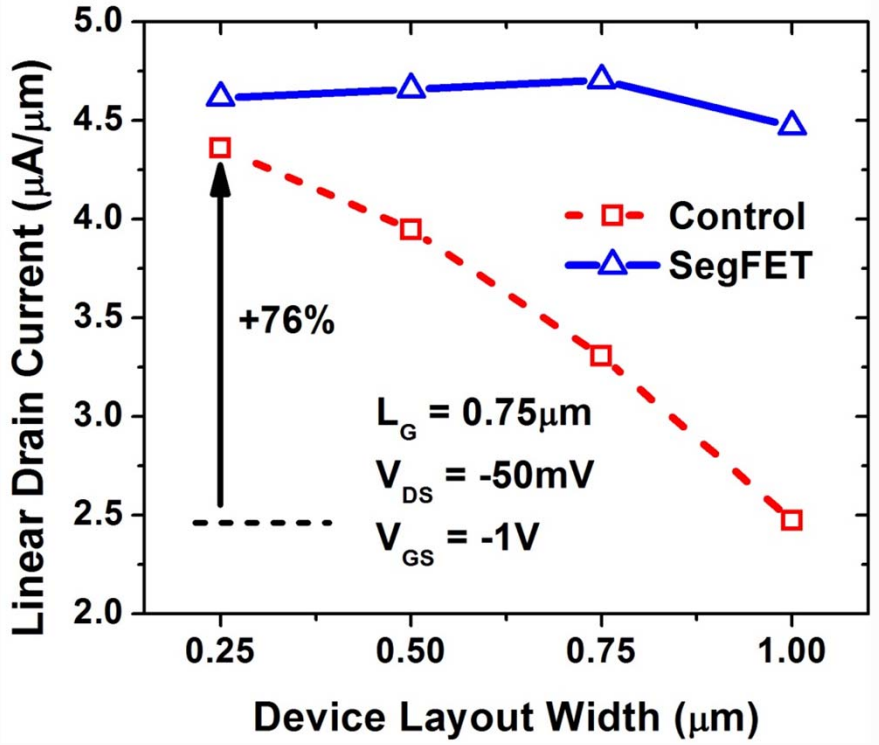
- Change in W → change in number of channel stripes
  - Each stripe has the same width (hence same V_T & current)

→ Width dependence is dramatically lower for SegFET

Saturation Threshold Voltage



Linear Drive Current



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Conclusion

- Corrugated substrate technology is advantageous for fabrication of $Si_{1-x}Ge_x$/Si pMOSFETs using a conventional process flow:
  - ✓ Higher hole mobility
  - ✓ Improved electrostatic control
  - ✓ Dramatically reduced dependence on active area width

→Higher performance and reduced variability

…facilitating continued scaling

Acknowledgements

- Semiconductor Research Corporation
  - GRC Graduate Fellowship
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- UC Berkeley Marvell Nanofabrication Laboratory