Sanjit A. Seshia

Curriculum Vitae

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Research Interests

Dependable Computing, Computational Logic, Formal Methods, Embedded/Cyber-Physical Systems, Computer Security, Electronic Design Automation, Synthetic Biology, Theory.

Academic Appointments

07/2011-date **University of California, Berkeley**, USA
Associate Professor
Department of Electrical Engineering and Computer Sciences
Group in Logic and the Methodology of Science

02/2013-05/2013 **Massachusetts Institute of Technology**, USA
Visiting professor
Computer Science and Artificial Intelligence Laboratory

07/2005-06/2011 **University of California, Berkeley**, USA
Assistant Professor
Department of Electrical Engineering and Computer Sciences

Education

1998-2005 **Carnegie Mellon University**, Pittsburgh, USA

- ***Ph.D. in Computer Science*** (May 2005)
  Thesis: Adaptive Eager Boolean Encoding for Arithmetic Reasoning in Verification
  Advisor: Prof. Randal E. Bryant
  Committee: Prof. Randal E. Bryant, Prof. Edmund M. Clarke, Prof. Jeannette M. Wing, and Prof. David L. Dill
- ***M.S. in Computer Science*** (August 2000)

1994-1998 **Indian Institute of Technology Bombay**, India

- ***B.Tech. in Computer Science & Engineering*** (May 1998)
  GPA: 9.44/10
  Thesis: Multisensor Image Alignment and Fusion
  Advisors: Prof. Sharat Chandran and Prof. Rakesh Lal

Selected Awards and Honors

- Prof. R. Narasimhan Lecture Award, Tata Institute of Fundamental Research, India (2013)

- Presidential Early Career Award for Scientists and Engineers – PECASE
  Awarded by the White House in 2008; one of 67 awardees nation-wide in all fields of science and engineering
- Alfred P. Sloan Research Fellowship (2008)
- Hellman Family Faculty Fund Award, UC Berkeley (2008)
- NSF CAREER Award (2007)
- School of Computer Science Distinguished Dissertation Award, Carnegie Mellon University (2005)
  Nominated for 2005 ACM Doctoral Dissertation Award
- National Defense Science and Engineering Graduate (NDSEG) Fellowship (1999-2002)
- Indian National Mathematics Olympiad Awardee (1993)
- National Talent Search (NTS) Scholarship, India (1992-1998)

Previous Work Experience

Carnegie Mellon University, Pittsburgh, PA, USA
Graduate Research Assistant — September 1998 – May 2005
Teaching Assistant — Fall 1999 & Fall 2001

Compaq/HP Systems Research Center, Palo Alto, CA, USA
Intern — May 2001 – August 2001
Consultant — September 2001 – May 2002

Cadence Berkeley Laboratories, Berkeley, CA, USA
Intern — May 1999 – August 1999

Indian Institute of Technology Bombay, Mumbai, India
Undergraduate Research Assistant — January 1997 – June 1998

Tata Institute of Fundamental Research, Mumbai, India
Intern, Visiting Student Research Program — May 1997 – July 1997

Publications

(Electronic copies of papers are available at http://www.eecs.berkeley.edu/~sseshia/#pubs.)

Books, Book Chapters, Edited Volumes, and Ph.D. Thesis

- *Introduction to Embedded Systems: A Cyber-Physical Systems Approach*,
  Edward A. Lee and Sanjit A. Seshia,
  Second Edition, http://LeeSeshia.org, 2015.
  – First Edition published in 2011.
- *An Introductory Lab in Embedded and Cyber-Physical Systems*,
  Jeff C. Jensen, Edward A. Lee and Sanjit A. Seshia,
  First Edition, http://LeeSeshia.org/lab/, 2014.
- *Modeling for Verification*,
  Sanjit A. Seshia, Natasha Sharygina, and Stavros Tripakis,
  Chapter in Handbook of Model Checking, Springer-Verlag, 2014.
- *Satisfiability Modulo Theories*,
  Clark Barrett, Roberto Sebastiani, Sanjit A. Seshia, and Cesare Tinelli,
  Chapter in Handbook of Satisfiability, IOS Press, 2009.

- *Proceedings of the 24th International Conference on Computer Aided Verification (CAV)*,
  P. Madhusudan and Sanjit A. Seshia (editors),
  LNCS vol. 7358, Berkeley, CA, USA, July 7-13, 2012.
- *Adaptive Eager Boolean Encoding for Arithmetic Reasoning in Verification*,
  Sanjit A. Seshia,
  Ph.D. Thesis, Carnegie Mellon University, May 2005.
  Co-winner, 2005 SCS Distinguished Dissertation Award.

Refereed Conference and Journal Papers

1. Xiaoqing Jin, Alexandre Donzé, Jyotirmoy Deshmukh, and Sanjit A. Seshia,
   Mining Requirements from Closed-Loop Control Models,
   IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, to appear.
   Conference version in Proceedings of the International Conference on Hybrid Systems: Computation and Control (HSCC), April 2013, pages 43–52.
2. Jyotirmoy Deshmukh, Alexandre Donzé, Shromona Ghosh, Xiaoqing Jin, Garvit Juniwal, and Sanjit A. Seshia,
   Robust Online Monitoring of Signal Temporal Logic,
   In Proceedings of the International Conference on Runtime Verification (RV), September 2015.
3. Ankush Desai, Shaz Qadeer, and Sanjit A. Seshia,
   Systematic Testing of Asynchronous Reactive Systems,
   In Proceedings of the ACM SIGSOFT Symposium on the Foundations of Software Engineering (FSE), August 2015.
4. Yasser Shoukry, Alberto Puggelli, Pierluigi Nuzzo, Alberto L. Sangiovanni-Vincentelli, Sanjit A. Seshia, and Paulo Tabuada,
   Sound and Complete State Estimation for Linear Dynamical Systems Under Sensor Attacks Using Satisfiability Modulo Theory Solving,
   In Proceedings of the American Control Conference (ACC), July 2015.
   Extended version: Arxiv.org technical report, vol. 1412.4324, December 2014.
5. Ankush Desai, Sanjit A. Seshia, Shaz Qadeer, David Broman, and John C. Eidson,
   Approximate Synchrony: An Abstraction for Distributed Almost-Synchronous Systems,
   In Proceedings of the 27th International Conference on Computer-Aided Verification (CAV), July 2015.
   Extended version: Technical report UCB/EECS-2015-158, EECS Department, UC Berkeley, May 2015.
6. Vasumathi Raman, Alexandre Donzé, Dorsa Sadigh, Richard M. Murray, and Sanjit A. Seshia,
   Reactive Synthesis from Signal Temporal Logic Specifications,
   In Proceedings of the 8th International Conference on Hybrid Systems: Computation and Control (HSCC), April 2015, pages 239–248.
7. Supratik Chakraborty, Daniel J. Fremont, Kuldeep S. Meel, Sanjit A. Seshia, and Moshe Y. Vardi,
   On Parallel Scalable Uniform SAT Witness Generation,
   In Proceedings of the 21st International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), April 2015, pages 304–319.
8. Garvit Juniwal, Sakshi Jain, Alexandre Donzé, and Sanjit A. Seshia,
   Clustering-Based Active Learning for CPSGrader,
   In Proceedings of the Second ACM Conference on Learning @ Scale (L@S), March 2015, pages 399–403.
9. Vasumathi Raman, Alexandre Donzé, Mehdi Maasoumy, Richard M. Murray, Alberto Sangiovanni-Vincentelli, and Sanjit A. Seshia,
   Model Predictive Control with Signal Temporal Logic Specifications,

In Proceedings of the 53rd IEEE Conference on Decision and Control (CDC), December 2014, pages 81–87.

10. Dorsa Sadigh, Eric S. Kim, Samuel Coogan, Shankar Sastry, and Sanjit A. Seshia,
A Learning Based Approach to Control Synthesis of Markov Decision Processes for Linear Temporal Logic Specifications,
In Proceedings of the 53rd IEEE Conference on Decision and Control (CDC), December 2014, pages 1091–1096.
11. Garvit Juniwal, Alexandre Donzé, Jeff C. Jensen, and Sanjit A. Seshia,
CPSGrader: Synthesizing Temporal Logic Testers for Auto-Grading an Embedded Systems Laboratory,
In Proceedings of the 14th International Conference on Embedded Software (EMSOFT), October 2014, pages 24:1–24:10.
12. Alberto Puggelli, Alberto Sangiovanni-Vincentelli, and Sanjit A. Seshia,
Robust Strategy Synthesis for Probabilistic Systems Applied to Risk-Limiting Renewable-Energy Pricing,
In Proceedings of the 14th International Conference on Embedded Software (EMSOFT), October 2014, pages 13:1–13:10.
13. Susmit Jha, Krishnendu Chatterjee, Sanjit A. Seshia, and Stavros Tripakis,
Game-Theoretic Secure Localization in Wireless Sensor Networks,
In Proceedings of the 4th International Conference on the Internet of Things (IoT), October 2014.
14. Daniel Holcomb and Sanjit A. Seshia,
Compositional Performance Verification of Network-on-Chip Designs,
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, September 2014, Vol. 33, Num. 9, pages 1370–1383.
15. Indranil Saha, Rattanachai Ramaithitima, Vijay Kumar, George J. Pappas, and Sanjit A. Seshia,
Automated Composition of Motion Primitives for Multi-Robot Systems from Safe LTL Specifications,
In Proceedings of the IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS), September 2014, pages 1525–1532.
16. Alexandre Donzé, Rafael Valle, Ilge Akkaya, Sophie Libkind, Sanjit A. Seshia, and David Wessel,
Machine Improvisation with Formal Specifications,
In Proceedings of the 40th International Computer Music Conference (ICMC), September 2014, pages 1277–1284.
17. David Broman, Patricia Derler, Ankush Desai, John C. Eidson, and Sanjit A. Seshia,
Endlessly Circulating Messages in IEEE 1588-2008 Systems, In Proceedings of the 8th International IEEE Symposium on Precision Clock Synchronization for Measurement, Control and Communication (ISPCS), September 2014, pages 7–12.
18. Dorsa Sadigh, Henrik Ohlsson, S. Shankar Sastry, and Sanjit A. Seshia,
Robust Subspace System Identification via Weighted Nuclear Norm Optimization,
In Proceedings of the 19th World Congress of the International Federation of Automatic Control (IFAC), August 2014, pages 9510–9515.
19. Supratik Chakraborty, Daniel J. Fremont, Kuldeep S. Meel, Sanjit A. Seshia and Moshe Y. Vardi,
Distribution-Aware Sampling and Weighted Model Counting for SAT,
In Proceedings of the 28th AAAI Conference on Artificial Intelligence (AAAI), July 2014, pages 1722–1730.
20. Wei Yang Tan, Rohit Sinha, John Manferdelli, and Sanjit A. Seshia,
Formal Modeling and Verification of CloudProxy,
In 6th Working Conference on Verified Software: Theories, Tools, and Experiments (VSTTE), July 2014,

pages 87–104.

21. Wenchao Li, Dorsa Sadigh, S. Shankar Sastry, and Sanjit A. Seshia,
Synthesis for Human-in-the-Loop Control Systems,
In Proceedings of the 20th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), April 2014, pages 470–484.
22. Ashish Tiwari, Bruno Dutertre, Dejan Jovanovic, Thomas de Candia, Patrick Lincoln, John M. Rushby, Dorsa Sadigh, and Sanjit A. Seshia,
Safety Envelope for Security,
In Proceedings of the 3rd International Conference on High Confidence Networked Systems (HiCoNS), April 2014, pages 85–94.
23. Pramod Subramanyan, Nestan Tsiskaridze, Wenchao Li, Adria Gascon, Wei Yang Tan, Ashish Tiwari, Natarajan Shankar, Sanjit A. Seshia, and Sharad Malik,
Reverse Engineering Digital Circuits Using Structural and Functional Analyses,
IEEE Transactions on Emerging Topics in Computing (TETC), March 2014, Vol. 2, Num. 1, pages 63–80.
24. Pierluigi Nuzzo, Huan Xu, Necmiye Ozay, John B. Finn, Alberto L. Sangiovanni-Vincentelli, Richard M. Murray, Alexandre Donzé, Sanjit A. Seshia,
A Contract-Based Methodology for Aircraft Electric Power System Design,
IEEE Access, January 2014, Vol. 2, pages 1–25.
25. Rüdiger Ehlers, Sanjit A. Seshia, and Hadas Kress-Gazit,
Synthesis with Identifiers,
In Proceedings of the 15th International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI), January 2014, pages 415–433.
26. Cynthia Sturton, Rohit Sinha, Thurston H.Y. Dang, Sakshi Jain, Michael McCoyd, Wei-Yang Tan, Petros Maniatis, Sanjit A. Seshia, and David Wagner,
Symbolic Software Model Validation,
In Proceedings of the 10th ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), October 2013, pages 97–108.
27. Alberto Puggelli, Wenchao Li, Alberto Sangiovanni-Vincentelli, and Sanjit A. Seshia,
Polynomial-Time Verification of PCTL Properties of MDPs with Convex Uncertainties,
In Proceedings of the 25th International Conference on Computer-Aided Verification (CAV), July 2013, pages 527–542.
28. Wenchao Li, Adria Gascon, Pramod Subramanyan, Wei Yang Tan, Ashish Tiwari, Sharad Malik, Natarajan Shankar, and Sanjit A. Seshia,
WordRev: Finding Word-Level Structures in a Sea of Bit-Level Gates,
In Proceedings of the IEEE Conference on Hardware-Oriented Security and Trust (HOST), June 2013, pages 67–74.
29. Rohit Sinha, Cynthia Sturton, Petros Maniatis, Sanjit A. Seshia, and David Wagner,
Verification with Small and Short Worlds,
In Proceedings of the IEEE Conference on Formal Methods in Computer-Aided Design (FMCAD), October 2012, pages 68–77.
30. Wenchao Li and Sanjit A. Seshia,
Sparse Coding for Specification Mining and Error Localization,
In Proceedings of the International Conference on Run-time Verification (RV), September 2012, pages 64–81.
31. Daniel Holcomb, Alexander Gotmanov, Michael Kishinevsky, and Sanjit A. Seshia,

Compositional Performance Verification of NoC Designs,
In Proceedings of the 10th ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), pages 1–10, July 2012.

32. Wenchao Li, Sanjit A. Seshia, and Somesh Jha,
CrowdMine: Towards Crowdsourced Human-Assisted Verification,
In Proceedings of the Design Automation Conference (DAC), pages 1254–1255, June 2012.
33. Sanjit A. Seshia,
Sciduction: Combining Induction, Deduction, and Structure for Verification and Synthesis,
In Proceedings of the Design Automation Conference (DAC), pages 356–365, June 2012.
Extended version: Technical report UCB/EECS-2011-68, EECS Department, UC Berkeley, May 2011.
34. Wenchao Li, Zach Wasson, and Sanjit A. Seshia,
Reverse Engineering Circuits Using Behavioral Pattern Mining,
In Proceedings of the IEEE Conference on Hardware-Oriented Security and Trust (HOST), pages 83–88, June 2012.
Nominated for best paper award.
35. Sanjit A. Seshia and Alexander Rakhlin,
Quantitative Analysis of Systems Using Game-Theoretic Learning,
ACM Transactions on Embedded Computing Systems (ACM TECS), 11(S2), 55:1–55:27, 2012.
36. John C. Eidson, Edward A. Lee, Slobodan Matic, Sanjit A. Seshia, and Jia Zou,
Distributed Real-Time Software for Cyber-Physical Systems, Proceedings of the IEEE, 100(1), 45–59, January 2012.
37. Orna Kupferman, Dorsa Sadigh, and Sanjit A. Seshia,
Synthesis with Clairvoyance,
In Proceedings of the Haifa Verification Conference (HVC), pages 5–19, December 2011.
38. Jonathan Kotker, Dorsa Sadigh, and Sanjit A. Seshia,
Timing Analysis of Interrupt-Driven Programs under Context Bounds,
In Proceedings of the IEEE Conference on Formal Methods in Computer-Aided Design (FMCAD), pages 81–90, October 2011.
39. Bryan Brady, Randal E. Bryant, and Sanjit A. Seshia,
Learning Conditional Abstractions,
In Proceedings of the IEEE Conference on Formal Methods in Computer-Aided Design (FMCAD), pages 116–124, October 2011.
40. Susmit Jha, Sanjit A. Seshia, and Ashish Tiwari,
Synthesis of Optimal Switching Logic for Hybrid Systems,
In Proceedings of the 11th International Conference on Embedded Software (EMSOFT), pages 107–116, October 2011.
41. Wenchao Li, Lili Dworkin, and Sanjit A. Seshia,
Mining Assumptions for Synthesis,
In Proceedings of the 9th ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), pages 43–50, July 2011.
42. Daniel Holcomb, Bryan Brady, and Sanjit A. Seshia,
Abstraction-Based Performance Analysis of NoCs,
In Proceedings of the Design Automation Conference (DAC), pages 492–497, June 2011.
43. Sanjit A. Seshia and Jonathan Kotker,
GameTime: A Toolkit for Timing Analysis of Software,

In Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), pages 388–392, March 2011.

44. Bryan Brady, Daniel Holcomb, and Sanjit A. Seshia,
Counterexample-Guided SMT-Driven Optimal Buffer Sizing,
In Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 329–334, March 2011.
45. Pierluigi Nuzzo, Alberto Puggelli, Sanjit A. Seshia, and Alberto Sangiovanni-Vincentelli,
CalCS: SMT Solving for Non-Linear Convex Constraints,
In Proceedings of the IEEE Conference on Formal Methods in Computer-Aided Design (FMCAD), pages 71–79, October 2010.
46. Bryan Brady, Randal E. Bryant, Sanjit A. Seshia, and John W. O'Leary,
ATLAS: Automatic Term-Level Abstraction of RTL Designs,
In Proceedings of the Eighth ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), pages 31–40, July 2010.
47. Wenchao Li, Alessandro Forin, and Sanjit A. Seshia,
Scalable Specification Mining for Verification and Diagnosis,
In Proceedings of the Design Automation Conference (DAC), pages 755–760, June 2010.
48. Susmit Jha, Sumit Gulwani, Sanjit A. Seshia and Ashish Tiwari,
Oracle-Guided Component-Based Program Synthesis,
In Proceedings of the International Conference on Software Engineering (ICSE), pages 215–224, May 2010.
49. Susmit Jha, Sumit Gulwani, Sanjit A. Seshia and Ashish Tiwari,
Synthesizing Switching Logic for Safety and Dwell-Time Requirements,
In Proceedings of the International Conference on Cyber-Physical Systems (ICCPS), pages 22–31, April 2010.
50. Dave King, Susmit Jha, Divya Muthukumaran, Trent Jaeger, Somesh Jha, and Sanjit A. Seshia,
Automating Security Mediation Placement,
In Proceedings of the European Symposium on Programming (ESOP), pages 327–344, March 2010.
51. Cynthia Sturton, Susmit Jha, Sanjit A. Seshia, and David Wagner,
On Voting Machine Design for Verification and Testability,
In Proceedings of the 16th ACM Conference on Computer and Communications Security (CCS), pages 463–476, November 2009.
52. Susmit Jha, Rhishikesh Limaye, and Sanjit A. Seshia,
Beaver: Engineering an Efficient SMT Solver for Bit-vector Arithmetic,
In Proceedings of the 21st International Conference on Computer-Aided Verification (CAV), pages 668–674, June 2009.
53. Daniel E. Holcomb, Wenchao Li, and Sanjit A. Seshia,
Design as You See FIT: System-Level Soft Error Analysis of Sequential Circuits,
In Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 785–790, April 2009.
54. Wenchao Li, Marco Di Natale, Paolo Giusto, Wei Zheng, Alberto Sangiovanni-Vincentelli, and Sanjit A. Seshia,
Optimizations of an Application-Level Protocol for Enhanced Dependability in FlexRay,
In Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 1076–1081, April 2009.

55. Randal E. Bryant, Daniel Kroening, Joël Ouaknine, Sanjit A. Seshia, Ofer Strichman, and Bryan Brady,
An Abstraction-Based Decision Procedure for Bit-Vector Arithmetic,
In International Journal on Software Tools for Technology Transfer (STTT), vol. 11(2), pages 95–104, 2009.
Earlier version appeared as *Deciding Bit-Vector Arithmetic with Abstraction*, Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), LNCS 4424, pages 358–372, March 2007.

56. Sanjit A. Seshia and Alexander Rakhlin,
Game-Theoretic Timing Analysis,
In Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pages 575-582, November 2008.

57. Orna Kupferman, Wenchao Li, and Sanjit A. Seshia,
A Theory of Mutations with Applications to Vacuity, Coverage, and Fault Tolerance,
In Proceedings of the IEEE International Conference on Formal Methods in Computer-Aided Design (FMCAD), November 2008.

58. Dave King, Trent Jaeger, Somesh Jha, and Sanjit A. Seshia,
Effective Blame for Information-Flow Violations,
In Proceedings of the 16th ACM SIGSOFT International Symposium on Foundations of Software Engineering (FSE), pages 250-260, November 2008.

59. Susmit K. Jha, Bryan Brady, and Sanjit A. Seshia,
Symbolic Reachability Analysis of Lazy Linear Hybrid Automata,
In Proceedings of the International Conference on Formal Modeling and Analysis of Timed Systems (FORMATS), pages 241–256, October 2007.

60. Sanjit A. Seshia, K. Subramani, and Randal E. Bryant,
On Solving Boolean Combinations of UTVPI Constraints,
Journal of Satisfiability, Boolean Modeling, and Computation (JSAT), vol. 3, pages 67–90, 2007.

61. Dirk Beyer, Arindam Chakrabarti, Thomas A. Henzinger, and Sanjit A. Seshia,
An Application of Web-Service Interfaces,
In Proceedings of the IEEE International Conference on Web Services (ICWS), pages 831–838, July 2007.

62. Sanjit A. Seshia,
Autonomic Reactive Systems via Online Learning,
Proceedings of the IEEE International Conference on Autonomic Computing (ICAC), June 2007.

63. Armando Solar-Lezama, Gilad Arnold, Liviu Tancau, Rastislav Bodik, Vijay Saraswat, and Sanjit A. Seshia,
Sketching Stencils,
ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), pages 167–178, June 2007.

64. Sanjit A. Seshia, Wenchao Li, and Subhasish Mitra,
Verification-Guided Soft Error Resilience,
Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 1442-1447, April 2007.

65. Huining T. Feng, Lynn T-N. Wang, Wei Zheng, Sri Kanajan, and Sanjit A. Seshia,
Automatic Model Generation for Black Box Real-Time Systems,
Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 930-935, April 2007.

66. Armando Solar-Lezama, Liviu Tancau, David Turner, Rastislav Bodik, Vijay Saraswat, and Sanjit A. Seshia,
Combinatorial Sketching for Finite Programs,
12th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), pages 404-415, ACM Press, October 2006.

67. Sanjit A. Seshia and Randal E. Bryant,
Deciding Quantifier-Free Presburger Formulas Using Parameterized Solution Bounds,
Logical Methods in Computer Science journal, vol. 1 (2:5), pages 1–26, December 2005.
Earlier version in 19th IEEE Symposium on Logic in Computer Science (LICS), pages 100–109, July 2004.
Among 10 invited papers from 40 accepted conference papers and 168 submissions.

68. Cormac Flanagan, Stephen N. Freund, Shaz Qadeer, and Sanjit A. Seshia,
Modular Verification of Multithreaded Programs,
Theoretical Computer Science, vol. 338, issues 1-3, 10 June 2005, pages 153–183.
Awarded "Top Cited Article, 2005-10" in this journal.
Earlier version in 14th International Conference on Computer-Aided Verification (CAV), LNCS 2404, pages 180–194, July 2002.

69. Mihai Christodorescu, Somesh Jha, Sanjit A. Seshia, Dawn Song, and Randal E. Bryant,
Semantics-Aware Malware Detection,
IEEE Symposium on Security and Privacy, Oakland, May 2005, pages 32–46.

70. Vinod Ganapathy, Sanjit A. Seshia, Somesh Jha, Thomas W. Reps, and Randal E. Bryant,
Automatic Discovery of API-Level Exploits,
27th International Conference on Software Engineering (ICSE), May 2005, pages 312–321.

71. Sanjit A. Seshia, Randal E. Bryant and Kenneth S. Stevens,
Modeling and Verifying Circuits Using Generalized Relative Timing,
11th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), March 2005, pages 98–108.
Runner-up for best paper award.

72. Daniel Kroening, Joël Ouaknine, Sanjit A. Seshia, and Ofer Strichman,
Abstraction-Based Satisfiability Solving of Presburger Arithmetic,
16th International Conference on Computer-Aided Verification (CAV), LNCS 3114, pages 308–320, July 2004.

73. Shuvendu K. Lahiri and Sanjit A. Seshia,
The UCLID Decision Procedure (system description),
16th International Conference on Computer-Aided Verification (CAV), LNCS 3114, pages 475–478, July 2004.

74. Randal E. Bryant, Shuvendu K. Lahiri, and Sanjit A. Seshia,
Convergence Testing in Term-Level Bounded Model Checking,
12th Conference on Correct Hardware Design and Verification Methods (CHARME), LNCS 2860, pages 348-362, October 2003.

75. Sanjit A. Seshia and Randal E. Bryant,
Unbounded, Fully Symbolic Model Checking of Timed Automata Using Boolean Methods,
15th International Conference on Computer-Aided Verification (CAV), LNCS 2725, pages 154–166, July 2003.

76. Sanjit A. Seshia, Shuvendu K. Lahiri, and Randal E. Bryant,
A Hybrid SAT-Based Decision Procedure for Separation Logic with Uninterpreted Functions,

40th Design Automation Conference (DAC), pages 425–430, June 2003.
Best paper finalist. In top 14 out of 152 accepted papers and 628 submissions.

77. Shuvendu K. Lahiri, Sanjit A. Seshia, and Randal E. Bryant,
Modeling and Verification of Out-of-Order Microprocessors Using UCLID,
4th International Conference on Formal Methods in Computer-Aided Design (FMCAD), LNCS 2517, pages 142-159, November 2002.
78. Randal E. Bryant, Shuvendu K. Lahiri, and Sanjit A. Seshia,
Modeling and Verifying Systems Using a Logic of Counter Arithmetic with Lambda Expressions and Uninterpreted Functions,
14th International Conference on Computer-Aided Verification (CAV), LNCS 2404, pages 78–92, July 2002.
79. Ofer Strichman, Sanjit A. Seshia, and Randal E. Bryant,
Deciding Separation Formulas with SAT,
14th International Conference on Computer-Aided Verification (CAV), LNCS 2404, pages 209–222, July 2002.
80. Sanjit A. Seshia, R. K. Shyamasundar, Anup K. Bhattacharjee, and S. D. Dhodapkar,
A Translation of Statecharts to Esterel,
1st World Congress on Formal Methods (FM), LNCS 1709, pages 983–1007, September 1999.
81. Anup K. Bhattacharjee, S. D. Dhodapkar, Sanjit A. Seshia, and R. K. Shyamasundar,
PERTS: A Graphical Environment for the Specification and Verification of Reactive Systems,
Journal of Reliability Engineering and System Safety, 71(3), 2001, pages 299–310 (erratum: vol. 72(2)).
Earlier version in SAFECOMP'99, LNCS 1698, pages 431–444, September 1999.

Invited Papers and Tutorials

82. Sanjit A. Seshia,
New Frontiers in Formal Methods: Learning, Cyber-Physical Systems, Education, and Beyond,
CSI Journal of Computing, Vol. 2, No. 4, pages R1:3–R1:13, June 2015.
83. Sanjit A. Seshia, Dorsa Sadigh, and S. Shankar Sastry,
Formal Methods for Semi-Autonomous Driving, In Proceedings of the Design Automation Conference (DAC), June 2015, pages 148:1–148:5.
84. Edward A. Lee *et al.*,
The Swarm at the Edge of the Cloud,
IEEE Design and Test of Computers, Special Issue on Cloud Computing for Embedded Systems, 2014.
85. Rajeev Alur, Rastislav Bodik, Garvit Juniwal, Milo M. K. Martin, Mukund Raghothaman, Sanjit A. Seshia, Rishabh Singh, Armando Solar-Lezama, Emina Torlak, and Abhishek Udupa,
Syntax-Guided Synthesis,
In Proceedings of the IEEE International Conference on Formal Methods in Computer-Aided Design (FMCAD), October 2013, pages 1–17.
86. Sanjit A. Seshia,
Verifying High-Confidence Interactive Systems: Electronic Voting and Beyond,
In 14th International Conference on Distributed Computing and Networking (ICDCN), pages 1–10, January 2013.
87. Jeff C. Jensen, Edward A. Lee, and Sanjit A. Seshia,
An Introductory Capstone Design Course on Embedded Systems,
In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), May 2011.

88. Sanjit A. Seshia,
Quantitative Analysis of Software: Challenges and Recent Advances,
Invited paper at the 7th International Workshop on Formal Aspects of Component Software, October 2010.
89. Subhasish Mitra, Sanjit A. Seshia, and Nicola Nicolici,
Post-Silicon Validation: Opportunities, Challenges and Recent Advances,
Invited special session paper at the Design Automation Conference (DAC), pages 12–17, June 2010.
90. Edward A. Lee, Slobodan Matic, Sanjit A. Seshia, and Jia Zou,
The Case for Timing-Centric Distributed Software,
Invited paper at the 2nd International Workshop on Cyber-Physical Systems (WCPS), pages 57–64, June 2009.
91. Daniel Kroening and Sanjit A. Seshia,
Formal Verification at Higher Levels of Abstraction,
Invited tutorial at International Conference on Computer-Aided Design (ICCAD), pages 572–578, November 2007.
92. Randal E. Bryant and Sanjit A. Seshia,
Decision Procedures Customized for Formal Verification,
Invited paper at the Conference on Automated Deduction (CADE), pages 255–259, July 2005.

Refereed Workshop Papers

93. Matthew Fong and Sanjit A. Seshia,
Stoichiometrically Minimal Source Pathways via Model Checking,
In Proceedings of the 7th International Workshop on Bio-Design Automation (IWBDA), August 2015.
94. Yasser Shoukry, Pierluigi Nuzzo, Alberto Puggelli, Alberto L. Sangiovanni-Vincentelli, Sanjit A. Seshia, Mani Srivastava, and Paulo Tabuada,
Imhotep-SMT: A Satisfiability Modulo Theory Solver for Secure State Estimation,
In 13th International Workshop on Satisfiability Modulo Theories (SMT), July 2015.
95. Susmit Jha and Sanjit A. Seshia,
Are There Good Mistakes? A Theoretical Analysis of CEGIS,
In 3rd Workshop on Synthesis (SYNT), July 2014, pages 84–99.
96. Daniel J. Fremont and Sanjit A. Seshia,
Speeding Up SMT-Based Quantitative Program Analysis,
In 12th International Workshop on Satisfiability Modulo Theories (SMT), July 2014.
97. Dorsa Sadigh, Katherine Driggs-Campbell, Alberto Puggelli, Wenchao Li, Victor Shia, Ruzena Bajcsy, Alberto L. Sangiovanni-Vincentelli, S. Shankar Sastry, and Sanjit A. Seshia,
Data-Driven Probabilistic Modeling and Verification of Human Driver Behavior,
Formal Verification and Modeling in Human-Machine Systems, AAAI Spring Symposium, March 2014.
98. Jeff C. Jensen, Edward A. Lee, and Sanjit A. Seshia,
Virtualizing Cyber-Physical Systems: Bringing CPS to Online Education,
In First Workshop on CPS Education (CPS-Ed), April 2013.
99. Susmit Jha and Sanjit A. Seshia,
Synthesis of Optimal Fixed-Point Implementations of Numerical Software Routines,
In 6th International Workshop on Numerical Software Verification (NSV), April 2013.
100. Wenchao Li, Susmit Jha, and Sanjit A. Seshia,
Generating Control Logic for Optimized Soft Error Resilience,
In 9th Workshop on Silicon Errors in Logic - System Effects (SELSE), March 2013.

101. Saurabh Srivastava, Tim Hsiau, Sarah Chasins, Jonathan Kotker, Yen-Sheng Ho, Paul Ruan, Jeff Tsui, Stephi Hamilton, Jene Li, J. Christopher Anderson, Sanjit A. Seshia, and Rastislav Bodik,
Biochemistry as a Programming Language,
In Off the Beaten Track (OBT/POPL), January 2013.
102. Dorsa Sadigh, Sanjit A. Seshia, and Mona Gupta,
Automating Exercise Generation: A Step towards Meeting the MOOC Challenge for Embedded Systems,
In Proceedings of the Workshop on Embedded Systems Education (WESE), ESWeek, October 2012.
103. Saurabh Srivastava, Jonathan Kotker, Stephi Hamilton, Paul Ruan, Jeff Tsui, J. Christopher Anderson, Rastislav Bodik, and Sanjit A. Seshia,
Pathway Synthesis Using the Act Ontology,
In Proceedings of the 4th International Workshop on Bio-Design Automation (IWBDA), June 2012.
104. Edward A. Lee and Sanjit A. Seshia,
An Introductory Textbook on Cyber-Physical Systems,
In Proceedings of the Workshop on Embedded Systems Education (WESE), ESWeek, October 2010.
105. Susmit Jha, Wenchao Li, and Sanjit A. Seshia,
Localizing Transient Faults Using Dynamic Bayesian Networks,
In IEEE International High Level Design Validation and Test (HLDVT) Workshop, November 2009.
106. Randal E. Bryant, Shuvendu K. Lahiri, and Sanjit A. Seshia,
Deciding CLU Logic Formulas via Boolean and Pseudo-Boolean Encodings,
1st International Workshop on Constraints in Formal Verification (CFV), associated with Principles and Practice of Constraint Programming (CP), September 2002.
107. Nicholas J. Hopper, Sanjit A. Seshia, and Jeannette M. Wing,
A Comparison and Combination of Theory Generation and Model Checking for Security Protocol Analysis,
Workshop on Formal Methods in Computer Security (FMCS), associated with Computer-Aided Verification (CAV), July 2000.

Technical Reports (those that do not substantially overlap with the above papers)

108. Rohit Sinha, Sriram Rajamani, Sanjit A. Seshia, and Kapil Vaswani,
Verification of Confidentiality Properties of Enclave Programs,
Technical Report UCB/EECS-2015-162, EECS Department, UC Berkeley, June 2015.
109. Sanjit A. Seshia, Ed.,
Formal Methods for Engineering Education,
Technical Report UCB/EECS-2015-170, EECS Department, UC Berkeley, June 2015.
110. Daniel Bundala and Sanjit A. Seshia,
On Systematic Testing for Execution-Time Analysis,
ArXiv e-prints, vol. 1506.05893, June 2015.
111. Susmit Jha and Sanjit A. Seshia,
A Theory of Formal Synthesis via Inductive Learning,
ArXiv e-prints, vol. 1505.03953, May 2015.
112. Daniel J. Fremont, Alexandre Donzé, Sanjit A. Seshia, and David Wessel,
Control Improvisation,
ArXiv e-prints, vol. 1411.0698, November 2014.
113. Edward A. Lee *et al.*,
The TerraSwarm Research Center (TSRC) (A White Paper),
Technical report UCB/EECS-2012-207, EECS Department, UC Berkeley, November 2012.

114. Shuvendu Lahiri and Sanjit A. Seshia, Eds.,
Proceedings of the 9th International Workshop on Satisfiability Modulo Theories (SMT) 2011,
Technical report UCB/EECS-2011-80, EECS Department, UC Berkeley, July 2011.
115. Daniel Holcomb, Wenchao Li, and Sanjit A. Seshia,
Algorithms for Green Buildings: Learning-Based Techniques for Energy Prediction and Fault Diagnosis,
Technical report UCB/EECS-2009-138, EECS Department, UC Berkeley, October 2009.
116. John C. Eidson, Edward A. Lee, Slobodan Matic, Sanjit A. Seshia, and Jia Zou,
Time-centric Models For Designing Embedded Cyber-physical Systems,
Technical report UCB/EECS-2009-135, EECS Department, UC Berkeley, October 2009.
117. Sumit Gulwani and Sanjit A. Seshia, Eds.,
Proceedings of the 1st Workshop on Quantitative Analysis of Software (QA'09), Technical report UCB/EECS-2009-93, EECS Department, UC Berkeley, June 2009.
118. Susmit Jha, Sanjit A. Seshia, and Rhishikesh Limaye,
On the Computational Complexity of Satisfiability Solving for String Theories,
Technical report UCB/EECS-2009-41, EECS Department, UC Berkeley, March 2009.
119. Bryan Brady, Randal E. Bryant and Sanjit A. Seshia,
Abstracting RTL Designs to the Term Level,
Technical report UCB/EECS-2008-136, EECS Department, UC Berkeley, October 2008.
120. Orna Kupferman, Wenchao Li, and Sanjit A. Seshia,
On the Duality between Vacuity and Coverage,
Technical report UCB/EECS-2008-26, EECS Department, UC Berkeley, March 2008.
121. Dave King, Susmit Jha, Trent Jaeger, Somesh Jha, and and Sanjit A. Seshia,
On Automatic Placement of Declassifiers for Information-Flow Security,
Technical Report NAS-TR-0083-2007, Network and Security Research Center, Pennsylvania State University, November 2007.
122. Sanjit A. Seshia,
Integrated Verification for Robust Computing,
Technical report UCB/EECS-2006-103, EECS Department, UC Berkeley, July 2006.
123. Sanjit A. Seshia, Guy E. Blelloch, and Robert W. Harper,
A Performance Comparison of Interval Arithmetic and Error Analysis in Geometric Predicates,
CMU-CS-00-172, Computer Science Department, Carnegie Mellon University, December 2000.
124. Sanjit A. Seshia and Randal E. Bryant,
The Hardness of Approximating Minima in OBDDs, FBDDs and Boolean functions,
CMU-CS-00-156, Computer Science Department, Carnegie Mellon University, August 2000.

Patents

- J. Christopher Anderson, Timothy Hsiau, Saurabh Srivastava, Paul Ruan, Jonathan Kotker, Rastislav Bodik, and Sanjit A. Seshia,
Method for Biosynthesis of Acetaminophen,
U.S. Patent Application No.: 62/056,866, filed September 29, 2014.
- Xiaoqing Jin, Alexandre Donzé, Jyotirmoy Deshmukh, and Sanjit A. Seshia,
Systems and Methods for Mining Temporal Requirements from Block Diagram Models of Control Systems,
U.S. Patent Application No. 13/651,961, filed October 15, 2012.

Selected Software Releases and Technology Transfer

(All software listed below is publicly available, typically under the open source BSD license, at http://www.eecs.berkeley.edu/~sseshia/#software.)

- **UCLID** is a software system for modeling and verifying hardware, software, and protocols in a subset of first-order logic with background theories. A major component of this system is a collection of SAT-based decision procedures (SMT solvers) for the underlying logics. UCLID was one of the systems that pioneered the development of SMT solvers and SMT-based verification methods, and continues to be used by academic and industry research groups around the world.
- **GameTime** is a toolkit for timing analysis of embedded software. It has been used to analyze timing behavior of automotive control software at Toyota Technical Center, and in academic research projects at institutions worldwide.
- **Breach** is a Matlab/C++ toolbox for the simulation-based verification of temporal logic properties of hybrid dynamical systems. The *requirement mining* feature of Breach (developed in the HSCC'13 paper in the Publications list) is being evaluated for production use by Toyota, and is under use by Bosch and Denso R&D.
- **CPSGrader** is an automatic grading and feedback system for lab-based courses in science and engineering, including cyber-physical systems, robotics, mechatronics, etc. It has been successfully used in a massive open online course on the edX platform, EECS149.1x, and also in an on-campus lab course at UC Berkeley.
- **BluSTL** is a Matlab toolkit for automatically generating hybrid controllers from signal temporal logic specifications. Although released only recently, in Spring 2015, it is already starting to be adopted by other researchers working in applications as diverse as traffic control, building automation systems, and autonomous driving.
- **Complan** is a tool for compositional multi-robot motion planning based on a reduction to SMT solving. It has been successfully used to improve programmability of teams of robots, by compiling high-level declarative objectives in linear temporal logic for teams of quadrotors into code, as demonstrated in this brief video.
- **Beaver** is a satisfiability modulo theories (SMT) solver for finite-precision bit-vector arithmetic, a logic with a wide range of applications. While Beaver is currently not actively supported, it has been downloaded by several companies in the electronic design automation, embedded systems, and software analysis areas (e.g., NuSym, Intel, Toyota, Coverity), and was incorporated into a product at NuSym (since acquired by Synopsys).

Talks

Invited Talks/Tutorials/Panels

1. *Formal Methods for Semi-Autonomous Driving*,
   Invited talk at the 52nd Design Automation Conference, San Francisco, CA, June 11, 2015.
2. *Synthesis and Inductive Learning*,
   Invited lecture series at the NSF ExCAPE Summer School on Synthesis, Cambridge, MA, June 23-25, 2015.
3. *Verification by, for, and of Humans: Formal Methods for Cyber-Physical Systems and Beyond*,
   ECE Colloquium, University of Illinois at Urbana-Champaign, March 19, 2015.
4. *Formal Methods for Lab-Based MOOCs: Cyber-Physical Systems and Beyond*,
   Keynote talk at Workshop on Embedded and Cyber-Physical Systems Education (WESE), October 16, 2014.
   • Also given at the Indian Institute of Technology, Bombay, India, October 20, 2014.
5. *The Logic of Cars: Reasoning about Cyber-Physical Systems with Computational Logic*,
   Logic Colloquium, University of California, Berkeley, CA, October 3, 2014.

6. *Design and Verification of Cyber-Physical Systems and Robotics*,
   Invited talk at National Instruments (NI) Week, Austin, TX, August 5, 2014.
   • Also given at the NI CPS Round Table, Pisa, Italy, November 24, 2014.
7. *Lab-based MOOCs: Cyber-Physical Systems, Robotics, and Beyond*,
   Invited talk at National Instruments (NI) Week, Austin, TX, August 4, 2014.
   • Shorter version given at the Learning with MOOCs (LWMOOCs) workshop, Cambridge, MA, August 13, 2014.
8. *Human-in-the-Loop Robotics: Specification, Verification, and Synthesis*,
   Invited talk at 5th Workshop on Formal Methods for Robotics and Automation (FMRA/RSS), Berkeley, CA, July 12, 2014.
9. *Validation of Industrial-Scale Real-Time Embedded Systems*,
   Invited Tutorial at 51st Design Automation Conference (DAC), San Francisco, CA, June 2, 2014.
10. *Integrating Induction and Deduction for Synthesis*,
    Invited talk at Americal Control Conference (ACC), Special Session on Software Synthesis, Washington, DC, June 19, 2013.
11. *Term-Level Verification of the Secure Thin Intermediation Layer*,
    Dagstuhl Seminar on Bugs and Defects in Electronic Systems: the Next Frontier, Schloss Dagstuhl, Germany, April 22, 2013.
12. *Quantitative Verification of Embedded Software: The GameTime Approach*,
    Invited talk at LCCC Workshop on Formal Verification of Embedded Control Systems, Lund, Sweden, April 19, 2013.
13. *Verifying High-Confidence Interactive Systems: Electronic Voting and Beyond*,
    Keynote talk, 14th International Conference on Distributed Computing and Networking (ICDCN), January 5, 2013.
    A version of this talk also given as:
    - Prof. R. Narasimhan Memorial Lecture, Tata Insitute of Fundamental Research (TIFR), Mumbai, India, January 9, 2013.
14. *Verification and Synthesis for Cyber-Physical Properties*,
    Invited talk, 50th Annual Allerton Conference on Communication, Control, and Computing, Allerton, IL, October 3, 2012.
15. *Verification of Cyber-Physical Software Systems: Challenges and Recent Advances*,
    Keynote talk, 5th ICES Annual Conference on World-wide Trends and Challenges in Embedded Systems, Stockholm, Sweden, August 30, 2012.
16. *Verification and Synthesis by Sciduction*,
    Invited talk, University of Texas, Austin, October 31, 2011.
    Versions of this talk also given at the following venues:
    - IST Austria, April 17, 2012.
    - Microsoft Research, Cambridge, UK, April 19, 2012.
    - Université Libre de Bruxelles, Brussels, Belgium, April 23, 2012.
17. *UCLID's Elements: Term-Level Verification and SMT Solving*,
    Invited talk, SMT/SAT Summer School, MIT, Cambridge, MA, June 15, 2011.
18. *Verifying Timing-Centric Software Systems*,
    Invited talk, 11th Annual Conference on High Confidence Software and Systems (HCSS), May 4, 2011.
19. *Voting Machines and Automotive Software: Explorations with SMT at Scale*,
    Seminar on Deduction at Scale, Ringberg Castle, Germany, March 7, 2011.

20. *Quantitative Verification of Software: Challenges and Recent Advances*,
Invited talk, 24th IEEE International Conference on VLSI Design and 10th Conference on Embedded Software, Chennai, India, January 6, 2011.
Also given at Coverity, Inc., February 8, 2011.
21. *On Voting Machine Design for Verification and Testability*,
Invited talk, 2nd IEEE International Workshop on Reliability Aware System Design and Test, Chennai, India, January 6, 2011.
22. *The Challenge of Environment Modeling in Verifying Cyber-Physical Software Systems*,
Workshop on Usable Verification, Redmond, WA, November 15, 2010.
23. *Formal Methods for Dependable Computing: From Models, through Software, to Circuits*,
Invited talk, CITRIS Research Exchange, Berkeley, CA, November 3, 2010.
24. Invited panelist, *The Verification Challenge of Low-Level Embedded Software*,
IEEE International Conference on Formal Methods in Computer Aided Design (FMCAD), Lugano, Switzerland, October 22, 2010.
25. *Quantitative Analysis of Software: Challenges and Recent Advances*,
Keynote talk, 7th International Workshop on Formal Aspects of Component Software, Guimaraes, Portugal, October 16, 2010.
26. *Quantitative Verification and Synthesis of Systems*,
Invited talk, Strategic Directions in Software at Scale (SaS), Berkeley, CA, August 18, 2010.
27. *Integrating Induction and Deduction for Verification and Synthesis*,
Software Seminar, Computer Science Department, Stanford University, June 1, 2010.
28. *Voting Machine Design for Verification and Testability*,
Microsoft Research, Redmond, WA, March 19, 2010.
29. *Verification-Guided Error Resilience*,
Sundaram Seshu Scholar Lecture, Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, October 29, 2008.
• Also given at the CANDE Workshop, Pacifica, CA, November 8, 2008.
30. *Mutations for Evaluating Coverage and Fault Tolerance*,
Microsoft Research, Bangalore, India, August 5, 2008.
31. *Formal Verification at Higher Levels of Abstraction*,
Tutorial at International Conference on Computer-Aided Design (ICCAD), November 8, 2007.
32. *Diagnosis, Repair, and Multi-Armed Bandits*,
SRI International, Menlo Park, May 23, 2007.
33. *Adaptive Eager Boolean Encoding for Arithmetic Reasoning in Verification*,
SCS Distinguished Lecture Series, Carnegie Mellon University, February 2, 2006.
34. *SAT-Based Decision Procedures and Malware Detection*,
Software Seminar, Computer Science Department, Stanford University, November 29, 2005.
35. *Reasoning about Reliability and Security Using Boolean Methods*,
General Motors India Science Laboratory, July 21, 2005.
36. *UCLID: Deciding Combinations of Theories via Eager Translation to SAT*,
Stanford/SRI Summer School on Combination of Decision Procedures, August 10, 2004.
37. *The Small Model Property of Integer Linear Arithmetic*,
Computer Science and Artificial Intelligence Laboratory, MIT, Cambridge, MA, July 22, 2004.
38. *First-Order Decision Procedures Based on Eager SAT-Encodings*,

Tata Institute of Fundamental Research, Mumbai, India, January 2, 2004.

39. *Translating Quantified Separation Logic to Quantified Boolean Logic*,
Dagstuhl Seminar on Deduction and Infinite-State Model Checking, Germany, April 24, 2003.
40. *A SAT-Based Decision Procedure for Infinite-State System Verification*,
Microsoft Research, Redmond, November 8, 2002.
41. *A Translation of Statecharts to Esterel*,
Microsoft Research, Cambridge, U.K., September 24, 1999.

Selected Conference Presentations

42. *CPSGrader: Formal Methods for Lab-Based MOOCs*,
3rd Workshop on Programming Languages Technology for Massive Open Online Courses (PLOOC), Portland, OR, June 14, 2015.
43. *Meeting the MOOC Challenge for Embedded Systems*,
1st Workshop on Programming Languages Technology for Massive Open Online Courses (PLOOC), Seattle, WA, June 21, 2013.
44. *Virtualizing Cyber-Physical Systems: Bringing CPS to Online Education*,
First Workshop on CPS Education (CPS-Ed), CPSWeek, Philadelphia, April 8, 2013.
45. *Sciduction: Combining Induction, Deduction, and Structure for Verification and Synthesis*,
Design Automation Conference (DAC), San Francisco, June 5, 2012.
46. *Satisfiability Modulo Theories*,
Tutorial at International Conference on Computer-Aided Design (ICCAD), San Jose, November 2, 2009.
47. *Game-Theoretic Timing Analysis*,
IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Jose, November 11, 2008.
48. *Teaching Embedded Systems to Berkeley Undergraduates*,
NSF Workshop "From Embedded Systems to Cyber-Physical Systems: A Review of the State-of-the-Art and Research Needs", St. Louis, April 21, 2008.
49. *Autonomic Reactive Systems via Online Learning*,
4th International Conference on Autonomic Computing (ICAC), June 14, 2007.
50. *Verification-Guided Soft Error Resilience*,
10th International Conference on Design Automation and Test in Europe (DATE), April 19, 2007.
51. *Modeling and Verifying Circuits Using Generalized Relative Timing*,
11th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), March 15, 2005.
52. *Deciding Quantifier-Free Presburger Arithmetic Using Parameterized Solution Bounds*,
19th Annual IEEE Symposium on Logic in Computer Science (LICS), July 14, 2004.
53. *Unbounded, Fully Symbolic Model Checking of Timed Automata Using Boolean Methods*,
15th International Conference on Computer-Aided Verification (CAV), July 10, 2003.
54. *A Hybrid SAT-Based Decision Procedure for Separation Logic with Uninterpreted Functions*,
40th Design Automation Conference (DAC), June 4, 2003.
55. *Modeling and Verifying Systems Using CLU Logic*,
14th International Conference on Computer-Aided Verification (CAV), July 28, 2002.
56. *A Translation of Statecharts to Esterel*,
1st World Congress on Formal Methods (FM), September 21, 1999.

Selected Seminars and Colloquia

57. *Model Counting, Random Sampling, and Improvisation*,
Qualcomm Research Silicon Valley, Santa Clara, CA, June 9, 2015.
58. *Solvers, Abstraction, and Inductive Learning*,
Dagstuhl Seminar on Decision Procedures and Abstract Interpretation, August 27, 2014.
59. *Human-in-the-Loop Embedded Systems: Specification, Design, and Verification*,
Given at the following venues:
    - Tata Institute of Fundamental Research, India, January 2, 2014
    - Indian Institute of Technology, Bombay, India, Jaunary 7, 2014.
    - Microsoft Research India, Bangalore, India, January 10, 2014.
60. *Formal Performance Verification of NoC Designs*,
Seminar, CSAIL, MIT, Cambridge, MA, May 2, 2013.
61. *Verification with Small and Short Worlds*,
CSAIL Security Seminar, MIT, Cambridge, MA, April 3, 2013.
62. *Integrating Induction, Deduction, and Structure for Synthesis*,
ExCAPE Summer School, Berkeley, CA, June 12, 2013.
A version of this talk also given at Verimag Laboratory, Grenoble, France, March 19, 2013.
63. *Specification Mining for Controller Verification and Synthesis*,
CMACS Seminar, Carnegie Mellon University, Pittsburgh, PA, May 22, 2013.
64. *From Security to Cyber-Physical Systems: The Sciductive Approach to Verification and Synthesis*,
Joint CSE/EE Seminar, Indian Institute of Technology, Bombay, January 3, 2011.
65. *On Voting Machine Design for Verification and Testability*,
Tata Institute of Fundamental Research, Mumbai, December 28, 2010.
66. *Integrating Induction and Deduction for Verification and Synthesis*,
Given at the following venues:
    - University of Texas, Austin, TX, April 15, 2010.
    - PRECISE Center Seminar, University of Pennsylvania, Philadelphia, PA, May 19, 2010.
    - CMACS Seminar, Carnegie Mellon University, Pittsburgh, PA, May 21, 2010.
67. *Game-Theoretic Quantitative Analysis of Embedded Software*,
Given at the following venues:
    - Princeton University, Princeton, NJ, November 12, 2009.
    - EPFL, Lausanne, Switzerland, July 3, 2009.
    - Technical University of Vienna, Austria, July 10, 2009.
    - University of Salzburg, Austria, July 13, 2009.
    - Bruno Kessler Foundation (FBK), Trento, Italy, July 14, 2009.
68. *Game-Theoretic Timing Analysis*,
Given at the following venues:
    - CHESS Seminar Series, UC Berkeley, September 23, 2008.
    - Microsoft Research, Redmond, WA, November 18, 2008.
    - Intel Strategic CAD Labs, Hillsboro, OR, November 21, 2008.
69. *Diagnosis, Repair, and Multi-Armed Bandits*,
DES/CHESS Seminar, University of California, Berkeley, May 8, 2007.
70. *SAT-Based Decision Procedures and Software Security*,
Programming Systems Seminar, University of California, Berkeley, October 24, 2005.

71. *Reasoning about Timed Systems Using Boolean Methods*,
CHESS Seminar, University of California, Berkeley, October 11, 2005.
72. *Boolean Methods in Computer Reliability and Security*,
Joint CSE/EE Seminar, Indian Institute of Technology, Bombay, August 11, 2005.
73. *Reasoning about Reliability and Security Using Boolean Methods*,
Given at the following venues:
- Dept. of Computer Science and Engineering, UC San Diego, April 27, 2005.
- Computer Sciences Department, University of Wisconsin, Madison, April 25, 2005.
- Information Science and Technology Seminar, California Inst. of Technology, April 20, 2005.
- Microsoft Research, Redmond, April 18, 2005.
- EECS Special Seminar, Massachusetts Institute of Technology, April 14, 2005.
- EECS Colloquium, University of California, Berkeley, April 6, 2005.
- CSE Colloquium, University of Washington, Seattle, March 31, 2005.
- Dept. of Electrical and Computer Engineering, University of Texas, Austin, March 24, 2005.
74. *Boolean Methods for Arithmetic Reasoning*,
Dept. of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, March 8, 2005.
75. *Modular Verification of Multithreaded Software*,
SCS Student Seminar Series, Carnegie Mellon University, April 12, 2002.

Teaching and Advising Experience

Teaching at UC Berkeley

Spring 2015, Fall 2012, Spring 2011, Fall 2009, Spring 2007 & 2006	*Computer-Aided Verification* (EECS 219C). Advanced graduate course on formal methods with a focus on algorithmic techniques such as model checking and satisfiability solving (SAT/SMT). Recent innovations include new material on inductive learning and synthesis, and their role in formal methods.
Spring 2014	*Formal Methods for Engineering Education* (CS 294-98). Research-oriented graduate course exploring the use of formal methods to develop technologies for education, especially for online education.
Fall 2013, Fall 2012, Spring 2011, Spring 2009 & Spring 2008	*Introduction to Embedded Systems* (EECS 149). Upper-division undergraduate course on embedded systems. Co-created and developed this undergraduate course at UC Berkeley, taught for the first time in Spring 2008. • The Spring 2008 offering was numbered EECS 124. Co-taught with Prof. Edward Lee in Fall 2013 & 2012, Spring 2011 and Spring 2008.
Fall 2013, 2010 & 2011	*Fundamental Algorithms for System Modeling, Analysis, and Optimization* (EECS 144/244). A joint offering of an upper-division undergraduate course (144) and core graduate course (244) on fundamental algorithmic techniques underlying the design methodology for complex systems, using integrated circuit design as an example (co-taught with Professors Edward Lee, Jaijeet Roychowdhury, and Stavros Tripakis). Co-created EECS 144, an undergraduate course at UC Berkeley, offered for the first time in Fall 2010. The existing graduate course EECS 244 has been revised significantly.

Spring 2010, Spring 2008, & Fall 2006	*Computability and Complexity* (CS 172). Upper-division undergraduate course on automata theory, computability, and complexity theory.
Fall 2005, 2007, & 2008	*Introduction to Computer-Aided Design of Integrated Circuits* (EECS 244, co-taught with Prof. Kurt Keutzer). Core graduate course on CAD for ICs.
Fall 2007	*Current Berkeley Research in Programming Systems* (CS 294-25). Research-oriented graduate course in programming systems (co-taught with Professors R. Bodik, K. Sen, D. Song, and K. Yelick).

Massive Open Online Courses (MOOCs): Led the creation and offering of EECS149.1x, a MOOC on *Cyber-Physical Systems* offered on the edX platform. This course, based on EECS 149 at UC Berkeley, is amongst the *first* courses on this topic offered on any of the three leading platforms for online courses. This MOOC is also the first to deploy automatic grading technology based on formal methods with custom-designed "virtual lab" software, CPSGrader.

Past Teaching: As a graduate and undergraduate student, I served as a teaching assistant for classes on Computer Systems (CMU, 15-213), Algorithms (CMU, 15-451), and Introductory Programming (IIT Bombay, CS101).

Graduate Student Advisees

Current:

- Ankush Desai, Ph.D. in EECS (August 2013 – date)
- Daniel Fremont, Ph.D. in Logic & the Methodology of Science (August 2013 – date)
- Eric Kim, Ph.D. in EECS (May 2014 – date) (co-advised with Prof. M. Arcak)
- Dorsa Sadigh, Ph.D. in EECS (August 2012 – date) (co-advised with Prof. S. Shankar Sastry)
- Rohit Sinha, Ph.D. in EECS (August 2011 – date)
- Nishant Totla, Ph.D. in EECS (May 2013 – date)

Graduated:

- Wenchao Li, Ph.D. in EECS (graduated December 2013), *current position: Research Scientist, SRI International*
  ⋆ Recipient of the ACM/SIGDA Outstanding Dissertation Award, June 2015.
- Daniel Holcomb, Ph.D. in EECS (graduated December 2013), *current position: Asst. Professor, University of Massachusetts at Amherst*
- Susmit Jha, Ph.D. in EECS (graduated December 2011), *current position: Research Scientist, United Technologies Research Center*
- Bryan Brady, Ph.D. in EECS (graduated May 2011), *current position: Senior Software Engineer, C3Energy*
- Garvit Juniwal, M.S. in EECS (graduated December 2014)
- Matthew Fong, M.S. in EECS (graduated May 2015)
- Zachariah Wasson, M.S. in EECS (graduated May 2014)
- Wei Yang Tan, M.S. in EECS (graduated May 2014)
- Jonathan Kotker, M.S. in EECS (graduated May 2013)
- Rhishikesh Limaye, M.S. in EECS (graduated May 2010)

Visiting Student: Luigi Di Guglielmo (Univ. Verona, Italy, 05/2011 - 11/2011)

Postdoctoral Researchers

- Daniel Bundala (Sep. 2014 - date)
- Alexandre Donzé (Mar. 2012 - date)
- Markus Rabe (Apr. 2015 - date)
- Vasumathi Raman (July 2013 - June 2015) (co-advised with Prof. R. Murray, Caltech), *current position: Research Scientist, United Technologies Research Center*
- Indranil Saha (July 2013 - June 2015) (co-advised with Prof. G. Pappas, U. Penn), *current position: Asst. Professor, IIT Kanpur, India*
- Rüdiger Ehlers (Sep. 2012 - Aug. 2013) (co-advised with Prof. H. Kress-Gazit, Cornell), *current position: Professor, University of Bremen, Germany*

Undergraduate Advisees

Linh Pham (EECS, UC Berkeley, May 2015 - date); Nathan Mull (Math., UC Berkeley, May 2015 - date); James Ferguson (EECS, UC Berkeley, Jan. 2012 - Dec. 2013); Sophie Libkind (Swarthmore College, SUPERB/NSF REU participant, Jun. - Aug. 2013); Paul Ruan (EECS, UC Berkeley, Jan. 2012 - May 2013); Jacob Levine (EECS, UC Berkeley, Jan. 2012 - May 2012); Mona Gupta (EECS/NE, UC Berkeley, May 2012 - Dec. 2012); Hanchen Tang (EECS, UC Berkeley, May - Aug. 2012); Xu Chen (EECS, UC Berkeley, Jan. - Dec. 2012); Dorsa Sadigh (EECS, UC Berkeley, Jan. - Dec. 2011); Lisa Yan (EECS, UC Berkeley, Jan. - Dec. 2011); Johny Lam (EECS, UC Berkeley, May - Dec. 2010); Rohan Desai (EECS, UC Berkeley, May - Jun. 2010); Lili Dworkin (Haverford College, SUPERB/NSF REU participant, Jun. - Aug. 2010); Min Xu (EECS, UC Berkeley, Aug. 2008 - Jun. 2009); Jeff Jensen (EECS, UC Berkeley, Aug. - Dec. 2008); Lei Huang (EECS, UC Berkeley, Aug. - Dec. 2008); Adam Harwayne (EECS, UC Berkeley, Aug. - Dec. 2008); Daniel Wong (EECS, UC Berkeley, Jan. - Jun. 2008); Kedar Kanitkar (EECS, UC Berkeley, Jan. - Dec. 2007); Wenchao Li (EECS, UC Berkeley, Jun. 2006 - May 2007); Timothy Washington (CIS, Clark Atlanta University, SUPERB-IT participant, Jun. - Aug. 2006); Yinmeng N. Zhang (Computer Science, CMU, Sep. 2004 - May 2005); Andrew P. Lin (Mathematical Sciences, CMU, May 2003 - Apr. 2004).

Ph.D. Qualifying Exam / Dissertation Committees

Adam Chlipala (EECS, UC Berkeley, Apr. 2006), Donald Chai (EECS, UC Berkeley, May 2006), David Molnar (EECS, UC Berkeley, May 2006), Wei Zheng (EECS, UC Berkeley, Oct. 2006), Michael Case (EECS, UC Berkeley, May 2007), Nathan Kitchen (EECS, UC Berkeley, May 2007), Guoqiang Wang (EECS, UC Berkeley, May 2007), Haibo Zeng (EECS, UC Berkeley, May 2007), Thomas Feng (EECS, UC Berkeley, Jan. 2008), Armando Solar-Lezama (EECS, UC Berkeley, Feb. 2008). Mark Whitney (EECS, UC Berkeley, Mar. 2008), Gilad Arnold (EECS, UC Berkeley, Mar. 2008), Matthew Moskewicz (EECS, UC Berkeley, Feb. 2009), Yang Yang (EECS, UC Berkeley, Oct. 2009). Shanna-Shaye Forbes (EECS, UC Berkeley, Dec. 2010), Sayak Ray (EECS, UC Berkeley, April 2011), Cynthia Sturton (EECS, UC Berkeley, Dec. 2011), Dai Bui Nguyen (EECS, UC Berkeley, May 2012), Tobias Welp (EECS, UC Berkeley, May 2012), Chia Yuan Cho (EECS, UC Berkeley, Dec. 2012), Eloi Periera (CEE, UC Berkeley, Dec. 2012), Pierluigi Nuzzo (EECS, UC Berkeley, Jul. 2013), Chung-Wei Lin (EECS, UC Berkeley, Nov. 2013), Michael Zimmer (EECS, UC Berkeley, Nov. 2013), Sam Coogan (EECS, UC Berkeley, Feb. 2014), Jiang Long (EECS, UC Berkeley, Mar. 2014), Alberto Puggelli (EECS, UC Berkeley, May 2014), Ilge Akkaya (EECS, UC Berkeley, Jun 2014), Yifei Yuan (CS, U.Penn., Apr. 2015), Baruch Sterin (EECS, UC Berkeley, Apr. 2015).

M.S. Dissertation Committees

Thomas Feng (EECS, UC Berkeley, Fall 2008), Shanna-Shaye Forbes (EECS, UC Berkeley, Spring 2009),

Jeff Jensen (EECS, UC Berkeley, Fall 2009), Cynthia Sturton (EECS, UC Berkeley, Fall 2010), Nikunj Bajaj (EECS, UC Berkeley, Fall 2014), John Finn (EECS, UC Berkeley, Spring 2015).

University Service

At UC Berkeley:

2013-15	Member, Regents' and Chancellor's Scholarship Subcommittee, Committee on Undergraduate Scholarships, Honors, and Financial Aid
2010-11	Member, College of Engineering ABET Preparation Committee
2014-15	Member, EECS Faculty Hiring Committee
2005-11 & 2013-14	Member, EECS Graduate Admissions/Advising Committee
2011-14	Member, EECS Student Awards Committee
2010-12	Member, EECS Undergraduate Study Committee
2006-15	Member, Preliminary Examination Committee in Computer-Aided Design for VLSI
2006-15	Undergraduate Advising, EECS Department

Elsewhere:

2000-03	Co-organizer, SCS Student Seminar Series, a forum at CMU in which students from all areas of Computer Science and Engineering participated.
1996-97	Technical Co-ordinator, Computer Science and Engineering Association, IIT Bombay. Conducted city-wide technical workshops.

Professional Activities and Service

Professional Memberships: ACM, IEEE (Senior Member), IEEE Computer Society, Sigma Xi.

Editorial Boards and Conference Committees:

- Associate Editor, IEEE Transactions on Computer-Aided Design of Circuits and Systems (TCAD) (7/2012 - 12/2014)
- Associate Editor, CSI Journal of Computing, Computer Society of India (7/2011 - date)
- Associate Editor, IEEE Embedded Systems Letters (12/2008 - 12/2010)
  – co-edited special issue on Automotive Embedded Systems (March-May, 2010)
- Program co-chair, 24th International Conference on Computer-Aided Verification (CAV), 2012.
- Program co-chair, 7th Working Conference on Verified Software: Theories, Tools, and Experiments (VSTTE), 2015.
- Chair of Verification track and Member of Technical Program Committee, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2010 & 2011.
- Program co-chair, 9th International Workshop on Satisfiability Modulo Theories (SMT), 2011.
- Program co-chair, 1st Workshop on Quantitative Analysis of Software (QA), 2009.
- Co-organizer, Dagstuhl Seminar on Decision Procedures and Abstract Interpretation, Schloss Dagstuhl, Germany, August 24-29, 2014.

- Member, Program Committee, 17th International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI), 2016.
- Member, Program Committee, 20th International Symposium on Formal Methods (FM), 2015.
- Member, ACM Student Research Competition Selection Committee, ACM/IEEE 17th International Conference on Model Driven Engineering Languages and Systems (MODELS), 2014.
- Member, Program Committee, 23rd International Conference on Computer-Aided Verification (CAV), 2011.
- Member, Program Committee, 3rd NASA Formal Methods Symposium, 2011.
- Member, Program Committee, International Conference on Embedded Software (EMSOFT), 2010.
- Member, Program Committee, ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), 2010.
- Member, Program Committee, Hardware Verification Workshop (HWVW), 2010.
- Member, Program Committee, 16th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), 2010.
- Member, Technical Program Committee, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2008 & 2009.
- Member, Program Committee, 4th International Workshop on Automated Formal Methods (AFM), 2009.
- Member, Program Committee, International Conference on Formal Modelling and Analysis of Timed Systems (FORMATS), 2009.
- Member, Program Committee, 21st International Conference on Computer-Aided Verification (CAV), 2009.
- Member, Program Committee, IJCAR '08 Workshop on Practical Aspects of Automated Reasoning (PAAR), 2008.
- Member, Best Paper Award Committee, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2007.
- Member, Program Committee, 18th International Conference on Computer-Aided Verification (CAV), 2006.

Large Project/Center Leadership: Co-leader of Theme on *Methodologies, Models, and Tools*, the *TerraSwarm Research Center*, a multi-institution, multi-year project funded by SRC/DARPA, 2013-17.

Reviewing Grant Proposals: (2006-15)

- National Science Foundation Panels.
- Israel-U.S. Binational Science Foundation, Austrian Science Foundation.

Last updated: July 2015