Pramod Subramanyan

CONTACT INFORMATION

545 Cory Hall
Berkeley CA 94720

Email: spramod@eecs.berkeley.edu
http://eecs.berkeley.edu/∼spramod

EDUCATION

Princeton University, Princeton, NJ.

Ph.D. Department of Electrical Engineering, 2011-2016

- Thesis: Deriving Abstractions to Address Hardware Platform Security Challenges
- Advisor: Professor Sharad Malik
- GPA: 3.97/4.00

Indian Institute of Science, Bangalore.

M.Sc. (Engg.), SERC, 2008-2011

- Thesis: Efficient Redundant Execution in Chip Multiprocessors
- Advisor: Professor Virendra Singh
- GPA: 8.00/8.00

R. V. College of Engineering, Bangalore.

B.E., Electronics and Communication Engineering, 2002-2006

- Aggregate marks: 80.18%, first class with distinction

JOURNAL PUBLICATIONS AND BOOK CHAPTERS

- "Verifying Security Properties in Modern SoCs using Instruction-Level Abstractions", Pramod Subramanyan and Sharad Malik. *Hardware IP Security and Trust*, edited by Prabhat Mishra, Swarup Bhunia and Mark Tehranipoor. Springer-Verlag, January 2017.
- "Boolean Satisfiability: Solvers and Extensions", Georg Weissenbacher, Pramod Subramanyan and Sharad Malik. *Software Systems Safety*, IOS Press, May 2014.
- "Reverse Engineering Digital Circuits Using Structural and Functional Analyses", Pramod Subramanyan, Nestan Tsiskaridze, Wenchao Li, Adria Gascon, Wei Yang Tan, Ashish Tiwari, Natarajan Shankar, Sanjit A. Seshia and Sharad Malik. *IEEE Transactions on Emerging Topics in Computing: Special Issue on Nanoscale Architectures for Hardware Security, Trust and Reliability. (**TETC 2014**)*, March 2014.

CONFERENCE PUBLICATIONS

- Malware Detection using Machine Learning Based Analysis of Virtual Memory Access Patterns. Zhixing Xu, Sayak Ray, Pramod Subramanyan and Sharad Malik. *To appear in the Proceedings of Design Automation and Test in Europe.* **(DATE 2017)**. Lausanne, Switzerland. March 2017.

- (**Invited**) "Specification and Modeling for Systems-on-Chip Security Verification", Sharad Malik and Pramod Subramanyan. *Proceedings of the Design Automation Conference (**DAC 2016**)*, June 2016, Austin, TX.

- "Verifying Information Flow Properties of Firmware using Symbolic Execution", Pramod Subramanyan, Sharad Malik, Hareesh Khattri, Abhranil Maiti and Jason Fung. *Proceedings of Design Automation and Test in Europe (**DATE 2016**)*, March 2016, Dresden, Germany.

- "Template-based Synthesis of Instruction-Level Abstractions for SoC Verification", Pramod Subramanyan, Yakir Vizel, Sayak Ray and Sharad Malik. *Proceedings of 15th Conference on Formal Methods in Computer-Aided Design. (**FMCAD 2015**)*, September 2015, Austin, TX.

- (**Best Student Paper**) "Evaluating the Security of Logic Encryption Algorithms", Pramod Subramanyan, Sayak Ray and Sharad Malik. *Proceedings of the IEEE International Symposium on Hardware-Oriented Security and Trust (**HOST 2015**)*, May 2015, McLean, VA.

- "Template-based circuit understanding", Adria Gascon, Pramod Subramanyan, Bruno Dutertre, Ashish Tiwari, Dejan Jovanovic and Sharad Malik. *Proceedings of 14th Conference on Formal Methods in Computer-Aided Design. (**FMCAD 2014**)*, October 2014, Lausanne, Switzerland.

- "Formal Verification of Taint-propagation Security Properties in a Commercial SoC Design", Pramod Subramanyan and Divya Arora. *Proceedings of Design Automation and Test in Europe (**DATE 2014**)*, March 2014, Dresden, Germany.

- "All-SAT using Minimal Blocking Clauses", Yinlei Yu, Pramod Subramanyan, Nestan Tsiskaridze and Sharad Malik. *Proceedings of the 27th International Conference on VLSI Design (**VLSID 2014**)*, January 2014, Mumbai, India.

- "WordRev: Finding Word-Level Structures in a Sea of Bit-Level Gates", Wenchao Li, Adria Gascon, Pramod Subramanyan, Wei Yang Tan, Ashish Tiwari, Sharad Malik, Natarajan Shankar and Sanjit A. Seshia. *Proceedings of the IEEE International Symposium on Hardware-Oriented Security and Trust **(HOST 2013)***, June 2013, Austin, TX.

- "Reverse Engineering Digital Circuits Using Functional Analysis", Pramod Subramanyan, Nestan Tsiskaridze, Kanika Pasricha, Dillon Reisman, Adriana Susnea and Sharad Malik, *Proceedings of Design Automation and Test In Europe (**DATE 2013**)*, March 2013, Grenoble, France.

- "Adaptive Execution Assistance for Multiplexed Fault-Tolerant Chip Multiprocessors", Pramod Subramanyan, Virendra Singh, Kewal Saluja and Erik Larsson, *Proceedings of the 29th IEEE International Conference on Computer Design, (**ICCD 2011**)*, October 2011, Amherst, MA.

- "Energy-Efficient Fault Tolerance in Chip Multiprocessors Using Critical Value Forwarding", Pramod Subramanyan, Virendra Singh, Kewal Saluja and Erik

Larsson, *Proceedings of the 40th IEEE/IFIP International Conference on Dependable Systems and Networks (**DSN 2010**)*, June 2010, Chicago, IL.

- "Energy-Efficient Fault Tolerance in Chip Multiprocessors", Pramod Subramanyan, Virendra Singh, Kewal Saluja and Erik Larsson, *Proceedings in the 20th ACM Great Lakes Symposium on VLSI (**GLSVLSI 2010**)*, May 2010, Providence, RI.
- "Multiplexed Redundant Execution: A Technique for Efficient Fault Tolerance in Chip Multiprocessors", Pramod Subramanyan, Virendra Singh, Kewal Saluja and Erik Larsson. *Proceedings of Design Automation and Test In Europe (**DATE 2010**)*, March 2010, Dresden, Germany.

Other Publications

- "Generation of Minimal Leakage Input Vectors with Constrained NBTI Degradation", Pramod Subramanyan, Ram Rakesh Jangir, Jaynarayan Tudu, Erik Larsson and Virendra Singh. *Proceedings of the 7th East-West Design and Test Workshop (**EWDTS 2009**)*, September, Moscow, Russia.
- "Power-Efficient Redundant Execution for Chip Multiprocessors", Pramod Subramanyan, Virendra Singh, Kewal Saluja and Erik Larsson. *Proceedings of the 3rd Workshop on Dependable and Secure Nanocomputing (**WDSN 2009**) held in conjunction with DSN 2009*, June 2009, Lisbon, Portugal.
- "Accelerating Signal Processing Applications Using Graphics Processors", Ashwin Prasad and Pramod Subramanyan. *Proceedings of the 14th National Conference on Communications, (**NCC 2008**)*, February 2008, Mumbai, India.

Patents

- US Patent 8,040,276, October 18, 2011. "*Generation of Multi-satellite GPS Signals in Software*", Sastry Vadlamani, Vrishti Agrawal, Sanjeev G. Dhumawad, Pramod Subramanyan and Abhay Samant.
- "*Cache System With Biased Cache Line Replacement Policy and Method Therefor*", William L. Walker, Robert F. Krick, Tarun Nakra and Pramod Subramanyan. (Pending)

Awards

- Honorable Mention, IEEE SVDTC Student Research Award. (2016)
- Wu Prize for Excellence, School of Engineering and Applied Science, Princeton University. (2015)
- Best Student Paper Award, IEEE International Symposium on Hardware-Oriented Security and Trust. (2015)
- Teaching Assistant Award, Department of Electrical Engineering, Princeton University for ELE 206/COS 306. (2014)
- Subramaniam Rajalakshmi Medal for best M.Sc (Engg.) thesis at the Supercomputer Education and Research Center, Indian Institute of Science. (2012)

Teaching Experience

- Assistant in Instruction for "Introduction to Logic Design" (ELE 206/COS 306) taught by Professor Sharad Malik, Princeton University, Fall 2013.
- Assistant in Instruction for "Designing Secure Systems" (ELE 476) taught by Professor Prateek Mittal, Princeton University, Fall 2014.

Professional Experience

University of California, Berkeley. Berkeley, CA.

Postdoctoral Researcher (January 2017-Present)

I am a postdoctoral researcher in Electrical Engineering and Computer Sciences at UC Berkeley. I work on applying formal verification to hardware and system security concerns. My mentor is Professor Sanjit Seshia.

Intel Corporation. Santa Clara, CA and Hillsboro, OR.

Graduate Student Intern (Summers of 2013/14/15)

I worked in the Security Center of Excellence (SeCoE) and used formal techniques to verify security properties of hardware and firmware in Intel designs.

Advanced Micro Devices. Bangalore, India.

Design Engineer II (July 2010 to August 2011)

I worked in AMD India's performance modeling team where I developed simulators for core modeling, studied hardware features and enhancements and worked on the correlation of simulator and hardware (RTL) performance.

National Instruments. Bangalore, India.

Staff Software Engineer (May 2008 to July 2008)

Software Engineer (July 2006 to April 2008)

I helped develop high-performance signal processing algorithms for various radio frequency signal processing libraries.

Reviewing

Journals: IEEE TCAD, IEEE TETC, IEEE TIFS, IEEE ToC, Springer JETTA. Conference sub-reviewing: DAC 2017, FMCAD 2016, SAT 2015, ICCAD 2015, ICCD 2011.

Professional Memberships

Member of the IEEE and ACM.