Monolithic Integration of O-band Photonic Transceivers in a “Zero-change” 32nm SOI CMOS

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Monolithic Silicon Photonics

Enhanced CMOS enables new applications!

CMOS Radios
Rudell & Gray (1997)

Inductors in IC process
Nguyen & Meyer 1990

mmWave
CMOS Amplifier
Niknejad & Brodersen (2004)

SiPh Transmitter in 45nm CMOS
Stojanovic, Popovic, Ram (2012)
Photonics Next to The Fastest Transistors

- $f_T/f_{\text{max}}$ have not improved since 32nm node
- $f_T/f_{\text{max}}$ affect speed, energy-efficiency, ... of electronic-photonic systems
- 32/45nm: Fastest Transistors + Thick-enough Si bodies to guide the light
  - Si body in SOI nodes below 32nm (FDSOI) cannot guide the light!

[GlobalFoundries (GF)]
IBM/GF SOI CMOS

- 300mm wafer, commercial process
- MOSIS and TAPO MPW access
- Advanced processes used in microprocessors
- Photonic enhancement enables photonic SoC

IBM Cell
45nm

AMD Llano APU
32nm

IBM Power 7+
32nm
Photonic System-on-Chips in 45nm SOI

Millions of transistors + Hundreds of photonic devices!

[C. Sun, Nature 2015]
“Zero-Change” Platforms

- Photonics for free! (No modification to the process)
- Closest proximity of electronics and photonics
- Single substrate removal post-processing step

Monolithic photonics platform with the fastest transistors
GF 32nm SOI CMOS

- First node with High-k/Metal gate (HKMG)
- 33% faster logic than 45nm node
- High-performance SoCs: AMD Llano APU, Power 7+, ...
- Extra epitaxial SiGe layer to improve photonics

Waveguides
Grating Couplers

PMOS Cross-section [A. Kerber, SEMATECH AGST 2010]
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![PMOS Cross-section](A. Kerber, SEMATECH AGST 2010)
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Active Devices (Modulator/PD)

PMOS Cross-section [A. Kerber, SEMATECH AGST 2010]
Post-Processing with Electrical Packaging

- Thin BOX causes optical leakage into substrate
- Removing Si substrate to lower optical loss
- Enables electrical flip-chip packaging
Post-Processing for Probing

- Substrate transfer to access the pads for probing
- Bidirectional vertical grating couplers

*NOA: None Optical Adhesive
Waveguides

- Built in crystalline silicon (cSi) layer by blocking dopings
- 3db/cm loss achieved in 45nm node [J.S. Orcutt, Opt. Express 2012]
- Measured loss in 32nm:
  - 25dB/cm @1310nm (O-band)
  - 20dB/cm @1550nm (C-band)
- Extra loss due to un-intentional dopings
Bidirectional Grating Couplers

- Backside Coupling: 4.9dB loss with 84nm 1dB bandwidth
- Topside Coupling: 7.5dB loss (excess loss due to inter-layer dielectrics)
- Sub-2dB coupling can be achieved by adding polysilicon grating to break directionality symmetry [M. T. Wade, OI 2015]
Ring-resonators

- Resonance wavelength: \( \lambda_0 = n_{\text{eff}} L / m \), \( m = 1, 2, 3, \ldots \)
  - Q-factor: \( Q = \lambda_0 / \Delta \lambda \)
- Free spectral range (FSR) = \( \lambda^2 / n_g L \)
  - Total available optical bandwidth in multi-wavelength communication
- 5μm-radius high-Q rings in 32nm due to high lithography precision
Ring-resonator based Optical Transceivers

- Based on carrier plasma effect in silicon

- Modulation Scheme:
  1. Deplete/Inject carriers using PN junctions
  2. $\Delta$free carriers $\rightarrow$ $\Delta$index of refraction
  3. On-Off Keying (OOK) modulation in frequency domain

[Courtesy of C. Sun]
Spoked-ring Modulators

- Interleaved planar PN junctions
  - Enabled by advanced lithography of this process
- Spoked-shape contacts to avoid metallic optical loss
Spoked-ring Modulators

- 5μm radius (FSR of 18.9nm)
- Loaded Q-factor of 6k (intrinsic Q >12k)
- 20pm/V resonance shift efficiency in the depletion mode (reverse bias PN junctions)
Embedded Heater in Microrings

- Resistive heater in cSi layer with 500Ω resistance
- Used in tuning the ring for thermal and process variations
  - Essential for multi-wavelength systems [C. Sun, JSSC 2016]
- Heater tuning efficiency: 0.8nm/mW (14μW/GHz)
  - Flip-chip packaged chip has higher tuning efficiency (3.7μW/GHz)
O-band Light Detection

- SiGe layers originally used to improve PMOS performance
- Larger Ge% in cSiGe than eSiGe
Resonant Photo-detectors (PD)

- Both types implemented with responsivities of:
  - eSiGe-based: 0.06 A/W
  - cSiGe-based: 0.13 A/W
- 150nA dark current
Resonant PD Characteristics

- Loaded Q-factors of 6.5k (intrinsic Q >15k)
- 12.5GHz electro-optical bandwidth
Transmitter Block-diagram

- High-swing (2.4V) thick-oxide drivers
- Depletion mode: 0V or -2.4V applied on PN junctions
- Electrical speed (>25Gb/s) with 30fF capacitance to drive
Two-segmented resonant PD (Split PD)
- Mitigates common-mode noise
- 13kΩ with 5GHz electrical bandwidth (TIA gain: 4.5kΩ)
- Tested by externally modulated light
Transceivers Results

- **Transmitter**: 13.5Gb/s with extinction ratio (ER) of 3.7dB and insertion loss (IL) of 2.8dB
- **Receiver**: 12Gb/s (limited by TIA bandwidth)
**Platform Summary**

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Waveguides</th>
<th>Grating Couplers</th>
<th>Ring Modulators</th>
<th>Resonant PDs</th>
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<td><img src="image1.png" alt="Transistor Image" /></td>
<td><img src="image2.png" alt="Waveguide Image" /></td>
<td><img src="image3.png" alt="Grating Coupler Image" /></td>
<td><img src="image4.png" alt="Ring Modulator Image" /></td>
<td><img src="image5.png" alt="Resonant PD Image" /></td>
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<td><strong>32nm SOI</strong></td>
<td><strong>Loss: 20db/cm</strong></td>
<td><strong>Loss: 4.9db (84nm 1-db BW)</strong></td>
<td><strong>Q-factor: 6k</strong></td>
<td><strong>Res: 0.13A/W</strong></td>
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<td><em>f_max: 390/350GHz</em></td>
<td><em>Loss: 3db/cm</em></td>
<td><em>Adding polysilicon grating (3dB improvement)</em></td>
<td><em>BW &lt; 10GHz</em></td>
<td><em>BW: 12.5GHz</em></td>
</tr>
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<td><em>One of the fastest CMOS nodes with &lt;5fF parasitic cap to photonic devices</em></td>
<td><em>Loss: Sub-2dB</em></td>
<td><em>Optimizing PN junction RC / lower waveguide loss</em></td>
<td><em>Q-factor &gt; 10k</em></td>
<td><em>Res: 0.5A/W</em></td>
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<td><em>BW &gt; 20GHz</em></td>
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[B. Greene, VLSI 2009]
### Platform Applications

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*Fig. 2 Cross-section after full process.*

[Courtesy of M. Ramo]

[Oak Ridge HPC]

[Gophotonics.com]
Conclusion

- Monolithic silicon photonics with fastest transistors
  - Demonstration of 12Gb/s O-band transceivers

- Continuation of “zero-change” approach to more advanced and complex (e.g. HKMG) SOI CMOS technologies

- Potentially revolutionize many applications despite slowdown in CMOS scaling
  - VLSI compute and network infrastructure just a start …
Acknowledgment

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