University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS 150
Fall 2000

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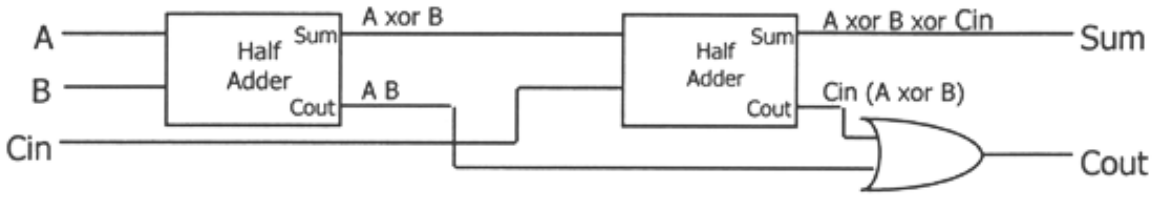
Homework Quiz # 3 (22 September)

Name: _____ **SID:**_____

Consider the following implementation of the full adder in terms of cascaded half adders:



Show how to implement the full adder Sum and Carryout in multilevel form using ***NAND gates only***. You may assume that the input variables A, B, Cin and their complements are available. Sketch your solution as a logic schematic in the space below (you may only use NAND gates):