EECS 150   R. H. Katz
Fall 2000

Problem Set # 3 (Assigned 14 September, Due 22 September)

1. Map the following multilevel AND/OR Boolean functions into (i) NAND-only and (ii) NOR-only implementations. Do not simplify these expressions—there is no need to minimize them in this problem. You may insert inverters if you need them. Draw your schematics, or use the Xilinx software and attach printouts.
    (a) F(A,B,C,D) = (A B C + A' B') (C + D)
    (b) G(B,C) = B' C'; F(A,B,C,D) = [(A + B) (A' + C) + G] G' (A' C' + G)
    (c) F(A,B,C,D) = [(A' + B' + C) (B + C') (C + D')' (A + B' + C')'] + A C D' + B C' D'
2. Show how to implement the following Boolean functions in AND-OR-INVERT form. Draw your schematics using AND-OR-Invert gates and Inverters only:
    (a) F(A,B,C) = AB + BC + AC (e.g., the full adder carry out)

    (b) F(A,B,C) = A ⊕ B ⊕ C (e.g., the full adder sum)
    (c) F(A,B,C,D) = 1 if the 2-bit binary quantity A B is strictly less than the 2-bit binary quantity C D in magnitude.
3. Consider the following circuits with feedback, that is, the output also serves as an input to the function.
    (a) Determine the output of NOR gate U3 in the schematic below when the switch to ground alternates between being closed and being open. Draw a timing diagram to illustrate your answer.
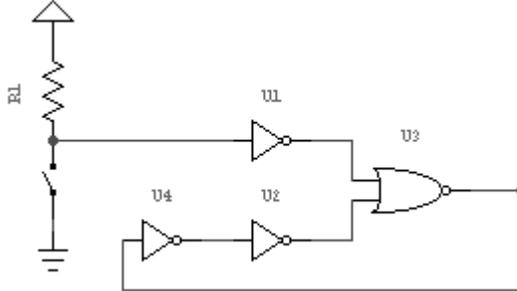
    (b) Repeat your analysis for the following circuit that looks similar to 3(a). Draw a timing diagram to explain its time dependent behavior. Does this circuit generate an oscillating output? If so, why? If not, why not?
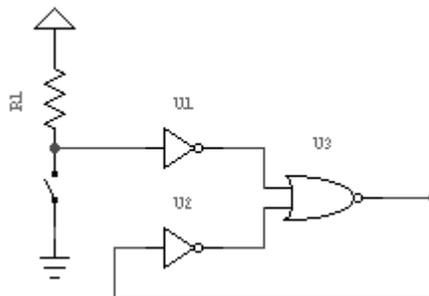
4. Implement the functions F(A,B,C,D) in Problem 1(a),(b),(c) and 2(c) using a single 8:1 Multiplexer for each function. Implement the functions F(A,B,C) in Problem 2(a),(b) using a single 4:1 Multiplexer for each function.
5. Implement the six functions of Problems 1 and 2 using a single PLA (Hint: you will need to transform these into a sum of products form). The PLA is defined over the four inputs A, B, C, D and the six outputs F1a, F1b, F1c, F2a, F2b, F2c. Implement the functions in such a way as to minimize the number of rows (shared product terms) in the PLA.