CoreUART v4.0

Handbook

Actel
POWER MATTERS

Actel Corporation, Mountain View, CA 94043

Printed in the United States of America

Part Number: 50200095-1

Release: February 2009

Trademarks

Table of Contents

Introduction

General Description

CoreUART is a serial communication controller with a flexible serial data interface that is intended primarily for embedded systems. CoreUART can be used to interface directly to industry standard UARTs. CoreUART is intentionally a subset of full UART capability to make the function cost-effective in a programmable device. Figure 1 illustrates the various usages of CoreUART.

Case A in Figure 1 represents the interface to an industry standard UART, such as an 8251 or a 16550. In Case B, CoreUART is transferring data from the 8051 to the system monitor through the RS-232 interface and vice versa.

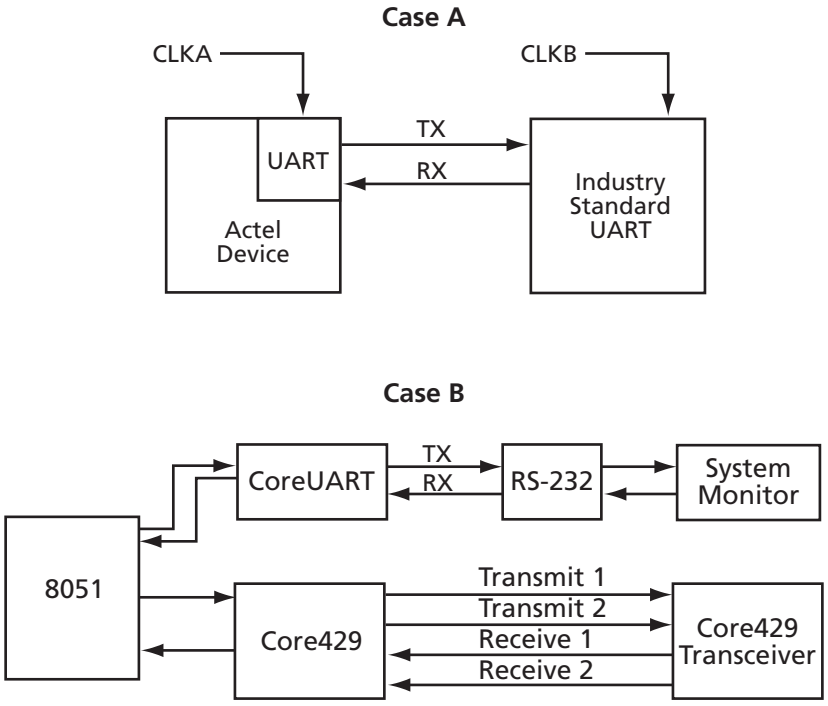

Figure 1 · System Block Diagram Depicting CoreUART Usage

Core Versions

This handbook applies to CoreUART v4.0. The release notes provided with the core list known discrepancies between this handbook and the core release associated with the release notes.

Supported Families

- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3L
- ProASIC PLUS®
- Fusion
- Axcelerator®
- RTAX-S
- SX-A
- RTSX-S

1 Functional Block Description

Figure 1-1 shows the block diagram of the CoreUART normal mode functionality. Figure 1-2 on page 8 shows the block diagram of CoreUART with FIFO mode functionality. The baud generator creates a divided down clock enable that correctly paces the transmit and receive state machines.

The function of the receive and transmit state machines is affected by the control inputs BIT8, PARITY_EN, and ODD_N_EVEN. These signals indicate to the state machines how many bits should be transmitted. In addition, the signals suggest the type of parity and whether parity should be generated or checked. The activity of the state machines is paced by the outputs of the baud generator.

To transmit data, it is first loaded into the transmit data buffer in normal mode, and into the transmit FIFO in FIFO mode. Data can be loaded into the buffer until the TXRDY signal is driven inactive. The transmit state machine will immediately begin to transmit data and will continue transmission until the data buffer is empty in normal mode, and until the transmit FIFO is empty in FIFO mode. The state machine first transmits a START bit, followed by the data (LSB first), then the parity (optional), and finally the STOP bit. The data buffer is double-buffered in normal mode, so there is no loading latency.

The receive state machine monitors the activity of the RX signal. Once a START bit is detected, the receive state machine begins to store the data in the receive buffer in normal mode and the receive FIFO in FIFO mode. When the transaction is complete, the RXRDY signal indicates that valid data is available. Parity errors are reported on the PARITY_ERR signal (if enabled), and data overrun conditions are reported on the OVERFLOW signal. Framing errors are reported on the FRAMING_ERR signal. A framing error is defined as a missing stop bit detected by the UART receiver.

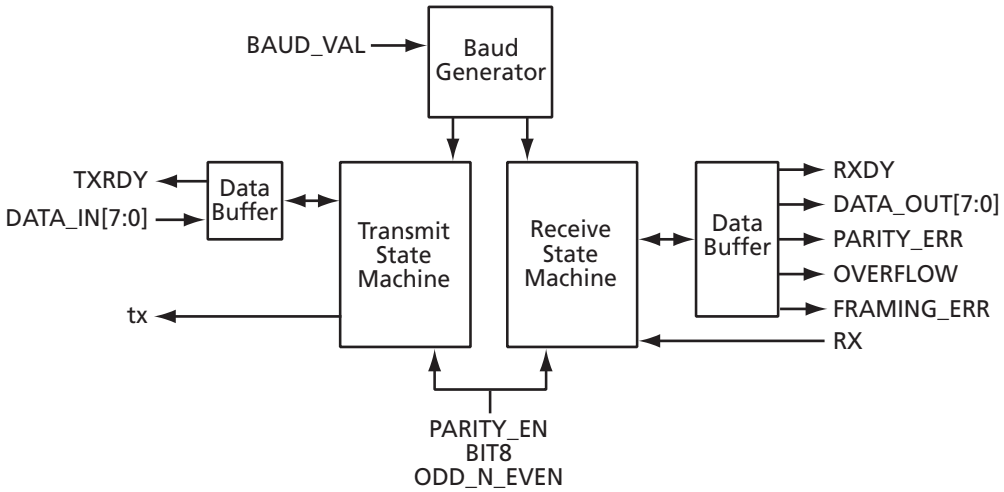

Figure 1-1 · Block Diagram of CoreUART Normal Functionality

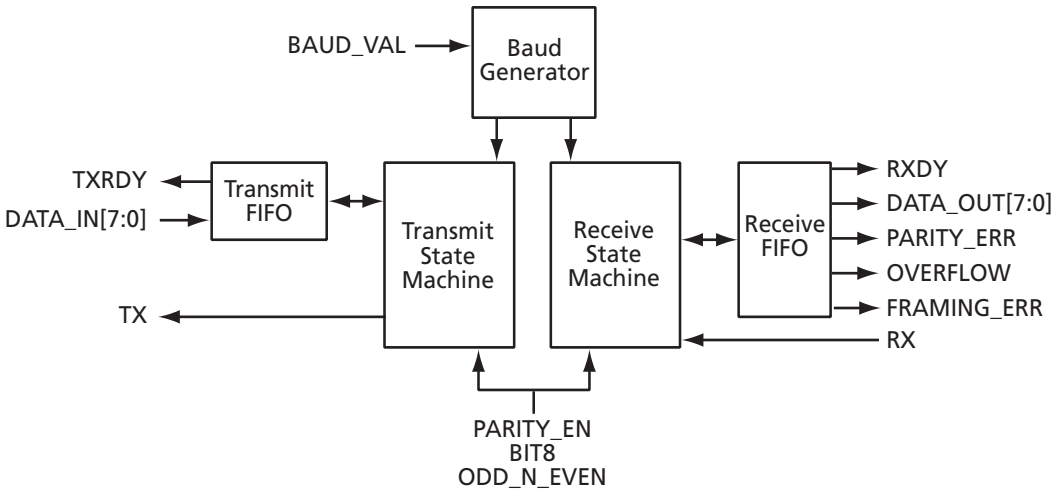

Figure 1-2 · Block Diagram of CoreUART with FIFO Functionality

Device Utilization and Performance

Utilization statistics for targeted devices are listed in Table 1-1 and Table 1-2 on page 9.

Table 1-1 · CoreUART Utilization in FIFO Mode

Family	Cells or Tiles			Memory Blocks	Utilization		Performance MHz
	Sequential	Combinatorial	Total		Device	Total	
IGLOO® IGLOOe IGLOO PLUS	116	192	308	2	AGL600V5	2%	71
ProASIC®3 ProASIC3E ProASIC3L	116	192	308	2	A3P600	5%	128
ProASIC^{PLUS}®	118	281	399	2	APA600	13%	68
Fusion	116	192	308	2	AFS600	2%	127
Axcelerator®	171	215	386	2	AX250	9%	194
RTAX-S	195	199	394	2	RTAX250S	9%	153
SX-A	430	309	739	0	A54SX16A	51%	96
RTSX-S	432	308	740	0	RT54SX32S	26%	62

Notes:

1. *CoreUART supports all standard baud rates, including 110, 300, 1,200, 2,400, 4,800, 9,600, 19,200, 38,400, 57,600, 115,200, 230,400, 460,800, and 921,600 baud.*
2. *The depth of the FIFO for SX-A , and RTSX-S is 16. For the other families, the depth of the FIFO is 256.*

Table 1-2 · CoreUART Utilization in Normal Mode

Family	Cells or Tiles			Memory Blocks	Utilization		Performance MHz
	Sequential	Combinatorial	Total		Device	Total	
IGLOO® IGLOOe IGLOO PLUS	84	167	251	0	AGL600	2%	116
ProASIC®3 ProASIC3E ProASIC3L	84	167	251	0	A3P600	4%	198
ProASIC[PLUS]	85	254	339	0	APA600	11%	89
Fusion	84	167	251	0	AFS600	2%	197
Axcelerator	86	108	194	0	AX500	5%	185
RTAX-S	86	108	194	0	RTAX250S	5%	138
SX-A	82	93	750	0	A54SX16SA	12%	138
RTSX-S	80	92	172	0	RT54SX32S	6%	87

Note: CoreUART supports all standard baud rates, including 110, 300, 1,200, 2,400, 4,800, 9,600, 19,200, 38,400, 57,600, 115,200, 230,400, 460,800, and 921,600 baud.

Programmable Options

There are four programmable inputs to CoreUART: BAUD_VAL (baud rate), BIT8 (number of data bits), PARITY_EN (parity enable), and ODD_N_EVEN (odd or even parity).

Number of Data Bits

The input BIT8 is used to define the number of valid data bits in the serial bitstream. The most significant bit is a "don't care" for the seven-bit case.

Parity

Parity is enabled/disabled with the input PARITY_EN. When parity is enabled, the ODD_N_EVEN input defines the type of parity.

Baud Rate

This baud value is a function of the system clock and the desired baud rate. The value should be set according to EQ 1-1.

$$\text{baud rate} = \frac{\text{clk}}{(\text{baudval} + 1) \times 16}$$

EQ 1-1

where

clk = the frequency of the system clock in hertz
baud rate = the desired baud rate
baudval = BAUD_VAL input

The term baudval must be rounded to the nearest integer. For example, a system with a 33 MHz system clock and a desired baud rate of 9,600 should have a baud_value of 214 decimal or D6 hex. So, to get the desired baud rate, the user should assign 16#D6 to BAUD_VAL input.

Tool Flows

SmartDesign

CoreUART is available for download to the SmartDesign IP Catalog via the Libero® Integrated Design Environment (IDE) web repository. For information on using SmartDesign to instantiate, configure, connect, and generate cores, please refer to the Libero IDE online help.

The Figure 2-1 shows the CoreUART configuration window, as well as cross references to the corresponding top-level parameters.

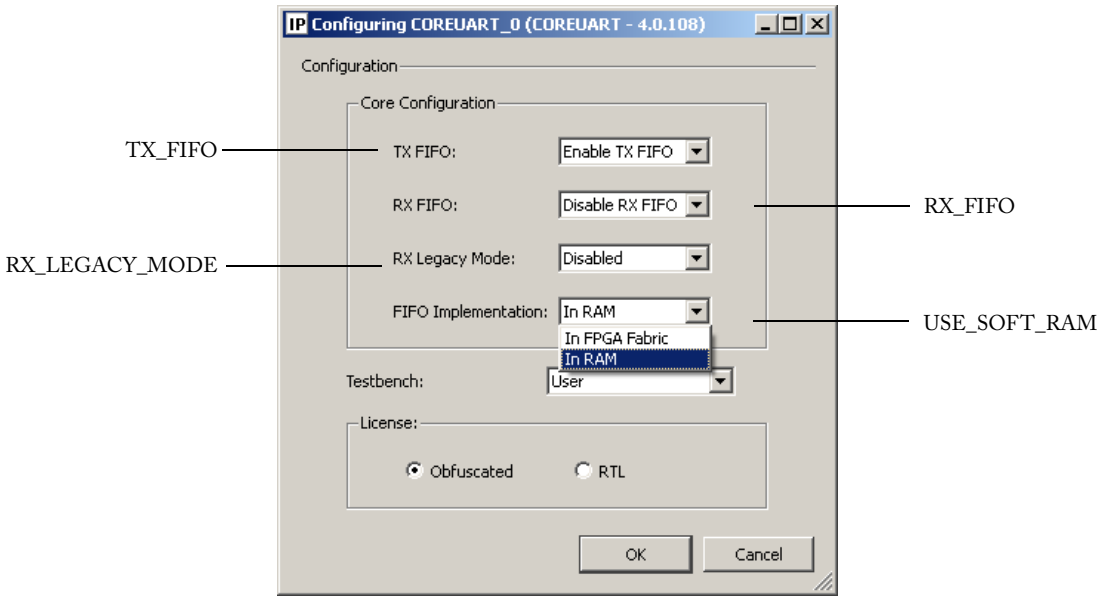

Figure 2-1 · CoreUART Configuration Window

3 Core Interfaces

Signal descriptions for CoreUART are defined in Table 3-1.

Table 3-1 · CoreUART Signals

Name*	Type	Description
CLK	Input	Main system clock
RESET_N	Input	Active low asynchronous reset
DATA_IN[7:0]	Input	Transmit write data bus
DATA_OUT[7:0]	Output	Receive read data bus
WEN	Input	Active low write enable. This signal indicates that the data presented on the DATA_IN[7:0] bus should be registered by the transmit buffer/FIFO logic. This signal should only be active for a single clock cycle per transaction and should only be active when the TXRDY signal is active.
OEN	Input	Active low read enable. This signal is used to indicate that the data on DATA_OUT[7:0] has been read and will reset the RXRDY bit and any error conditions (OVERFLOW or PARITY_ERR).
CSN	Input	Active low chip select. The CSN signal qualifies both the WEN and OEN signals. For embedded applications, this signal should be tied to logic 0.
BIT8	Input	Control bit for data bit width for both receive and transmit functions. When BIT8 is logic 1, the data width is 8 bits; otherwise, the data width is 7 bits, data defined by DATA_IN[7] is ignored, and DATA_OUT[7] is “don’t care.”
PARITY_EN	Input	Control bit to enable parity for both receive and transmit functions. Parity is enabled when the bit is set to logic 1.
ODD_N_EVEN	Input	Control bit to define odd or even parity for both receive and transmit functions. When the PARITY_EN control bit is set, a '1' on this bit indicates odd parity and a '0' indicates even parity.
BAUD_VAL[12:0]	Input	13-bit control bus used to define the baud rate
TXRDY	Output	Status bit; when set to logic 0, indicates that the transmit data buffer/FIFO is not available for additional transmit data.
RXRDY	Output	Status bit; when set to logic 1, indicates that data is available in the receive data buffer/FIFO to be read by the system logic. The data buffer/FIFO controller must be notified of the receipt by simultaneous activation of the OEN and CSN signals to prevent erroneous overflow conditions.
PARITY_ERR	Output	Status bit; when set to logic 1, indicates a parity error during a receive transaction. This bit is synchronously cleared by simultaneous activation of the OEN and CSN signals.
OVERFLOW	Output	Status bit; when set to logic 1, indicates that a receive overflow has occurred. This bit is synchronously cleared by simultaneous activation of the OEN and CSN signals.
RX	Input	Serial receive data

Notes:

1. **Active low signals are designated with a trailing uppercase* N..
2. *When RX_FIFO is enabled, PARITY_ERR is asserted when a parity error occurs, but deasserted before CoreUART receives the next byte. It is the user's responsibility to monitor the PARITY_ERR signal (e.g., treat it as an interrupt signal), as it is non-persistent when RX_FIFO = 1.*

Table 3-1 · CoreUART Signals (continued)

Name*	Type	Description
TX	Output	Serial transmit data
FRAMING_ERR	Output	Status bit; when set to logic 1, indicates that a framing error (missing stop bit) has occurred. This bit is synchronously cleared by simultaneous activation of the OEN and CSN signals.

Notes:

1. **Active low signals are designated with a trailing uppercase* N..
2. *When RX_FIFO is enabled, PARITY_ERR is asserted when a parity error occurs, but deasserted before CoreUART receives the next byte. It is the user's responsibility to monitor the PARITY_ERR signal (e.g., treat it as an interrupt signal), as it is non-persistent when RX_FIFO = 1.*

Core Parameters

CoreUART Configurable Options

There are a number of configurable options that apply to CoreUART, as shown in Table 3-2. If a configuration other than the default is required, the user should use the configuration dialog box in CoreConsole to select appropriate values for the configurable options.

Table 3-2 · CoreUART Configurable Options

Configurable Options	Default Setting	Description
TX_FIFO	Disabled	Enables or disables transmit FIFO
RX_FIFO	Disabled	Enables or disables receive FIFO
FAMILY	ProASIC3	Selects target family. Must be set to match the supported FPGA family. 8 – SX-A 9 – RTSXS 11 – Axcelerator 12 – RTAX-S 14 – ProASIC^{PLUS} 15 – ProASIC3 16 – ProASIC3E 17 – Fusion 20 – IGLOO 21 – IGLOOe 22 – ProASIC3L 23 – IGLOO PLUS
RX_LEGACY_MODE	Disabled	When disabled, the RXRDY signal is synchronized with the FRAMING_ERR output, which occurs after the stop bit. When enabled (Legacy mode), the RXRDY signal is asserted after all data bits have been received, but before the stop bit.
USE_SOFT_FIFO	Disabled	When disabled, the FIFO is implemented using a device-specific hard macro. When enabled, a 16-byte FIFO is implemented in FPGA logic instead. RTAX and RTSX-S devices use this soft FIFO by default.

4

Timing Diagrams

The UART waveforms can be broken down into a few basic functions: transmit data, receive data, and errors. Figure 4-1 shows serial transmit signals, and Figure 4-2 on page 16 shows serial receive signals. Figure 4-3 on page 16 and Figure 4-4 on page 17 show the parity and overflow error cycles, respectively. The number of clock cycles required is equal to the clock frequency divided by the baud rate. All waveforms assume that eight bits of data and parity are enabled. All waveforms, except the 'Framing Error" (Figure 4-5 on page 17), assume Legacy mode is ENABLED.

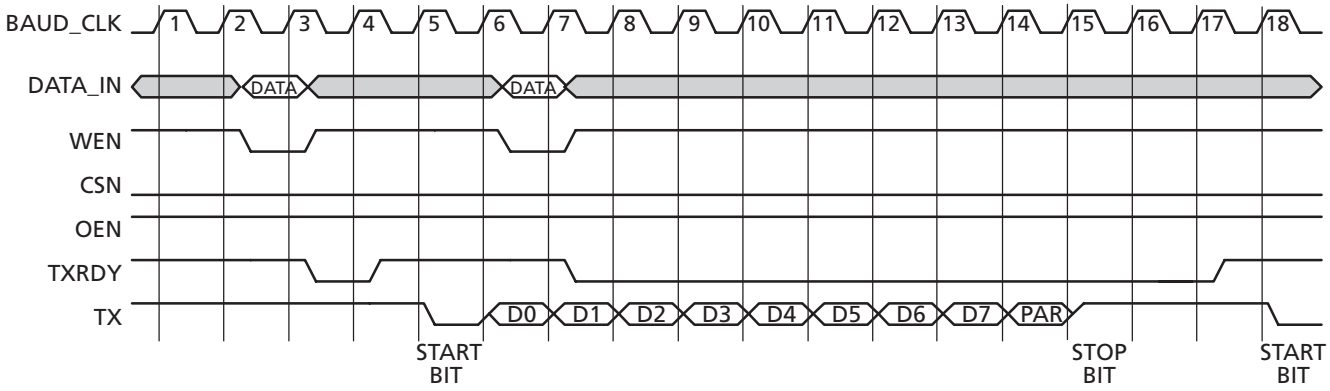

Figure 4-1 · Serial Transmit

Notes:

1. *A serial transmit is initiated by writing data into CoreUART. This is accomplished by providing valid data and asserting the WEN and CSN signals. The TXRDY signal will become inactive for one cycle while the data is being transferred from the transmit hold register to the transmit register that begins the serial transfer.*
2. *The transmission begins with a START bit, followed by data bits 0 through 6, the optional seventh bit, the optional parity bit, and finally the STOP bit.*
3. *Because the UART is double-buffered, data can be queued in the transmit hold register (cycle 7). The TXRDY line, when LOW, indicates that no more data can be transferred to the UART.*

Once the previous serial transfer is complete, the data in the transmit hold register is passed to the transmit register, and the transfer begins. The TXRDY line is also asserted, indicating that the next data byte can be loaded.

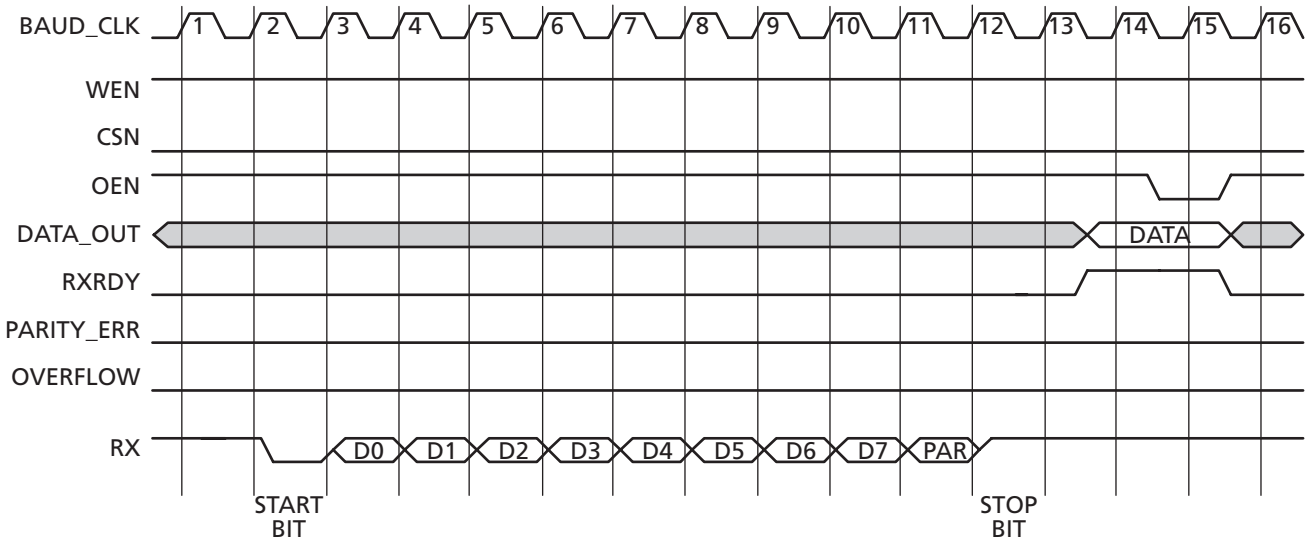

Figure 4-2 · Serial Receive

Notes:

1. *CoreUART continuously monitors the RX line, polling for a START bit. Once the START bit is detected, CoreUART registers the data stream. The optional parity bit is also registered and checked. A START bit is defined as logic 0-bit value on the RX line when the core is idle.*
2. *The data is then loaded into the receive hold buffer, and the RXRDY signal is asserted. The RXRDY signal will remain asserted until the data is read externally, indicated by the simultaneous assertion of CSN and OEN.*

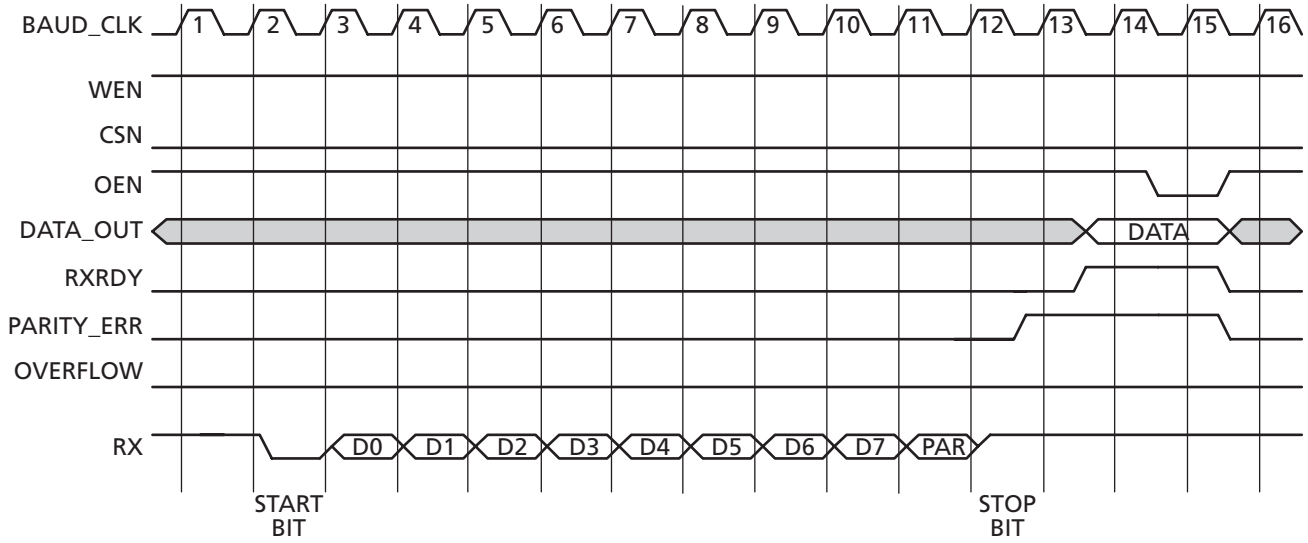

Figure 4-3 · Parity Error

Notes:

1. *When a parity error occurs, the PARITY_ERR signal is asserted.*
2. *The error is cleared by the same method used to read the data, simultaneous assertion of CSN and OEN.*

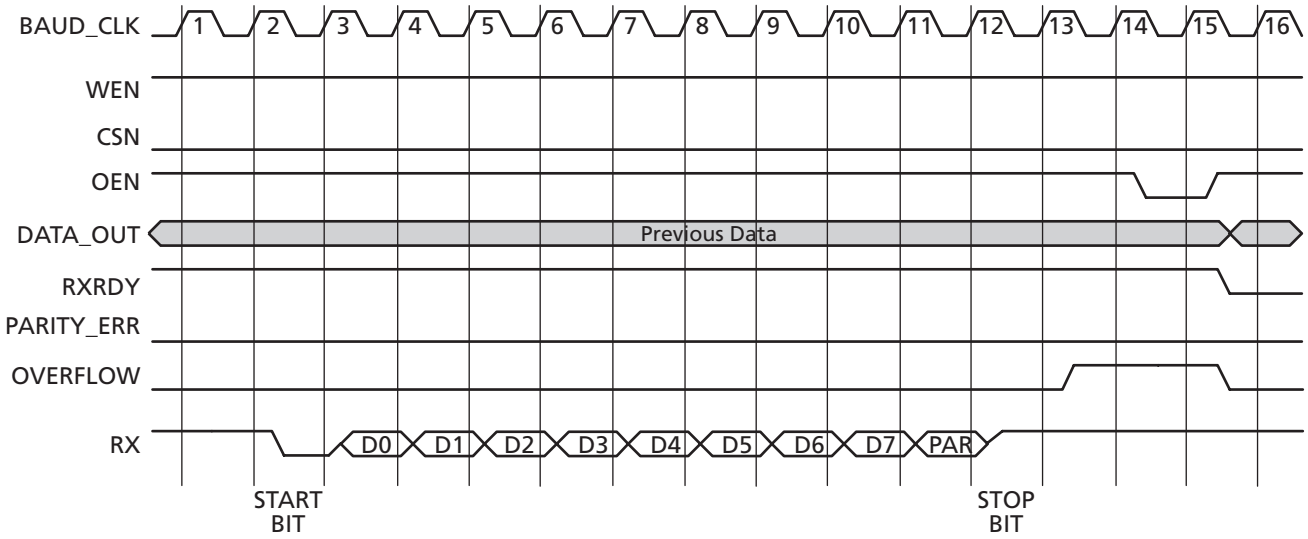

Figure 4-4 · Overflow Error

Notes:

1. *When a data overflow error occurs, the OVERFLOW signal is asserted.*
2. *The previous data is held and the new data is lost. The error is cleared by the same method used to read the data, simultaneous assertion of CSN and OEN.*

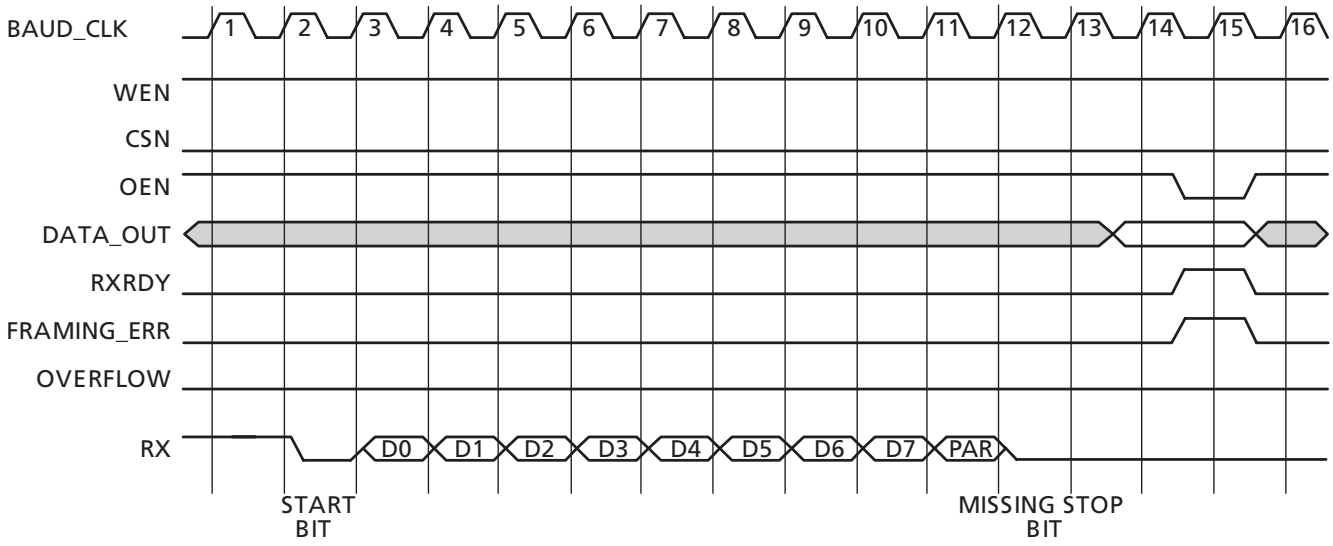

Figure 4-5 · Framing Error

Notes:

1. *Legacy mode is disabled in this timing diagram.*
2. *In Normal (non-Legacy) mode, RXRDY and FRAMING_ERR are synchronized. They are asserted in the same clock cycle.. The error is cleared using a read operation – simultaneous assertion of OEN and CSN.*

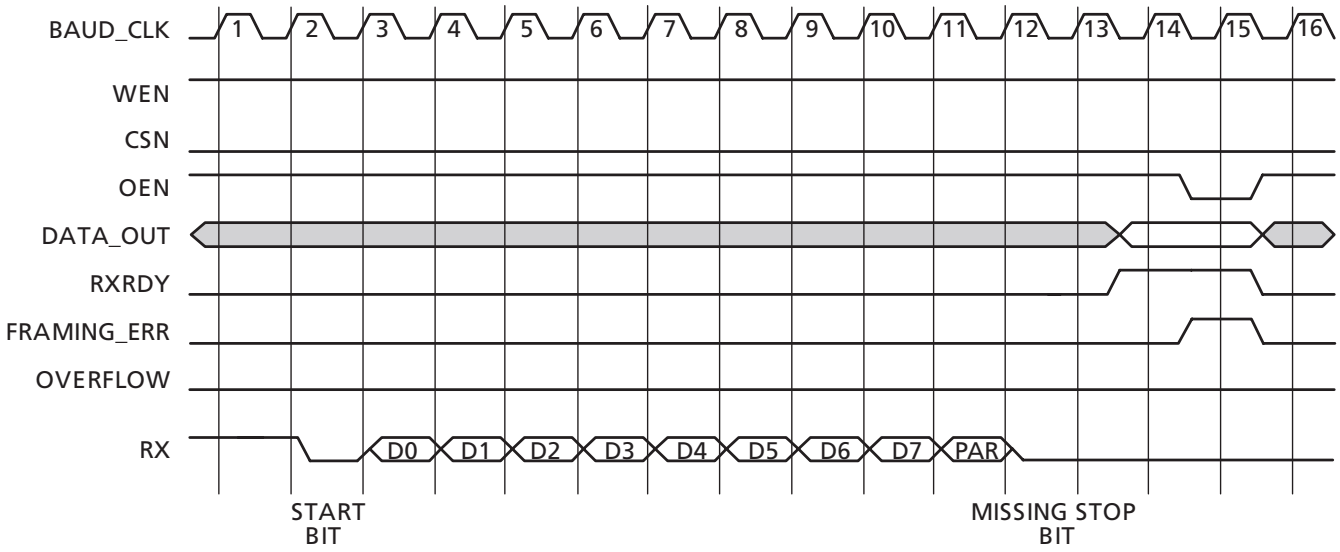

Figure 4-6 · Framing Error in Legacy Mode

Notes:

1. *Legacy mode is enabled in this timing diagram.*
2. *In Legacy mode, RXRDY is asserted one cycle before FRAMING_ERR is asserted. The error is cleared using a read operation: simultaneous assertion of OEN and CSN.*

5 Testbench Operation

Two testbenches are provided with CoreUART: Verilog and VHDL verification testbenches. These are complex testbenches that verify core operation. These testbenches exercise all the features of the core. Actel recommends not modifying these testbenches.

User Testbench

CoreUART is provided with a user testbench (Figure 5-1) to demonstrate sample UART operation. The testbenches are available in both Verilog and VHDL and contain two instances of CoreUART connected to each other. The source code is made available with Obfuscated and RTL licenses of the core.

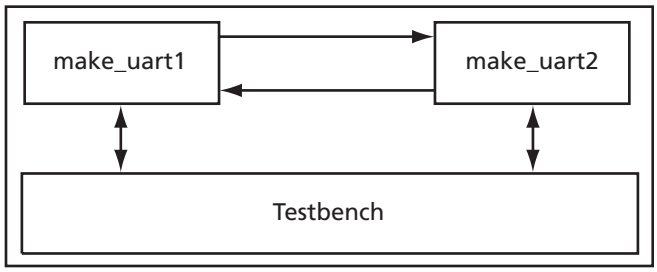

Figure 5-1 · Verification Testbench

The testbench contains the tests listed in Table 5-1.

Table 5-1 · Verification Tests

No.	Bit	Parity	Parity Setting	Parity Error	Overflow Error	Framing Error	Procedure Call
1	8	Enabled	Even	No	No	No	txrxtest
2	8	Enabled	Odd	No	No	No	txrxtest
3	7	Enabled	Even	No	No	No	txrxtest
4	7	Enabled	Odd	No	No	No	txrxtest
5	8	Disabled	N/A	No	No	No	txrxtest
6	8	Disabled	N/A	No	No	No	txrxtest
7	7	Disabled	N/A	No	No	No	txrxtest
8	7	Disabled	N/A	No	No	No	txrxtest
9	8	Enabled	Even	Yes	No	No	paritytest
10	8	Enabled	Odd	Yes	No	No	paritytest
11	7	Enabled	Even	Yes	No	No	paritytest
12	7	Enabled	Odd	Yes	No	No	paritytest
13	8	Enabled	Odd	No	Yes	No	testoverflow
14	8	Enabled	Odd	No	No	Yes	N/A

The procedure calls *txrxtest*, *paritytest*, and *testoverflow* are defined in the file *tbpack.vhd*. The top-level testbench, *testbench.vhd*, utilizes these procedures to perform the corresponding tests listed in Table 5-1.

Refer to the *source* directory on the release CD for source code for the testbench.

6 Ordering Information

Ordering Codes

CoreUART can be ordered through your local Actel sales representative. It should be ordered using the following number scheme: CoreUART-XX, where XX is listed in Table 6-1.

Table 6-1 · Ordering Codes

XX	Description
OM	RTL for Obfuscated RTL – multiple-use license
RM	RTL for RTL source – multiple-use license

Note: CoreUART-OM is included free with a Libero IDE license

A

List of Document Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v2.1)	Page
December 08	Added framing error (FRAMING_ERR signal) support	7
	Updated tool flow section with SmartDesign flow	11
	Updated Table 3-1 to include FRAMING_EERR signal	13
	Updated Table 3-2 with new configurable options	14
	Added Framing Error and Framing Error in Legacy Mode timing diagrams	17–18

B

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