2.1 Sampling and Triggering Architecture

My proposed storage-centric sensing architecture is shown in Figure 2. Traditional analog sampling architectures (shown in gray) include a sensor, optional fixed-gain amplifier (FGA), low-pass filter (LPF), programmable gain amplifier (PGA), and an analog-to-digital converter (ADC), while triggering support is provided with an optional detector and a comparator. My proposed changes to this architecture (shown in black) include adding sample-and-hold (S/H) and adding two queues between the ADC and processor.

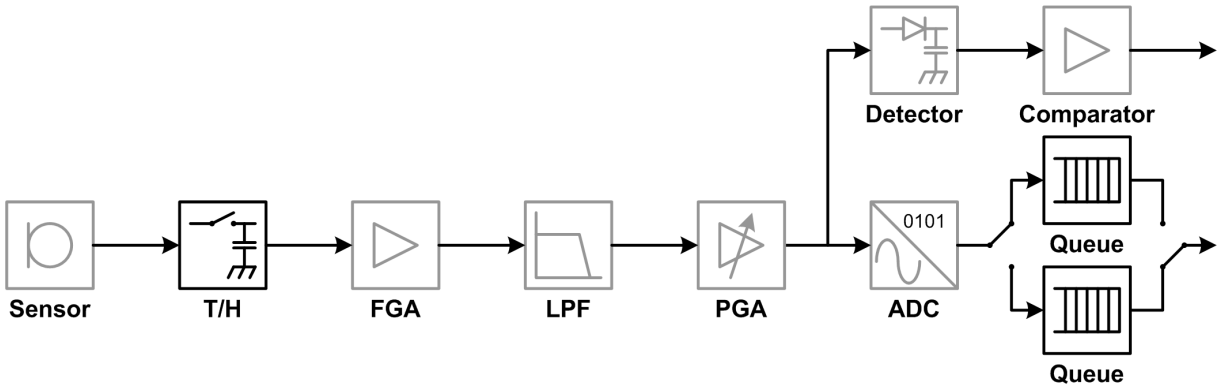

Figure 2: The proposed sensing architecture. Storage in the form of a sample-and-hold (S/H) and two queues allows efficient, reliable, and high-throughput, low-jitter sampling. The sample-and-hold can track or acquire an analog voltage on the input and then hold this voltage on the output even after the input voltage is removed. The queue holds digitized samples until they can be processed.

The efficiency gains in this architecture come from decoupling the sensing, signal conditioning, and digital signal processing and letting each operate relatively independently of the others. In a synchronous streaming architecture, duty cycling is typically implemented by the processor by waking up once per sample, turning on the sensor and ADC, waiting until the output of the low-pass filter settles, and taking a sample. Since the elements in the signal chain operate synchronously, the overall minimum on time is the maximum on time for any element. Many sensors like accelerometers, magnetometers, and microphones have much faster startup times (in the range of 1 μs to 1 ms) than the settling time of a typical anti-aliasing low-pass filter (30 ms to 50 ms). Therefore, the sensor may remain turned on for orders of magnitude longer than necessary, which severely impacts energy-efficiency. Placing a sample-and-hold – a single analog storage element – allows the sensor to be duty cycled at a lower rate than the rest of the signal conditioning chain, enabling greater energy-efficiency. Similarly, using an external ADC allows a much broader selection of circuits to be considered. Rather than being limited to the ADC integrated into the processor, this allows us to choose more energy-efficient options that have faster startup times, much lower quiescent power, and a very low but variable active power that scales with the conversion frequency.

The reliability of signal reconstruction is enabled by moving the ADC outside of the processor and placing a queue between the two elements. In exceptional event detection, for example, the goal is to both detect and classify an ephemeral event (e.g. gunshot). To avoid false positives, signals are averaged and detection thresholds are set high, but such filtering creates a phase lag in the detector output with respect to the original signal. As a result, by the time the processor begins capturing data, the event signature is lost and classification is not possible. The storage-centric sensing architecture avoids this problem by buffering samples using a queue with head-drop semantics. This way, signal samples taken just before the detector fires are available for processing and signal reconstruction.

The proposed pipeline architecture [38, 45] should offer high throughput sampling with low jitter. The addition of a queue provides a way to decouple the sensing and signal conditioning from the digital signal processing on the processor. This allows processing to occur on batches of samples, eliminates the need to synchronize the acquisition and processing of data, and allows the processor to handle other time-critical tasks, such as network or flash I/O, without affecting the timing of sample acquistion. The second queue allows samples to be double-buffered, allowing one queue to be drained while the other is filled.