An SOI Process for Integrated Solar Power, Circuitry and Actuators for Autonomous Microelectromechanical Systems

by

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Abstract

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A new process has been developed for fabricating integrated, solar-powered microelectromechanical systems (MEMS) on a silicon-on-insulator (SOI) wafer. The process provides for the fabrication of high voltage solar cell arrays, high aspect ratio electrostatic actuators and high voltage switches which can be controlled with a low voltage input. To demonstrate the capabilities of this process, an electrostatic actuator was operated with power provided by an on-chip solar array and controlled with an on-chip power switch.

One of the primary challenges in creating a successful autonomous microsystem, such as a microrobot or a distributed sensor node, is providing sufficient power. If electrostatic actuation is used, the power should be both high in voltage for effective operation and sustainable to extend the usefulness of the device. Using a large number of solar cells wired in series solves both of these problems. Furthermore, by integrating the fabrication of the solar cells with the other elements of the microsystem, the complete device can be simplified and its size can be minimized.

Three versions of the process are presented which differ in fabrication complexity and circuit capabilities. The most basic variation, which requires only one dopant drive-in

step, can provide NMOS circuits and uses metal for the gates of the FETs. The next step up provides CMOS circuitry while still using metal gates. However, this added capability requires an extra drive-in step. The final version provides CMOS circuits with self-aligned polysilicon gates which has improved performance and reduced size for the circuitry but is more difficult to fabricate. Some of the other features of this process include the following: a highly doped back surface field and an anti-reflective oxide layer over the solar cells to improve efficiency; isolation trenches etched through the device layer and backfilled with nitride and undoped polysilicon; a second metal layer to provide a light block for the circuit elements; and a layer of germanium which is deposited over the solar cells and circuits to protect them during the HF release of the electrostatic actuators.

This process has been used to fabricate solar cells with up to 200 cells wired in series. The best performance for a 20 cell array had an estimated efficiency of 11.7% under solar illumination. The highest voltage achieved was 88.5 V from an array with 200 cells. The efficiency of this array was estimated at 8.3%. To provide effective switching, the transistors need to have a high drain-to-source breakdown voltage and a low threshold voltage. The NMOS transistors had a breakdown voltage greater than 25 V and a threshold voltage of approximately 2.25 V. The simplest switch which has been fabricated in this process is an NMOS transistor with a pull-up resistor. This switch has been shown to effectively switch a 25 V signal with an input less than 5 V. Gap-closing, electrostatic actuators have also been fabricated and successfully operated with power provided by an on-chip solar array and controlled by an on-chip switch.

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Professor Albert P. Pisano, Chair Date

Dedicated to my wife, Van.

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1. INTRODUCTION

1.1 MOTIVATION

Advances in the research areas of microelectromechanical systems (MEMS) and low power circuits have enabled the development of autonomous microsystems. Two examples which are intended as target applications for the research presented here are microrobots [1-4] and distributed sensor networks [5,6]. Although examples exist of each of these which require external power connections, the benefits gained by freeing them from this constraint are considerable.

For the case of distributed sensor networks, the benefit varies depending on the setting. For networks that monitor locations with a power infrastructure in place, like a building or an industrial plant, external power is typically available. The cost of installing the network, however, increases significantly if every single node has to be connected to the power grid. The flexibility is also reduced in that, if a node needs to be repositioned, considerably more effort is required to do so. Additionally, if the power supply of the building is interrupted, the viability of the network may be threatened as well.

For other situations, providing external power to the network may not be an option. If a distributed sensor network were used to monitor a forest for fires or animal movement patterns, the nodes would have to be autonomous. The battlefield is yet another location where autonomy is critical to the successful operation of the network.

The same is true for microrobots. Although a number of devices have been demonstrated that rely on external tethers or specially designed environments for power [2][7], the full potential of the microrobot cannot be realized without being autonomous.

Creation of successful, autonomous microsystems requires the power problem to be addressed from both sides. This includes the amount of power required for operation and

the amount which is available. As previously mentioned, the development of low power circuits has already had a positive effect [8]. Because the devices are independent, the power must either be stored on-board or scavenged from the environment. A number of options exist for energy storage, including batteries, charged capacitors, radioactive materials and liquid fuels [12]. Since the amount of energy that is stored is directly related to the volume of the storage medium, then the design of a device that relies solely on stored energy must be balanced between the size and the lifetime.

If, however, the device is able to scavenge energy from its environment, then its size can be reduced and/or its lifetime can be extended. Depending on the system requirements and the environment, scavenging can either replace energy storage or it can supplement it. For example, a power system that uses a solar cell to recharge a small battery can provide a flexible and effective solution [9].

A few examples of power sources for scavenging are solar and artificial light, mechanical vibrations and the heat emitted by living organisms [10][11]. The best choice for a specific device depends on many different factors, including its power needs and its surroundings. Because light is present for at least some portion of the day in most places, both indoors and out, it is the most logical choice for many applications. The amount of power available ranges from approximately 1 mW/mm^2 outside on a sunny day to 1-10 $\mu W/mm^2$ for typical indoor settings, depending on the type of lighting used [20].

Another benefit of using photogenerators is that, by wiring a large number of solar cells in series, high voltages can be easily achieved. This makes them especially well suited to microsystems which utilize either electrostatic or piezoelectric actuation. Both of these actuation schemes work well with high voltage, low current supplies.

There are a number of different materials which can be used to generate power from light. They include common semiconductor materials like single crystal silicon, gallium arsenide and amorphous silicon and less common materials like cadmium tellurium and cadmium sulfide [25]. It is even possible to create a solar cell out of spinach and

toothpaste, although that choice would be more difficult to integrate with a MEMS process [14]. The graph in Fig. 1-1 shows the theoretical maximum efficiencies for some common solar cell materials [15].

When deciding what material to use for power generation, an important material property which affects the design of the device is whether the material has a direct or indirect bandgap. For a direct bandgap material, like GaAs or a-Si, a photon of light which has an energy greater than the bandgap can create an electron-hole pair by simply raising an electron to a higher energy band. In an indirect bandgap material, like silicon, a two step process is required. Because the conduction band has a non-zero crystal momentum, a shift in crystal momentum is required for an electron-hole pair to be generated. This shift is provided by a quantum particle called a phonon, which has very little energy but large momentum. Therefore, power generation in an indirect bandgap material requires the interaction of both a photon and a phonon which has a lower

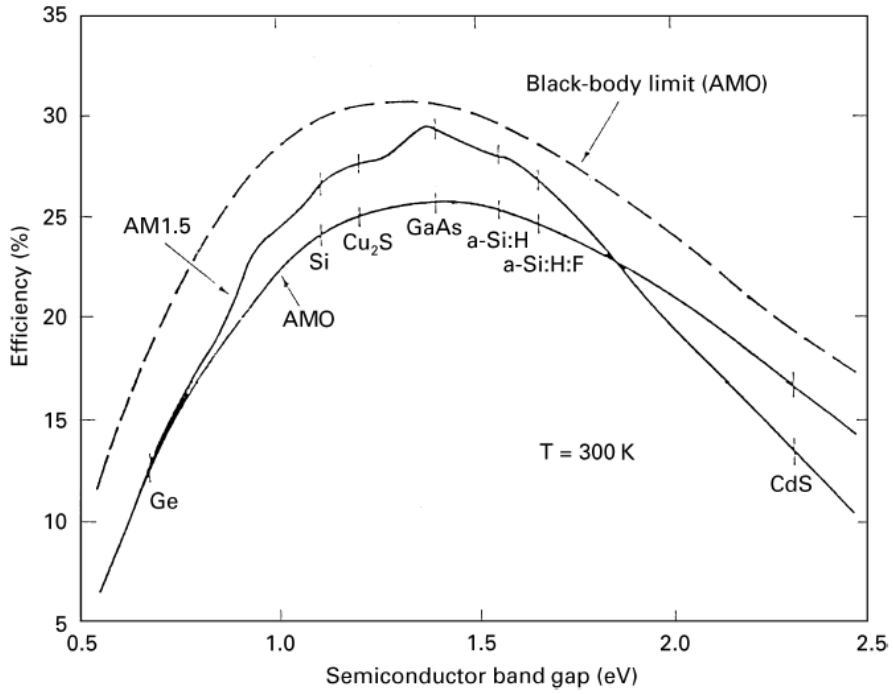


Figure 1-1. *Solar cell materials and their theoretical maximum efficiencies [15].*

probability of occurring than the simpler action of a photon in a direct bandgap material.

The design of a cell is affected because an indirect bandgap material requires a much thicker cell to absorb the same amount of energy when compared to a direct bandgap material. For example, a 100 μm thick silicon solar cell is needed to absorb 90% of the energy whereas a GaAs cell would only need to be 1 μm thick (See Fig. 2-3). For this reason, most of the previous research on solar power for MEMS have used direct bandgap materials.

Autonomous microsystems are often comprised of many devices. For example, the latest Smart Dust sensor node [16] contained a finite-state controller, a photosensor, an oscillator, an optical receiver with filter, an analog-digital converter, a corner-cube retroreflector and a high voltage solar cell array. These devices were fabricated on three separate die. Additionally, a fourth die was to include an accelerometer.

The final assembly of a microsystems separate components into a complete device, including making the necessary electrical connections between them, can often prove difficult. One solution to this problem is the use of self-assembly processes which allow separate components to be positioned and attached automatically, including the electrical connections between devices [17][18]. Alternatively or additionally, maximizing the amount of device integration in order to minimize the number of die can be beneficial. Co-fabrication may also help in reducing the overall size of the device.

In order to consider the possible types of integration, it is assumed that a solar-powered, autonomous microsystem is made up of three types of components. They are circuits, actuators and sensors, and solar cells. Several schemes for the integration of actuators and circuits has been previously demonstrated. They include the integrated fabrication of polysilicon MEMS structures with polysilicon TFTs [13], the side-by-side integration of MEMS actuators and CMOS circuitry on SOI wafers [30][37] and the fabrication of silicon germanium structures on top of a CMOS die [36]. A potential drawback of the side-by-side integration is that the die area that is reserved for the MEMS

structures represents a loss in value. The same price must be paid for the MEMS areas as is paid for the CMOS circuits. Additionally, standard CMOS chips typically operate below 5 V, which may limit the performance of electrostatic MEMS devices.

Another possibility is to integrate the solar cells with the CMOS circuits. Fabricating serially connected solar cell arrays would require the an SOI wafer and device layer isolation. The voltage output of the solar cells could also be potentially limited by the maximum voltage of the CMOS chip. Lastly, the processing would be optimized for the performance of the circuits which may limit the performance of the solar cells.

The third combination would be to integrate the solar cells with the MEMS actuators. One method by which this could be accomplished is to fabricate thin solar cells on the surface of the MEMS chip using a direct bandgap material. Because silicon is a more common material for MEMS processes, it may be difficult to integrate gallium arsenide solar cells with MEMS devices. Amorphous silicon cells would be easier to integrate, but they typically have lower efficiencies which tend to decrease further as they age.

An alternative scheme would be to integrate single crystal silicon solar cells with MEMS structures on an SOI wafer. Using a sufficiently thick device layer would allow for efficient solar cells and high aspect ratio MEMS devices to be made side-by-side. Additionally, the processing required for the solar cells could also be used to fabricate basic, high voltage circuits. Isolation of the device layer through the use of back-filled isolation trenches allow the creation of high voltage solar cell arrays.

The system architecture for an autonomous microsystem using this idea would include a MEMS/power chip and a CMOS control chip. The first chip would have high voltage solar cell arrays and high aspect ratio MEMS structures. There would also be high voltage buffers connecting the solar arrays to the MEMS devices. The CMOS control chip, which would be powered by a separate, lower voltage solar cell array, would control the MEMS devices by switching the high voltage buffers.

The goal of this research project was to develop and demonstrate a process for fabricating the MEMS/power chip.

1.2 PREVIOUS RESEARCH ON SOLAR-POWERED MEMS

The use of solar power for MEMS devices has previously been demonstrated. Some examples include the following.

Ohsawa *et al*. fabricated an array of gallium arsenide solar cells [22]. 24 cells were wired in series to provide an open circuit voltage of 22.5 V. The total area of the array was 1.2 mm^2 with each cell measuring 150 x 160 μm. The array was built on a GaAs substrate with a surface doping of Cr-O. Metal-organic chemical vapor deposition (MO-CVD) was then used to deposit p and n type layers of GaAs to a total thickness of 2.4 μm. The individual cells were isolated from one another and wired in series by etching a 3 μm wide trench around each cell, insulating with a layer of polyimide and applying gold interconnects. Although the open circuit voltage was good, the estimated efficiency based on the reported performance figures was less than 2% when illuminated with 5 W of 815 nm wavelength light. Although intended as the power supply for a micro-solar boat.

Lee *et al*. fabricated an array of 100 hydrogenated, amorphous silicon solar cells with a total area of 1 cm^2 [23]. Each stacked cell was made up of three single cells, with the structure p-i-n/p-i-n/p-i-n. Each three cell stack had an open circuit voltage between 1.8 and 2.3 V. The open circuit voltage for the entire array under AM1.5 illumination was 150 V and the estimated efficiency was 3.2%. The array was used to actuate an electrostatic micromirror which was fabricated separately. The two devices were packaged next to each other and wire bonds were used to connect them together.

Aksyuk *et al*. fabricated a novel device that used an optically-powered limiter for the intensity of light in a fiber optic line [24]. Their device used a 30 cell, InGaAs photogenerator to drive a MEMS variable optical attenuator. The photogenerator derived its power from the signal travelling through the fiber optic line such that no external power

was required for its operation.

1.3 PREVIOUS RESEARCH ON SILICON-ON-INSULATOR SOLAR CELLS

To provide a starting point for the design of the solar cells, the work of Hebling *et al*. was used as a model [26]. The solar cells from that research were thin film cells fabricated on a SIMOX SOI wafer. SIMOX, or Separation by Implanted Oxygen, wafers are created by implanting a silicon wafer with oxygen and subsequently annealing it to create a buried oxide layer between the handle wafer and a very thin silicon layer. An epitaxial CVD step was then done to increase the device layer thickness to 46 μm. The cells used a surface texturization created in a KOH bath to decrease the amount of light lost to reflection from the top surface. Diffusions followed by drive-ins were used to introduce the necessary dopants to create the solar cells. Contact to both the p and n regions were made through metal collector lines.

The output of the cells was measured to have an efficiency of 18.2% under AM1.5 solar illumination. Because the entire device layer was a continuous, the wafer functioned as a single solar cell with an open circuit voltage output of less than 1 V. Addition of a means to isolate parts of the device layer is necessary before individual solar cells could be wired in series to provide the high voltage output useful for electrostatic MEMS devices.

1.4 MOTIVATING EXAMPLE

Before the development of the process presented here, the research focus was to develop MEMS devices to aid in the deployment of sensor nodes in air. These were modeled after two designs that plants use to disperse seeds. They include floating specimens, like dandelion seeds, and autorotating specimens, like maple seeds. The goal was to fabricate MEMS devices using the HexSil molding process [27] that approximated

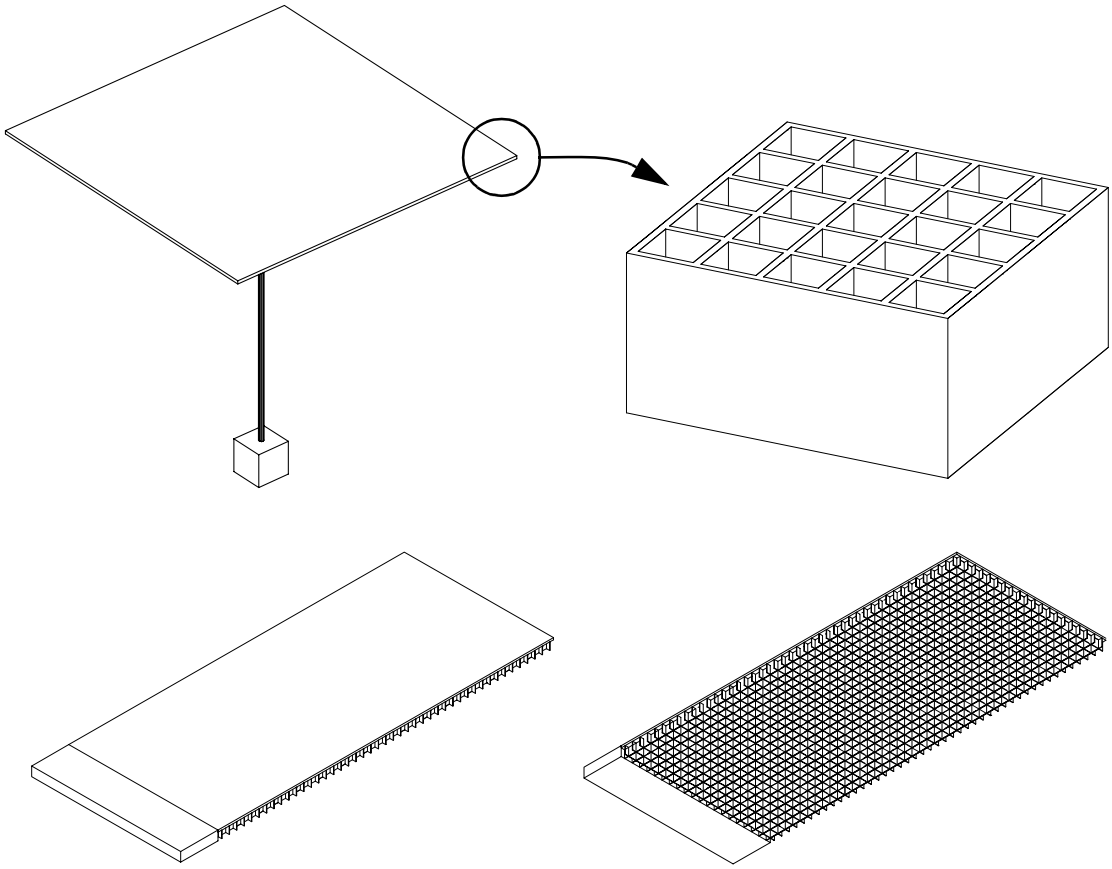


Figure 1-2. *Conceptual drawings for MEMS dandelion seeds and maple seeds.*

the seeds. Conceptual drawings of each device are shown in Fig. 1-2.

The concept behind the dandelion seeds is that the individual hairs of the actual seed or the beams of the MEMS device are small enough to cause the flow around them to be laminar. This creates a larger drag force in the air than would be attained with a parachute or solid sheet of the same size. The MEMS dandelion seeds were created by etching trenches into a silicon wafer, growing a sacrificial oxide on the walls of the trenches and then filling them up with polysilicon. After the polysilicon was removed from the top surface of the wafer, the structures were released by etching away the sacrificial oxide layer. A resulting device is shown in Fig. 1-3. By varying the size of the open areas, it

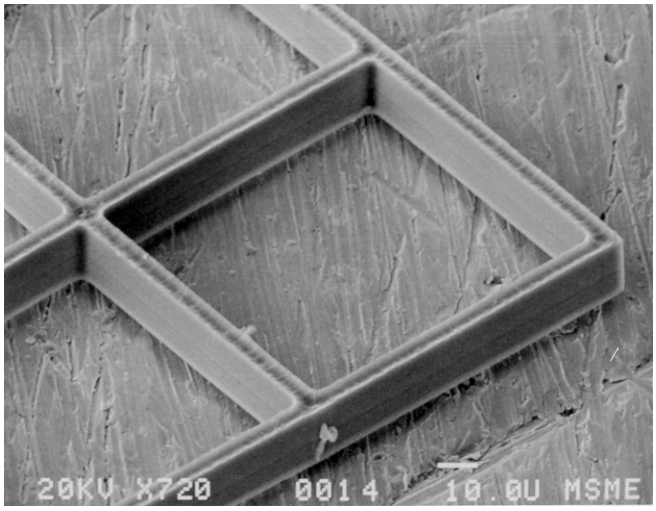


Figure 1-3. *SEM of a fabricated MEMS dandelion seed. Beams are approximately 5 μm wide and 20 μm tall.*

was possible to vary the flight dynamics in air. Devices with large openings of 100 to 200 μm between beams would fall slowly through the air and remain horizontal. This indicated that the majority of air was travelling through the mesh. Devices with smaller openings of 25 to 50 μm would fall more quickly and would tumble as they fell. These devices behaved as if they were solid sheets and therefore had less drag.

The dynamics which cause maple seeds to autorotate as they fall are primarily based on the weight distribution of the seeds and not the design of the wings [28]. This made it well suited to MEMS fabrication because one could fabricate a flat plate and by controlling the location of devices on it, could cause it to autorotate when dropped. HexSil was once again used to fabricate the devices except that the face sheets were left on the device. By varying the size of the cells, it was possible to adjust the density of the structure in different areas. This can be seen in Fig. 1-4 with the majority of the wing area having large cells except for the leading edge which has small cells. A close up of the transition from large to small cells is also shown.

Because the wing area was relatively large, it was an ideal location to place a solar cell array that would be able to assist in powering the payload both during flight and after the

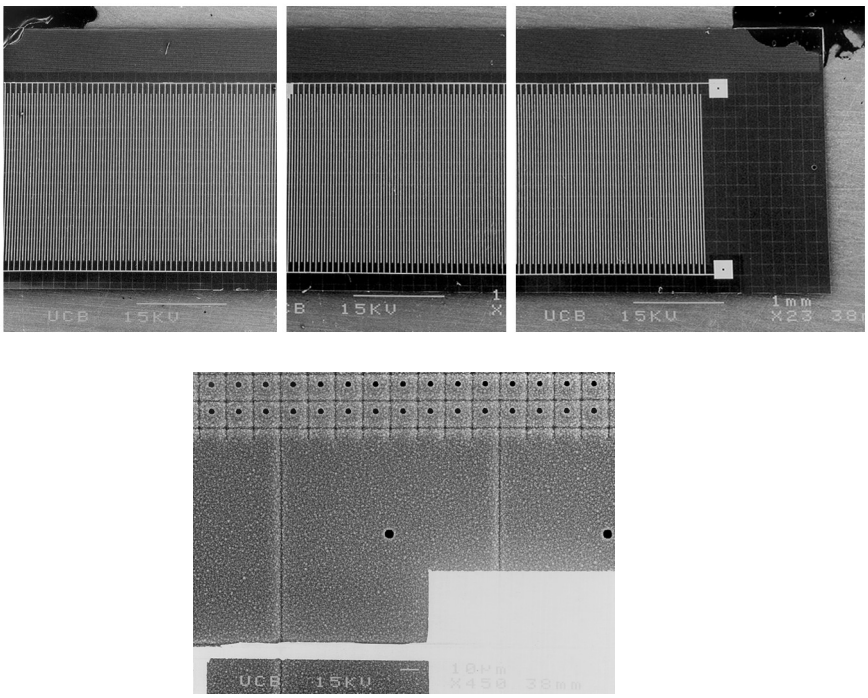


Figure 1-4. *SEM of a HexSil maple seed. Close-up shows the transition from large cells to small cells. Hole at center of each cell is used to release sacrificial layer underneath*

seed had landed. Unfortunately the material used to fabricate the wing, polysilicon, is not well suited to being the basis for efficient solar cells. Additionally there was no simple means of isolating individual cells from one another, so it was not possible to wire a number of cells in series to generate high voltages. The research focus was then switched to developing the integrated, solar powered MEMS process presented here so that higher efficiency, high voltage solar cell arrays could be produced.

2. THE SOI PROCESS FOR INTEGRATED SOLAR POWERED MEMS

2.1 INTRODUCTION

In this chapter, the SOI process which has been developed for fabricating integrated solar powered MEMS will be presented. The goal in developing it was to provide a fabrication process to designers of autonomous microsystems that would have a broad range of capabilities to help them meet their design goals of integrating many different devices together on one silicon chip. The process can be used to create high voltage solar cell arrays, basic circuitry elements capable of handling higher voltages than standard CMOS, and a wide range of electrostatic MEMS actuators and devices.

The integrated SOI process can be broken down into four stages. The first stage includes the creation of the SOI wafers which are used for the process. The second stage includes the formation and back-filling of the isolation trenches. The third stage has the fabrication of the electrical devices, including the solar cells and circuitry elements, and the final stage includes the etching and release of the MEMS structures.

Although the overall structure of the process is similar to the process developed by Brosnihan for the integrated fabrication of standard foundry CMOS and high-aspect-ratio MEMS on an SOI wafer [30], it differs in a number of important areas. First of all, the primary goal in designing the process was to allow the fabrication of efficient solar cells. Although one could make solar cells in a standard CMOS process, they would not be optimized for solar cell performance and would have a lower efficiency. Secondly, although the fabrication of the solar cells and circuits is, in a general way, similar to a CMOS process, it is much simpler. This process is missing many of the steps that are unnecessary for meeting the goals of this research.

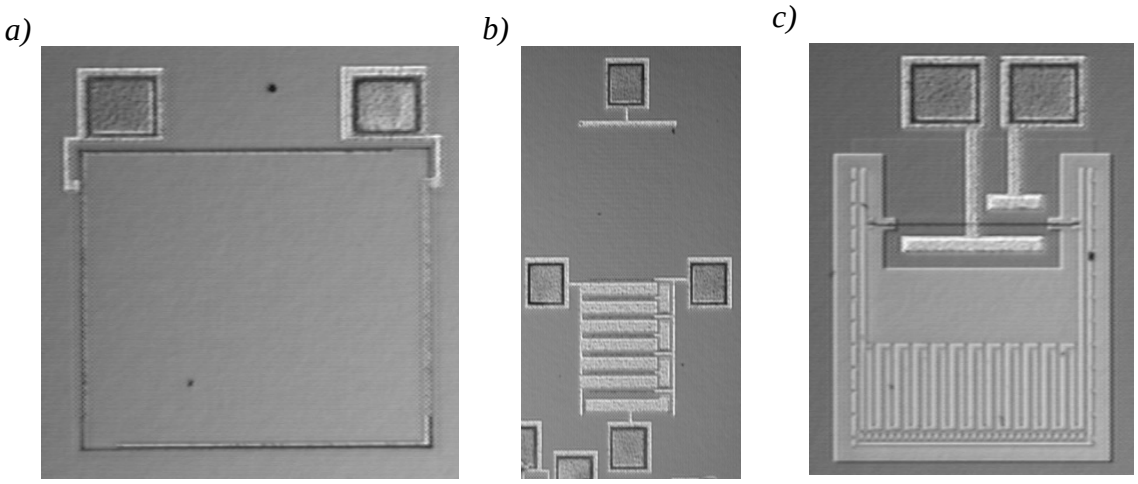


Figure 2-1. *Pictures of the various desired devices from this process. They include a) a solar cell, b) an NMOS inverter and c) an electrostatic actuator.*

In order to provide a frame of reference for the description of the process and the discussion of the important point that will follow in this chapter, the types of desired devices will be briefly described. Considerably more information on each will be given in the next three chapters. They include solar cells, basic circuit elements and electrostatic actuators. Each of these is shown in Fig. 2-1. The solar cell is a large area p-n diode which is surrounded by a back-filled trench so that it is isolated from the rest of the SOI device layer. The circuit elements are basic MOS field-effect transistors and bipolar junction transistors. The electrostatic actuators are high aspect ratio devices that are etched through the SOI device layer. Back-filled isolation trenches are used to isolate the energized and grounded parts of the device, as shown in Fig. 2-1.

In the following sections each of the four process stages will be described in detail followed by a discussion of the important processing considerations.

2.2 PROCESSING STAGE 1: SOI WAFER FABRICATION

2.2.1 PROCESS DESCRIPTION

The steps involved in the fabrication of the SOI wafers which are used for this process are shown in Fig. 2-2. The wafer which will become the device layer is a boron doped silicon wafer. The front surface of this wafer, which will be bonded to the handle wafer, is first implanted with more boron to create highly doped region near the surface (Fig. 2-2a). A one micron thick, wet thermal oxide is then grown on both the handle wafer and the device wafer at 1100°C (Fig. 2-2b). This oxidation step also drives in the implanted boron. The wafers are then hydrated, bonded together by hand and annealed at 1100°C in a steam environment (Fig. 2-2c). At this point, the wafers are inspected using an IR light source and a CCD camera. This will show any voids at the bonding surface. Assuming that there are no large voids, the wafers are ground and polished to the desired device layer thickness (Fig. 2-2d).

2.2.2 DISCUSSION

Because of the specific requirements for the wafers which are used for this process, the wafers were custom fabricated. The three important parameters in the design of the SOI wafers were the device layer doping concentration, the device layer thickness and the bonding oxide layer thickness.

2.2.2.1 DEVICE LAYER DOPANT CONCENTRATIONS

The primary reason for fabricating the SOI wafers instead of purchasing them was to obtain the appropriate doping levels in the device layer for good solar cell performance. The chosen resistivity of the boron doped device wafers was in the range 0.1 - 0.5 Ω-cm. Good quality wafers with resistivities in this range can be difficult to find because the primary market for them would be the solar cell industry, but because most fabricators of

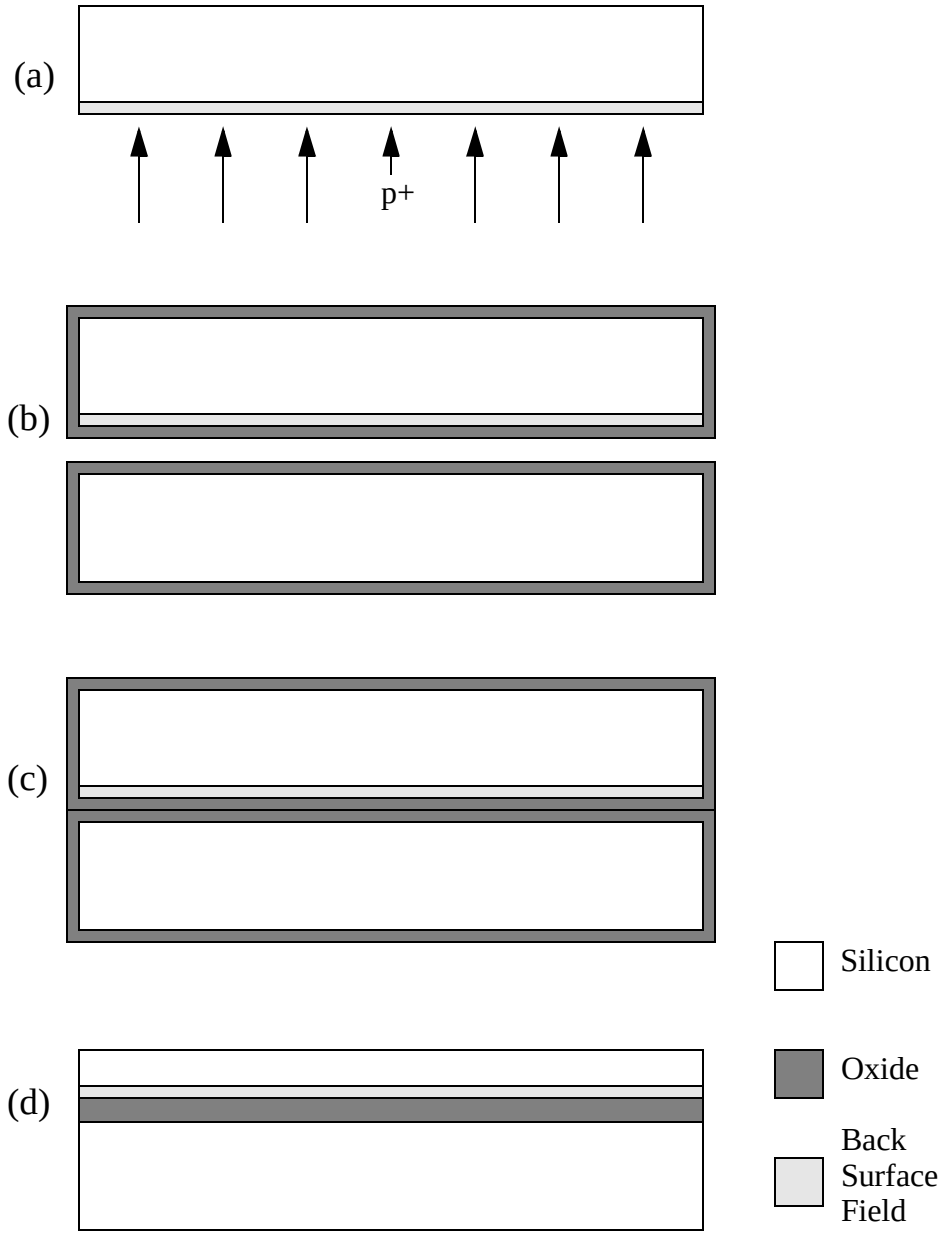


Figure 2-2. *SOI wafer fabrication process.*

solar cells are interested in keeping costs to a minimum, they usually use lower grade silicon.

The other feature which made it more practical to fabricate the wafers was the back

surface field for the solar cells. A back surface field (BSF) is a highly doped region on the bottom of the cell, which is discussed in more detail in Section 3.3.4. The dopant type is the same as the bulk of the cell. Its presence improves the efficiency of the solar cells. Because it is buried at the bottom of the device layer, it must be implanted before the wafer is bonded. Although it would be possible to purchase special SOI wafers with the correct doping and a BSF, the extra time and money required for such a unique wafer made that option impractical.

2.2.2.2 DEVICE LAYER THICKNESS

The thickness of the device layer affects the performance of the final components in many ways. First, it affects the maximum possible efficiency of the solar cells. As light travels through the solar cells, individual photons are absorbed and converted into electrical energy. This process, however, does not occur immediately as the light first hits the silicon. The photons travel some distance into the silicon before being absorbed. If the solar cell is too thin, most of the photons will pass all the way through, never being converted into electrical energy. The graph in Fig. 2-3 shows how the thickness of a solar cell affects the maximum possible electrical output. There is an important difference, however, between the results shown in Fig. 2-3 and the performance of cells fabricated in this process. Because the solar cells fabricated in this process have an oxide layer on the bottom side of the cell, some of the light that passes all the way through is reflected back into the cell, giving it a second chance at absorbing the energy. This reflection effect was previously modeled and reported by Hebling [26].

The thickness of the device layer also has a considerable effect on the performance of the MEMS structures. Electrostatic MEMS structures are made up of three basic components; flexures, proof masses and capacitive plates. These components are all directly affected by the thickness of the device layer, assuming that the photolithography and deep reactive ion etching capabilities do not limit the subsequent increase in aspect ratio. The most beneficial effect is on the flexures. For many MEMS structures, it is

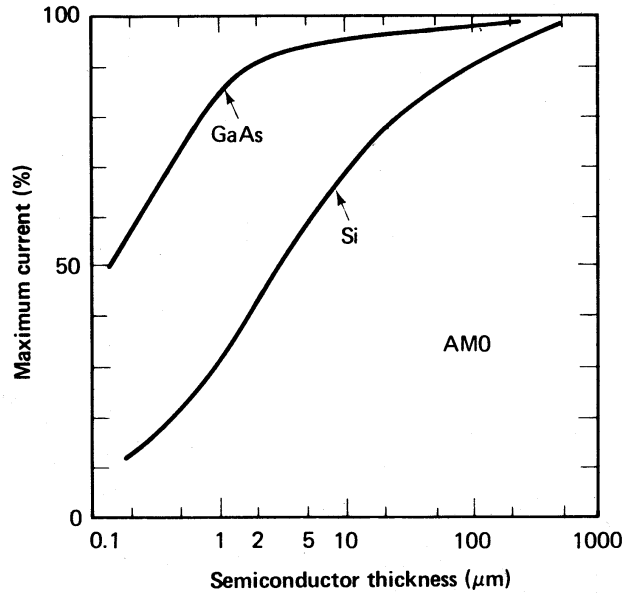


Figure 2-3. *Graph of percentage of maximum possible current as a function of cell thickness. [solar cell book]*

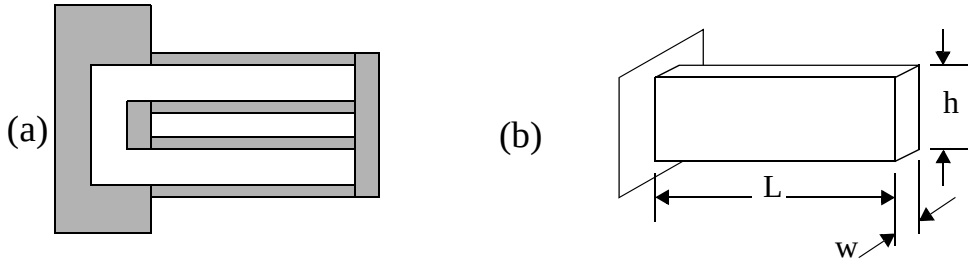


Figure 2-4. *A typical MEMS flexure and its basic building block, the cantilever beam.*

desirable to have a low in-plane stiffness and high out-of-plane stiffness. To demonstrate this, consider a typical MEMS flexure like the one shown in Fig. 2-4a. The basic building block of this is the cantilever beam, shown in Fig. 2-4b. The in-plane stiffness and out-of-plane stiffness for the cantilever beam are given by Eq. (2-1) and Eq. (2-2),

respectively [29], where E is the Young's Modulus.

$$K_x = \frac{Ehw^3}{4L^3} \tag{2-1}$$

$$K_z = \frac{Eh^3w}{4L^3} \tag{2-2}$$

As we increase the height of a flexure while keeping its width constant, we see that the in-plane stiffness increases linearly with height, but the out-of-plane stiffness increases cubically. The performance of the proof masses and capacitive plates are also improved as the height increases as both mass and capacitance increase linearly with height.

The final effect that the thickness of the device layer has is on the weight of the completed device. This is particularly important for microrobotic applications, both flying and crawling, where total weight must be kept to a minimum.

In addition to the design parameters listed above, processing limitations must also be considered. The primary limiting factors is the capabilities of the deep reactive ion etching (DRIE) tool. The smallest features which are etched through the device layer are the isolation trenches, which will be discussed in Section 2.3 and the gear teeth of the inch worm motors, which will be discussed in Section 2.5. The smallest feature size for both of these is 2 μm, based on the capabilities of the lithography used. If one assumes an aspect ratio of 25:1 for the silicon DRIE tool, then we are limited to a device layer thickness of 50 μm. Although higher aspect ratios are possible, they would lead to greater difficulty in the DRIE steps and lower yields.

Lastly, the variation in the grinding and polishing step must be considered. The source which was used during this research had a tolerance of 1 mil, or 25.4 μm. It would therefore be impractical to request a target of 50 μm since a large number of the wafers would likely be returned with device layers that were too thick.

Weighing all of these factors, the target for the device layer thickness was typically set

to be between 30 and 35 μm, which resulted in wafers that had device layers in the range of 25 - 55 μm. The expected efficiency for the solar cells, based on the graphs in Fig. 1-1 and Fig. 2-3, lies between 15 and 20%.

2.2.2.3 BONDING OXIDE LAYER THICKNESS

As mentioned above, the bonding oxide layer does affect the performance of the solar cells by reflecting light back into the cell that passes all the way through it. Although it may be possible to optimize the thickness of the bonding oxide layer to maximize the efficiency, the small gains that would be possible are outweighed by the needs of the MEMS structures. When the structures are released, the bonding oxide layer becomes the gap separating the structures from the handle wafer below. If this gap is too small, the structures may touch the substrate underneath and become stuck, rendering them inoperable. Based on this, it would be desirable to have a very thick bonding oxide layer, but because the bonding oxide layer is made up of thermal oxide layers that are grown on the device and handle wafers before they are bonded, there is a practical limit on the bonding oxide layer thickness. For this process, the thickness was chosen to be 2 μm. This could be fairly easily increased to about 4 μm using the furnaces available at the Berkeley Microfabrication Laboratory and even greater if specialized, high temperature furnaces were used.

2.2.2.4 ALTERNATIVE PROCESS METHODS

There are other methods for fabricating SOI wafers which could be considered as an alternative to the method used here. The first is the SIMOX (Separation by IMplanted OXygen) process, which involves implanting oxygen into a silicon wafer and annealing it, to create a buried oxide layer underneath a thin silicon layer. Hebling used SIMOX wafers to fabricate thin-film, SOI solar cells [26] by using the thin silicon device layer as a seed layer for an epitaxial growth that increased its thickness from 0.2 μm to 46 μm. The benefit in this is that the doping concentration of the device layer can be easily controlled during the epitaxial growth. The drawback is that there is a limit to the bonding oxide

layer thickness of about 0.2 μm, which is too thin for creating moving, electrostatic MEMS structures.

This process could be modified, though to use a hydrogen cut SOI wafer [38]. The hydrogen cut process involves implanting a silicon wafer with hydrogen and then bonding it to another wafer. The first wafer can then be cleaved along the plane of implanted hydrogen by either mechanically separating the wafers or by heating them. It would then be possible to bond a hydrogen implanted wafer to a handle wafer with a sufficiently thick bonding oxide layer, cleave it and grow the remaining device layer epitaxially. This would allow precise control over the dopant concentration and the device layer thickness.

2.3 PROCESSING STAGE 2: FORMATION AND BACK-FILLING OF THE ISOLATION TRENCHES

2.3.1 PROCESS DESCRIPTION

The second stage of the process, the formation and back-filling of the isolation trenches, is shown in Fig. 2-5. A wet thermal oxide layer is first grown on the SOI wafers. This protects the surface of the silicon, which is important for the performance of the circuit elements. Photoresist is spun on the wafer and the pattern for the isolation trenches is applied. The pattern is first etched into the oxide layer using a dry, plasma etch (Fig. 2-5a). Without removing the photoresist mask, the isolation trenches are then etched through the device layer in a Surface Technology Systems (STS) deep reactive ion etching (DRIE) machine (Fig. 2-5b). The photoresist is removed and wafers are cleaned.

The trenches are then lined with a conformal deposition of low stress nitride and filled with a deposition of undoped polysilicon (Fig. 2-5c). The back-fill materials then must be removed from the surface of the wafer so that the devices can be fabricated. The polysilicon is removed first by doing a blanket dry plasma etch, stopping on the nitride layer. The nitride is then removed in hot phosphoric acid. A final etch of the protective oxide layer is done in hydrofluoric acid. The device layer of the wafers is now separated

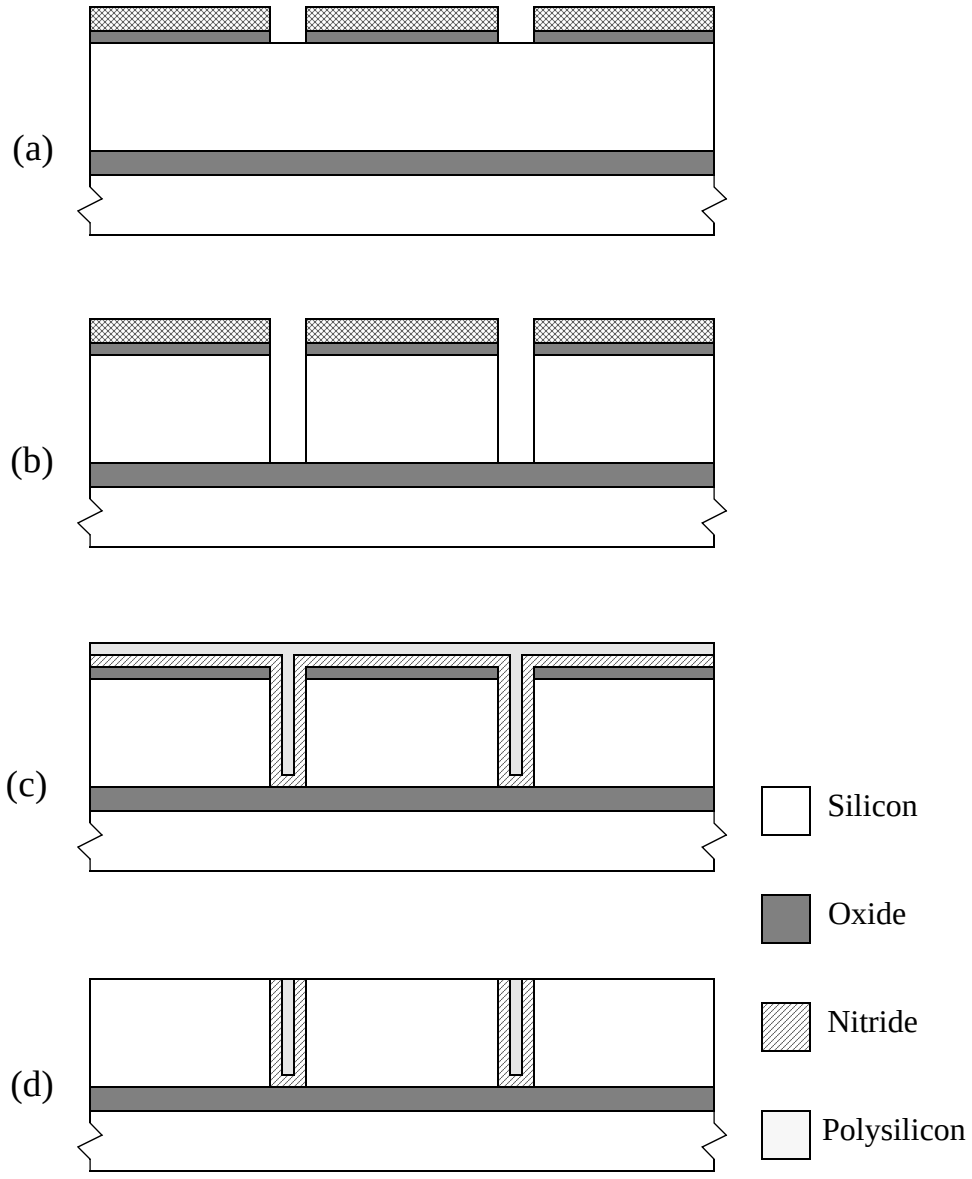


Figure 2-5. *Process steps for the formation and back-filling of the isolation trenches.*

into discrete, electrically isolated regions, ready for the fabrication of solar cells and circuits (Fig. 2-5d).

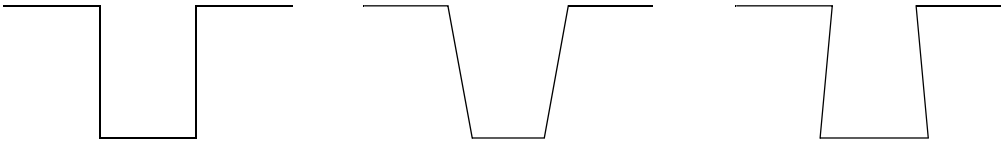


Figure 2-6. *Basic isolation trench profiles. (a) Straight, (b) Tapered and (c) Re-entrant.*

2.3.2 DISCUSSION

The back-filled isolation trenches play an important role in the overall success of this process. The ability to fabricate high voltage solar cell arrays and prewired electrostatic MEMS devices hinges on the electrical and mechanical properties of the isolation technique. The back-filled isolation trenches used in this process are similar to those used by Brosnihan [30]. The isolation trench profile, keyhole reduction and keyhole tolerant design techniques, back-fill materials and alternative processing methods for this stage will be discussed in the following sections.

2.3.2.1 ISOLATION TRENCH PROFILES

Three trench profiles are shown in Fig. 2-6. These ignore complications created by excessive scalloping and footing, common problems associated with deep reactive ion etching of silicon. The straight profile is an idealization that is nearly impossible to attain regularly in practice. The tapered profile may seem like the best choice, because, as the back-fill materials are conformally deposited, they will completely fill the trench without leaving any voids, or keyholes. To see where the problem arises with using a tapered isolation trench, we must consider how the isolation trenches are interfaced with the MEMS structure etch at the end of the process (Section 2.5) to create structures which are electrically isolated but mechanically connected.

Fig. 2-7a shows a U-shaped isolation trench in a block of silicon. Because it is open, it

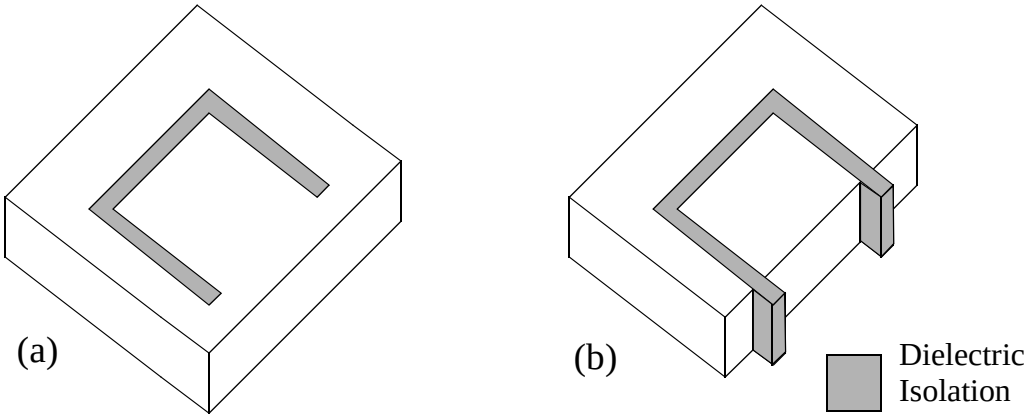


Figure 2-7. *Interface between back-filled isolation trench and silicon DRIE used to create electrically isolated but mechanically connected MEMS structures.*

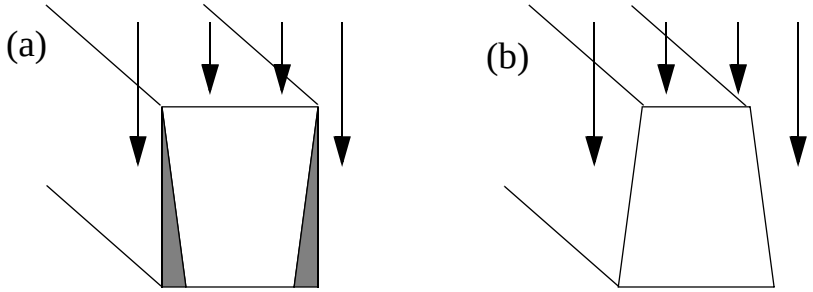
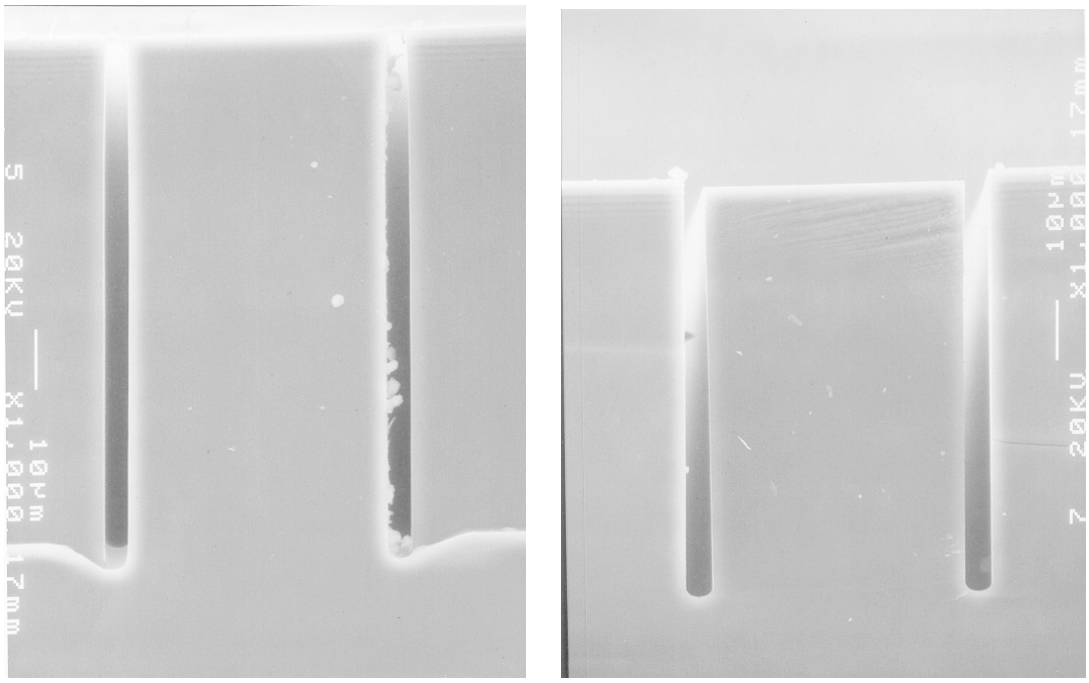


Figure 2-8. *Cross- sections of back-filled isolation trenches. (a) Tapered trench profiles lead to silicon stringers which prohibit complete isolation. (b) Re-entrant trench profiles eliminate stringers.*

obviously provides no electrical isolation, but if the tips of the isolation trench are intersected by a silicon DRIE etch, as shown in Fig. 2-7b, then the silicon on one side of the trench is electrically isolated, but still mechanically connected to the silicon on the other side. To ensure complete electrical isolation, it is very important that there are not any silicon stringers left which complete a circuit around the tip of the back-filled isolation trench. In Fig. 2-8, a cross-section of a tapered isolation trench after a silicon DRIE clearly shows how some of the silicon is in the shadow of the back-fill material protecting it from the anisotropic silicon etch. This silicon stringer would connect around the tip, providing an electrical short.

In Fig. 2-9, the cross-sections of two isolation trench are shown. On the left, the



(a) (b)

Figure 2-9. *Scanning electron micrographs of isolation trenches. The profile of (b) is slightly re-entrant compared to the slightly bowed walls of (a).*

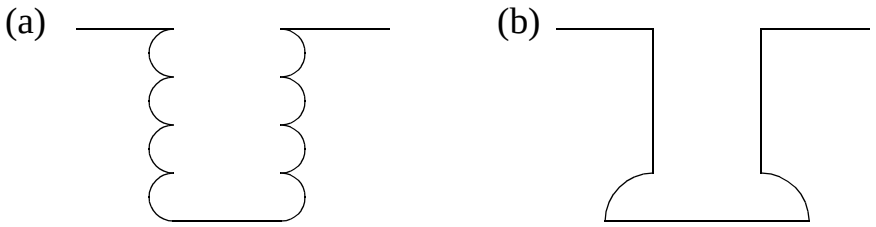


Figure 2-10. *Sidewall profiles for trenches with (a) excessive scalloping and (b) footing.*

trenches are slightly bowed, slightly wider at the middle than at the top or bottom. On the right, the trenches continue to flair slightly as they go deeper. This is the desired profile for the isolation trenches.

The effects of excessive scalloping and footing, shown in Fig. 2-10, must be also be considered. If excessive scalloping were present along the full height of the trench, the isolation around the trenches would be compromised because thin silicon stringers would

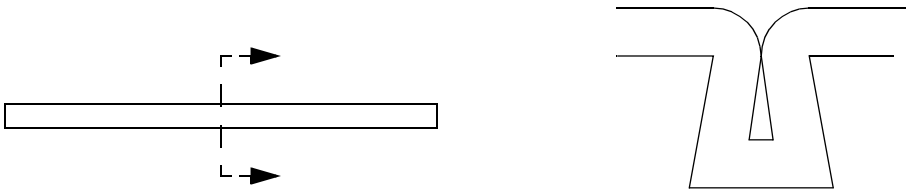


Figure 2-11. *Keyhole characteristics for a straight isolation trench.*

be left underneath the folds of the scallops. Fortunately, scalloping is typically present only at the very top of the trenches. Any stringers left at the top would be completely removed due to the undercutting effect of the silicon etch. This undercutting occurs because as the etch continues through the silicon, the exposed sidewalls at the top get slowly etched laterally, causing an undercut. Footing is also not a large concern because the width is always increasing down the profile, eliminating any possible shorts. However footing may cause a larger keyholes, which will be discussed in the next section, at the bottom of the filled trench. This should not greatly affect the function of the backfilled isolation trenches.

2.3.2.2 KEYHOLE REDUCTION TECHNIQUES

The weakness of the re-entrant profile is the formation of keyholes during the back-filling process. These keyholes form because conformal depositions eventually close off the narrow throat at the top of the trench, stopping the flow of deposition gases to the lower portions. For a straight isolation trench, as shown in Fig. 2-11, the tip of the keyhole would be at the same level as the top of the silicon substrate. Depositing more back-fill material would have no effect on the size of the keyhole. Once the back-fill material was removed from the surface, there would most likely be small openings to the keyhole, causing problems during later processing. For example chemical etchants could get inside the keyhole and be difficult to remove.

The majority of isolation trenches, though, are not straight. Corners are actually beneficial to the trench filling situation because the amount of conformal deposition

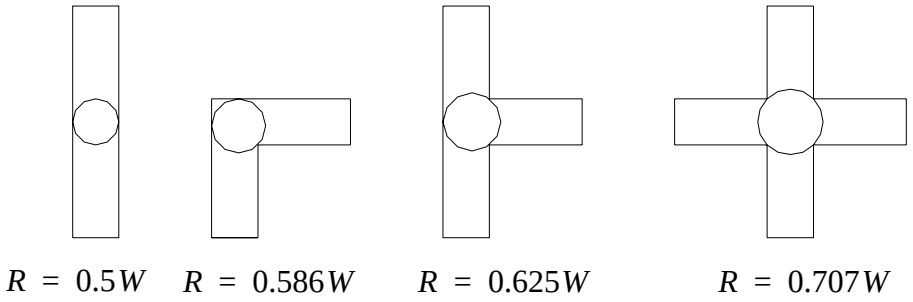


Figure 2-12. *Isolation trench intersections and the amount of back-fill required to close them where W is the width of the trench straight sections and R is the radius of the inscribed circle.*

required to close the corners is greater than that required to close a straight section. When the straight sections have just closed, the corners are still open, allowing gases to enter and continue to fill the insides of the trenches. This will bring the tip of the keyhole down below the surface of the silicon, reducing the chances of opening the keyholes during later processing.

The amount of time that it takes to eventually close a corner depends on what type of corner that it is. In Fig. 2-12, three types of corners are compared to a straight section. A simple way to compute the amount of back-filling required to close a specific corner is to place the largest possible circle inside the junction. The amount of deposition must be greater than the radius of the circle. Although the corners help reduce the size of the keyholes in the straight sections, the fact that they close at different rates produces variability across the wafer.

Another factor which was not considered above was the effect that mask undercut has on the keyholes. When one etches with the STS DRIE machine, the sidewalls of the trenches have a tendency to recess under the mask during the etch. This effect occurs whether a photoresist mask or an oxide mask is used for the etch. When a photoresist mask is used, the trenches do undercut the mask, but when the photoresist is removed after etching, the top of the trench is still smooth, as shown in Fig. 2-13a. Because there is a

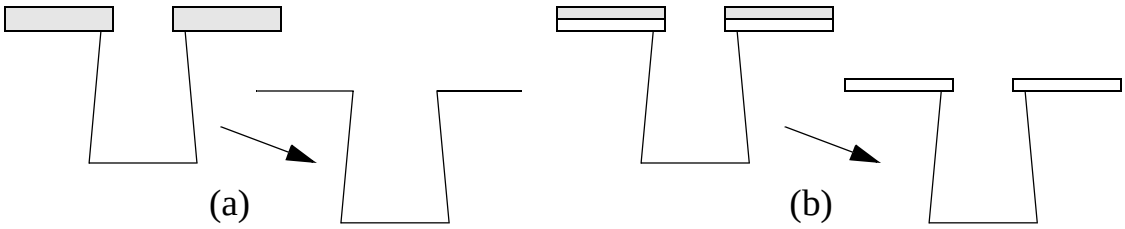
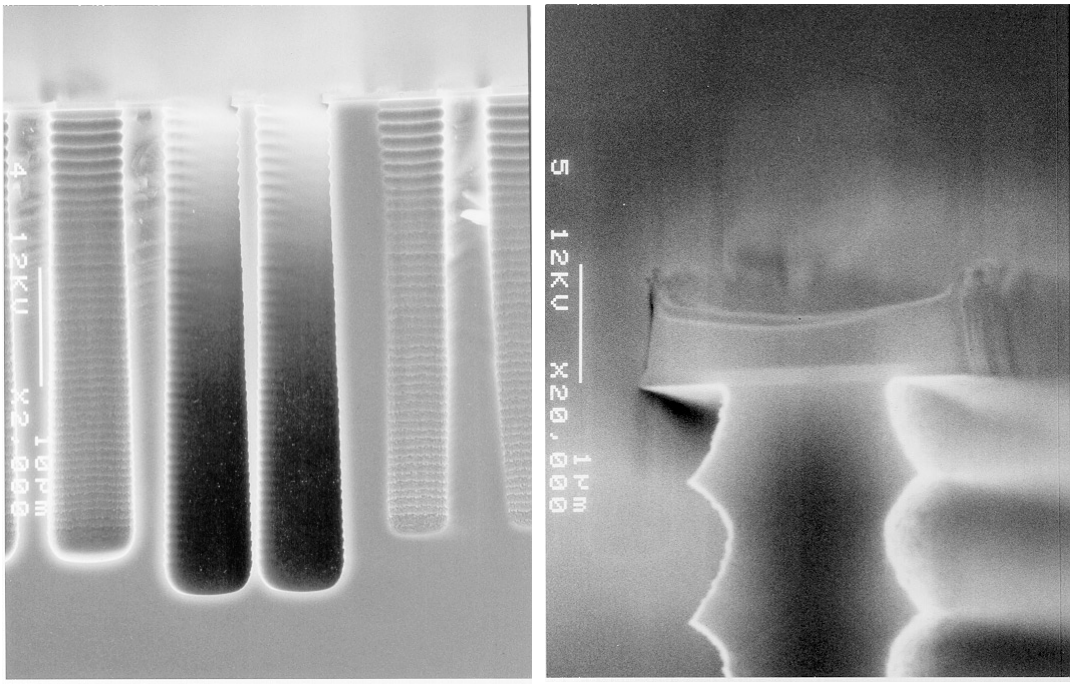


Figure 2-13. *Comparison of mask undercut with (a) a photoresist mask and (b) a photoresist and oxide mask.*



(a) (b)

Figure 2-14. *(a) SEM of STS etched re-entrant trenches. (b) A close-up showing the undercut beneath the oxide masking layer.*

protective oxide layer underneath the photoresist mask in this process, that does not get removed before the back-fill materials are deposited, the keyhole problem is made considerably worse. The critical dimension for deposition cutoff is now the oxide mask and not the width of the trenches. Fig. 2-14a shows a scanning electron micrograph (SEM) of an isolation trench with a re-entrant profile. In Fig. 2-14b, the protective oxide and the mask undercut can clearly be seen.

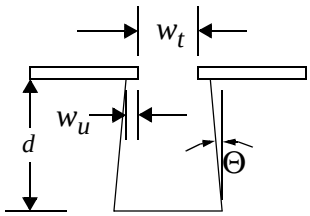


Figure 2-15. *Important dimensions for determining amount of deposition needed to fill an isolation trench without keyholes.*

A solution is needed that helps reduce the size of the keyholes and does so in a consistent manner. By placing larger holes along the trench, the size of the keyholes along the straight sections can be reduced. There will still be keyholes underneath these keyhole reduction features, but their location will be known and can be accounted for throughout the rest of the design.

The size of the features should be set based on the expected mask undercut and re-entrant angle of the isolation trenches. The features should close later than the keyholes in the straight sections. An example is shown in Fig. 2-15. The important dimensions are the width of the trench in the mask design, w_t, the amount of undercut of the mask, w_u, the angle of the sidewalls, θ, and the depth of the trench, d. The amount of deposition required to close the keyhole, D_k is then approximated as half of the width at the bottom of the trench, given by Eq. (2-3).

$$D_k = \frac{w_t}{2} + w_u + d\sin\Theta \tag{2-3}$$

As an example, assume that w_t is 2 μm, w_u is 0.5 μm, θ is 1° and d is 50 μm. There should then be 2.4 μm of deposition to close the keyholes along the straight sections. The keyhole reduction features should then have a width twice as large, or 4.8 μm.

A convenient place to put the keyhole reduction features is at the intersections of the trenches since these areas would automatically have a variation in the size of the keyholes.

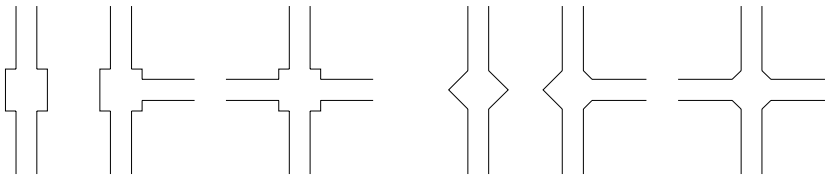
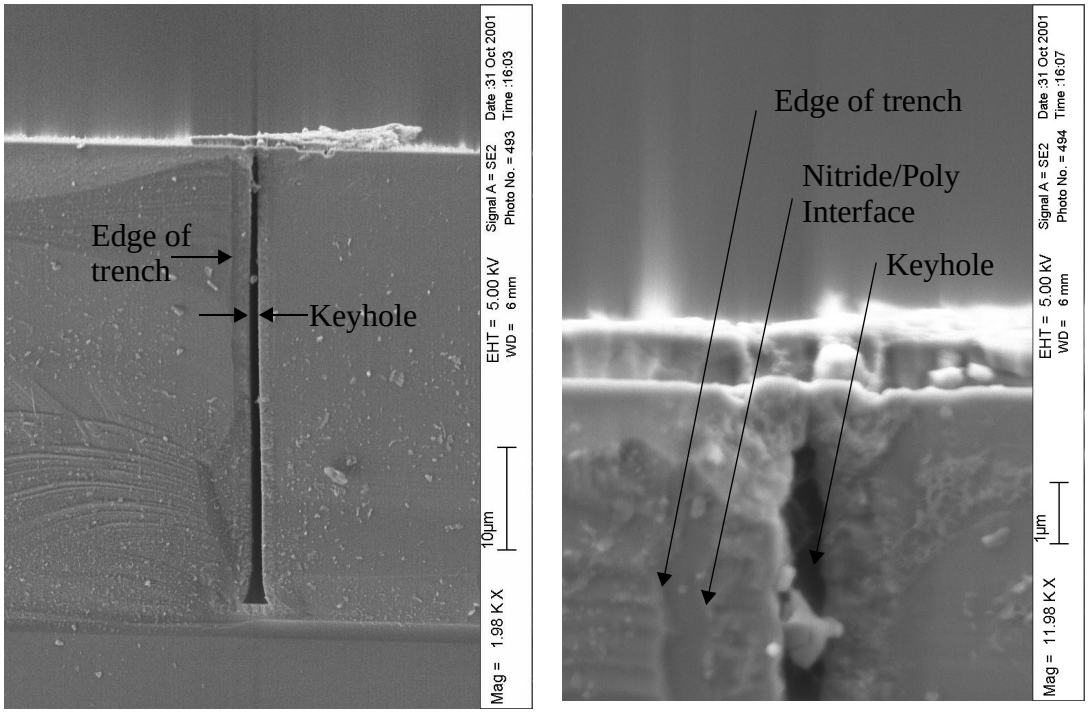


Figure 2-16. *Intersection configurations for rotated and non-rotated keyhole reduction features.*

For long straight sections that do not have intersections, keyhole reduction features can be placed anywhere along the length. For absolute consistency in the time it takes to close them off, they should also be rotated 45°. The reason for this is that when not rotated, the required deposition time varies slightly depending on the number of intersecting trenches. This happens because the minimum dimension that determine the pinch off comes from the middle of the side of the keyhole reduction feature, not the corner. If rotated, the middle of the side is always present, maintaining a consistent deposition time for any intersection configuration, as shown in Fig. 2-16.

2.3.2.3 KEYHOLE TOLERANT DESIGN

Even if the keyhole reduction features are used, the rest of the process and design should be made tolerant of the presence of keyholes. Fig. 2-17a shows a back-filled isolation trench with a large keyhole. Although the keyhole reaches almost all the way to the top, Fig. 2-17b shows that it is in fact closed. The major concern now is that if etchants can get into the trench, they will be able to travel to other parts of the device and could potentially cause problems. The most likely etchant to get into trenches is the concentrated HF used to release the MEMS structures (Section 2.5). Because the etch of the structures intersects the isolation trenches (Fig. 2-7), the ends will be opened, exposing the keyholes. The HF would most likely come out at the keyhole reduction features along those trenches. Any materials that would be etched by the HF should then be removed from above the keyhole reduction features.



(a) (b)

Figure 2-17. *Back-filled isolation trench. Although the keyhole seems to stretch almost the full height of the trench, (b) shows that it is closed at the top.*

2.3.2.4 BACK-FILL MATERIALS

The isolation trenches used in this process were back-filled with low stress nitride and undoped polysilicon. The trenches are first lined with 0.5 µm of nitride and then the remainder of the trench is filled with the silicon. These materials were chosen because they are deposited conformally and they are compatible with the other processing steps in the process. A potential alternative to the silicon nitride layer would be a conformal oxide which could be either deposited, using a conformal TEOS deposition system, or by growing it in a steam environment. The primary drawback of using oxide, though, would arise during the concentrated HF release of the MEMS structures. An oxide layer would be quickly attacked whereas the silicon nitride has a much slower etch rate.

The trenches are not completely filled with silicon nitride for two reasons. The primary reason is that the residual stress of silicon nitride is higher than that of undoped

polysilicon, which would lead to a higher chance of breaking wafers during processing. Secondly, low stress nitride deposits at a slower rate than polysilicon. Only a thin layer of silicon nitride is required to provide sufficient protection against breakdown across the isolation trenches.

An important concern involving the back-fill materials is the effect of the residual stress of the films. It is particularly important during the steps that remove the films from both the front and the back side. If one or both of the films is removed from one side and not the other, the wafers can be bowed enough to cause some problems with the handling of the wafers by the fabrication equipment. The largest problem arises if the STS DRIE tool is used to remove the polysilicon layer from either side. The STS uses an electrostatic chuck to hold the wafers down and helium is flowed onto the back side of the wafer to keep it cool. If the wafers are bowed, the helium flow can cause the wafer to become displaced inside the chamber. For this reason, it is preferable to use a silicon etcher which physically holds the wafer down. The preferred order of film removal to maintain machine compatibilities is to remove the backside poly first with a blanket etch, then a blanket etch of the front side poly followed by the hot phosphoric etch of the nitride.

2.3.2.5 ALTERNATIVE PROCESS METHODS

An alternative to using plasma etches to remove the polysilicon layer is to use a chemical-mechanical polisher (CMP). The benefit of using CMP is that the tops of the trenches will be especially smooth and flat. By comparison, when using a blanket plasma etch, the tops of the trenches are typically recessed between 2500 and 5000 A. The smoother the tops of the trenches are, the more reliable the metal electrical lines that cross them will be. The drawback is that the processing would be more complex. The CMP at the Berkeley Microfabrication Lab does a fairly good job of removing polysilicon and stops fairly well on silicon nitride, but if the polysilicon layer covers the entire wafer uniformly, it can take a very long time to remove all the polysilicon. The machine also has a tendency to remove material at the edges faster than material at the center. Attempts at

doing a blanket CMP of the poly layer resulted in the silicon nitride being completely removed from the edges of the wafer before the polysilicon was completely removed from the middle.

A solution exists to this problem which involves an extra lithography step and a plasma etch. The process is shown in Fig. 2-18. Lithography is first done to protect the polysilicon layer directly over the isolation trenches (Fig. 2-18a). Then the unprotected polysilicon is removed using a dry plasma etch (Fig. 2-18b). The photoresist is removed and the wafers are then polished (Fig. 2-18c). Because the total area of polysilicon to be polished is now greatly reduced and because the polishing attacks edges better than a smooth layer, the polishing goes much more quickly. Finally, the nitride and protective oxide layers are removed (Fig. 2-18d).

Two options are available for the photolithography step. The first one uses a dedicated mask for the protection which has the same design as the isolation trench mask but with the features scaled up to provide sufficient protection over the trench. The drawbacks of this is that an extra mask is required and if a wafer stepper is used for the lithography, as it was for this research, the polysilicon in the areas between the dies will not be removed, diminishing the benefits of the polysilicon removal. The other option uses the same isolation trench mask and either a negative photoresist or an image reversal technique with positive resist. This allows the polysilicon in the areas between the dies to be removed as well, but because the same mask is used, something must be done to make the features larger than the trenches themselves. This can be accomplished by doing a “bad” job during the exposure of the photoresist. By setting the focus to an incorrect setting and doing two separate exposures with much longer than needed exposure times, satisfactory results can be obtained.

In the end, the CMP option was not used because of the extra processing steps and because the CMP is more likely than most machines to break wafers. Also, because there are two layers of nitride and oxide underneath the polysilicon which have a total thickness

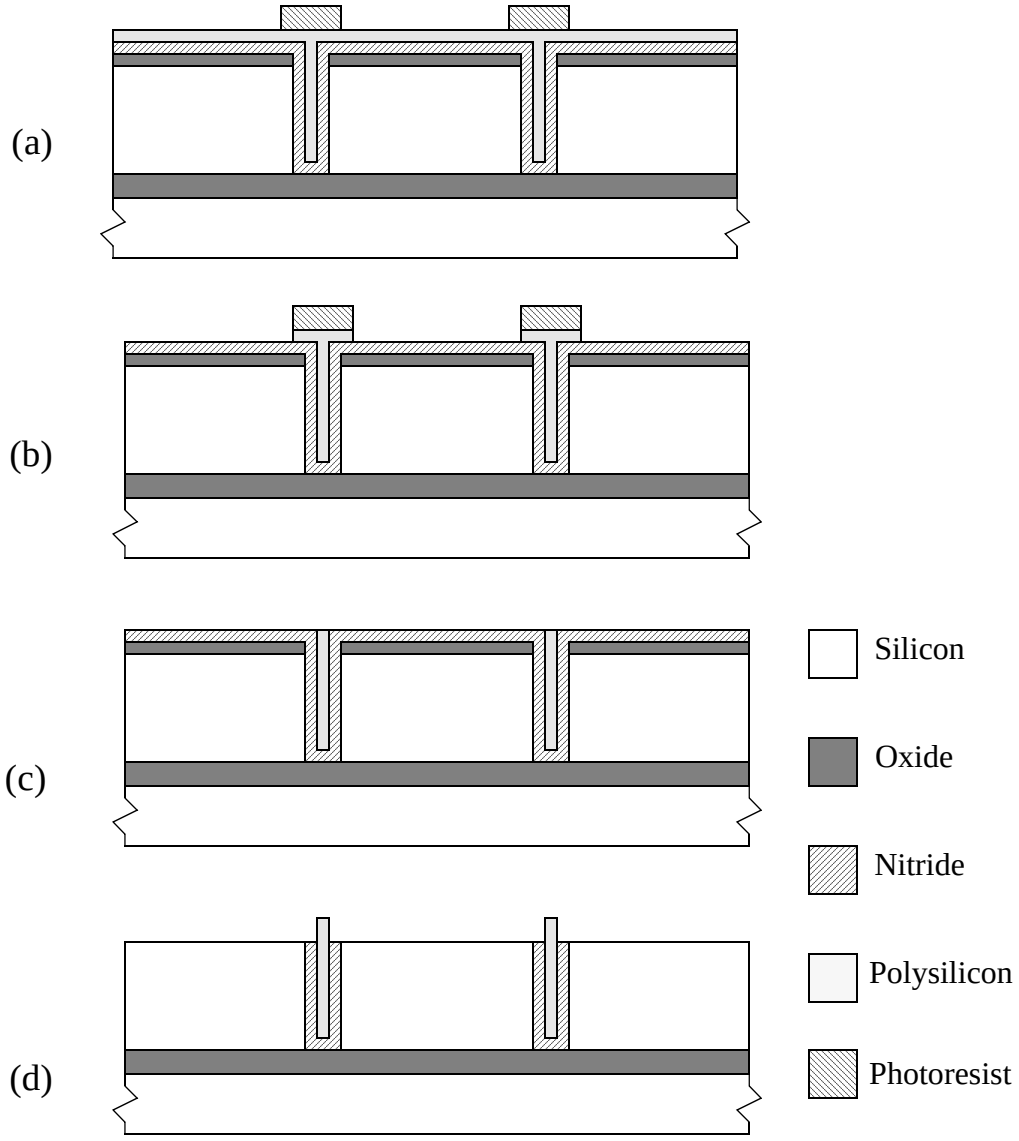


Figure 2-18. *Process for alternative back-fill material removal using a chemical-mechanical polisher. Although the polysilicon plugs are in fact proud of the surface after the nitride and oxide are removed, it is not as severe as what is shown in (d).*

of approximately 8000 A, the polysilicon plug actually ends up being proud of the surface after those layers are removed, causing new difficulties in creating reliable metal lines.

2.4 PROCESSING STAGE 3: SOLAR CELL AND CIRCUIT FABRICATION

2.4.1 PROCESS DESCRIPTION

There are three different versions of the process which vary in their circuit capabilities and in their processing complexities. The most basic version is capable of producing NMOS circuits with metal gates. It is the simplest version to fabricate, requiring a single drive-in step for all of the ion implanted dopants. This was the first version of the process to be developed, and the primary goal for it was to simply make high voltage solar cell arrays. The NMOS transistors were added when it was realized that all the processing elements were present to make them as well. The second version requires an additional drive-in step to allow the fabrication of both NMOS and PMOS circuits, yet still uses metal for the gates of the field effect transistors. It was implemented because it only required slight processing modifications that did not alter the design of the solar cells but greatly improved the circuit capabilities. The third version is the most complex from a processing standpoint, but also has the most sophisticated circuitry. It is capable of producing CMOS circuitry and uses self-aligned polysilicon gates. This produces more consistent performance from the transistors and allows the size to be dramatically reduced. It was the last version to be developed and is the one most similar to commercial CMOS processes.

In the process descriptions given in the following sections, the specific parameters for the ion implantations are not given. Because their development was so closely tied to the design of the solar cells and circuits, they will be discussed in detail in chapters 3 and 4.

2.4.1.1 VERSION 1: NMOS CIRCUITS WITH METAL GATES

The process steps for the simplest version of the circuits process is shown in Fig. 2-19. Three ion implantations are done, each masked with a 2 μm thick layer of photoresist. These implantations are for an n- region, an n+ region and a p+ region (Fig. 2-19a). The order in which the three implantations are done is not important. The wafers are then cleaned and a dry thermal oxidation step is performed, which simultaneously drives in all

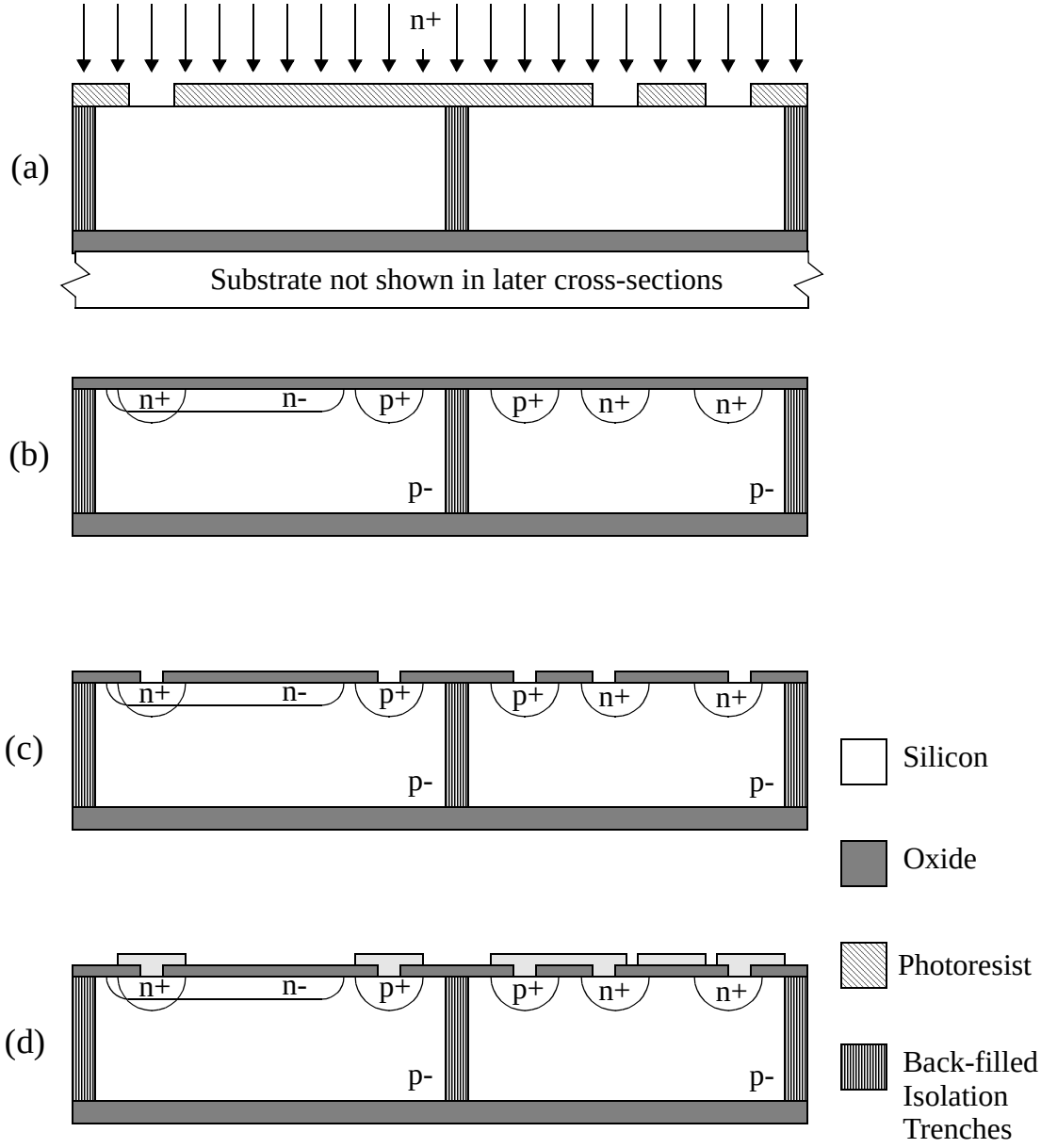


Figure 2-19. *Process for fabricating solar cells and circuits. Version 1: NMOS circuits with metal gates. A solar cell is shown on the left and an NMOS transistor is shown on the right. (a) Ion implantations masked with photoresist. (b) Ions driven in during a thermal oxide growth. (c) Contacts opened and (d) metal sputtered and patterned.*

of the dopants and grows a high quality thermal oxide layer (Fig. 2-19b). The mask for the contacts is applied and the contacts are wet etched using a buffered oxide etch (BOE)

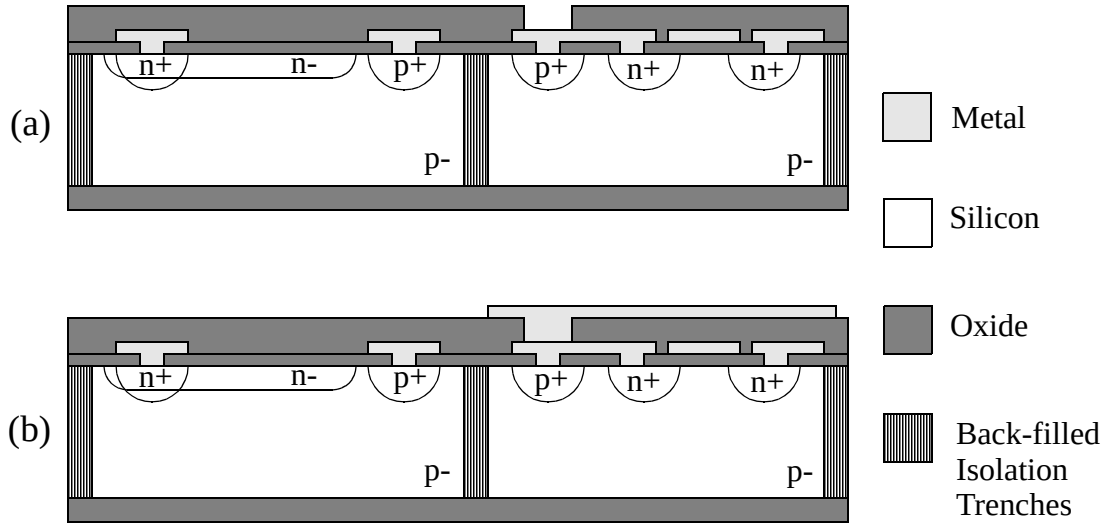


Figure 2-20. *Process steps for applying an intermetal dielectric layer and a second metal layer. (a) Intermetal dielectric deposited and contact holes opened. (b) Second metal layer applied and patterned.*

(Fig. 2-19c). The wafers are cleaned, including a brief HF dip to ensure that the contact holes are completely free of oxide, and aluminum with 2% silicon is sputtered onto the wafers. Lithography is done and the metal is etched with a dry plasma etching machine (Fig. 2-19d). The aluminum is then sintered to ensure a good contact to the silicon. One important thing which should be noted in Fig. 2-19 is that the n+ and p+ regions are deeper than the n- region. Because a single drive-in is used, the regions with the higher concentrations travel to a deeper level than those with lower concentrations.

At this point, the fabrication of the solar cells and circuits is complete. Additional processing can be done to apply an intermetal dielectric layer and a second layer of metal, if it is required. This second metal layer is primarily used as a light blocking layer over the circuits, but it could also be used for making metal connections between devices. The processing steps for this are shown in Fig. 2-20. A layer of low temperature oxide (LTO) is deposited on the wafers at 400°. The LTO is patterned and etched using a plasma etching machine (Fig. 2-20a). A layer of titanium is sputtered, followed by a thin layer of titanium nitride. These are then patterned and etched with a wet titanium etchant

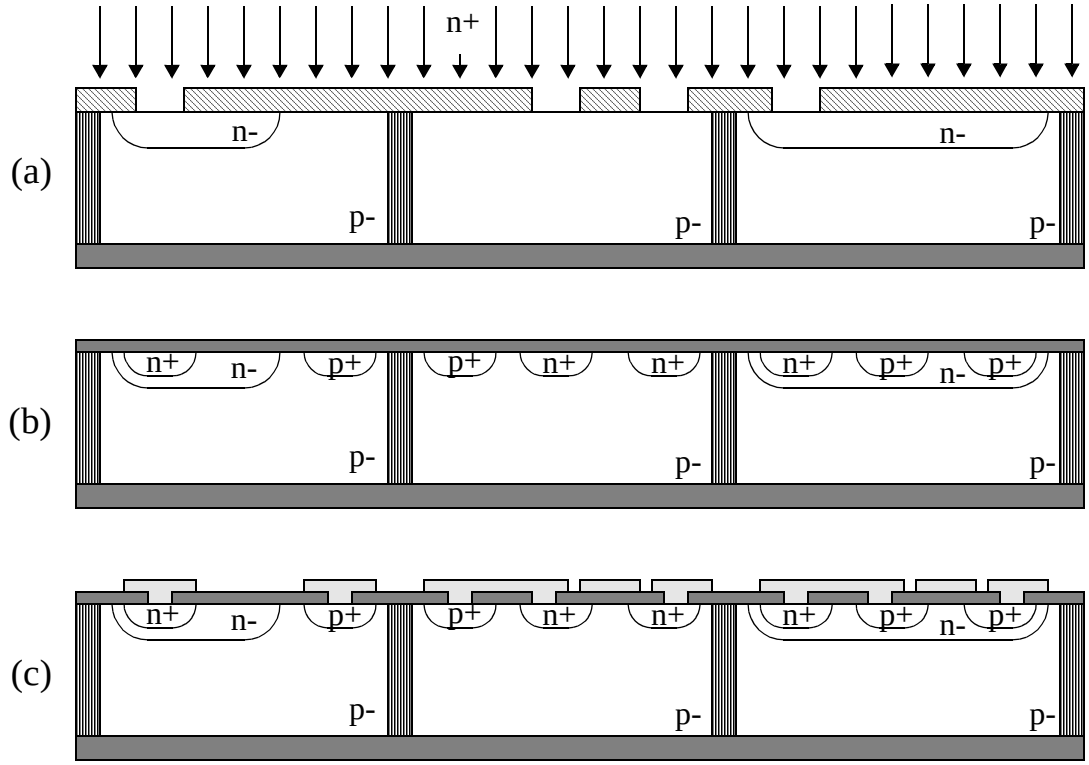


Figure 2-21. *Process for fabricating solar cells and circuits. Version 2: CMOS circuits with metal gates. A solar cell is shown on the left, an NMOS transistor in the middle and a PMOS transistor on the right. (a) After n- regions are implanted and driven in, ion implantations are performed for the n+ and p+ regions, masked with photoresist. (b) Wet thermal oxide growth drives in n+ and p+ regions to a shallower depth than the n- regions. (c) Contacts are etched and metal lines applied.*

(Fig. 2-20b). As indicated in Fig. 2-20, the light blocking layer is always grounded to eliminate any problems with charge build-up.

2.4.1.2 VERSION 2: CMOS CIRCUITS WITH METAL GATES

The second version is very similar to the first except that there are separate drive-ins for the n- region and the n+ and p+ regions. The process is shown in Fig. 2-21. The n- implant is performed, masked with a layer of photoresist. A drive-in is done at 1100°C which consists of a 30 minute dry thermal oxidation, which grows a thin oxide layer on the wafer, followed by a longer nitrogen anneal step. The oxide layer is stripped off in

hydrofluoric acid, and the implants are done for the n+ and p+ regions (Fig. 2-21a). A second drive-in is performed at a lower temperature in a steam environment (Fig. 2-21b). This limits the final depth of the n+ and p+ regions while still growing the same thickness oxide that was grown in the previous processing version. The remainder of the process is the same as the previous version with contacts etched and metal sputtered, etched and sintered (Fig. 2-21c). If a second metal layer is desired, the same process as before can be used, as shown in Fig. 2-20.

2.4.1.3 VERSION 3: CMOS CIRCUITS WITH POLYSILICON GATES

Whereas the first two versions of the circuit process vary only slightly, the third version is considerably different. In fact, it is much more similar to a commercial CMOS process than the others. The process steps are shown in Fig. 2-22. The n- region is implanted first, again masked with a photoresist mask. It is driven-in as in the last process, with a short dry oxidation step followed by a long anneal in a nitrogen environment. The thin oxide layer is stripped and new gate oxide is grown in a dry environment. Doped polysilicon is then deposited, followed by a lithography step and a dry plasma etch. The exposed oxide is also etched away (Fig. 2-22a), so that the following implantations for the n+ and p+ regions can be done at a low energy. After the n+ and p+ regions are implanted (Fig. 2-22b and Fig. 2-22c), they are driven-in. A layer of LTO is deposited and the mask for the contact etch is applied. The contacts are plasma etched and titanium and titanium nitride layers are sputtered. Finally, the metal is patterned and etched in wet titanium etchant (Fig. 2-22d).

2.4.2 DISCUSSION

2.4.2.1 MATERIAL USED FOR METALLIZATION

In the previous descriptions of the three versions for this stage of the process, the choice of material for the metallization varied between aluminum and titanium. The reason for this is to ensure that the materials used in stage three are compatible with the processing steps in stage four. In stage four, a protective layer of boron doped germanium

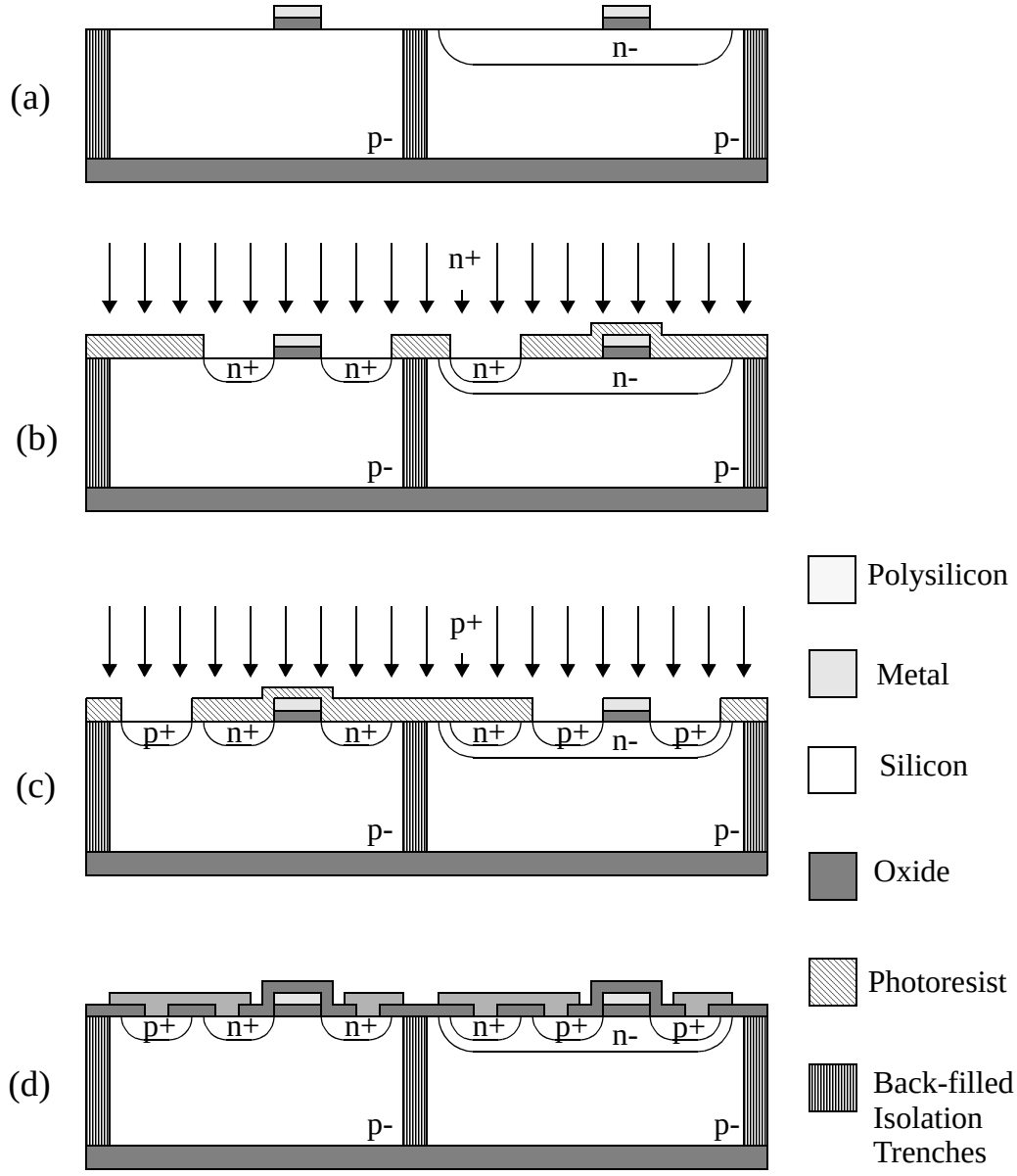


Figure 2-22. *Process for fabricating solar cells and circuits. Version 3: CMOS circuits with self-aligned polysilicon gates. (a) After implanting and driving in an n-well, gate oxide and polysilicon gates are deposited and etched. (b) n+ and (c) p+ regions are implanted. (d) Passivation and metal are applied and patterned.*

is deposited over the entire wafer to provide protection to the solar cells and circuits during the hydrofluoric acid release of the MEMS structures. It was found that there were

problems getting a good quality germanium film to deposit onto aluminum because it would diffuse into the metal layer and leave voids. This problem was solved by switching from aluminum to titanium, which was much more compatible with the germanium. It was not necessary to change the metal if was completely buried at the germanium deposition step. Therefore, for process version one and two, the first metal layer was aluminum and the second metal layer was titanium. For version three, the one metal layer was titanium.

2.5 PROCESSING STAGE 4: ETCHING AND RELEASE OF MEMS STRUCTURES

2.5.1 PROCESS DESCRIPTION

The processing steps for the etching and release of the MEMS structures is shown in Fig. 2-23. First, the any oxide over the MEMS structures area is removed with either a wet or dry etch (Fig. 2-23a). The wafer is then coated with a layer of boron doped germanium (Fig. 2-23b). This layer will provide protection to the solar cells and circuits during the release of the structures. The pattern for the structures is applied and the structures are etched through the device layer with an STS DRIE machine (Fig. 2-23c). The germanium layer is also etched at the start of the structures etch, but because it is thin and completely compatible with and easily etched by the STS etcher, it has little to no effect on the etch. The photoresist is then removed and the structures are released in 49% concentrated HF (Fig. 2-23d). When the release is complete, the wafer is rinsed to water, being careful to keep it wet so that the surface tension of the water does not cause the structures to stick to the handle wafer. The wafer is then put in hydrogen peroxide at 90°, which removes the germanium layer. The wafer is rinsed to water and then methanol for the CO_2 critical point drying [31] which completes the release (Fig. 2-23e).

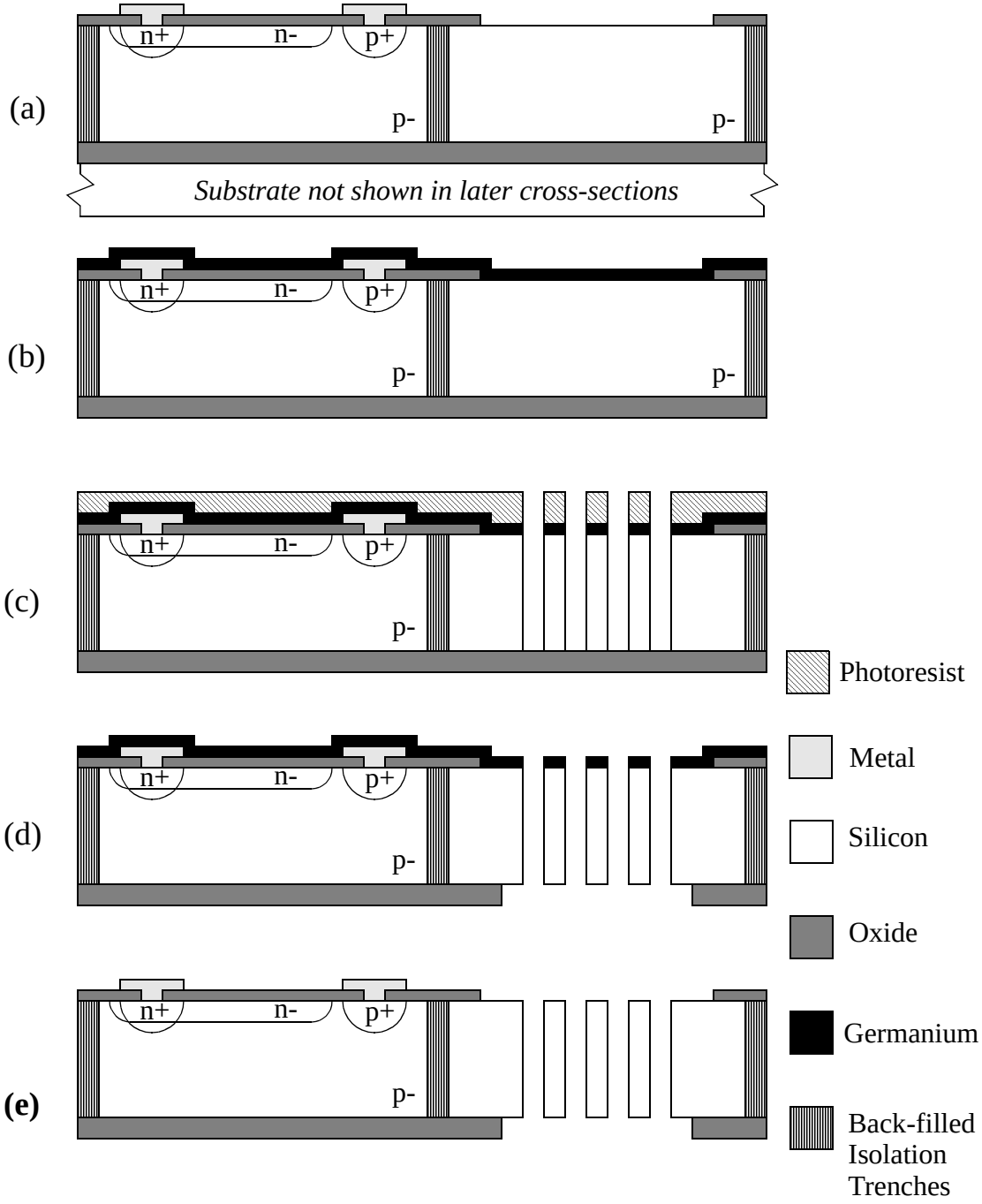


Figure 2-23. *Process steps for etching and releasing the MEMS structures. (a) Oxide is removed from structures area. (b) Germanium is deposited. (c) Pattern for structures is applied and germanium and silicon are DRIE etched. (d) Oxide is etched and (e) germanium is removed.*

2.5.2 DISCUSSION

2.5.2.1 OXIDE REMOVAL BEFORE STRUCTURE ETCH

The first step in the process for this stage involves removing any oxide that is covering the areas where the structures will be etched. It is possible to perform this etch during the previous oxide etch, which would eliminate a lithography step from the process. The previous etch would be either the contact etch for the circuits if a second metal layer is not used, or the via etch through the intermetal dielectric if the second metal layer is used. The only issue which must be considered is the how the removal of the subsequent metal layer might affect the exposed silicon. If a wet etch of the aluminum is used, then it is perfectly acceptable to do a combined oxide removal, because the wet aluminum etch stops well on silicon and does not adversely affect it. If, however, the metal is etched with a dry plasma etch, then the oxide should not be removed beforehand. Plasma etching of aluminum does not stop well on silicon and has a tendency to create a black layer on the surface, which is difficult if not impossible to remove.

2.5.2.2 TWO LEVEL STS ETCHES

The oxide which covers the structures area can also be used to expand the capabilities of the MEMS structures. By using two masking layers, an oxide mask and photoresist mask, for the structures etch, it is possible to create structures where some features are the full height of the device layer and others are some fraction of the full height [32]. The process steps for etching are shown in Fig. 2-24. The oxide layer is patterned first, followed by a photoresist layer over it. For areas where the devices will be the full height, either both masking layers are present or just the photoresist mask. For areas where the shorter height is desired, only the oxide mask should be present and areas that are completely removed should have neither mask (Fig. 2-24a). For this example, assume that the desired middle height is one half of the full device layer height. The DRIE is then performed for one half of the time necessary to etch completely through the device layer

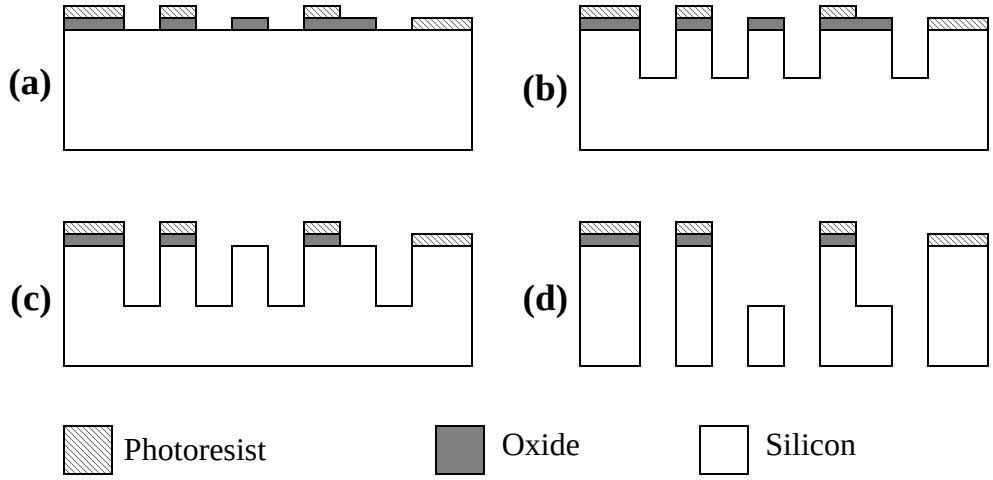


Figure 2-24. *Processing steps for creating variable height MEMS structures using two masks.*

(Fig. 2-24b). The exposed oxide mask is then removed (Fig. 2-24c) and the remainder of the silicon etch is completed (Fig. 2-24d). This technique has been employed to make some interesting and novel MEMS structures [32]. Although this technique was not demonstrated with this process, the necessary requirements are present and it is completely compatible.

2.5.2.3 Solar Cell and Circuit Protection During MEMS Structure Release

The problem of sufficiently protecting circuitry during the release of MEMS structures has long been a problem for those wishing to integrate the two into one complete device fabricated on an SOI wafer. The problem arises from the fact that the hydrofluoric acid needed to remove the bonding oxide layer to release the MEMS structures attacks the oxide and metal layers of the circuits very quickly. The two possible ways of solving this problem are to eliminate the need for a wet release of the structures or to sufficiently protect the circuit areas during the release.

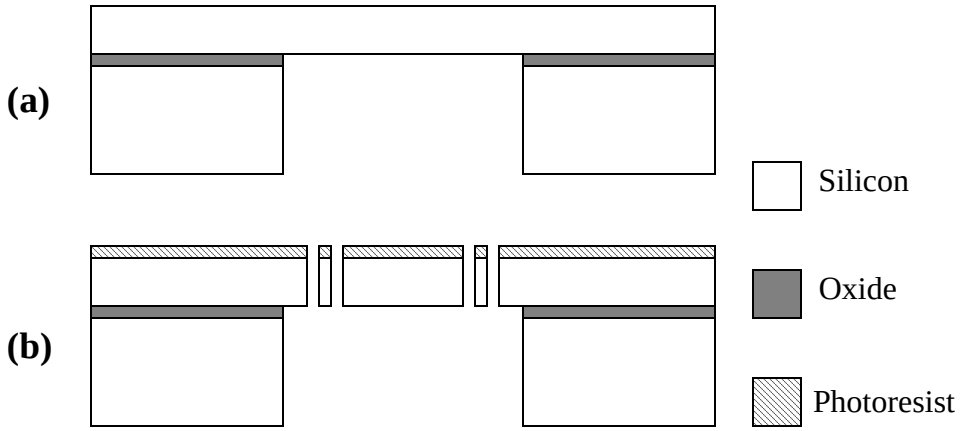


Figure 2-25. *Backside release process. The bonding oxide layer is removed from a hole through the handle wafer before the structures are etched.*

Wet Release Elimination Techniques

Backside Release

The first way to eliminate the need for a wet release of the structures is to do a back-side release. Holes can be etched through the handle wafer, exposing the bonding oxide layer underneath the MEMS structures. This etch can be done with either a DRIE or a wet etch in TMAH or KOH. The oxide can then be etched away with either a plasma etch or a wet etch before the structures are etched. When the structures are then etched, they will automatically be released. This is shown in Fig. 2-25

Unfortunately, there are a number of issues that make this technique undesirable. First, if the etch through the handle wafer is done with a wet etch, the front side of the wafer must still be protected. Wet etching was not considered because of the high risk of the etchant reaching the device side of the wafer. If the etching is done with a DRIE, the size of the holes and the depth of the etch will require a long etching time, typically greater than two hours, although it is still possible. When it comes to etching the bonding oxide layer, there are still protection issues if a wet etch is used and if a plasma etch is used, it

can be difficult to etch oxide at the bottom of deep holes.

Another issue is that the mask for the structures etch cannot be applied before the holes have been etched through the handle wafer. During the backside etch on the STS, the wafer must be photoresist bonded to a handle wafer, but because the only masking material available for the structures etch is photoresist, it cannot be done beforehand. After the etch, the wafers would be to fragile to reliably do lithography without breaking them.

Lastly, etching silicon in the STS generates a considerable amount of heat. If the handle wafer is missing beneath the device layer, the heat build-up can burn the photoresist mask, causing it to break down prematurely or making it very difficult to remove afterwards. For these reasons, the backside release technique was not used.

Patterned Bonding Oxide Layer

Another approach is to remove the oxide below the structures before the handle and device wafers are bonded together. Although this would be a possible solution for standard SOI MEMS devices, it is not compatible with this process. In order to create electrically isolated mechanical structures, the isolation trenches must intersect with the released structure areas. After the isolation trenches were etched, the back-fill materials would fill the evacuated bonding oxide layer underneath the structures, defeating the purpose.

Circuit Protection Techniques

Because a hydrofluoric acid release is necessary, a means of sufficiently protecting the solar cells and circuits must be found. There are three potential forms of the HF release which must be considered for each of the protective layers. First is 49% concentrated HF. This etches oxides, both thermal oxide and LTO quite quickly. The second option is to use a buffered oxide etch (BOE), which is made up mostly of ammonium fluoride with a small amount of hydrofluoric acid. The purpose of BOE is to maintain a consistent pH of the

acid during the etching. BOE may also contain surfactants which help the acid reach better into small areas. The third option is to use HF vapor etching.

Photoresist

The first protection layer to be considered was the photoresist mask used for etching the structures. The first consideration if photoresist is being used for protection is that concentrated HF cannot be used for the release. The concentrated HF will quickly peel away the photoresist, exposing the area underneath. Therefore, BOE, which is formulated to not peel photoresist, must be used instead. The drawback is that BOE etches oxide much more slowly than concentrated HF, with the 5 μm release needed to release the fabricated structures taking about an hour instead of just a few of minutes, as shown in Table 2-1.

Table 2-1. *Etch rates and times for wet oxide etches [33].*

Etchant	Thermal Oxide Etch Rate (A/min)	Time to Etch 5μm (min)
49% Concentrated HF	23,000	2.2
5:1 Buffered Oxide Etch	1,000	50

To determine if the photoresist would be able to remain intact for such a long release, a test wafer, which had oxide on the surface to simulate the devices on the actual wafers, was patterned with the structure mask and etched in the STS. It was etched for the same amount of time that is required to etch through the device layer of the actual wafers and then divided into quarters. A “release” was then done in both concentrated HF and BOE. The part of the wafer in the concentrated HF showed immediate signs of peeling, but the part in the BOE was able to withstand a full three hours of simulated release. This was three time as long as what was required for the actual release.

When an actual wafer was released, however, the photoresist only withstood a couple minutes in the BOE before failing. The photoresist most likely failed because the effects of the STS etch were more severe on the actual wafer. First, the actual wafers had more topography than the test wafers, providing potentially more places where small gaps in the

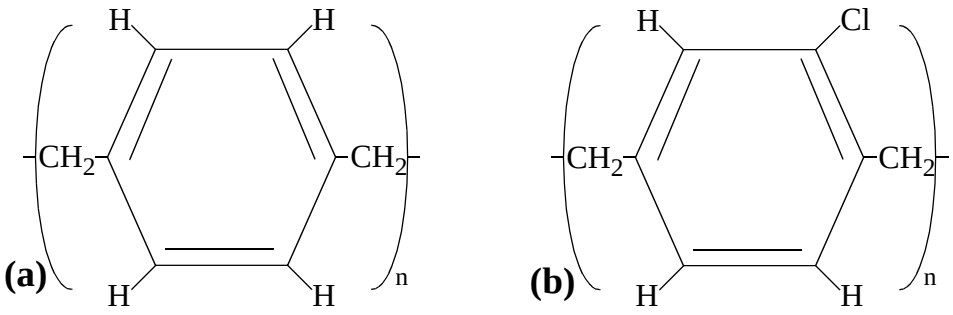


Figure 2-26. *The chemical structures for (a) Parylene N and (b) Parylene C.*

photoresist could allow the etchant to "break through" and get underneath. Second, because the thermal conductivity of SOI wafers is worse than regular wafers, they run hotter during etching in the STS. This would lead to greater breakdown of the photoresist. Although a thicker layer of photoresist may have provided better protection, but it would not have been possible to obtain the resolution needed for the smallest features.

Parylene

The second protective layer to be considered was parylene. Parylene is the generic name for the polymer poly-para-xylylene [34]. It is a conformal, vapor deposited polymer. The deposition process starts with a solid dimer which is vaporized at 150° C and then cleaved at 650° C. The resulting monomer is brought into the deposition chamber which is at room temperature where it polymerizes onto the surface. The basic form of parylene is called Parylene N, which is shown in Fig. 2-26a. A modified version of the polymer, called Parylene C, has one of the aromatic hydrogens replaced with a chlorine atom, as shown in Fig. 2-26b. There were a number of characteristics of parylene which made it seem well suited for this process. First, parylene is optically transparent in the visual light range. This would allow it to cover the solar cells without diminishing their performance. Second, it is a good electrical insulator with a high dielectric strength. The dielectric strength for Parylene N is 275 V/μm and it is 220 V/μm for Parylene C [34]. It could then be used as a replacement for oxide as the intermetal dielectric. Third, it

is easily etched in an oxygen plasma and can be patterned with a thick layer of photoresist.

The first test done to determine if parylene would provide suitable protection during an HF release involved growing a thermal oxide on a silicon wafer, coating it with parylene and then placing it in the oxide etchant. This was done with both concentrated HF and BOE and with Parylene N and Parylene C. In all situations, the etching ions were able to penetrate through the polymer and attack the oxide underneath, although on wafers coated with Parylene C, this occurred much more slowly than with Parylene N. This result is consistent with the gas permeabilities of the two types of parylene, which, for hydrogen at 25° C, is 540 (cm^3(STP)mil)/(in^2/d*atm) for Parylene N and 110 for Parylene C. This result indicated that parylene by itself would not work well as a protective layer but when paired with the photoresist it might be sufficient. A test wafer was then prepared with oxide and a patterned layer of Parylene C. The structures mask was applied and the wafers were again etched for the amount of time necessary to etch through the device layer of the actual wafers. A mock release was done again and the results looked very promising. The photoresist and the parylene combined to completely protect the areas away from the MEMS structures. When an actual wafer was prepared in the same way and released, the protective layers broke down, once again allowing the HF to reach the circuits. The problem again was believed to be a greater breakdown of the photoresist during the STS etching.

Germanium

The final protective layer that was tried was boron doped germanium. Polycrystalline germanium is deposited in a low pressure, chemical vapor deposition (LPCVD) furnace in a similar manner to LPCVD polysilicon. Silicon and germanium can actually be deposited together with any possible ratio between them, ranging from 100% polysilicon to 100% polycrystalline germanium. The ability to vary the ratio during a single deposition has opened the door to many exciting uses for this technology [35][36]. Germanium has a number of characteristics which make it perfectly suited to this process.

First, it is deposited at a low temperature, making it compatible with the existing metal layers. Second, it is completely resistant to HF and provide an excellent barrier to it. Third, it is easily removed in hydrogen peroxide at 90°C. Finally, it is completely compatible with silicon etching, allowing it to be deposited over the structures area and etched through at the same time as the structures. Boron doped germanium was chosen because the presence of boron lowers the temperature of deposition to only 350°C. This reduces the possibility of reducing the performance of the circuits from excessive temperature steps.

The use of germanium as a protective layer did force one change to the original process. It was found that if there was any exposed aluminum during the germanium deposition, the germanium would diffuse into the metal layer, leaving voids in the germanium film. These cavities allowed the hydrofluoric acid to quickly attack the metal layer during the structures release etch. This problem was solved by switching any exposed metal from aluminum to titanium, which did not have a problem with the germanium deposition. To keep the titanium from oxidizing excessively, a thin layer of titanium nitride was placed directly over the titanium. These two layers were patterned and etched together.

Tungsten

Tungsten, which has been used by Sandia National Labs to protect devices during an HF release [37], was also investigated as a possible alternative. It is similar to germanium in that it is not affected by HF and can easily be removed with hydrogen peroxide. It was not used here, however, because germanium provided an important benefit over tungsten. Because germanium is allowed in the DRIE silicon etcher, it was possible to put a blanket layer of germanium onto the wafer and pattern the structure etch over it. The DRIE etch then went through both the germanium layer and the silicon device layer. Tungsten is not allowed to be etched in the same machine so using it would have required and extra lithography and etch step to remove it from the device areas before the structures were

patterned. This drawback tipped the scales in the favor of using germanium instead.

3. SYSTEM COMPONENT 1: SOLAR CELLS AND SOLAR CELL ARRAYS

3.1 INTRODUCTION

In this chapter, the first component of the integrated solar powered MEMS, the solar cells, will be discussed. A solar cell is simply a device that converts energy in the form of light into electrical energy. In this process, the solar cells can be put to work as the power source for the autonomous microsystems. Beyond simply providing power, the ability to wire a number of cells together in series makes possible a wide variety of output voltages. This eliminates the need for inefficient power converters, such as charge pumps, to increase the voltage to a level where it is useful for electrostatic actuators.

In the next section, a brief overview will be given of how solar cells work, including definitions for the important parameters needed to discuss solar cell performance. This will be followed in Section 3.3 with a description of the design of the solar cells including the dopant concentration profiles, the metal collector lines and some techniques for improving the efficiency of solar cells. In Section 3.4 experimental results will be given for solar cells and solar cell arrays fabricated using this process.

3.2 BASICS OF SOLAR CELL OPERATION

When a photon of sufficient energy strikes a semiconducting material, like silicon, it can move an electron from a lower to a higher energy band. This creates an electron-hole-pair (EHP). This EHP will typically survive for a short amount of time until the electron gives up the energy it received and returns to its original orbital position. This effectively annihilates the EHP and is known as recombination.

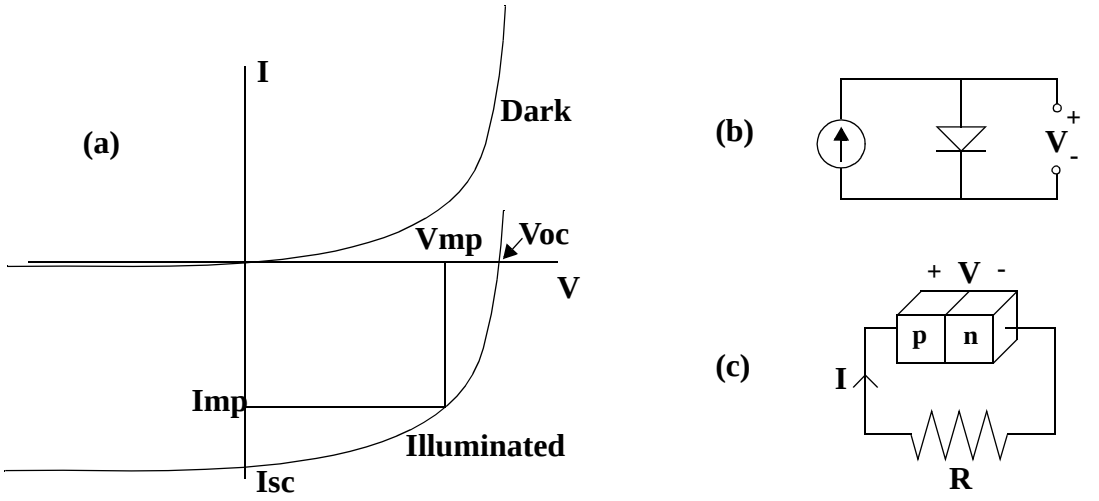


Figure 3-1. *a) Typical i-v curves for a solar cell under both dark and illuminated conditions. Important characteristic points are also shown. b) Basic model of a solar cell with an ideal current source in parallel with a diode. c) Schematic of an illuminated solar cell providing power to an external load, R.*

If this process occurs within a p-n junction, EHPs which are generated close enough to the depletion region of the junction, the transition zone between the n and p regions, will be separated from each other. If the device is wired into a complete circuit, the carriers will flow through the circuit so that they can return to the other side of the junction. This flow of current can then be used to do work in the circuit. In building a basic model of a solar cell, this light-induced generation of EHPs can be considered as an ideal current source placed in parallel with the p-n junction diode, as shown in Figure 3-1b. When there is no incident light, the expected i-v curve is simply that of the diode, as shown in Figure 3-1a. When light is applied, the effect is to lower the i-v curve an amount equal to the current generation.

In order to power an external load with a solar cell, the cell is operated in the fourth quadrant of the i-v curve. A few important characteristics of a solar cells performance are the short circuit current, I_{sc}, the open circuit voltage, V_{oc}, and the fill factor, FF. The I_{sc} is the value of the current at $V = 0$. Ideally, this should be equal to the amount of light

induced current. The V_{oc} is the point at which the i-v curve crosses the x-axis, where the current is zero. Every point along the curve defines a potential operating point, with an associated power. The voltage and current where the maximum power is attained are called V_{mp} and I_{mp}, respectively. The fill factor is then defined as

$$FF = \frac{V_{mp}I_{mp}}{V_{oc}I_{oc}} \tag{3-1}$$

and is a measure of how "square" the solar cell's output is. Good cells typically have a fill factor greater than 70%. The efficiency of a solar cell is simply the ratio between the maximum power output and the input power, P_{in}, shown in Eq. 3-2.

$$\eta = \frac{V_{mp}I_{mp}}{P_{in}} = \frac{V_{oc}I_{oc}FF}{P_{in}} \tag{3-2}$$

In order to better understand the results of the fabricated solar cells, the basic solar cell model shown in Figure 3-1 needs to be modified to make it slightly more representative of actual solar cells. Two additional elements, both parasitic resistances, need to be added, one in parallel with the diode and current source and one in series, as shown in Figure 3-2. The parallel resistance is called the shunt resistance, R_{sh}, and typically arises from crystal defects and impurities within the junction and leakage across the p-n junction on the periphery of the cell. The series resistance, R_s, arises from the resistance within the p and n regions, across the contacts from the silicon to the metal and within the metal lines. Both of these parasitic resistances can negatively affect the performance of the cell as shown in Figure 3-2.

3.3 DESIGN OF THE SOLAR CELLS

In this section, the design of the solar cells which were fabricated for this research will be discussed. These cells were fabricated on an SOI wafer with front side contacts for both p and n regions. The phosphorus and boron dopants were introduced through ion

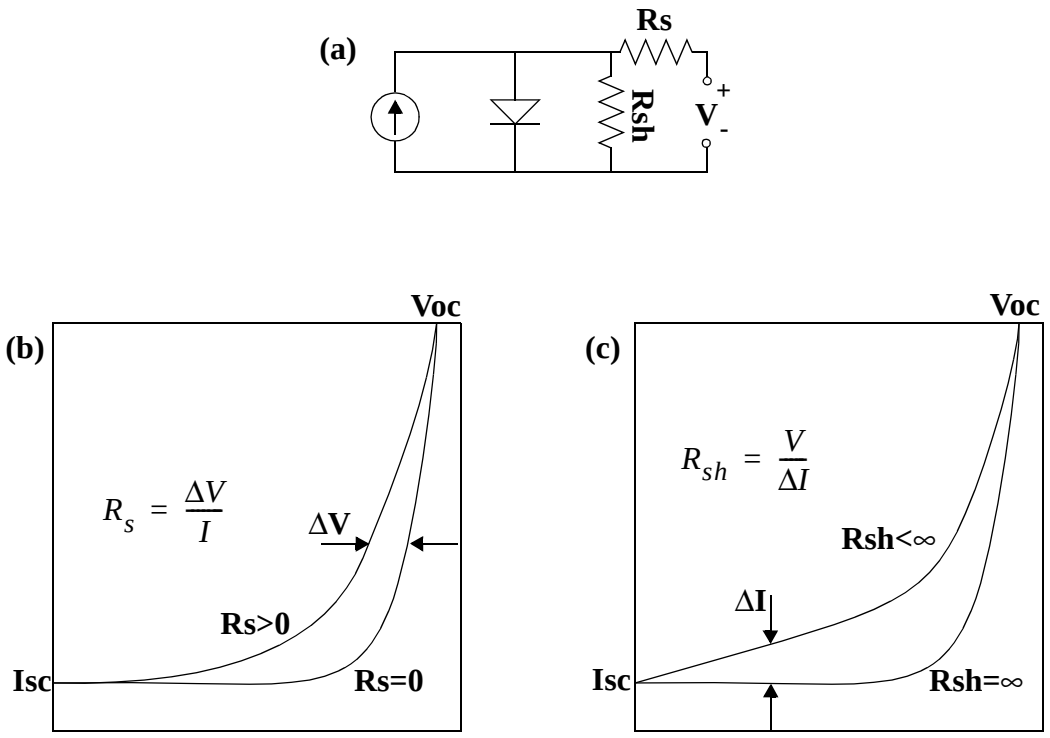


Figure 3-2. *a) Model of solar cell with parasitic resistances added. b) Effect that high series resistance has on fourth quadrant of solar cell i-v curve. c) Effect that low shunt resistance has on fourth quadrant of solar cell i-v curve.*

implantation. The solar cells were isolated through the use of back-filled isolation trenches which were deep reactive ion etched through the device layer of the SOI wafer and filled with low stress nitride and undoped polysilicon. The top surface of the solar cells was passivated with a thermal oxide, the thickness of which was chosen to act as an anti-reflective coating. The cells also had a highly doped back surface field to improve the efficiency.

The initial design for the solar cells, which constituted version 1 of the solar cell and circuit process (Section 2.4.1.1), was based on the previous research of Hebling et al [26] on thin film solar cells fabricated on SOI wafers. A description of this research can be found in Section 1.3.

Although the solar cells fabricated by Hebling had some similarities to the solar cells needed for this research, a number of modifications were necessary. The first change concerned the type of SOI wafer which was used. Hebling had used a SIMOX SOI wafer with the thickness of the device layer increased by growing silicon epitaxially. Although SIMOX wafers are an excellent choice for the fabrication of circuits with a very controllable oxide and silicon thickness, they are not well suited to MEMS applications. This is primarily due to the limitation on the thickness of the bonding oxide layer. It is simply not possible to create an oxide layer that is one to two microns thick, which is necessary for moving MEMS structures to function properly. If the oxide layer is too thin, the structures have a tendency to stick down to the handle wafer. The solution was to use an SOI wafer which was fabricated by bonding two wafers together and grinding and polishing the device layer back down to the desired thickness, as described in Section 2.2.

Another necessary change was the addition of a means to isolate individual solar cells so that they could be wired in series to provide the desired high voltage output. This was accomplished by etching isolation trenches through the device layer and back-filling them with silicon nitride and undoped polysilicon, as discussed in Section 2.3.

Another difference between the process used by Hebling and this process was that the metallization was changed from evaporated Ti/Pd/Ag with subsequent gold electroplating to a sputtered aluminum with 2% silicon. This eliminated the use of gold, which can easily contaminate other devices and would not be compatible with processing steps that would be necessary to create the MEMS structures. In addition, the aluminum can be easily patterned via a plasma etch, which allows better control over the dimensions of the metal layer. This is more of an issue for the versions of the process which use the metal layer for the transistor gates.

Other major differences between the thin film solar cells fabricated by Hebling, including the means of introducing the dopants and the use of surface texturization for improved efficiency, will be discussed in the following sections.

3.3.1 DOPANT CONCENTRATION PROFILES

3.3.1.1 VERSION 1: NMOS CIRCUITS WITH METAL GATES

As previously mentioned in Section 2.4, the simplest process for making solar cells and circuits is capable of creating NMOS circuits with metal gates. This was the first solar cell process developed and the dopant concentration profiles for this process will be discussed in this section.

A major difference between the solar cells fabricated by Hebling and those fabricated using the process presented here concerned the method of introducing the dopants into the silicon. Instead of diffusion, ion implantation was used. Ion implantation not only allowed for a more easily controlled doping process, but it simplified the process by reducing the number of furnace steps considerably. The doping parameters, though, had to be determined so that the resulting dopant concentration profiles were similar to those from the diffusion process used by Hebling. TSUPREM-4 was used to do the processing modeling with the results verified by calculating the diffusion profiles by hand. The output files of the models can all be found in the Appendix. The original diffusion process consisted of a p+ diffusion from a BBr_3 source with a drive-in at 1075ºC, an n+ diffusion from a $POCL_3$ source with a 1050ºC drive-in and an n- diffusion. A final oxide growth step in a TCA environment created the high quality oxide layer that acted as a passivating layer and an antireflective coating. The desired ion implantation process consisted of three implantations in a row for the p+, n+ and n- with a single drive-in step. This drive-in would be accomplished during a dry thermal oxide growth that would also create the passivating and antireflective oxide layer.

The doping parameters were chosen by working backwards through the process steps. The necessary parameters to create a 1500Å thick oxide layer in a dry thermal oxide environment were chosen first. At a chosen temperature of 1050ºC, the modeling software indicated that 172 minutes of oxide growth would be required. This result is easily verified by using the standard oxide growth charts in processing books [39]. The

doping parameters were determined next. The necessary parameters include the dopant type, implantation energy, implantation angle and dose. The dopant types chosen were boron for the p-type implant and phosphorus for the n-type implants. The ion implantation energy was chosen to be 25 keV for all three implants. Typically, the energy is chosen so that the depth of the implant is carefully controlled. For this process, however, the relatively long drive-in at fairly high temperature would be the dominant factor in determining the eventual depth of the dopants. A low value of 25 keV was chosen simply to get the dopants into the substrate. The implantation angle can have an effect on the eventual depth of the dopants due to a phenomenon called channeling. With certain crystal orientations, especially the <110> direction, there are relatively clear pathways through the crystal so that some dopants can easily travel deep into the material before coming to a stop. For this process, however, because the wafers had a <100> orientation and the depth achieved during the drive-in was so much greater than the implant depth, this was not a concern. All implants were done perpendicular to the surface of the wafers.

The final parameter, implantation dose, was the most important factor in controlling the final concentration profiles. The goal for determining the implantation dose for the n-region was to obtain a resulting sheet resistivity similar to that of the n- region of Hebling's device. That was estimated to be approximately 325 Ω/square. The implantation dose was varied in the SUPREM model until the desired resistivity was found. This occurred when a dose of 8.4×10^{13} ions/cm^2 was used. The predicted concentration curve is shown in Figure 3-3a. The output files for all SUPREM models can also be found in the Appendix.

To verify the validity of this result, the diffusion was also modeled analytically. The diffusion profile is governed by Fick's second law of diffusion, given in Eq. (3-3), where

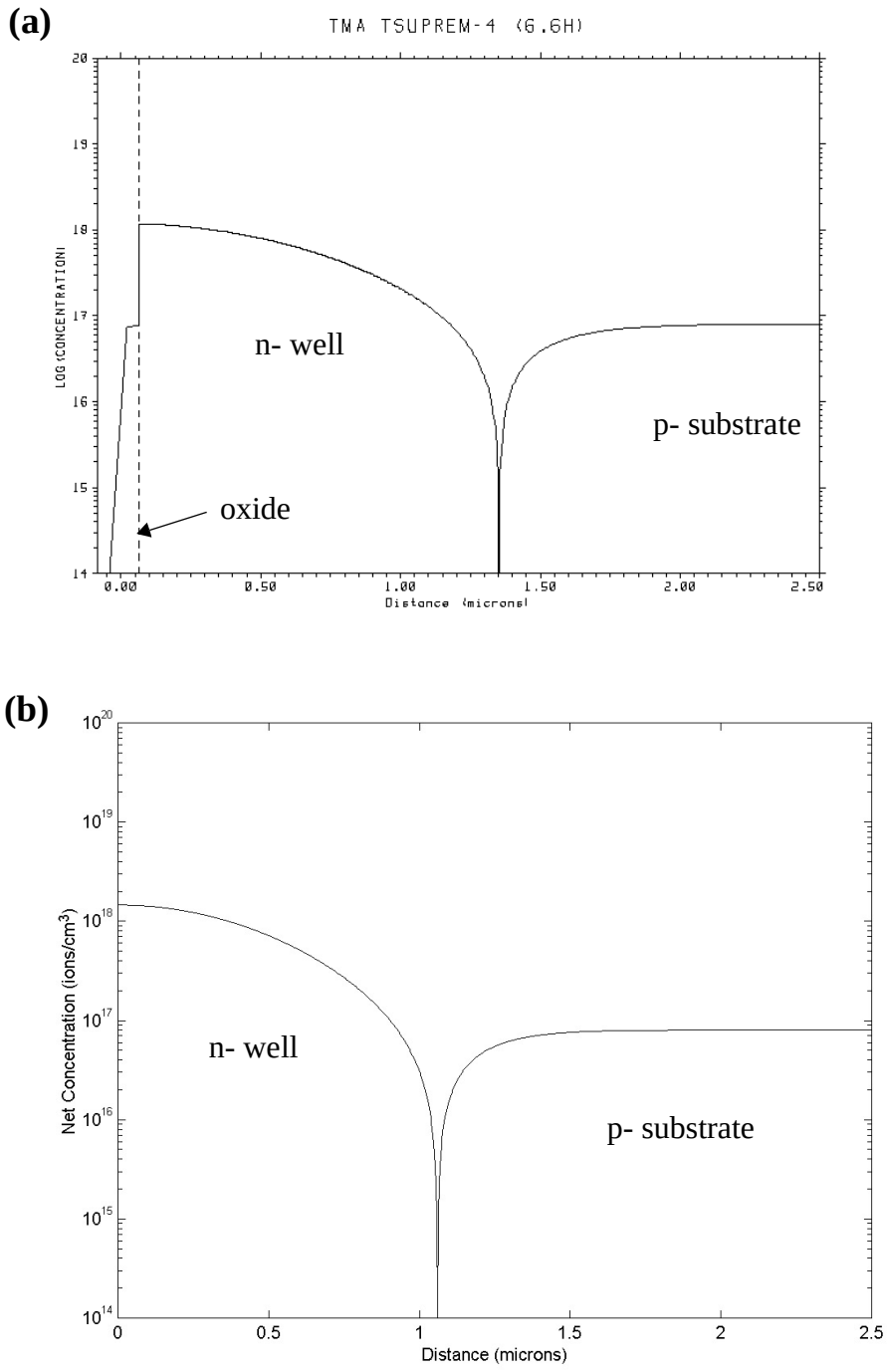


Figure 3-3. *Predicted concentration curves for n- region of process version one from (a) SUPREM computer simulation and (b) analytical solution.*

D, the diffusion coefficient is assumed to be independent of position.

$$\frac{\partial N}{\partial t} = D\frac{\partial^2 N}{\partial x^2} \tag{3-3}$$

Because the implantation energy was so low, the diffusion was modeled as a limited source diffusion. For this type of diffusion, the solution to Eq. (3-3) is given by

$$N(x, t) = \left(\frac{Q}{\sqrt{\pi Dt}}\right)\exp\left(\frac{-x}{\sqrt{2Dt}}\right)^2 \tag{3-4}$$

where Q is the dose of the implant. The diffusion coefficient follows an Arrhenius behavior and depends exponentially on the temperature. It can be calculated from Eq. (3-5).

$$D = D_0\exp\left(\frac{-E_A}{kT}\right) \tag{3-5}$$

The values for D_0 and E_A that were used for both the phosphorus and boron diffusions are given in Table 3-1.

Table 3-1. *Diffusion coefficient values.*

Element	D_0(cm^2/sec)	E_A(eV)
Phosphorus	10.5	3.69
Boron	10.5	3.69

The solution to Eq. 3-4 was then plotted using Matlab with the parameters for the n-implant and drive-in. The resulting net dopant concentration profile is shown in Fig. 3-3b. The other important results from the analytical model include the surface dopant concentration of 1.5 x 10^{18} ions/cm^3 and the junction depth of 1.06 μm. These compare to values of approximately 1.2 x 10^{18} ions/cm^3 and 1.26 μm from the SUPREM model. The analytical model's sheet resistance for the n- layer was then found from Irvin plots of surface dopant concentration versus the product of the sheet resistance and junction depth [39]. The indicated sheet resistance was found to be approximately 375 Ω/square, which

is quite similar the SUPREM value of 337 Ω/square.

For the n+ and the p+ highly doped regions, the primary fabrication goal was not the sheet resistance but the dopant concentration at the surface after drive-in. Because the primary purpose of these regions was to provide a good ohmic contacts to the aluminum collector lines, the target was set to be greater than 10^{19} atoms/cm^3. The doses were then chosen to be 3.2×10^{15} ions/cm^2 for the phosphorus and 4.0×10^{15} ions/cm^2 for the boron. The predicted concentration curves can be seen in Fig. 3-4a and Fig. 3-5a. The solutions were once again verified by solving Eq. (3-4) with the resulting curves shown in Fig. 3-4b and Fig. 3-5b. A trend is evident were the SUPREM model indicates a slightly deeper junction depth and a slightly lower surface concentration. In the case of the p+ region, the lower surface concentration can also be partially attributed to the fact that the boron is pulled into the oxide layer during the drive-in, lowering the effective dose in the silicon. This can be seen in Fig. 3-4a with a higher net dopant concentration in the oxide than in the neighboring silicon.

One other point of interest from the concentration curves is that the junction depth of the higher concentration regions is deeper than the depth of the lower concentration regions. This results from a single drive-in step being used for all three implants. One of the ramifications of this is that it is not possible to fabricate PMOS devices because the p+ regions necessary to create the source and drain would travel deeper into the substrate than the n- well. A process modification which solved this problem will be discussed in the next section.

3.3.1.2 VERSION 2: CMOS CIRCUITS WITH METAL GATES

As previously mentioned in Section 2.4, a dual drive-in process was developed from the initial solar cell process which had the capability of creating both NMOS and PMOS devices with metal gates. In order to make this possible, two separate drive-ins were necessary, a long, high temperature drive-in for the n- region and then a shorter, lower temperature drive-in for the n+ and p+ regions. This modification allowed the n- region to

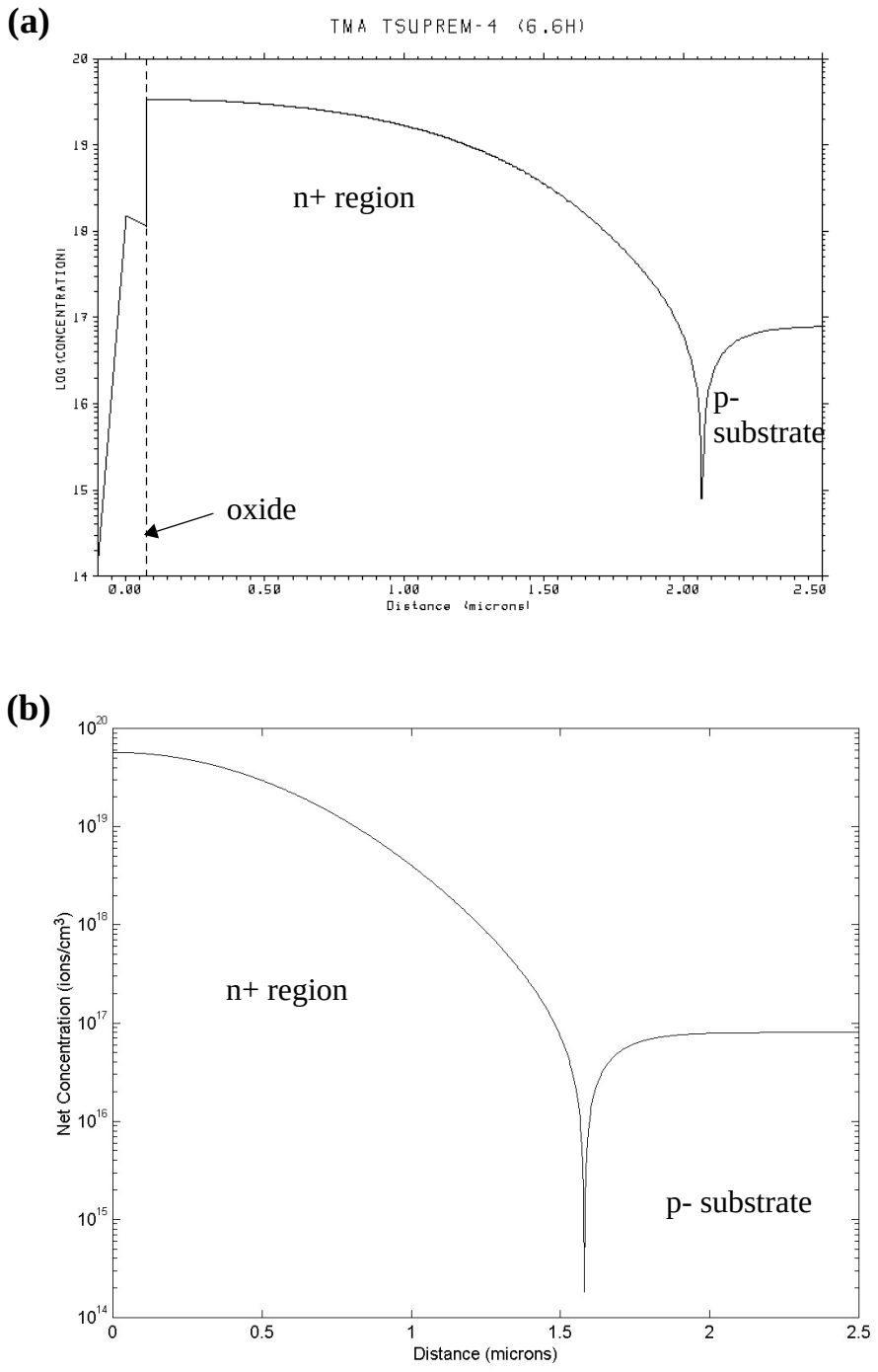


Figure 3-4. *Predicted concentration curves for n+ region of process version one from (a) SUPREM computer simulation and (b) analytical solution.*

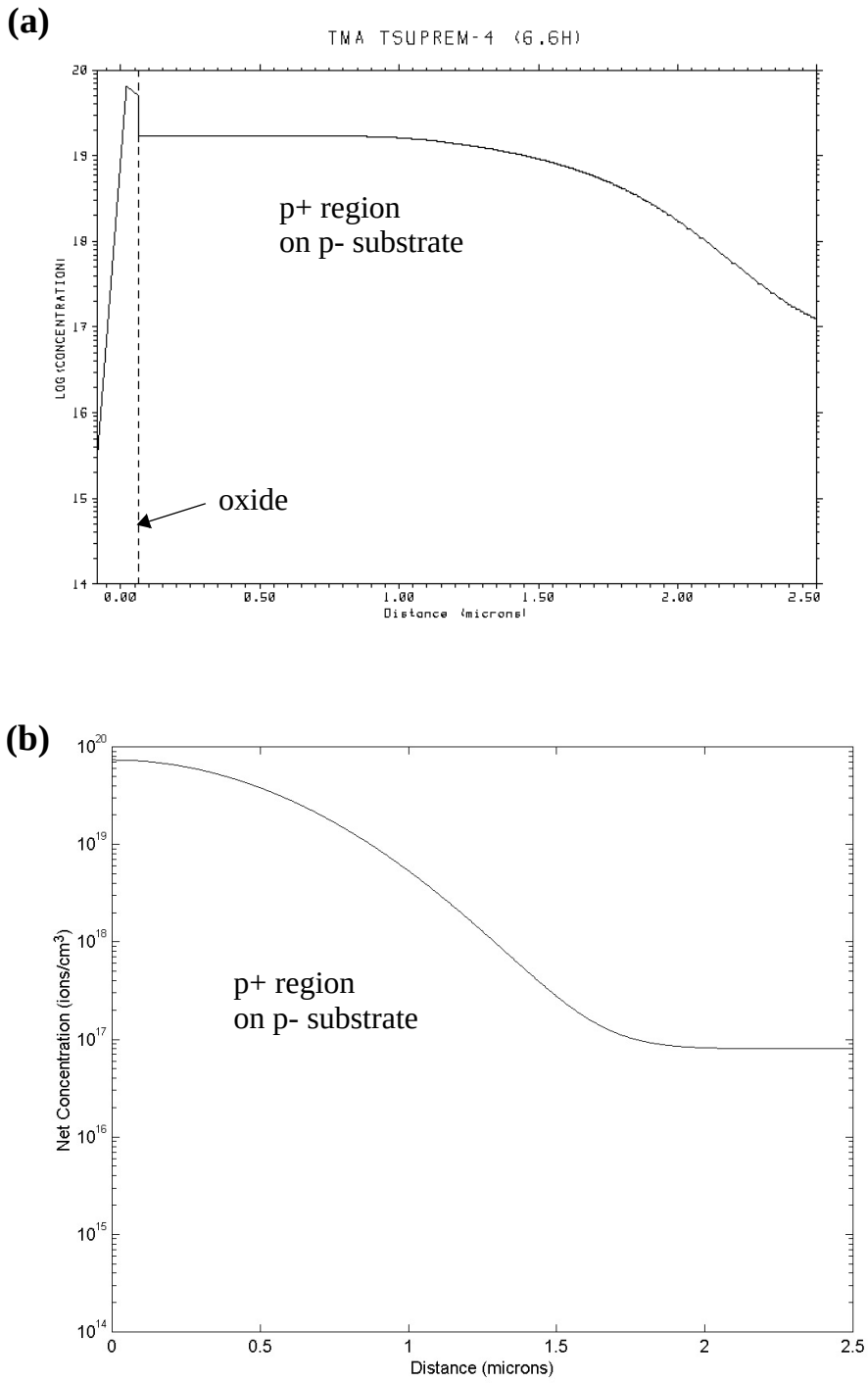


Figure 3-5. *Predicted concentration curves for p+ region of process version one from (a) SUPREM computer simulation and (b) analytical solution.*

act as a well for the PMOS devices.

The n- region is similar to the previous one. The implant parameters are identical but the drive-in is slightly different. It is done at a temperature of 1100°C for a total of 210 minutes. This is divided into 30 minutes of dry oxidation followed by 180 minutes of inert drive-in. This results in a slightly deeper junction, which is evident in Fig. 3-6. Once again, the SUPREM model is shown on top and the analytical result is shown below for comparison. Although the junction is deeper than before, the predicted sheet resistance is very similar, with a SUPREM result of 312 Ω/square and an analytical result of approximately 325 Ω/square. The analytical result was found from Irvin's curves for a surface concentration of 6.9×10^{17} and a junction depth of 1.85 μm.

After stripping the thin oxide, the n+ and p+ implants are performed and the dopants are driven-in. This is done at 850°C in a steam environment. A wet thermal environment is used so that a similar oxide thickness is grown even though the temperature is reduced so much from the NMOS process. The selected doses for these implants are 1×10^{15} ions/cm^2 for the n+ region and 5×10^{14} ions/cm^2 for the p+ region. The predicted concentration curves for these implants inside of the n- well are shown in Fig. 3-7 and Fig. 3-8, respectively.

These curves show a greater difference between the analytical model and the SUPREM model. The difference can be attributed to two factors. First, the diffusion coefficient has a dependence on the concentration level [40], which is not reflected in Eq. (3-3). Second, diffusion at low temperatures is much more dependent on defects in the silicon, which is again not reflected in the analytical model. Both of these factors would act to increase the diffusion coefficient, resulting in a dopant concentration curve closer to the SUPREM model.

3.3.1.3 VERSION 3: CMOS CIRCUITS WITH POLYSILICON GATES

Although the second version of the circuits process was successfully used to fabricate both NMOS and PMOS devices (chapter 4), their characteristics were not well matched,

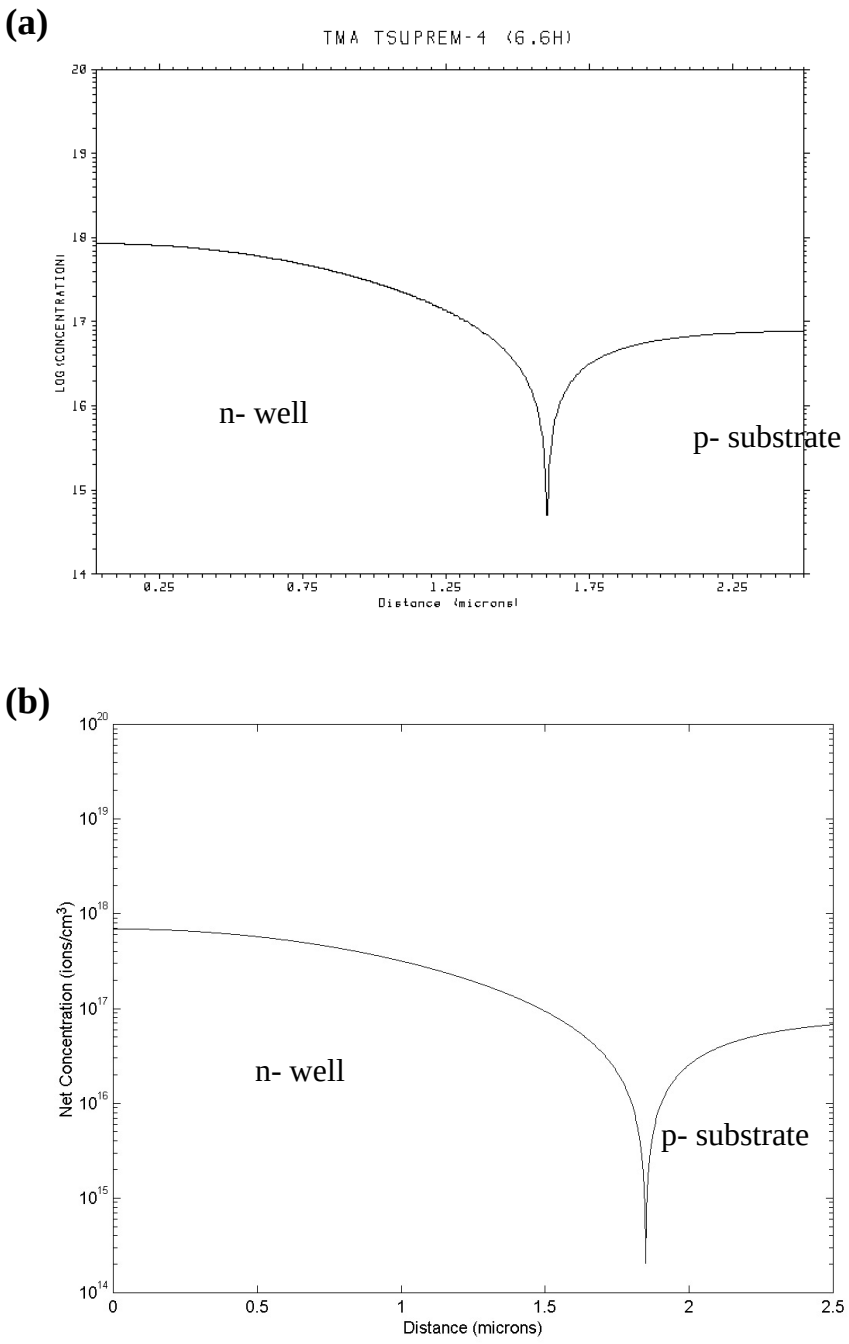


Figure 3-6. *Predicted concentration curves for n- region of process version two from (a) SUPREM computer simulation and (b) analytical solution.*

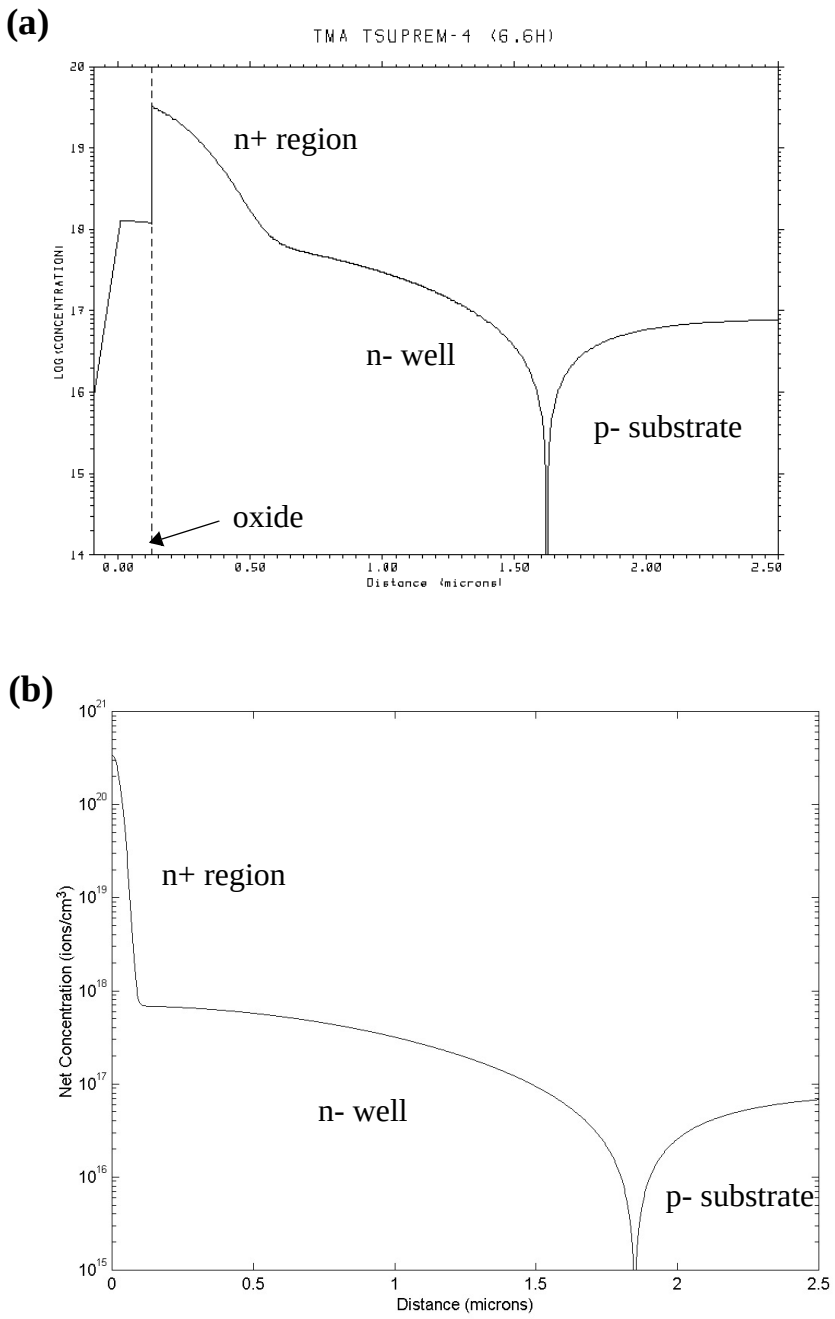


Figure 3-7. *Predicted concentration curves for n+ region of process version two from (a) SUPREM computer simulation and (b) analytical solution.*

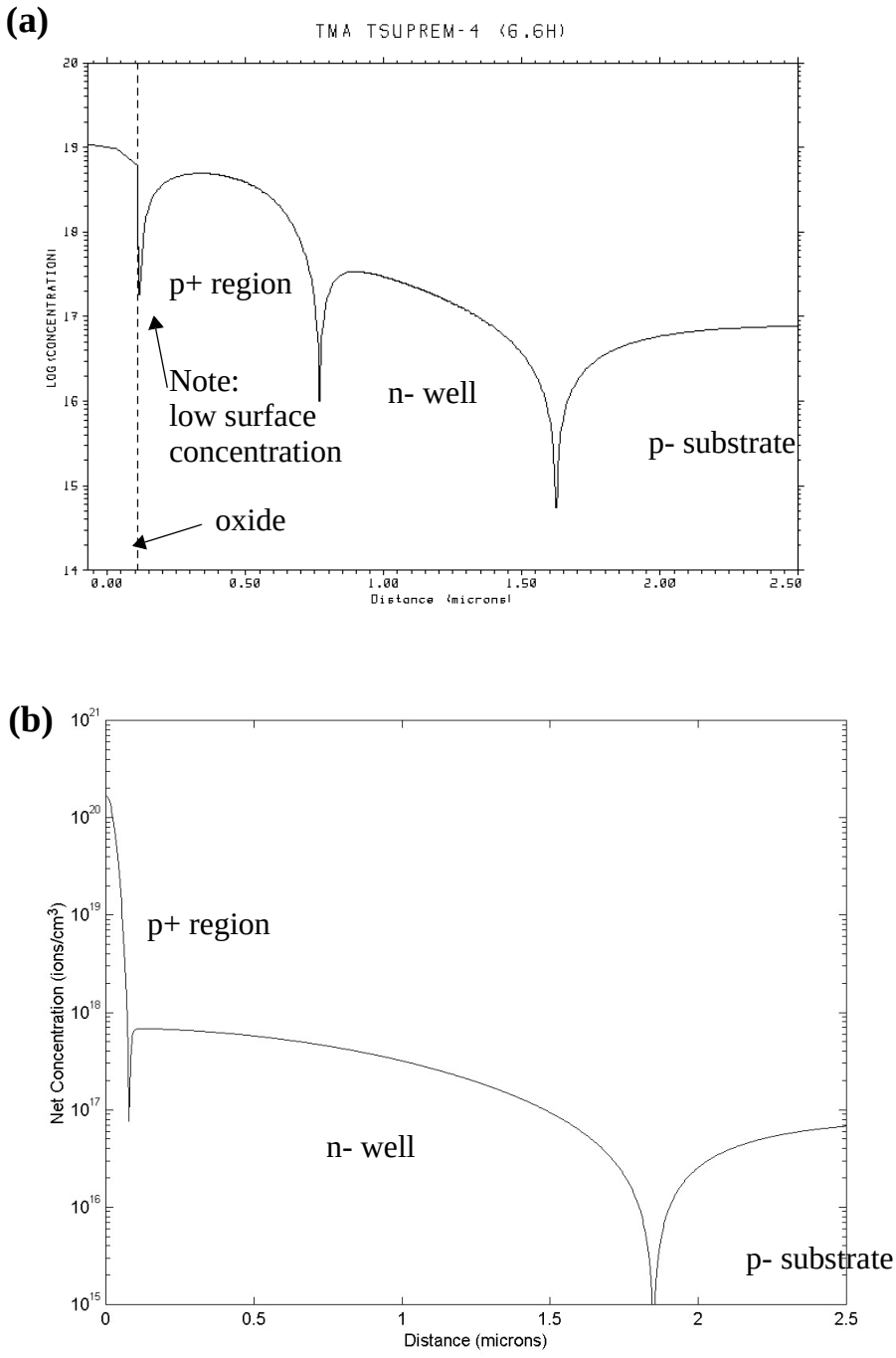


Figure 3-8. *Predicted concentration curves for p+ region of process version two from (a) SUPREM computer simulation and (b) analytical solution.*

limiting the usefulness of the circuits. This was primarily caused by the high doping level of the device layer, which had been chosen for the performance of the solar cells.

For the third version of the process, the parameters were chosen as a compromise between the needs of the solar cells and the circuits. The primary result of this was to start with a less heavily doped wafer. The resistivity was chosen to be 2.5 Ω-cm instead of the previously used 0.25 Ω-cm. This effects the output of the solar cells by having a potentially greater loss of power to the resistances of the n- and p- regions. This then requires a more careful design of the metal collector lines (Section 3.3.2).

The lower resistivity of the p- substrate lead to a lower resistivity of the implanted n- region as well. The target sheet resistance was chosen to be 1.7 KΩ/square. Because the n- region also acts as the well for the PMOS devices, the goal was to make the junction deeper in the silicon. This provided more room for the sources and drains and reduced the chance of breakdown. This was achieved by driving-in the n- implant at a higher temperature (1100°C vs. 1050°C) and for a much longer time (760 minutes vs. 210 minutes). The predicted net concentration curves from both the SUPREM model and the analytical model are shown in Fig. 3-9.

The n+ and p+ implants still needed to have a high enough surface concentration to ensure a good ohmic contact between the silicon and the aluminum. The target was still to have the surface concentration be greater than 10^{19} atoms/cm^3. The predicted concentration curves are shown in Fig. 3-10 and Fig. 3-11, respectively.

3.3.2 METAL COLLECTOR LINES

The design of the metal collector lines is important to the efficiency of the solar cells. A typical design has them arranged as interdigitated fingers. For good performance, the distance between the fingers must be carefully chosen to reduce resistive power losses. When an EHP is generated and separated, the hole travels through the p region and the electron travels through the n region until they reach their respective metal contacts. If the

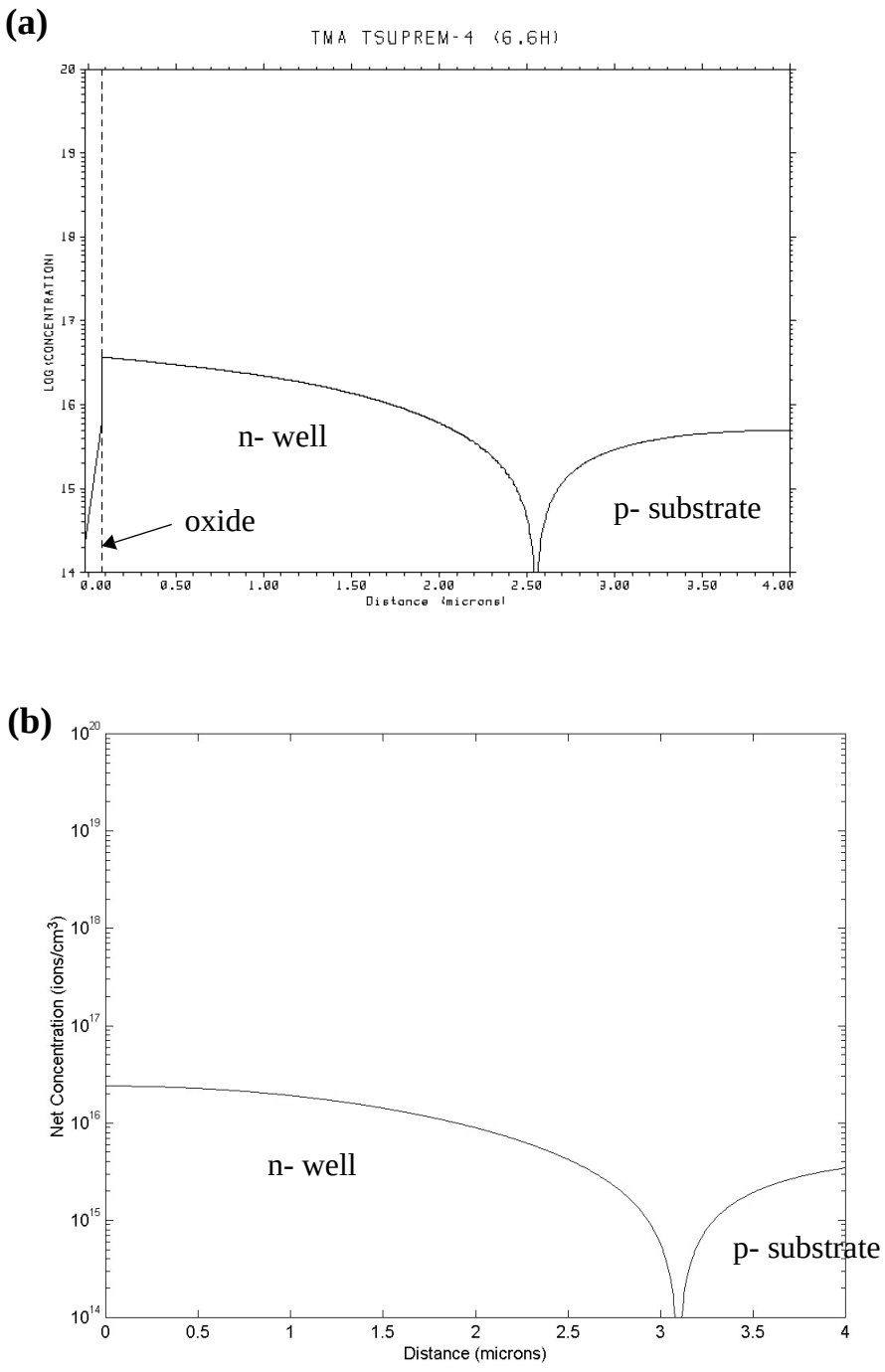


Figure 3-9. *Predicted concentration curves for n- region of process version three from (a) SUPREM computer simulation and (b) analytical solution.*

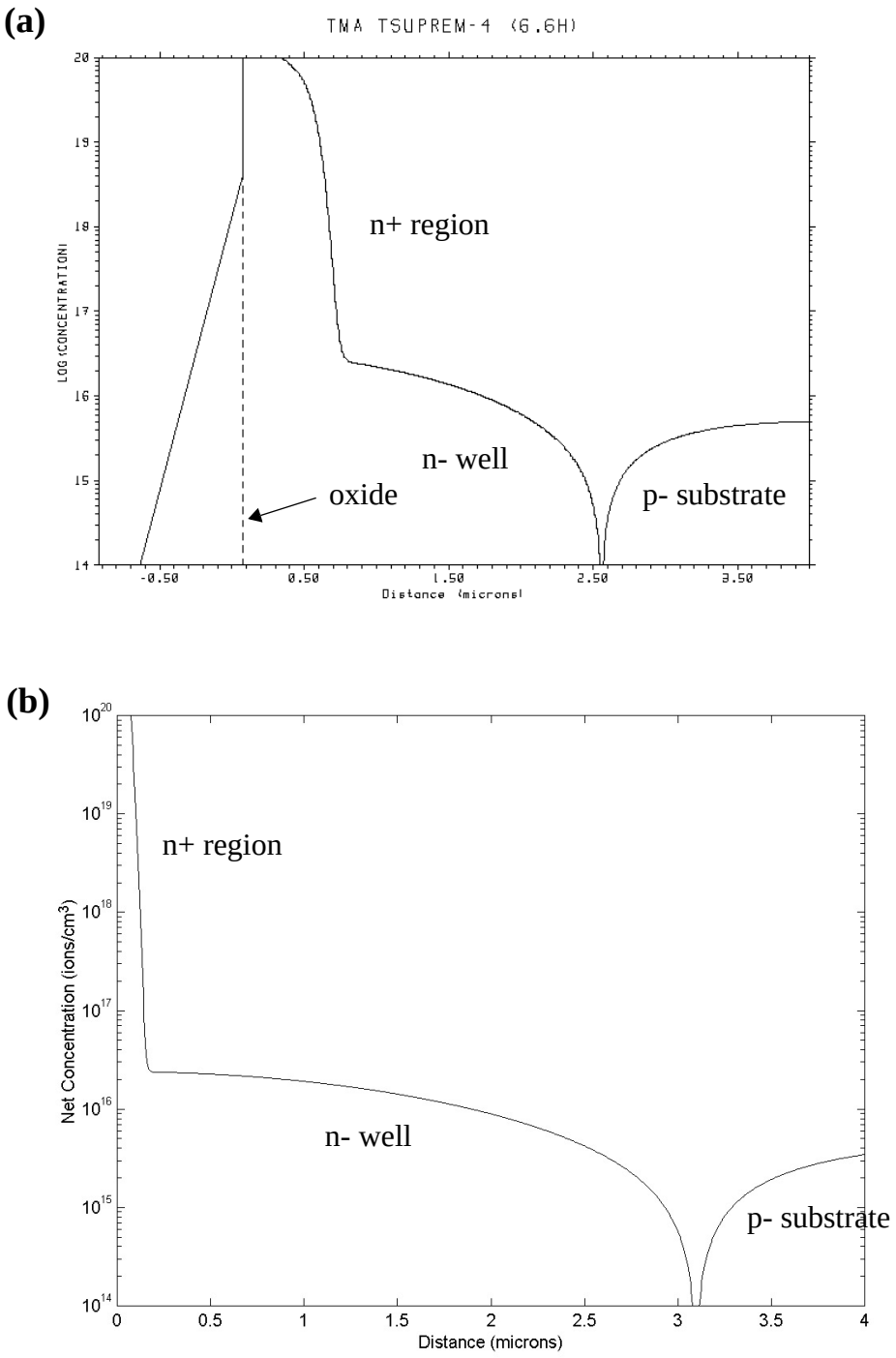


Figure 3-10. *Predicted concentration curves for n+ region of process version three from (a) SUPREM computer simulation and (b) analytical solution.*

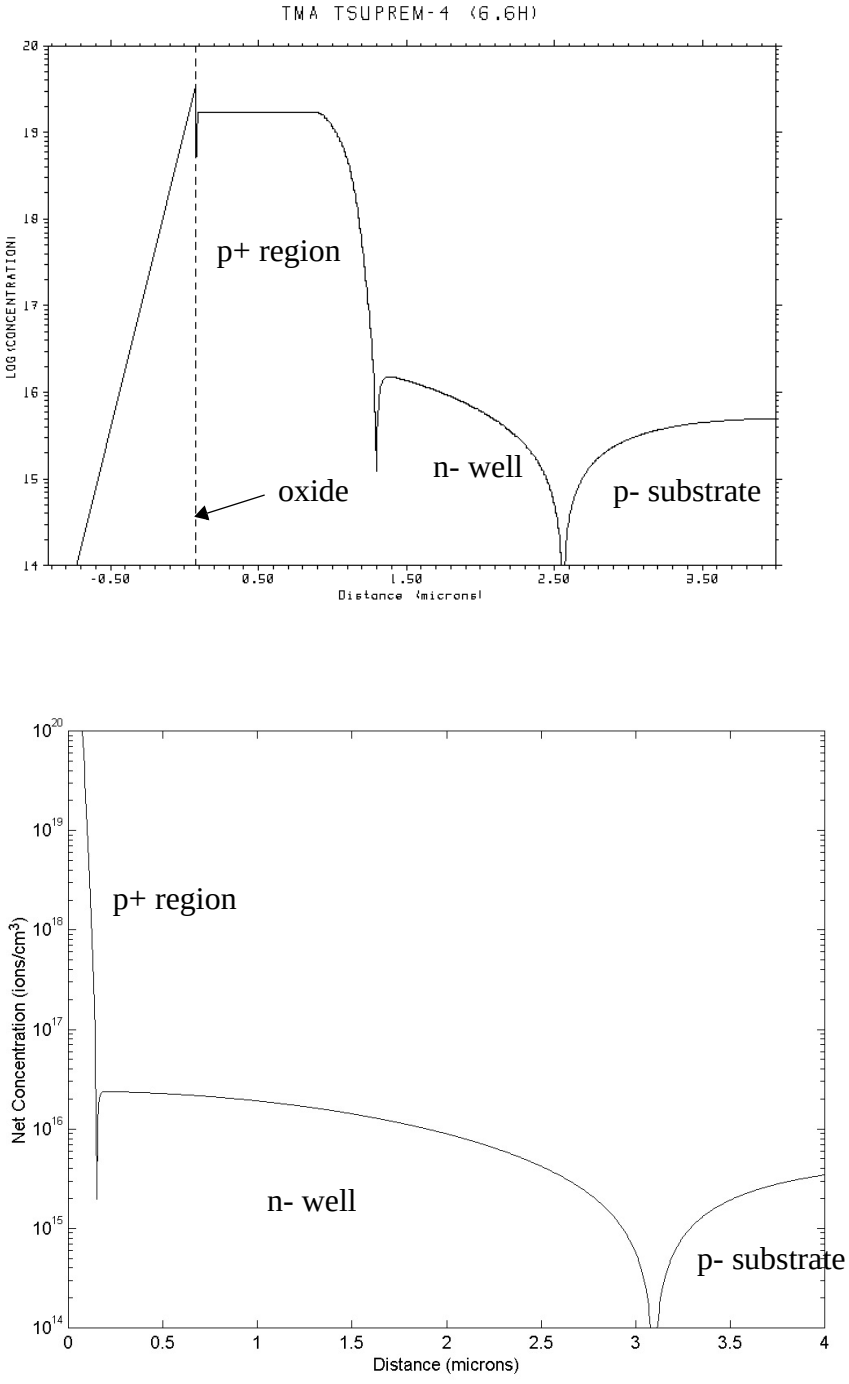


Figure 3-11. *Predicted concentration curves for p+ region of process version three from (a) SUPREM computer simulation and (b) analytical solution.*

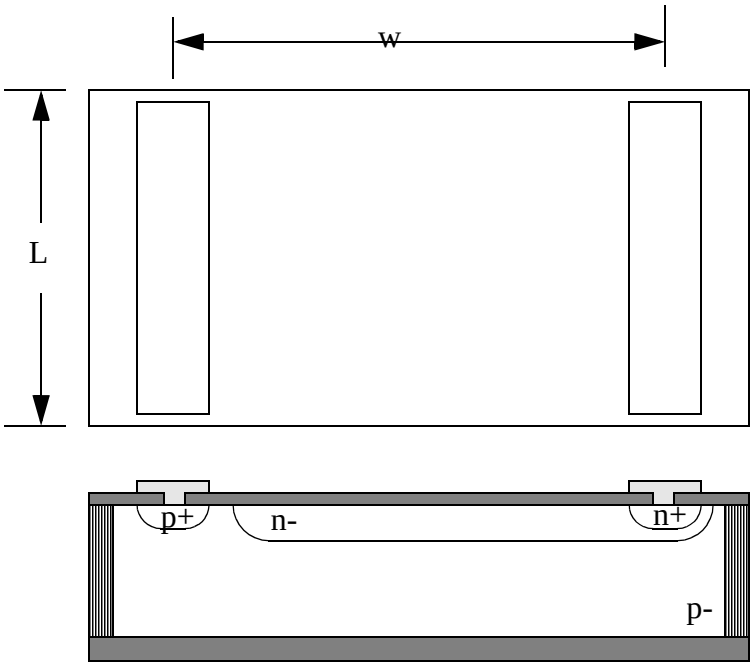


Figure 3-12. *Solar cell model for calculating resistive power losses.*

resistance through either of these regions is too large, power which could have been used to drive the load will be lost, lowering the efficiency of the cell. Two ways of reducing this problem are to increase the doping level in the regions so that there is less resistance to carrier motion, and to increase the density of the fingers so that the carriers have a shorter distance to travel. If the doping level is made too large, an increase in the recombination rate will occur, lowering the efficiency. As previously discussed, it may also be beneficial to have a lower doping level to increase the performance of the circuit elements. If the density of the metal contacts is increased, they will shadow the area under them and any light that strikes the metal fingers will be reflected away and will not be converted into usable power.

To estimate the amount of power lost to the resistivity of the p- and n- regions, consider the solar cell shown in Fig. 3-12. As electron-hole pairs are generated in the cell, the electrons will travel along the n- region to the right and holes will travel along the p- region to the left. If we consider the flow of electrons through the n- region, we see that

the current will increase linearly, assuming that EHPs are generated uniformly within the cell.

$$I = JxL \tag{3-6}$$

where J is the current density of the cell.

The power lost to resistivity is found from

$$P_R = \int_0^w I^2 dR \tag{3-7}$$

where I is given by *Eq. (3-6)* and dR is given by

$$dR = \rho\frac{dx}{L} \tag{3-8}$$

with ρ being the sheet resistance of the n- region. This gives

$$P_R = \int_0^w J^2 x^2 L\rho\, dx = J^2 L\rho\frac{w^3}{3}. \tag{3-9}$$

When the cell is operating at the maximum power condition, the power generated is

$$P_{mp} = V_{mp} J_{mp} wL \tag{3-10}$$

and the fractional power lost to the resistivity is

$$p = \frac{P_R}{P_{mp}} = \frac{J_{mp}}{V_{mp}}\rho\frac{w^2}{3}. \tag{3-11}$$

If we assume typical values for solar cells of $J_{mp} = 250\mu A/mm^2$ and $V_{mp} = 450mV$, then the minimum finger spacing can be found for a given sheet resistance and a maximum resistive power loss. For a maximum power loss of 1% and a sheet resistance of 300 Ω/square, the maximum spacing should be 424 μm.

3.3.3 ANTI-REFLECTIVE COATING

If the thickness of the oxide layer which is grown over the solar cells is carefully chosen, it can act to reduce the amount of light reflected off of the cells surface. In order for this to happen, its thickness needs to be matched to the dominant wavelength of the incident light. To minimize the reflection for a given wavelength, λ, the thickness, d, should be

$$d = \frac{\lambda}{4n} \tag{3-12}$$

where n is the refractive index of the antireflective layer. Because the dominant wavelength in the AM1.5 spectrum is 575 nm and assuming the refractive index of silicon dioxide as 1.4, we can calculate an optimal thickness of 1027Å. The actual target thickness is greater than this because some of it is removed during a final dip in diluted HF which is done before the metal is sputtered to ensure that there is no native oxide at the bottom of the contacts holes.

3.3.4 BACK SURFACE FIELD

A back surface field (BSF) is a highly doped region of the same impurity as the bulk of the device which is placed on the bottom of the cell. For an SOI solar cell, it lies at the bottom of the device layer, at the interface with the bonding oxide layer. Its purpose is to reduce the amount of recombination that occurs at the point where the silicon and the silicon dioxide meet. Normally, this edge of the crystal structure of the silicon would be an ideal place for the electrons to drop back down to their lower energy state, reducing the output of the cell, but because the doping level is high, electrons are much less likely to be at the surface. The previous SOI solar cell research by Hebling [26] showed that the presence of a BSF raised the efficiency of the cells from approximately 15% to 18%. For this reason, BSFs were used on all fabricated cells from this process.

3.3.5 ADDITIONAL TECHNIQUES FOR EFFICIENCY IMPROVEMENT

Another common technique which is used to increase the output of solar cells is to create surface texturization on the top of the cell. This causes the light to be reflected at an angle as it enters the cell, reducing the chance that it will travel straight through the cell and out the bottom. These are typically formed by using an anisotropic wet etch of the silicon, for example, with KOH. These were eliminated for this process. Because the texturization is done early in the process, all subsequent lithography steps are made more difficult due to the increased topology. In addition, the depth of the inverted pyramids would be more pronounced on the thinner device layers of this process. For example, on the devices fabricated by Hebling, the distance between the bottom of the pyramids to the bottom of the cell was 39 μm whereas this dimension on a 25 μm thick cell would only be 18 μm. This would undoubtedly have a greater effect on efficiency, possibly eliminating any benefit provided by the texturization in the first place. Texturization is also a feature which could be added later without affecting the rest of the design, only the difficulty of fabrication.

Another technique which may provide a higher efficiency extends the idea of the back surface field to the edges of the cell where the silicon meets the back-filled isolation trenches. Recombination is probably more likely to occur here than along the bottom of the cell because the DRIE leaves the surface rough. If the doping level at the cell edges was increased, it would reduce the amount of recombination and hence improve the efficiency. Although ion implantation would not be effective because the surfaces of interest are perpendicular to the surface of the wafer, a diffusion could be used after the isolation trenches had been etched but before the nitride lining was deposited.

3.3.6 SOLAR CELL LAYOUT

Square shaped cells are preferred over rectangular ones because this allows the perimeter edge area of the cell to be reduced for a given cell volume. This then reduces the opportunity for recombination to occur. Although the extreme of this would be to use

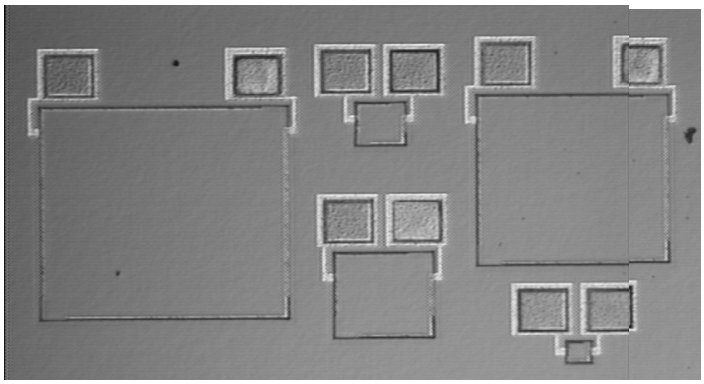


Figure 3-13. *Test solar cells for process versions one and two. Sizes are 50, 100, 200, 400 and 500 μm on a side.*

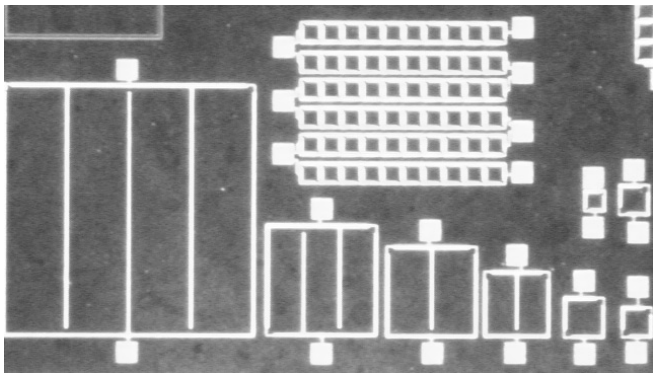


Figure 3-14. *Test solar cells for process version three. Sizes are 104, 150 (2 cells), 200, 325, 450, 550 and 1250 μm on a side.*

round cells, this would be inefficient because the numerous cells needed to generate high voltages could not be packed as tightly together.

The size of the test cells was varied to provide a comparison of how the size affected the performance. For the first and second version of the process, the cell sizes were 50, 100, 200, 400 and 500 μm on a side. The test cells can be seen in Fig. 3-13. For the third version of the process, which used a different layout than the other two versions, the sizes were 104, 150, 200, 325, 450, 550 and 1250 μm on a side, as shown in Fig. 3-14.

For cells that are not so large as to require an increased density of metal collector lines,

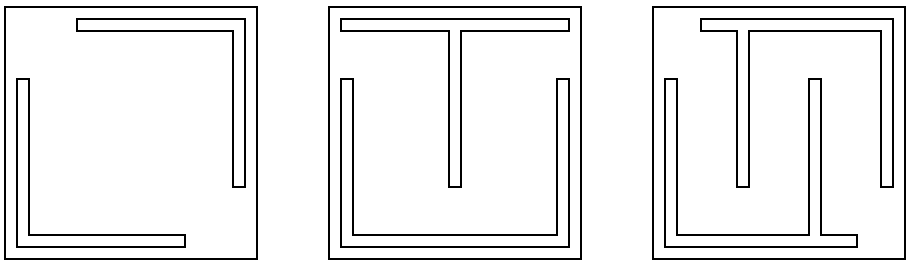


Figure 3-15. *Design for the metal collector lines as the required density increases.*

each of the lines runs along two sides of the solar cell in the shape of an L, as shown in Fig. 3-15a. If the cells are large enough or the resistivity is high enough to require more lines, then the lines are placed in an interdigitated pattern across the width of the cell. For example, the next step up from the L-shaped lines would be matching U and T-shaped lines, as shown in Fig. 3-15b. The pattern continues in this manner, with the next step, which has a total of four lines across the width, shown in Fig. 3-15c.

When the individual solar cells are wired in series to provide a high voltage output, each cell provides about 0.5 V to the total output. The primary solar array which was used to demonstrate the capabilities of this process had a total of 200 square cells, with each being 400 μm on a side. It covered approximately one half of the die, as shown in Fig. 3-16. The array was divided into ten sections of 20 cells each so that the total power output could be configured based on the desired voltage. This was accomplished by positioning the input and output pads for each section in a way that they could be easily wirebonded together. This also allowed an individual array to be bypassed if it did not work properly. Each of the first and last ten cells had wirebond pads so that the final output could be controlled even more precisely.

When designing arrays for very high voltages, special care must be taken to eliminate any possible shorts between cells that would keep the array from working properly. The first way that shorting could occur is by metal lines shorting through the passivating oxide layer to the substrate below. The thickness of this oxide layer was generally between 1000

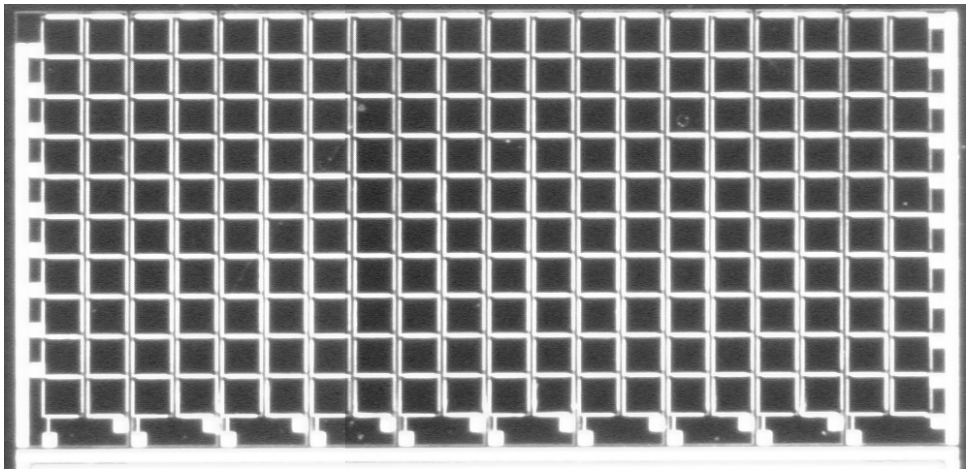


Figure 3-16. *200 cell solar array made up of 400 μm solar cells. Total area is approximately 0.5 cm^2.*

and 1500 A. Therefore, if two metal pads are over the same substrate, breakdown can occur if the potential between them is greater than about 50 V. This can be avoided by isolating the substrate areas underneath each of the pads. Another potential shorting path is along the back-filled isolation trenches. Because there is a fair amount of topography over the tops of the back-filled trenches, it can be difficult to completely remove all of the metal. If enough residual metal is left between two cells, they can be shorted together. For this reason, cells with greatly different potentials should not share isolation trenches.

3.4 RESULTS

3.4.1 SOLAR CELL TESTING PROCEDURES

The solar cells fabricated with this process were tested in two different ways. The first method used the light provided by the microscope of a probe station to illuminate the solar cells. This was convenient for doing side-by-side comparisons of solar cells. Because the incident light power was consistent, the relative outputs can be compared, even though the actual efficiency is not known.

For the second method, the solar cells were wirebonded into a package so that they

could be easily taken outside and illuminated by the sun. This allowed the actual efficiency of the cells to be estimated.

In order to approximate the efficiency of a solar cell, we need to know the amount of incident light power. Efficiency tests for solar cells fabricated for this research were performed with solar illumination on a clear day with no noticeable clouds or excessive haze. The amount of incident solar power is typically given by the air mass number, e.g. AM1.5, which is a measure of the path length that the light has traveled through the earth's atmosphere. Outside the earth's atmosphere, at AM0, the solar power is 1.353 kW/m^2 or 1.353 mW/mm^2. If the sun were directly overhead, the light hitting the surface of the earth would pass through exactly one atmosphere. This is referred to as AM1. If the sun is at an angle θ overhead, then the air mass value is given by Eq. 3-13.

$$AM = \frac{1}{\cos\theta} \tag{3-13}$$

As the distance that the sunlight has to travel through the atmosphere increases, the attenuation of the light power is also increased.

The standard air mass number for terrestrial solar cell testing has been chosen to be AM1.5 with the power raised so that the total incident power is 1 mW/mm2. The power at AM1.5 is actually 0.832 mW/mm2.

The air mass number can be easily estimated at any time from a comparison of the height of a vertical object and the length of its shadow. If an object of height *h* has a shadow of length *s* then we can calculate the air mass number using Eq. 3-14.

$$AM = \frac{1}{\cos\theta} = \sqrt{1 + \left(\frac{s}{h}\right)^2} \tag{3-14}$$

Assuming clear skies, the incident power can then be estimated by assuming a linear relationship between the path length through the atmosphere and the amount of power

attenuation. If the power decrease from AM0 to AM1.5 is

$$\Delta Power = 1.353 - 0.832 = 0.521\ mW/mm^2 \tag{3-15}$$

then the power for an arbitrary air mass number would be given by Eq. 3-16.

$$P_{in} = 1.353 - 0.521 \cdot \frac{AM}{1.5}\ mW/mm^2 \tag{3-16}$$

As an example at AM2, we can use Eq. 3-16 to calculate

$$P_{in,\,AM2} = 0.658\ mw/mm^2. \tag{3-17}$$

It should be noted that because the air mass equation assumes a flat atmosphere, these calculations are only valid up to a certain point. All results reported here, however, were taken at AM2 or lower which should be well within the range of applicability.

3.4.2 Individual Solar Cell Performance

3.4.2.1 Effect of Cell Size and Process on Performance

The individual cells from each of the three process versions were tested under the artificial illumination of the probe station light to compare their relative performance. Current vs. voltage curves were generated for each cell at two different light power settings, full and partial. A summary of the results for full illumination are given in Table 3-2 and for partial illumination in Table 3-3. Because all of the cells are square, the size is given as the length of one side. The area is then just the square of the side. The power density is similar to efficiency but because the input power is not known, it only provides a relative measurement. The input power is assumed to be constant for all cells with the same light setting. To make it easier to compare the results, the power density is plotted verses the cell area for all of the test cells in Fig. 3-17. The three curves at the top are for the full illumination and the lower ones are for the partial illumination. To help shed some light on why the performance varies between the three process, a graph of the short circuit

Table 3-2: Solar Cell Performance under Full Microscope Illumination

Process	Size (length of side in μm)	Short Circuit Current (μA)	Open Circuit Voltage (mV)	Max. Power Current (μA)	Max. Power Voltage (mV)	Maximum Power (μW)	Power Density (μW/mm^2)	Fill Factor
One	50	3.08	615	2.73	480	1.31	524	0.692
One	100	14.5	635	12.9	455	5.85	585	0.635
One	200	62.6	645	56.5	460	26	650	0.644
One	400	253	650	224	410	91.9	574	0.559
One	500	397	650	342	365	125	500	0.484
Two	50	3.06	550	2.58	350	0.904	362	0.537
Two	100	13.6	585	11.1	335	3.72	372	0.468
Two	200	58.7	610	49.2	335	16.5	413	0.461
Two	400	238	625	207	340	70.3	439	0.473
Two	500	377	630	330	325	107	428	0.451
Three	104	14	590	13.1	480	6.31	583	0.764
Three	150	31.3	590	29.4	480	14.1	627	0.764
Three	150	31.2	590	29.3	480	14.1	627	0.766
Three	200	57.1	600	52.7	490	25.8	645	0.753
Three	325	152	610	141	490	69.3	656	0.747
Three	450	297	610	277	470	130	642	0.718
Three	550	442	610	411	480	197	651	0.731
Three	1250	2300	610	2040	410	836	535	0.596

Table 3-3: Solar Cell Performance under Partial Microscope Illumination

Process	Size (length of side in μm)	Short Circuit Current (μA)	Open Circuit Voltage (mV)	Max. Power Current (μA)	Max. Power Voltage (mV)	Maximum Power (μW)	Power Density (μW/mm^2)	Fill Factor
One	50	0.703	555	0.625	435	0.272	109	0.697
One	100	3.37	585	3.02	460	1.39	139	0.705
One	200	14.5	610	12.9	485	6.27	157	0.709
One	400	56.7	620	51.9	485	25.1	157	0.714
One	500	89.9	620	81.9	470	38.5	154	0.691
Two	50	0.742	480	0.641	335	0.215	86	0.604
Two	100	3.27	525	2.81	360	1.01	101	0.588
Two	200	13.8	560	11.2	325	3.65	91	0.472
Two	400	57.2	585	49.5	405	20	125	0.598
Two	500	85.2	585	69.8	340	23.7	95	0.476
Three	104	3.22	530	2.98	440	1.31	121	0.768
Three	150	7.17	540	6.6	450	2.97	132	0.767
Three	150	7.16	540	6.59	450	2.97	132	0.768
Three	200	13.2	550	12.4	450	5.57	139	0.767
Three	325	34.9	550	32.5	460	15	142	0.781
Three	450	68.1	550	63.2	460	29.1	144	0.777
Three	550	101	550	95	460	43.7	144	0.787
Three	1250	531	550	501	440	220	141	0.753

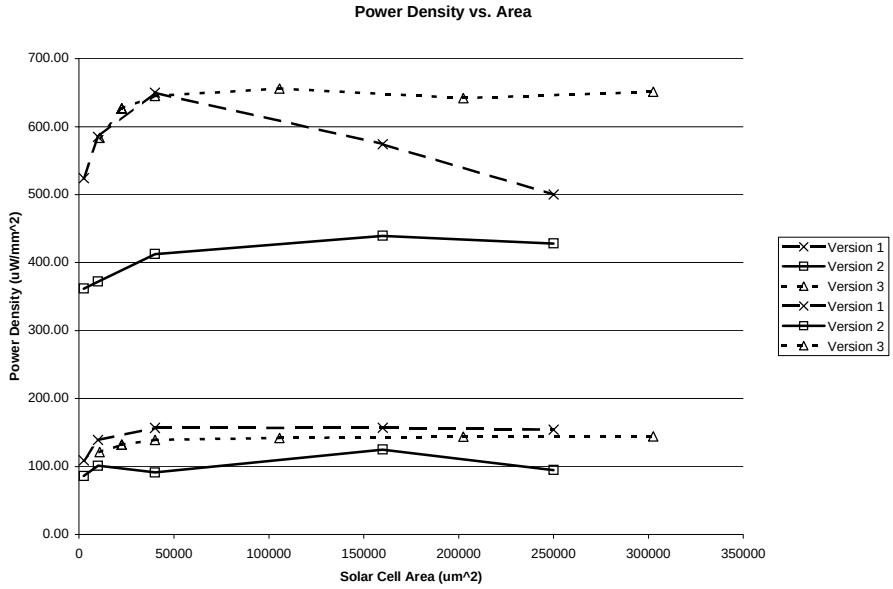


Figure 3-17. *Graph of power density vs. area for test cells from all three process versions.*

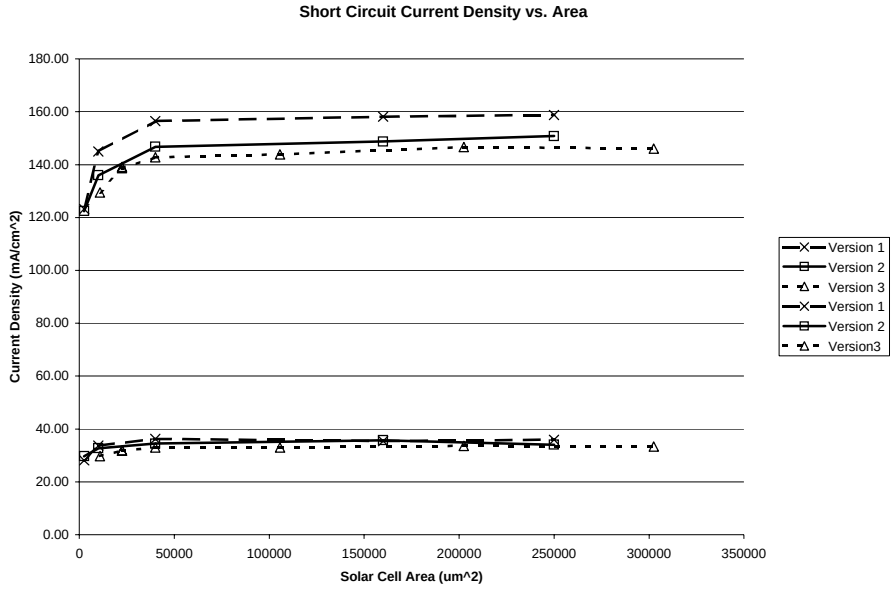


Figure 3-18. *Graph of short circuit current density vs. area for test cells from all three process versions.*

current density is plotted verses the area in Fig. 3-18. Again, the full illumination curves

are above the partial illumination curves.

A number of interesting observations can be made from these results. First, the third version of the process has the highest output under full illumination and the second highest under partial illumination in spite of the fact that it has the lowest short circuit current density. This indicates that some other factor is lowering the maximum power output of the other two process. This is further supported by the lower fill factors for the first two process. The cause of this can be seen by looking at the actual current vs. voltage curves for cells from each of the three processes, as shown in Fig. 3-19. The curve from the first process has an excessive slope, indicative of a parasitic series resistance problem, as discussed in Section 3.2. The second process version has a strange bend in the curve, indicative of a nonlinear contact resistance. The most likely source for this nonlinearity can be seen by looking at the predicted dopant concentration curve for this process, in Fig. 3-8a. Although the concentration in the p+ region is fairly high at its peak, the concentration at the surface is actually quite low. The surface concentration drops because the boron is pulled into the oxide during the drive-in. This does not occur with phosphorus, as shown in Fig. 3-7a. The low surface concentration can lead to a Schottky-barrier diode, which would cause the nonlinearity. The third version has the highest maximum power output because it has a desirable i-v curve with a high fill factor.

The second observation is that the performance drops off as the cells get smaller. This is caused by two factors. First, because the metal lines are the same width for all the cells at 5 μm, the percentage of shadowed area is higher for the smaller cells. For example, 16.4% of the 50 μm cell is shadowed by the metal collector lines, while only 7.3% of the 200 μm cell is shadowed. The second cause is that the ratio of cell surface area to cell volume is much higher for the smaller cells. This is important because the surface of the cell is were recombination of the electron-hole-pairs is most likely to occur. An increase in recombination leads to a lower power output.

Finally, the difference in performance is greater at the higher light intensity. When the

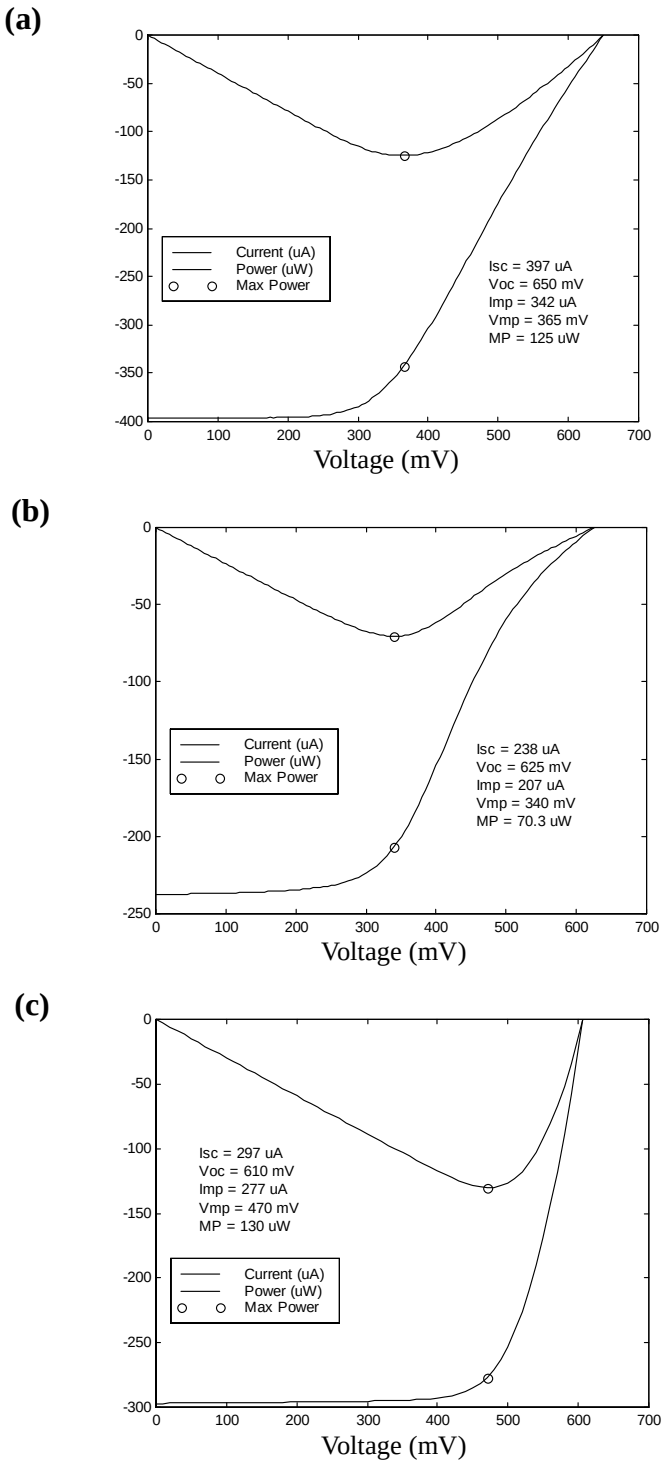


Figure 3-19. *Current vs. voltage curves for test cells from the three processes. (a) 400* μ*m cell from version 1. (b) 400* μ*m cell from version 2. (c) 450* μ*m cell from version 3.*

short circuit current output under both levels of artificial illumination is compared to the output under solar illumination (Section 3.4.3), it can be deduced that the light intensity of even the partial artificial light setting is greater than what can be expected from solar illumination. Therefore, cells from any of the three process would provide similar performance under typical conditions.

3.4.2.2 CONSISTENCY OF SOLAR CELL PERFORMANCE

When a large number of cells are wired together to create a high voltage output, it is important for the output of the individual cells to be fairly consistent. If any of the cells functions poorly, it can have a severe impact on the total performance. To test the consistency of the solar cell output, eight cells from the large array were tested at the same two microscope light settings as in the previous section. The results are summarized in Table 3-4. The most important performance parameters for good array performance are the short circuit current and the maximum power current. For the cells tested, the short circuit current does not vary more than 1 μA and the maximum power current does not vary more than 6 μA.

3.4.3 SOLAR CELL ARRAY PERFORMANCE

A high voltage solar array, as shown in Fig. 3-16, was mounted in a package and wirebonded so that it could be taken outside and tested under solar illumination. The particular array which was used was from the second version of the circuits process. The wirebonding was done so that the high output pad from one twenty cell array was connected to the same lead as the low output pad from the array next to it. This allowed each array to be tested individually by contacting two adjacent leads or easily testing a number of arrays wired in series by skipping leads. For example, contacting the first and third leads would allow testing of two arrays wired in series. The testing was done on a clear, sunny with a sun angle of 54.2°. This was used to calculate an air mass number of AM1.71. The testing results are given in Table 3-5. The first ten rows are for each of the 20 cell arrays. The next nine rows are for the series connections of the arrays. The arrays

Table 3-4: Solar Cell Performance of Individual Solar Array Cells

Illumination	Short Circuit Current (μA)	Open Circuit Voltage (mV)	Max. Power Current (μA)	Max. Power Voltage (mV)	Maximum Power (μW)	Power Density (μW/mm^2)	Fill Factor
Full	237	620	200	360	72.1	451	0.491
Full	237	620	204	360	73.5	459	0.500
Full	238	620	204	350	71.5	447	0.485
Full	238	620	203	340	68.9	431	0.467
Full	237	620	205	330	67.5	422	0.459
Full	238	620	204	340	69.2	433	0.469
Full	237	620	201	350	70.3	439	0.478
Full	237	620	199	340	67.5	422	0.459
Partial	129	600	108	350	37.7	236	0.487
Partial	129	600	112	370	41.5	259	0.536
Partial	130	610	112	380	42.4	265	0.535
Partial	130	610	112	370	41.6	260	0.525
Partial	130	600	112	370	413	258	0.529
Partial	129	600	109	360	39.3	245	0.508
Partial	130	610	111	380	42.1	263	0.531
Partial	130	610	113	370	41.8	261	0.527

Table 3-5: Solar Cell Array Performance under Solar Illumination (~AM1.71)

Number of Arrays	Area (mm^2)	Short Circuit Current (μA)	Open Circuit Voltage (V)	Max. Power Current (μA)	Max. Power Voltage (V)	Maximum Power (μW)	Incident Power (μW)	Efficiency	Fill Factor
1	3.2	41.8	8.4	34.1	5.3	181	2427	7.5%	0.515
1	3.2	41.7	8.6	32.2	5.9	190	2427	7.8%	0.530
1	3.2	41.7	11.1	35.3	7.8	275	2427	11.3%	0.594
1	3.2	41.6	11.3	35.4	8	283	2427	11.7%	0.602
1	3.2	39	11.2	35.6	7.7	274	2427	11.3%	0.627
1	3.2	41.6	11.2	35.5	7.9	281	2427	11.6%	0.603
1	3.2	41.1	10.7	34.3	7.9	271	2427	11.2%	0.616
1	3.2	40.4	9.1	33.1	6	199	2427	8.2%	0.541
1	3.2	41.5	10.1	35	7.3	255	2427	10.5%	0.608
1	3.2	41.7	11.3	34.8	8.1	282	2427	11.6%	0.598
2	6.4	41.9	16.8	33.2	11.1	369	4854	7.6%	0.524
3	9.6	41.7	28.4	33.3	19.9	662	7282	9.1%	0.559
4	12.8	41.9	39.1	34.6	26.8	928	9709	9.6%	0.566
5	16	41.6	47.1	35.7	31.4	1120	12136	9.2%	0.572
6	19.2	41.5	57.1	34	40.1	1370	14563	9.4%	0.578
7	22.4	41.6	65.1	34.9	44.5	1550	16990	9.1%	0.572
8	25.6	41.8	73.3	34.4	49.1	1690	19418	8.7%	0.552
9	28.8	41.6	80.1	33.6	55.3	1860	21845	8.5%	0.558
10	32	41.2	88.5	35.1	57.3	2010	24272	8.3%	0.551

were added in order, such that the two array results were for the first two arrays listed in the table. The three array result added the third array, and so on.

The data shows that the majority of arrays were very consistent, with estimated efficiencies between 10 and 12%. It also shows how the arrays with lower efficiencies bring down the overall efficiency when they are included. Variations in performance mount up as more arrays are added, such that the addition of the final array, which had an individual maximum power voltage of 10 V, only added 2 V to the maximum power voltage of the entire array. These results show that the processes presented here are capable of producing good efficiencies and high voltage outputs.

4. SYSTEM COMPONENT 2: CIRCUITS

4.1 INTRODUCTION

In this chapter, the second component of the integrated process, the circuits, will be discussed. The primary purpose of the circuits is to provide a means of controlling the power between the solar cell arrays and the electrostatic actuators. To do this effectively, they need to be able to withstand the high voltages which are possible in this process. Because this process is not optimized for the performance of the circuit elements, it would not be practical to use it to fabricate all of the circuits for an integrated system. Instead, a better plan for integration uses a CMOS control chip, which would be made in a commercial foundry process, to control the switching of the high voltage circuits fabricated in this process.

In the following sections, the circuit elements which have been fabricated in this process will be discussed. This includes metal-oxide-semiconductor (MOS) field-effect transistors (FETs) and bipolar junction transistors (BJTs). In addition, two simple power switches will be discussed which can be used to control the flow of power between solar cell arrays and electrostatic actuators.

4.2 FIELD EFFECT TRANSISTORS

4.2.1 BASICS OF FET OPERATION

A transistor is a three terminal device which allows the current between two of the terminals to be controlled by the third. In the case of a field-effect transistor, the current between the source and drain regions is controlled by adjusting the voltage on the gate. A model of an NMOS FET is shown in Fig. 4-1. When the gate voltage is zero, current

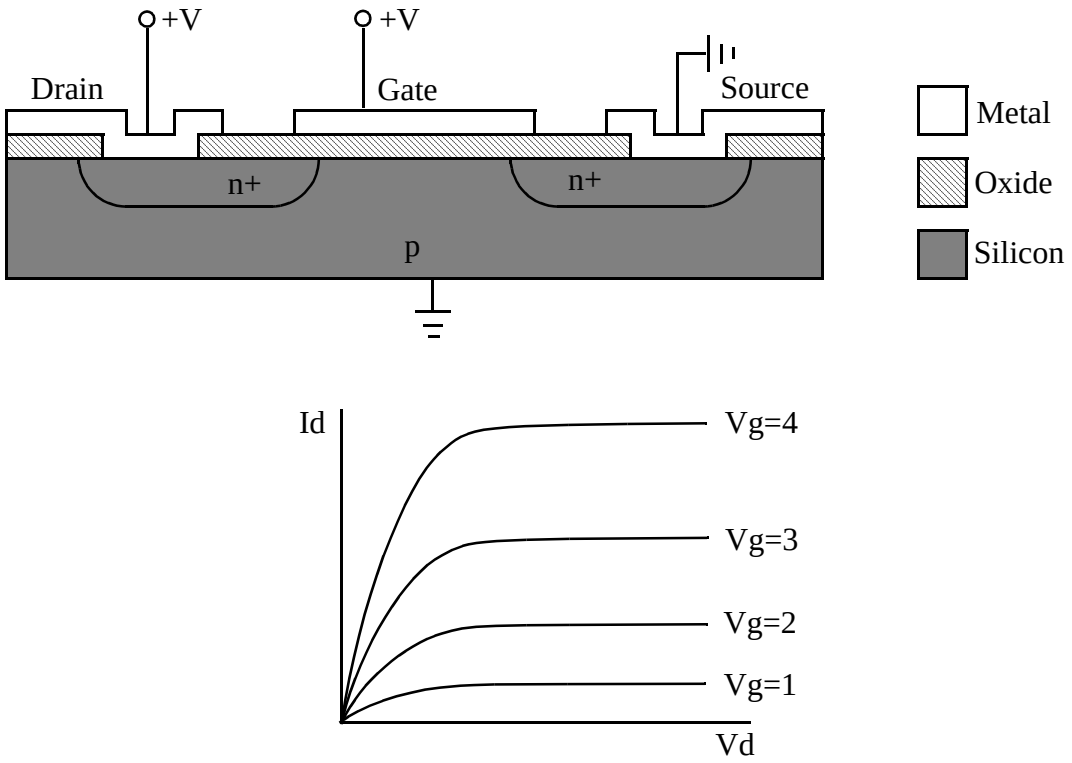


Figure 4-1. *Model of an NMOS transistor and the drain current vs. voltage as a function of the gate voltage.*

cannot flow from the source to the drain because the electrical pathway is an n-p-n junction. If, however, a positive voltage is applied to the gate relative to the substrate, positive charges accumulate on it. In response, negative carriers collect in the silicon layer. A thin layer of mobile electrons then connect the source and the drain, allowing current to flow between them. As the voltage on the drain is increased, the current rises until there is saturation of the channel. Even if the drain voltage is increased, there are no additional carriers to allow more current to flow. This can be seen in Figure 4-1 as the drain voltage-current curve becomes horizontal. A PMOS FET works in a similar manner except that a negative voltage is applied to the gate, which causes positive carriers to accumulate between the source and drain. The current in a PMOS device flows from the source to the drain, instead of drain to source as in an NMOS device.

Two important device characteristics for field effect transistors are the threshold

voltage, V_T, and the breakdown voltage. The threshold voltage is the minimum gate voltage that allows current to flow. As the gate voltage is increased, more electrons accumulate in the silicon layer and more current flows through the device. Even if there is no voltage applied to the gate, there is a limit to how much voltage can be applied between the source and drain before current will flow between them. This breakdown voltage is important because it is the maximum voltage that can be switched by the transistor. These two parameters are important because they tell us how well the transistors would perform as a buffer between a CMOS control chip and a high voltage solar cell. The threshold voltage needs to be lower than the maximum voltage output of the CMOS chip, which is typically 3.3 or 5 V, and the breakdown voltage is the maximum voltage that could be used to power an electrostatic actuator.

The amount of current which flows from the drain can be estimated for each of the two regions of operation. In the linear region, the current is given by Eq. (4-1),

$$I_d = \mu_n C_{ox} \frac{w}{L} (V_G - V_T - V_D/2) V_D \tag{4-1}$$

where μ_n is the average majority carrier mobility in the inversion layer, C_{ox} is the oxide capacitance per unit area and w and L are the width and length of the transistor, respectively. When the channel is saturated, the drain voltage can be estimated as the difference between the gate voltage and the threshold voltage, as in Eq. (4-2).

$$V_D(sat) \approx V_G - V_T \tag{4-2}$$

This leads to the drain current begin approximated by Eq. (4-3).

$$I_d(sat) \approx \mu_n C_{ox} \frac{w}{L} \frac{(V_G - V_T)^2}{2} \tag{4-3}$$

Once data has been taken for a given transistor, the data can be analyzed to extract some of the important device parameters. The oxide capacitance per unit area is estimated

from the geometry using Eq. (4-4).

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{4-4}$$

From the data and geometry, and using equations Eq. (4-3) and Eq. (4-4), it is then possible to estimate $\bar{\mu}_n$.

By finding the slope of the saturated regions of the i-v curves, it is possible to estimate the channel-length modulation, λ, which is given by Eq. (4-5).

$$\lambda = \frac{\left(\frac{\partial I_D}{\partial V_D}\right)_{sat}}{I_{d,\,sat}} \tag{4-5}$$

Finally, using Eq. (4-6), the maximum operating frequency, ω_t, is estimated from the channel transconductance, g_m, and the gate-to-source and gate-to-drain capacitances, C_{gs} and C_{gd}, respectively. The capacitances are estimated from the designed overlap between the gate and the source and drain regions and the modeled lateral diffusion of the implanted dopants.

$$\omega_t = \frac{g_m}{C_{gs} + C_{gd}} = \frac{2I_{D,\,sat}}{V_G - V_T} \cdot \frac{1}{C_{gs} + C_{gd}} \tag{4-6}$$

4.2.2 DESIGN OF THE FETS

4.2.2.1 FETS WITH METAL GATES

For the first version of solar cell and circuits process (Section 2.4.1.1), the NMOS FETs were fabricated using the process elements that had been designed for fabricating the high voltage solar cell arrays. This included metal gates of the same aluminum that was used for the collector lines and a gate oxide that was the same as the anti-reflective layer. The thickness of this oxide layer was typically between 1200 and 1400 A. The source and drain regions also used the same n+ implant and drive-in as the solar cells. For the second

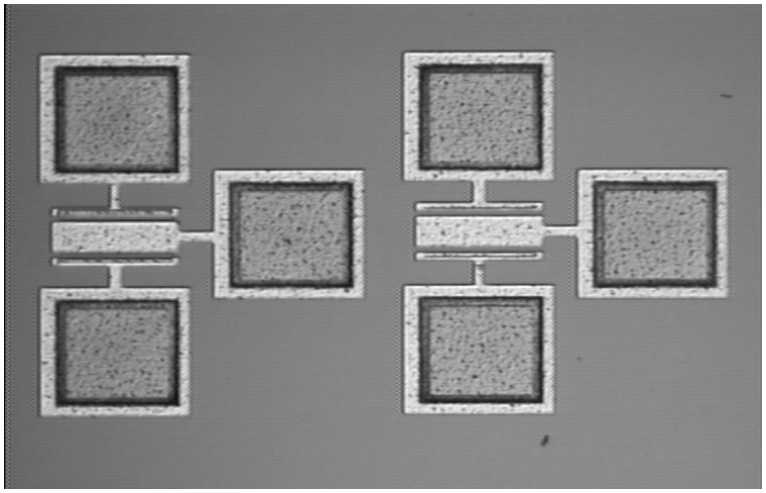


Figure 4-2. *Test field-effect transistors with L=30 μm and w=100 μm. The transistor on the left is an NMOS device and on the right is a PMOS device.*

version of the process (Section 2.4.1.2), the implant and drive-in parameters were modified slightly to allow the fabrication of both NMOS and PMOS devices. These FETs still used the anti-reflective oxide layer for the gate oxide and the metal for the gates.

Because the process was not optimized for the fabrication of the transistors, the design had to account for the subsequent limitations. To ensure that the edges of the source and drain regions were covered by the gate, a photolithographic overlap of 1 μm was used. In addition, the implanted dopants diffused about 1 μm laterally. The transistors were also quite large. This was done based on early test results which showed that the breakdown voltages of the NMOS transistors began to decrease as the channel length decreased below about 20 μm [41]. The transistor lengths ranged between 20 and 30 μm. The widths were either 50 or 100 μm for the basic FETs. A couple of test transistors are shown in Fig. 4-2. Where a high saturation current was desired, wider FETs were used which had an interdigitated design. The widest of these had a width of 1500 μm, as shown in Fig. 4-3. The interdigitated fingers require that electrical lines cross to make all necessary connections. Since only one metal layer is used for electrical connections, the cross-over is accomplished by simply connecting all of the source fingers to the substrate.

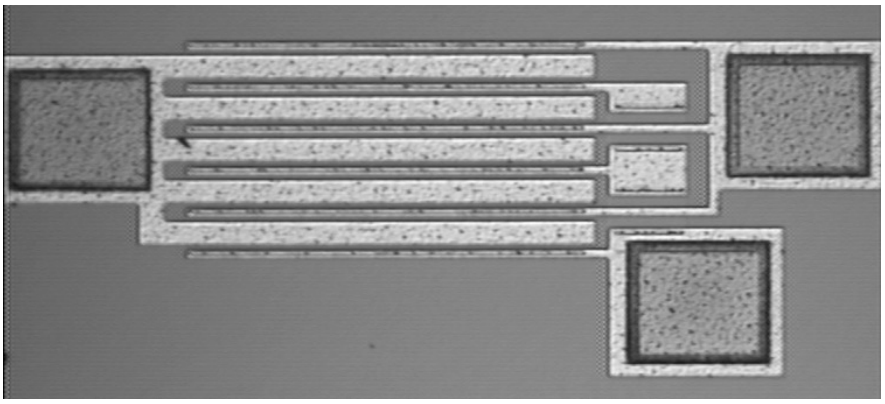


Figure 4-3. *A wide NMOS FET using an interdigitated design. The length is 20 μm and the width is 1500 μm.*

4.2.2.2 FETs WITH POLYSILICON GATES

The field-effect transistors fabricated with the third version of the process (Section 2.4.1.3) were considerably different from the previous versions. The changes were primarily due to the switch from metal to polysilicon for the gate material. Because the polysilicon gates were self-aligned, shorter gate lengths were feasible. The lengths used were 5 μm. The shorter gate lengths helped reduce the amount of area required for the circuit elements. The width of the gates was also reduced to 5 μm. Although the gate material switch did not affect this parameter, it was also done to reduce the circuit area. The final change was to the thickness of the gate oxide. Because the gate oxide thickness was no longer tied to the thickness of the anti-reflective coating for the solar cells, it could be selected for transistor performance. The thickness was therefore set to 1000 A.

4.2.3 RESULTS

The performance for the various fabricated field-effect transistors was measured using a Hewlett-Packard HP4145B Semiconductor Analyzer. Testing of the FETs consisted of sweeping the drain-source voltage for a number of gate voltages and measuring the

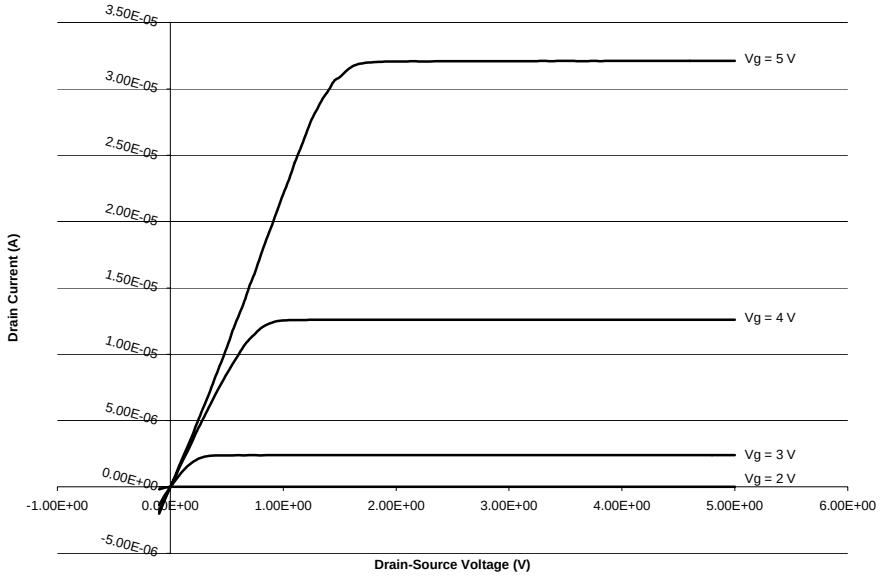


Figure 4-4. *Characteristics for an NMOS transistor with a gate length of 30* μm *and a width of* 100 μm*. This transistor was fabricated using version one of the process.*

resulting drain current. A plot of the data for a version one NMOS FET with a gate length of 30 μm and a width of 100 μm is shown in Fig. 4-4. The data was then analyzed to determine the threshold voltage for each of the transistors. This was done by selecting a drain-source voltage that was within the saturated region of the transistor curves and plotting the gate voltage verses the square root of the drain current, as shown in Fig. 4-5. The linear portion of the curve would then be extrapolated to find the x-axis intercept. The result was the threshold voltage for the transistor.

The transistors breakdown voltage would then be tested. This was done by setting the gate voltage to zero and ramping the drain-source voltage up until an abrupt jump in drain current was detected. The voltage where this occurred would be the breakdown voltage. The transistor would then be tested again to determine how the breakdown occurred. If the transistor continued to function normally, then the breakdown was due to nondestructive breakdown of the p-n diode between the drain and the bulk. If the

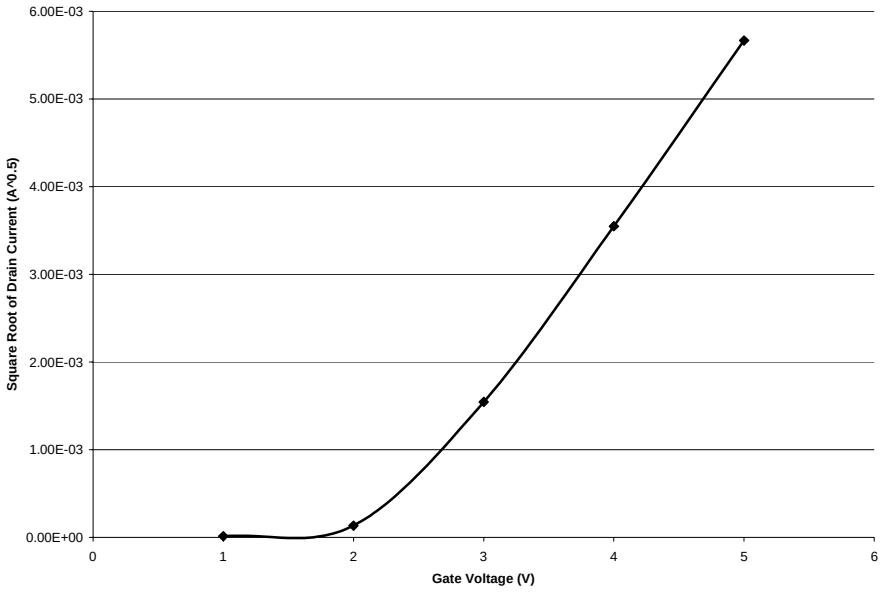


Figure 4-5. *Threshold voltage plot for transistor from Fig. 4-4. Extrapolation yields a V_T of 2.26 V.*

transistor stopped working, then the failure was catastrophic, caused by a breakdown of the gate oxide between the drain and the gate. Gate oxide breakdown was very rare and only occurred during testing of transistors from an early test run.

The results for the NMOS transistors from the first version of the process are summarized in Table 4-1. The data shows that both the threshold voltage and breakdown

Table 4-1. *NMOS Transistor results from Process Version One*

Length (μm)	Width (μm)	Threshold Voltage (V)	Breakdown Voltage (V)	C_{ox} (F/m^2)	μ_n (cm^2/V sec)	λ (1/V)	ω_t (rad/sec)
30	100	2.26	27.7	2.88E-4	3.78	2.22E-4	8.42E+6
20	1000	2.23	28.0	2.88E-4	47.6	2.53E-4	1.04E+8
20	1500	2.23	28.6	2.88E-4	68.0	2.74E-4	1.49E+8

voltage are consistent between devices of varying size. It also shows that these FETs would be well suited to the switching needs of this process. The threshold voltage is below both 3.3 V and 5 V, indicating that a standard foundry CMOS chip would be able to switch these transistors. The breakdown voltages are also sufficiently high to utilize high

voltage power to drive electrostatic actuators.

The results for both the NMOS and PMOS transistors from the second version of the process are summarized in Table 4-2. The first thing which to note is that the process

Table 4-2. *Transistor results from Process Version Two*

Type	Length (μm)	Width (μm)	Threshold Voltage (V)	Breakdown Voltage (V)	C_{ox} (F/m^2)	μ_n ($cm^2/V\ sec$)	λ (1/V)	ω_t (rad/sec)
NMOS	30	100	2.39	27.2	2.88E-4	0.47	-2.68E-3	1.08E+6
NMOS	20	1000	2.25	27.3	2.88E-4	5.86	-5.62E-3	1.29E+7
NMOS	20	1500	2.25	28.7	2.88E-4	9.27	-4.43E-3	2.04E+7
PMOS	20	50	-25.6	-8.3	2.88E-4	2.58	-8.23E-3	8.20E+5
PMOS	20	100	-25.4	-8.7	2.88E-4	3.09	-7.09E-3	1.07E+6
PMOS	30	50	-25.6	-8.4	2.88E-4	2.96	-3.87E-3	6.24E+5
PMOS	30	100	-25.7	-8.8	2.88E-4	2.52	-8.94E-3	4.94E+5

changes which were put in place to allow the formation of both NMOS and PMOS devices had very little effect on the performance of the NMOS devices. The threshold voltages and breakdown voltages are very similar to those from the first process version.

Unfortunately, the PMOS devices from this version are of very little utility. First, the difference in threshold voltages between the NMOS and PMOS devices is very large. Second, the threshold voltages for the PMOS devices are at a lower voltage than the breakdown voltages. This indicates that, although the devices do function, they could never be chained together with the source of some FETs being connected to the gates of other FETs.

Both of these problems can be traced back to the relatively high doping of the initial p-type silicon wafer. In order to create a well in which to make the PMOS devices, the n-implant had to be of a relatively high doping also. This highly doped n-type region required an excessively low gate voltage to invert it. The p+ implant to create the source and drain regions also had to be of an even higher doping level, leading to a decrease in

the breakdown voltage. This poor PMOS performance was one of the main driving factors in the development of the third version of the process. By starting with a lower doped p-type wafer, the threshold voltages and breakdown voltages could be controlled better.

A puzzling aspect of the data listed in Table 4-2 is that the channel length modulation values for all of the transistors from this process are negative. The drain current actually decreased slightly as V_{DS} was increased. This type of behavior is not typical for FETs fabricated on silicon wafers, but it is seen in gallium arsenide devices. Although it is not entirely clear why it happened on these devices, it may have been caused by the higher voltage increasing the energy level of some of the carriers to a level that had a lower mobility. This is the mechanism that causes the same behavior in gallium arsenide circuits. The extremely low mobilities for the devices may have also contributed. It is possible that in typical devices with shorter gate lengths, the factors which cause the slope to be positive are much more dominant than those that cause it to be negative, so it is not seen in regular practice. The fact that the devices fabricated in this process have longer gate lengths and higher channel doping may allow this effect to be seen.

The lighter doping of the wafer used for the third process version led to a problem which caused the NMOS devices from the third process to leak excessively. This can be seen in a plot of transistor performance, shown in Fig. 4-6. It is still possible to estimate the threshold voltage of the device by subtracting out the leakage current at zero gate voltage from the other curves, as shown in Fig. 4-7. The resulting threshold voltage was approximately 1.3 V. It was found through an analysis of the devices that there was a very thin phosphorus doped layer on all p- areas of the wafer. This thin layer provided a leakage path for current to flow from the drain to the source of the transistors around the end of the polysilicon gates. This layer did not affect any of the other devices on the wafer. This contamination, which most likely occurred during the drive-in step, only manifested itself in the third process version because the substrate doping was low

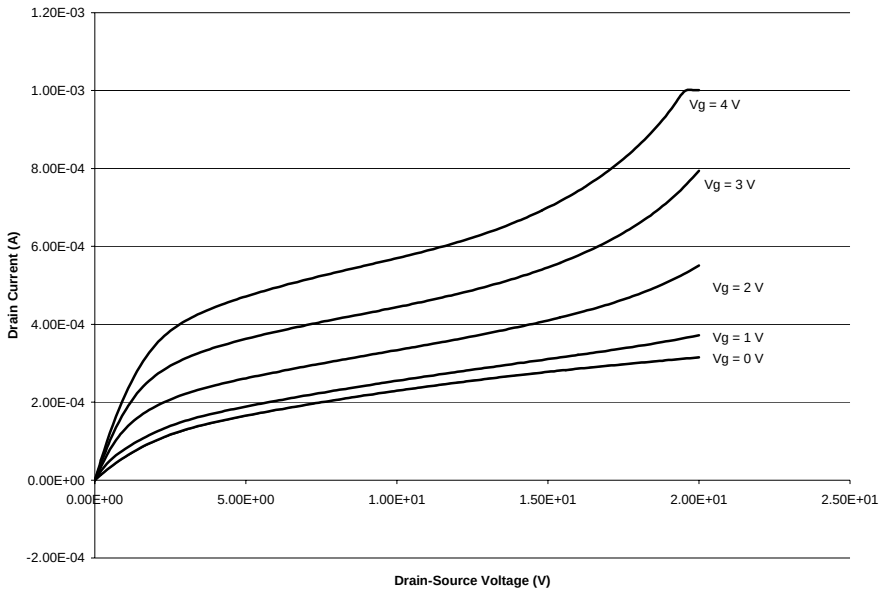


Figure 4-6. *Characteristics for an NMOS transistor with a gate length and width of 5 μm. This transistor was fabricated using version three of the process. Leakage at zero gate voltage is clearly evident.*

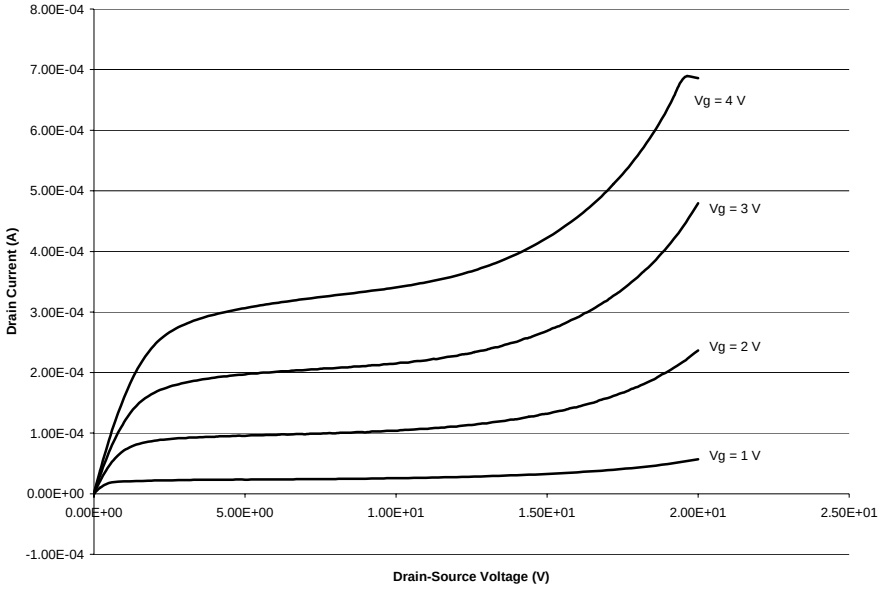


Figure 4-7. *Modified data for transistor from Fig. 4-6. The data for the zero gate voltage line has been subtracted from the other curves.*

enough; the substrate doping in the other processes was high enough to not be switched from p-type to n-type. The problem can be easily fixed by placing either a p+ region or a back-filled isolation trench around the transistors such that it passes under both ends of the gate. This eliminates the leakage path around the end of the gate.

The transistor results for the third process version are summarized in Table 4-3. It was still possible to determine the breakdown voltage of the NMOS devices even with the leakage by increasing the drain-to-source voltage and looking for an abrupt increase in current. The PMOS devices worked well with a threshold voltage which is much more compatible with the NMOS devices and a breakdown voltage which is sufficiently high to be useful in this process.

Table 4-3. *Transistor results from Process Version Three*

Type	Length (μm)	Width (μm)	Threshold Voltage (V)	Breakdown Voltage (V)
NMOS	5	5	1.3	20
PMOS	5	5	-4.3	-15

4.3 BIPOLAR JUNCTION TRANSISTORS

4.3.1 BASICS OF BJT OPERATION

In order to understand the basics of how a p-n-p bipolar junction transistor functions, it is useful to go back and reconsider the p-n junction used as a solar cell (Section 3.2). If the p-n junction is operated in the third quadrant instead of the fourth, it is useful as a photodetector instead of as a solar cell. In this mode, the current is a function of the amount of light impinging upon the cell, as shown in Fig. 4-8. The relationship is fairly linear and does not vary much with changes to the biasing voltage. The illumination acts as a hole injector which causes current to flow through the device. More light results in more holes which leads to more current.

The behavior of the device will be similar if we replace the light induced hole injection

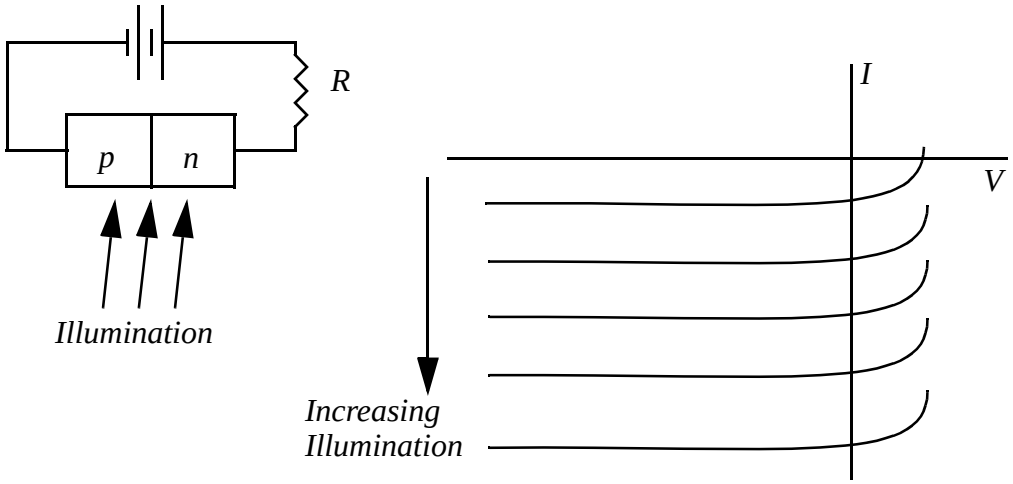


Figure 4-8. *Behavior of a reverse-biased p-n junction with illumination generating holes.*

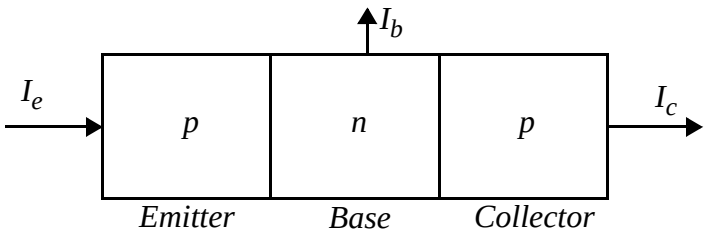


Figure 4-9. *A p-n-p bipolar junction transistor.*

with some other means of injecting holes. This can be done with a forward biased p-n junction. If we connect the forward biased p-n junction with the reverse biased p-n junction by sharing the n regions, the result is a p-n-p bipolar junction transistor, as shown in Fig. 4-9. The three terminals of the device are called the emitter, the base and the collector. The emitter is so named because the injected holes come from here and are then collected in the collector.

This device is useful because an amplification occurs from the base current, I_b, to the collector current, I_c. The amount of amplification is quantified by the base-to-collector

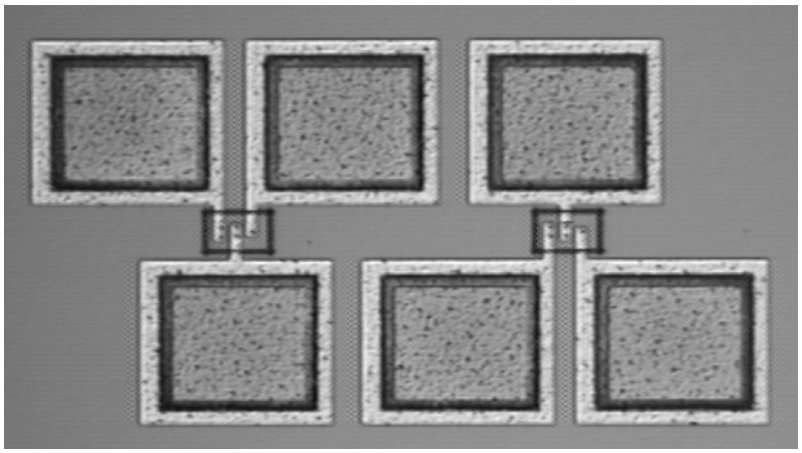


Figure 4-10. *Two designs of BJTs fabricated. Design on the right uses collector contacts on both sides of the n- well.*

current amplification factor, β, which is defined in Eq. (4-7).

$$\beta \equiv \frac{I_c}{I_b} \tag{4-7}$$

4.3.2 DESIGN OF THE BJTS

The BJTs fabricated in this process use the p-type substrate as the collector, the n- well as the base and a p+ region inside the well as the emitter. Highly doped regions were used underneath all metal contacts to ensure good ohmic contact between the metal and the silicon. Two different designs were fabricated, both shown in Fig. 4-10. The only difference between the two is that the design on the right has contacts to the collector on both sides of the emitter whereas the other only has a contact on one side.

4.3.3 RESULTS

The BJTs were tested with a Hewlett-Packard HP4145B Semiconductor Analyzer. The voltage between the collector and the emitter would be swept and the resulting collector current would be measured for a number of base currents. The data from one of these tests is shown in Fig. 4-11. The data is then analyzed by dividing the measured

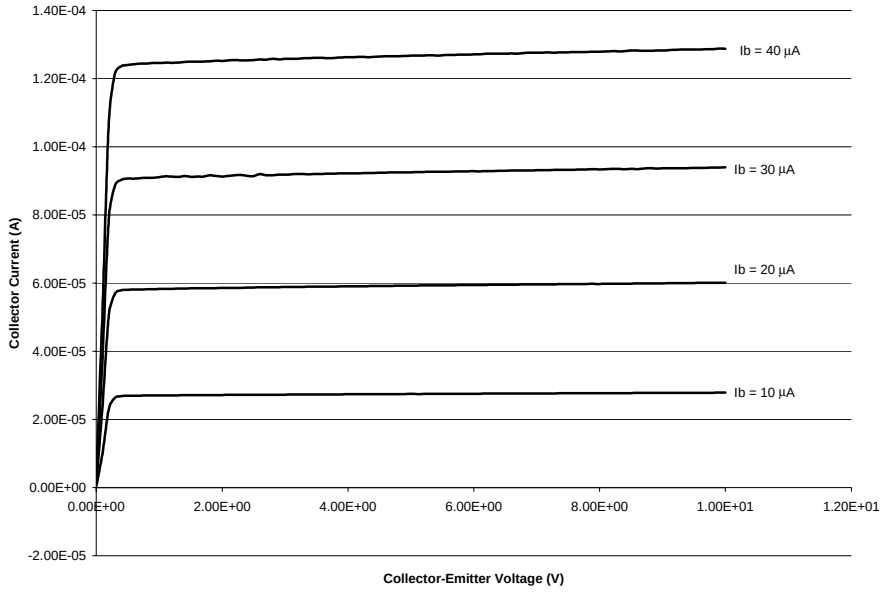


Figure 4-11. *Performance of fabricated BJT showing collector current as a function of collector-emitter voltage and base current.*

collector currents by the associated base currents to determine β, which is given by Eq. (4-7). This result is plotted in Fig. 4-12. Although the β varies slightly depending on the level of collector-emitter voltage and base current, it is approximately three. Both BJT designs which were fabricated had very similar results with $\beta \cong 3$.

The data was further analyzed to find the Early voltage. If the linear portions of the data curves in Fig. 4-11 are extended to the left, the voltage where they cross the x-axis is the Early voltage. The fabricated BJTs had Early voltages of approximately 300 V

4.4 SWITCHES

Because the primary purpose for including circuitry in this process is to provide a means of controlling the flow of power between the solar cell arrays and the MEMS structures, it is important to present devices that fulfill this role. Based on the performance of the various transistors presented in this chapter, the switches discussed here are based on NMOS transistors only.

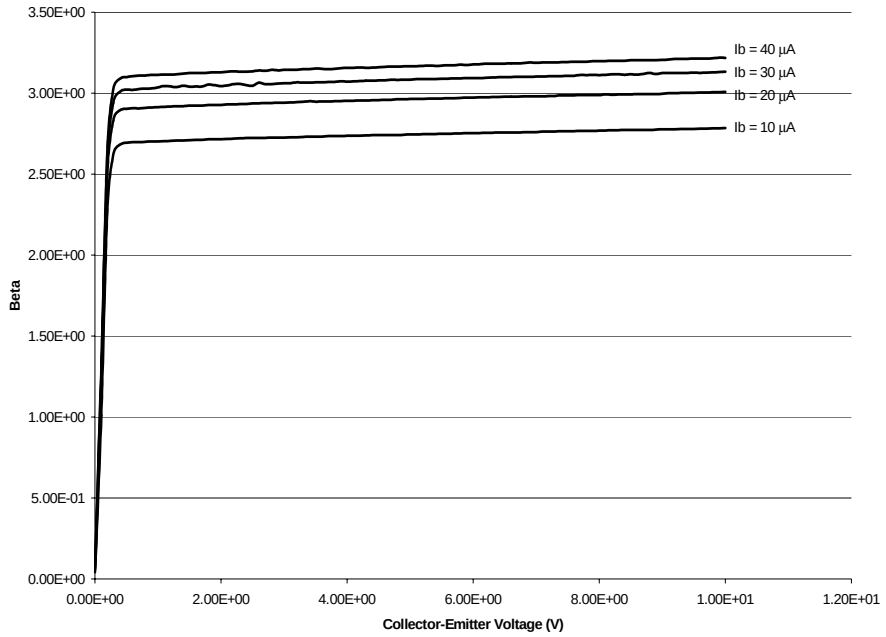


Figure 4-12. *Calculated* β *from BJT data in Fig. 4-11.*

4.4.1 DESIGN OF THE SWITCHES

The best performing high voltage buffer is just an NMOS inverter. It consists of an NMOS transistor with a pull-up resistor, as shown in Fig. 4-13. The transistor used an interdigitated finger design with a gate length of 30 µm and a gate width of 1200 µm. The resistor used the n- implant which had a resistivity of approximately 350 Ω/square. Given a length of approximately 2500 squares, the total resistance was approximately 875 kΩ. The inverter is used as a switch in the integrated process by having a solar cell array provide the power for the inverter. An external signal provides the input and the output is connected to the electrostatic actuator. When no input signal is present, the output is high, resulting in the attached device being actuated. When an input is provided, the output drops to ground and the actuator is released.

The second buffer design, shown in Fig. 4-14, utilized two NMOS transistors

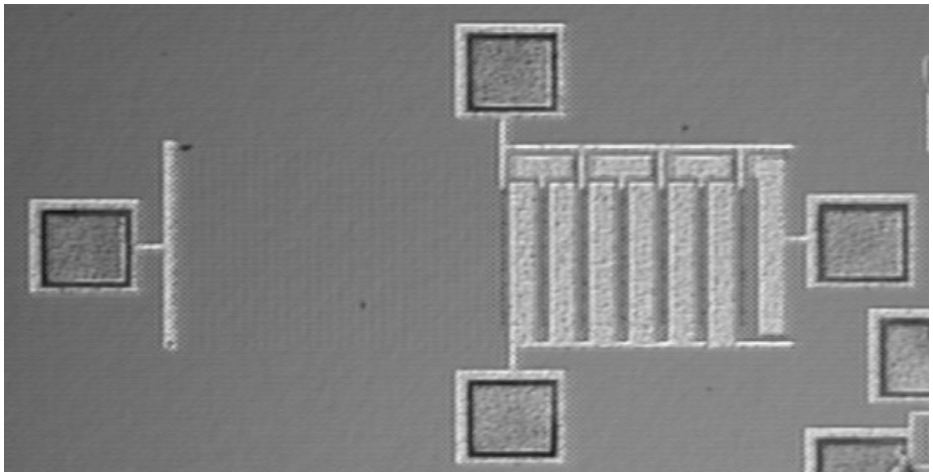


Figure 4-13. *Simple buffer consisting of an NMOS transistor with a pull-up resistor.*

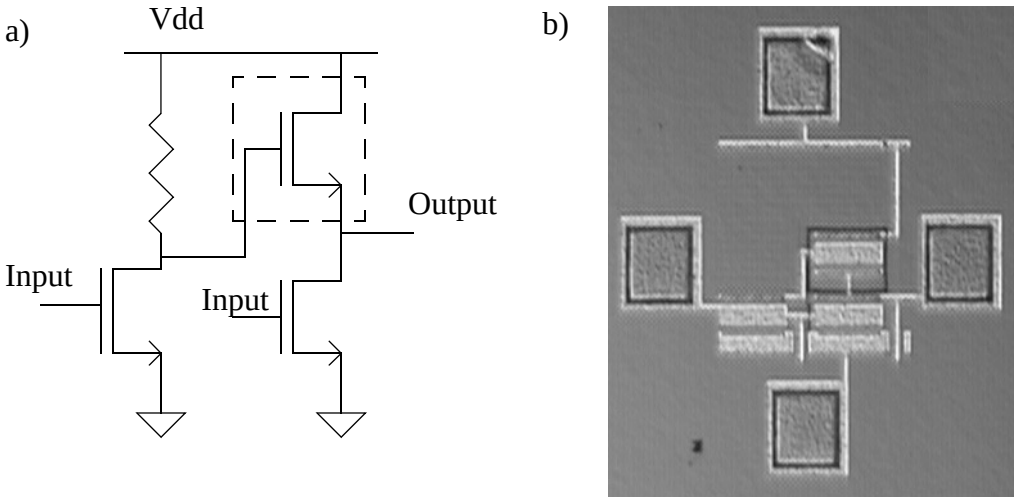


Figure 4-14. *Second buffer design. Schematic is shown in a) and actual fabricated device is shown in b). Dotted line in a) indicates a back-filled isolation trench.*

connected to the output. One transistor connected the output to the ground line and the other one connected it to the supply line. The latter supply-line transistor was isolated from the rest of the devices by placing a back-filled isolation trench around it. An inverter

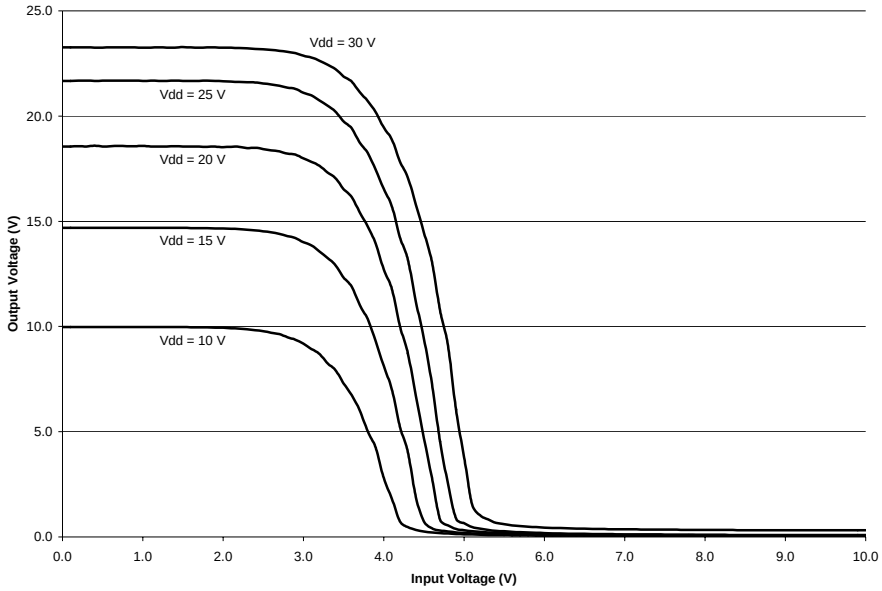


Figure 4-15. *Device characteristics for the NMOS inverter buffer shown in Fig. 4-13.*

similar to the first buffer design, which used an NMOS transistor with a pull-up resistor, was used to switch the input signal for the supply-line transistor. The input was then connected to both the gate of the ground-line transistor and the input to the traditional inverter such that when the input was low, the ground line transistor would be open and the inverter output would be high, turning on the supply line transistor. When the input was high, the inverter output would be grounded and the ground-line transistor would be on.

4.4.2 RESULTS

The performance of the buffers was tested with a Hewlett-Packard HP4145B Semiconductor Analyzer. Power was supplied to the inverter, the input signal was swept from zero to ten volts and the output voltage was measured. The data for the first buffer design are plotted in Fig. 4-15.

When the input voltage is zero, a decrease in output voltage is evident as the supply

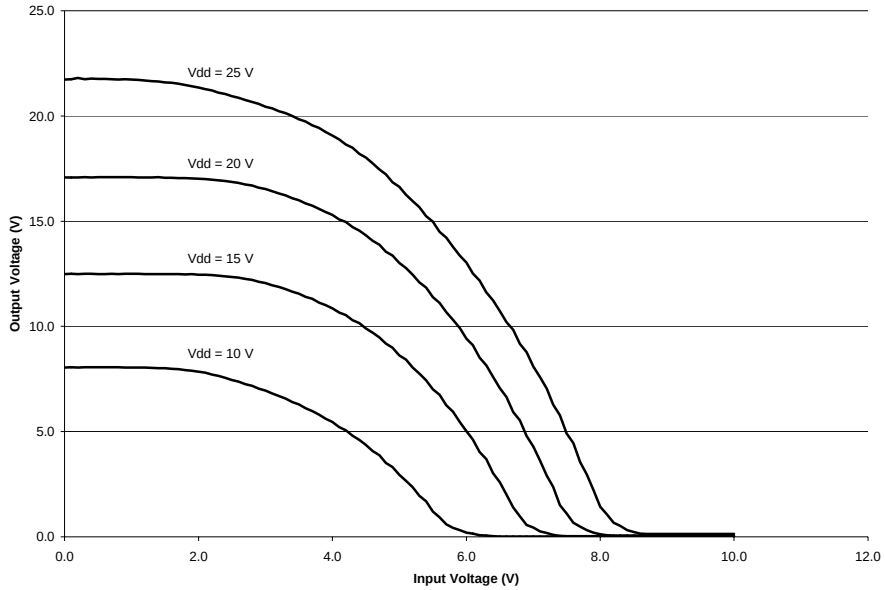


Figure 4-16. *Device characteristics for second buffer design, shown in Fig. 4-14.*

voltage, V_{dd}, is increased. This can be attributed to leakage in the transistor, which causes the output voltage to dip. As the supply voltage gets closer to the breakdown voltage of the transistor, the benefit in increasing the supply voltage diminishes.

When an input is provided, except for a supply voltage of 30 V, which is above the breakdown voltage of the transistor, all curves have switched at an input voltage of less than 5 V. This indicates that a 5 V CMOS foundry control chip would be able to control the flow of power to the electrostatic actuators. The output voltage in the off state is also low with a value less than 200 mV for a supply of voltage of 25 V. These results indicate that this switch is up to the task of providing switching for this integrated process.

The data for the second buffer design is shown in Fig. 4-16. The performance is not as good as the first design as the switching does not happen as abruptly and requires a higher input voltage.

5. SYSTEM COMPONENT 3: ELECTROSTATIC ACTUATORS

The integrated SOI process for solar-powered MEMS is capable of producing a wide range of electrostatic sensors and actuators. This includes single mask structures which have a uniform height or double mask structures which use a two stage STS etch for varying heights, and actuators that move in-plane or out-of-plane. Devices which have been demonstrated include a simple comb drive actuator, inch worm motors, corner cube reflector mirrors and an accelerometer.

5.1 SINGLE MASK STRUCTURES

A common method for making electrostatic actuators on an SOI wafer is to perform a single STS etch through the device layer followed by a timed HF release of the bonding oxide layer. By making the anchor structures much larger than the moving structures, they will remain attached while the rest will be free to move. Different parts can also be easily isolated by removing all of the silicon which connects them together. This technique has been widely used to create a number of MEMS devices.

To realize the full potential of integrating these devices with the integrated solar powered MEMS process, the removal of silicon to create isolation must be replaced with the use of back-filled isolation trenches. This allows metal lines to cross the trenches, eliminating the need to wirebond connections to the actuators.

In this chapter, two of the fabricated devices, inch worm motors and corner cube reflectors, will be discussed in detail. These were chosen because the associated lessons learned are useful when designing and modifying other devices for use with this process.

5.1.1 INCH WORM MOTOR

5.1.1.1 DESIGN

The primary device which was used to demonstrate the capabilities of the integrated SOI process for solar powered MEMS was the inch worm motor. This motor, which was originally designed and demonstrated by Kruglick and Yeh [42], is capable of moving a shuttle a large distance even though the gap closing actuators which drive it only move 2 μm at a time. This is accomplished by having two actuator modules which each have a clutch stage and a drive stage. The clutch stage of the first module engages the shuttle and the drive stage moves it 2 μm. The clutch stage of the second module then engages the shuttle, the first module releases and the second drive actuator moves it another 2 μm. This cycle is performed repeatedly until the desired shuttle motion is achieved. The ability to generate large displacements from an electrostatic actuator makes this motor especially well suited to microrobot applications. The shuttle would be attached to a tendon which would move an articulated leg.

The design for the inch worm motor which was used as a model for this process, shown in Fig. 5-1, is fabricated utilizing a single mask for the STS etch and a subsequent timed release step. Integrating this actuator into the solar powered MEMS process required a fair amount of modification. This was necessary because the flexures in the original design surrounded the anchors where the electrical inputs must be applied to run the motor. Although this allowed a very compact design, it required the use of probes or wirebonds for electrical connections. To realize the benefit of having the motors prewired to the rest of the device, the flexures for the drive stage had to be unfolded, as shown in Fig. 5-2. The amount of separation between the drive stage flexures affects the rotational stability, so two different designs were fabricated. The first had the same amount of separation as the original design while the second had a reduced separation. The area required for the motor is clearly affected by the flexure separation, so minimizing this

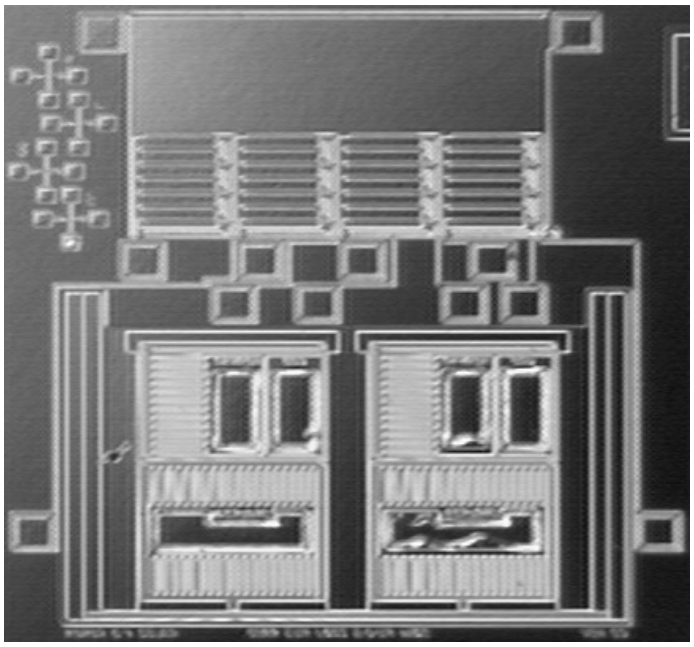


Figure 5-1. *Original design for the inch worm motor, fabricated in this process with a buffer positioned above it.*

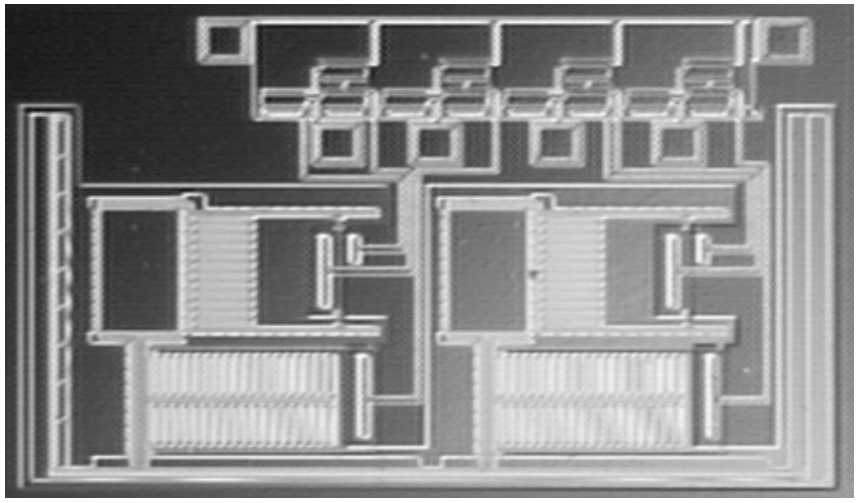


Figure 5-2. *Modified inch worm motors to allow prewiring of the contacts with an attached buffer array.*

while still providing sufficient stability is important.

Because each complete inch worm motor takes up a large amount of die space, smaller

a) b)

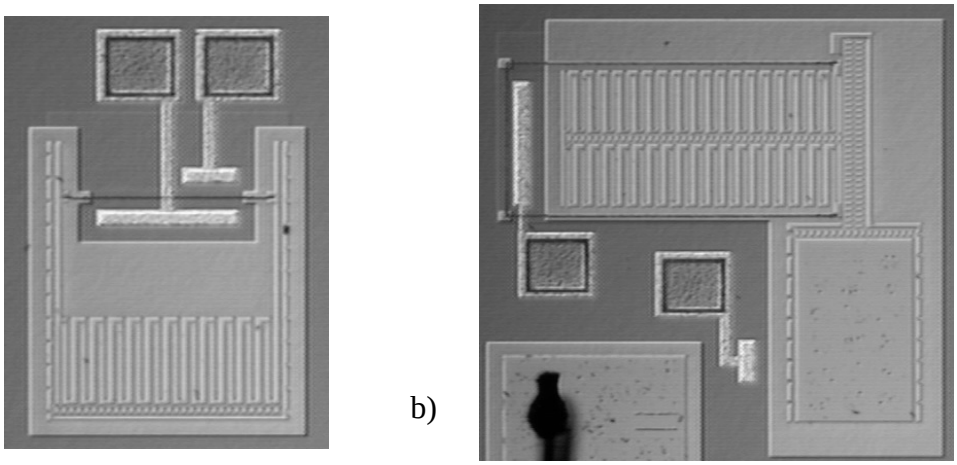


Figure 5-3. *Test devices for the two stages of the modified inch worm motors. Clutch stage is shown (a) and the drive stage is shown in (b).*

test actuators were needed. This was accomplished by fabricating the individual stages of the inch worm motor. These are shown in Fig. 5-3.

5.1.1.2 RESULTS

When voltage was applied to the test structures, it was discovered that the clutch stage structures could not be actuated. The voltage needed to actuate them was higher than what the metal lines connecting it to the contact pads could handle. The metal line connected to the drive fingers would short out at about 26 V. This is about the same voltage expected to pull-in the actuator.

The drive actuators, which typically require a lower actuation voltage, did not exhibit this problem. They would consistently pull-in at about 16 V. There was also no noticeable difference in the performance of the two versions of the drive actuators; the difference in separation between the flexures did not have any observed effect on performance.

The model inch worm design did not have these problems because the contact pads are completely isolated through the DRIE etch of the device layer. It was therefore possible to

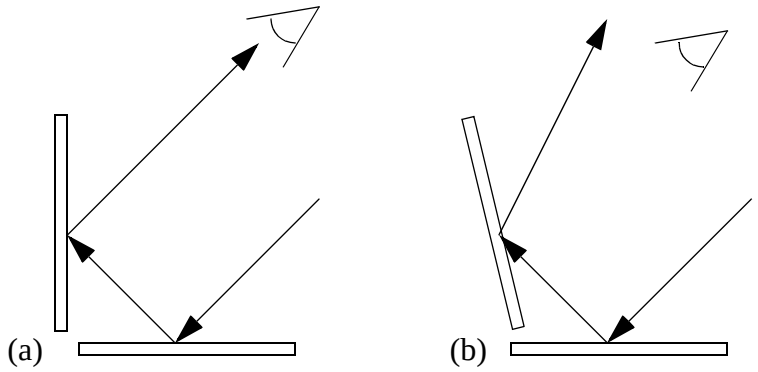


Figure 5-4. *Two dimension representation of how a corner cube reflector can be used to communicate optically.*

actuate both the clutch and drive stages of the model device. Because the clutch stages of the modified designs could not be driven, though, it was not possible to run them as complete devices and compare the overall performance differences.

5.1.2 CORNER CUBE REFLECTOR MIRROR

5.1.2.1 DESIGN

Another MEMS actuator which has been demonstrated is the actuated mirror of a corner cube reflector. This actuator was based on previous research and Zhou [43]. A corner cube reflector uses three orthogonal mirrors to reflect light back to a distant light source. If one of the mirrors is rotated so that it is no longer orthogonal with the other two, then the light will not return back to the source. Alternating between these two states allows digital communication with the light source.

A two dimensional representation of this is shown in Fig. 5-4. In Fig. 5-4a, the two mirrors are orthogonal, so the light is reflected back in the same direction with a slight offset. In Fig. 5-4b, the second mirror has been rotated, so that the reflected light does not return to the source.

Using a corner cube reflector allows an autonomous MEMS device to communicate optically over long distances without generating the light on board. This greatly reduces

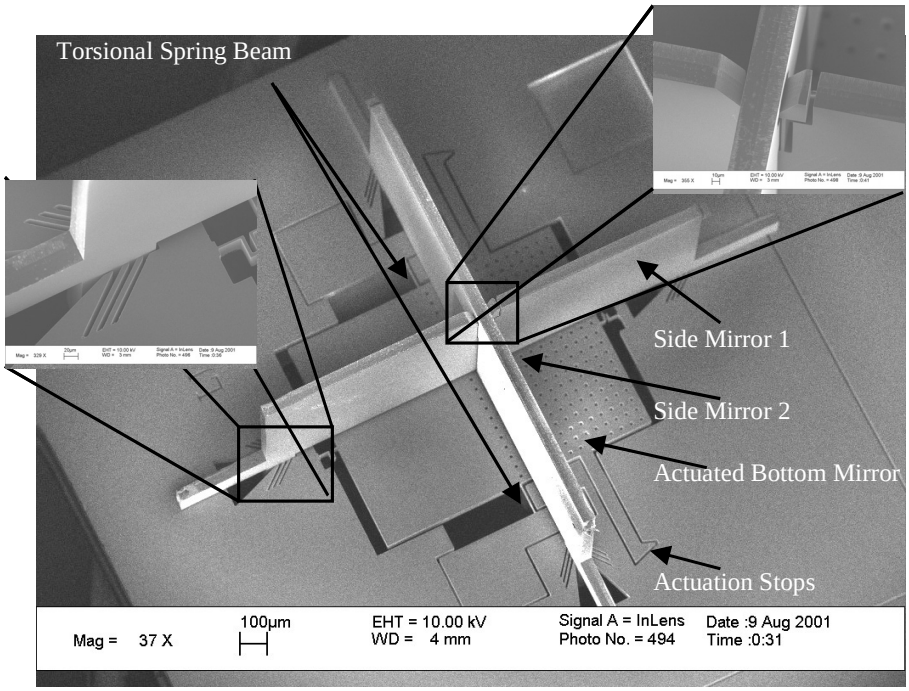


Figure 5-5. *SEM picture of an assembled corner cube reflector fabricated in the previous, non-integrated process (from Zhou [43]).*

the devices power requirements.

The model design for the CCR, shown in Fig. 5-5, used an SOI wafer with a device layer thickness of 50 µm. The actuated mirror, fabricated in the device layer, consisted of a square piece of silicon, suspended at the center of two opposite sides with torsional flexures. It was created by doing a single mask STS etch through the device layer. After releasing the device by etching the bonding oxide layer below the mirror, the mirror was rotated about the two flexures such that one side of the mirror pulled down toward the handle wafer and the other side rose up above it. It was actuated in this way by applying an electrical potential between the device and the handle layers.

In order for the mirror to tilt when the voltage was applied, the handle wafer had to be removed from underneath one side of the mirror. This was accomplished by doing another single mask STS etch of the handle layer. Etching the handle layer was also necessary to

create two blocks of silicon which were electrically isolated from the rest of the handle layer. These were used as actuator stops for the mirror to keep it from touching the energized part of the handle layer and creating a short.

Making the design compatible with the integrated solar-powered MEMS process required a considerable amount of modification but the result demonstrates how the back-filled isolation trenches allow a number of interesting design solutions. The primary element which required modification was the hole in the handle wafer below the unactuated side of the mirror. A way was needed to apply a potential to only one half of the mirror to allow actuation while also providing a safe actuator stop when the mirror reached the end of its travel.

This was accomplished by dividing the mirror into two sections with a back-filled isolation trench. The two sections, which could be maintained at different electrical potentials, were each connected electrically through one of the torsional flexures. The first section, which comprised the majority of the side of the mirror which would be pulled down during actuation, could have a variable electrical potential applied to it. This allowed it to be selectively attracted to the handle layer, which was always maintained at ground. The other portion, which was also maintained at ground, comprised the back half and the front edge of the mirror. Because the back half of the mirror was always at the same potential as the handle layer, it would not be attracted to it. The front edge included two pointed stops which were the first part of the mirror to touch the handle layer at the full amount of actuation, eliminating the possibility of shorting. Although the actuation stops in the fabricated device were connected to the back half of the mirror, this is not necessary. It would be sufficient to simply isolate them from the rest of the mirror, as any charge that might build up would be released into the handle wafer when it touched down.

When the actuation stops touch down, a bending moment is applied to the plate. A back-filled isolation trench that ran parallel to the mirror's axis of rotation would be placed under tension when this happened. Brosnihan had previously found that the

structural integrity of the back-filled isolation trenches was very good [30]. By connecting the base of a long beam to a straight, back-filled isolation trench and deflecting the beam laterally, he determined that the fracture stress of the joint was greater than 2.28 GPa. He also found that by placing bends in the path of the trenches, the strength could be increased to a point where the single crystal silicon would fracture before the back-filled isolation trench would fail. Therefore, to ensure that the mechanical strength would be sufficient to hold the mirror together, notches were placed along the path near the front edge. This created a section of the back-filled isolation trench that ran perpendicular to the axis of rotation, which would be under shear instead of tension when the stops touched down. These would then be less likely to fail, providing a more robust design.

5.1.2.2 RESULTS

In comparing the performance of the CCR mirrors fabricated in this process to those that have been previously fabricated [43], two important differences arise. They are an improvement in the settling time when the mirror is switched between the two positions and a degradation in the optical performance of the mirrors.

The settling time of the mirrors from this process was found to be significantly shorter when compared to mirrors from the previous process used. When comparing mirrors of similar size, the Q was reduced from about two for the earlier process to only one half for this process. A Q of only one half indicates that the mirror was critically damped. The improvement can be attributed to an increase in the amount of squeeze film damping on the mirror. In the earlier process, the handle wafer was removed from underneath one half of the mirror to allow the electrical driving force to only be applied to one side, causing the desired rotation. This resulted in only one half of the mirror feeling damping forces after switching. In this process, however, the handle wafer was present underneath the entire mirror, so the amount of damping was greater.

The optical performance of the mirror was degraded for two reasons. To limit the

amount of time needed to release the mirrors and maintain a relatively constant etch time for all devices included on the design, etch release holes were placed throughout the mirror at a spacing of 10 μm. These etch holes mar the surface of the mirror and scatter some of the interrogating light, which reduces the strength of the return light signal. If no other structures are negatively affected by having a longer release etch in hydrofluoric acid, then the number of etch holes can be reduced or they can be eliminated altogether.

A thin layer of gold is typically sputtered onto the surface of the mirror to improve its optical properties. This improves the reflectance from only 28% for bare silicon to 99% with a gold coating. When the mirror is fabricated separately, it is simple to sputter the gold layer over the entire mirror structure. If the mirror is integrated with solar cells and circuits, however, the gold would have to be masked so that it did not cover the solar cells or short out any of the electrical lines. A layer of gold also could not completely cover the mirror because it would provide an electrical short between the two halves of the mirror, which are at different potentials. For these reasons, gold was not used on the mirrors fabricated with this process. It was, however, applied to the other two, non-moving mirrors of the corner cube reflector such that only one of the three reflections had a significant reduction in signal.

6. COMPONENT INTEGRATION

Because all three components of this process, the high voltage solar cell arrays, the high voltage circuitry and the electrostatic actuators, are compatible with the entire process, integration is simple to achieve. Complete devices which utilize any or all of these elements can combined together into prewired, fully integrated devices.

In this chapter, the integration scheme for the fabricated devices will be presented and the successful integration of a demonstrated device will be described.

6.1 INTEGRATION SCHEME FOR FABRICATED DEVICES

Although fully integrated devices can be easily made in this process, the amount of area required for each of these would be considerable. Duplicating high voltage solar cell arrays for each device would consume most of the available die area and would severely limit the number of device variations. For this reason, a modular approach was taken to the layout with a large, configurable solar cell array taking up one half of the die and a number of integrated buffers and actuators taking up the other half. A picture of the layout is shown in Fig. 6-1. This arrangement allows one solar array to power all of the devices on the die. Additionally, devices can be selectively attached or disconnected such that a nonworking devices do not keep other devices from working properly.

The configurable solar array contains 200 individual solar cells. The cells are grouped into 10 arrays with 20 cells each. The target output voltage of each of these arrays is 10 V. Wire bond pads are situated at the base of each of these arrays to facilitate wiring them to each other. The arrays on both ends have pads at each cell to allow a finer tuning of the output voltage, if it is required. With this arrangement, any output voltage from 0.5 V to ~100 V can be generated.

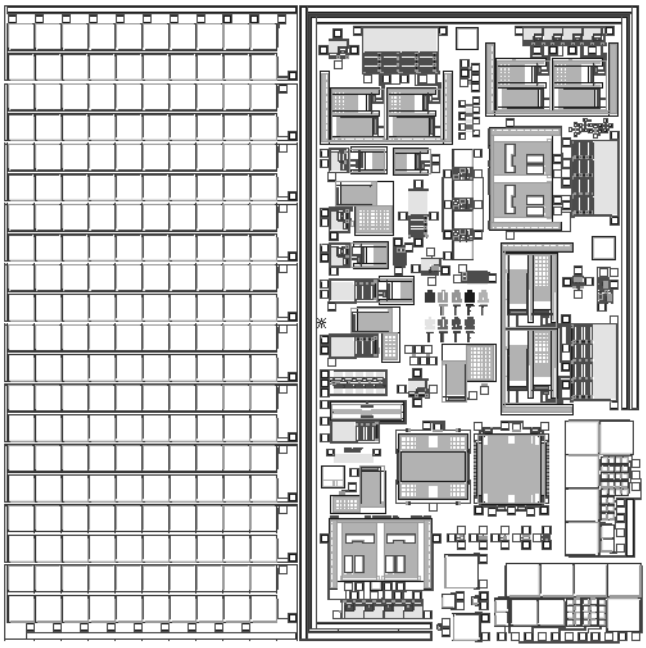


Figure 6-1. *Layout for devices fabricated in the integrated SOI process. Configurable solar cell arrays are on the left hand side of the die and the integrated buffers and actuators are on the right.*

The integrated buffers and actuators on the right hand side of the die are surrounded by two power busses. The outer line is isolated from the rest of the chip by a back-filled isolation trench and is used as the high voltage supply line for the devices. The inner line is the ground line and includes contacts to the substrate along its length. Just inside the power lines are three contact holes to the handle wafer which are etched through the device layer during the structures etch. These provide a convenient location to wire bond the ground line to the handle wafer to prevent the moving structures from being pulled down the substrate.

The buffers are arranged such that their ground and supply pads are next to the power busses for easy connection, again with wire bonding. Once the devices have been wired up, the only necessary external connections are for the control signal to turn the buffers on

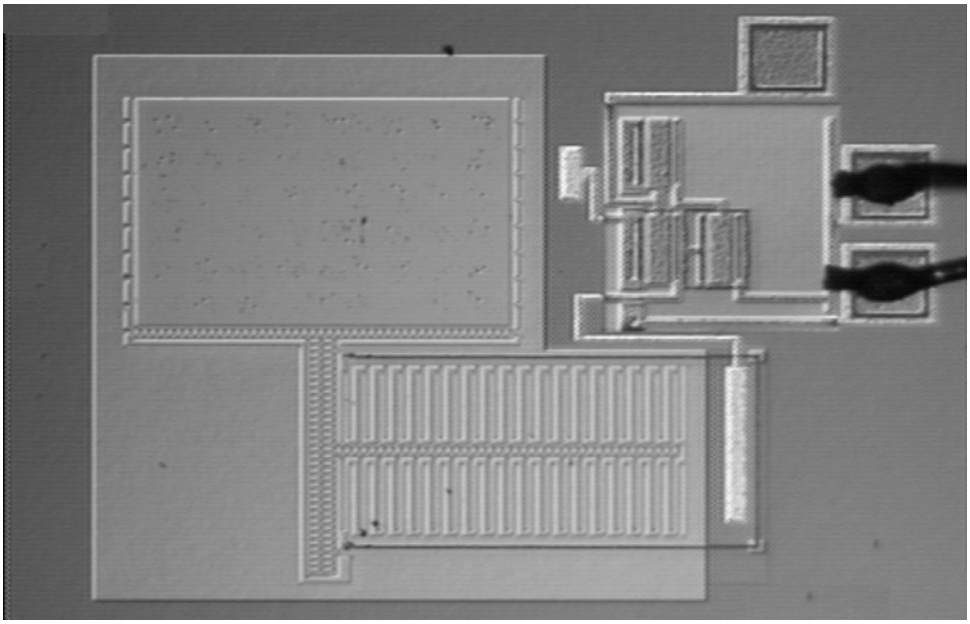


Figure 6-2. *Integrated buffer and motor which was used to demonstrate a fully integrated device. Wire bonds on the right connect the device to the power lines from the solar cell arrays.*

and off.

6.2 DEMONSTRATED INTEGRATED DEVICES

The successful integration of a complete device fabricated in this process has been demonstrated. The device was powered by five arrays of 40 solar cells each wired in parallel. The device included the second buffer design, described in Section 4.4.1, and the test drive actuator for the modified inch worm motor. The integrated buffer and actuator is shown in Fig. 6-2. All three components were on the same die and were connected together through wire bonds. The wire bonds connecting the power and ground of the buffer to the power busses (not visible to the right) can be seen in Fig. 6-2.

The solar cells were illuminated by a halogen lamp and were generating approximately 15 V. An external voltage was applied to the input pad of the buffer to

release the actuator. When the input voltage was zero, the actuator was pulled in to the stops. When the input voltage was increased to approximately 4.5 V, the actuator was completely released and in its static position.

The layout also included a pairing of the first buffer design and the same drive actuator. The expectation based on the buffer results in Section 4.4.2 was that this combination would perform even better. Unfortunately, a mask error over the transistor of the buffer created a short between the output and the ground.

7. CONCLUSIONS

A process has been developed for the fabrication of integrated devices consisting of high voltage solar cell arrays, electrostatic actuators and high voltage circuits on an SOI wafer. The intended use for this process is the fabrication of autonomous microsystems, such as microrobots and autonomous nodes for distributed sensor networks. The proposed system architecture for these devices includes two chips. The chip fabricated using the process presented here includes solar cell arrays for power generation and high aspect ratio MEMS devices for sensing and actuating. High voltage buffers allow a standard CMOS chip to control the flow of power between the solar cell arrays and the MEMS devices.

The process uses back-filled isolation trenches to allow a number of solar cells to be wired in series so that high voltage outputs can be generated. They also enable the fabrication of electrostatic sensors and actuators that have electrically isolated yet mechanically connected electrodes. This facilitates the wiring of the MEMS devices to the other components within the process, eliminating the need to wire bond them.

The process consists of four stages. The first stage is the fabrication of the SOI wafers. A highly doped region is implanted into the device wafer before bonding to create a back surface field at the interface of the device layer and the bonding oxide layer. This back surface field improves the efficiency of the solar cells. The second stage involves etching isolation trenches through the device layer and filling them with a thin liner of silicon nitride followed by undoped polysilicon. Removal of the back-fill materials from the surface of the wafer reveals an SOI device layer with isolated islands of silicon. The solar cells and circuits are fabricated in the third stage of the process. Three ion implantations are used to introduce dopants into the wafer. An oxide layer is grown during the dopant drive-in which acts as an anti-reflective coating for the solar cells. Two

metal layers are used so the circuits can be protected from the light that powers the solar cells. The final stage of the process includes the etching and release of the MEMS structures. A blanket layer of germanium is deposited over the wafer before the etch of the structures and remains in place during the HF release. It is then removed in hydrogen peroxide.

Three separate versions of the solar cell and circuits stage have been developed and fabricated. They vary in processing complexity and device capabilities. The first version requires a single drive-in step and can be used to fabricate NMOS FETs with metal gates. The second version uses two drive-in steps but can provide NMOS and PMOS FETs with metal gates and p-n-p BJTs. The third version uses different doping levels to improve the performance of the circuits and self-aligned polysilicon gates for better process control.

Solar cells and circuits have been fabricated and tested in all three process versions. The NMOS FETs from the first two process versions had consistent results with threshold voltages of approximately 2.25 V and breakdown voltages greater than 25 V. The NMOS FETs from the third version had a leakage path between the source and drain regions but the threshold voltage was estimated at 1.3 V and the breakdown at 20 V. The PMOS FETs from the second version were not useful because the threshold voltage was greater than the breakdown voltage. The PMOS FETs from the third version had a threshold voltage of -4.3 V and a breakdown of -15 V. The β for BJTs from version two was approximately 3 and the Early voltage was approximately 300 V.

Two types of buffers were demonstrated which utilize NMOS transistors. The simplest one was an NMOS FET with a pull-up resistor. This was capable of switching a 25 V supply with an input of less than 5 V.

A complete, integrated device was demonstrated by driving a gap closing actuator with an on-chip, 40 cell solar array with an output of 15 V. The solar power was controlled through a buffer with an external input. A high input of 5 V would turn off the actuator.

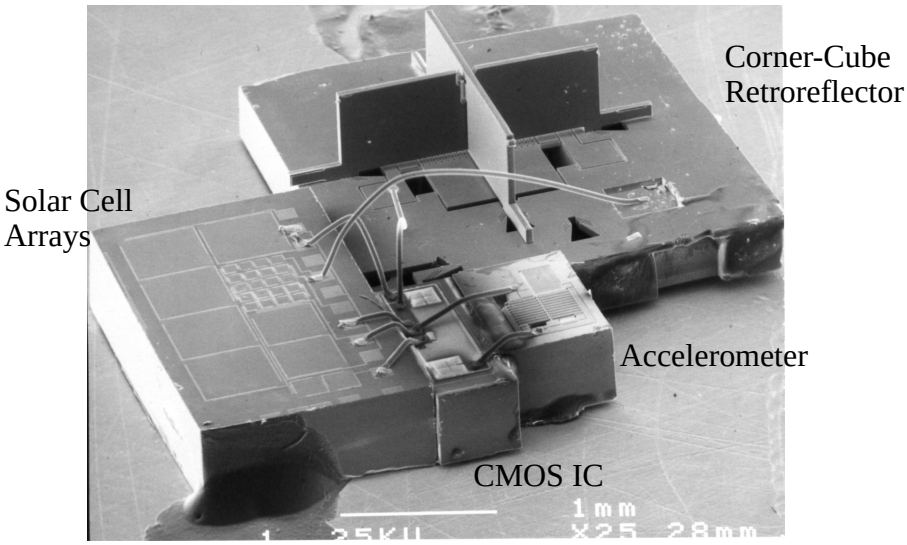


Figure 7-1. *An SEM of Golem Dust [16], the latest version of the Smart Dust sensor motes. Use of the integrated SOI process could reduce the number of die from four to two.*

The application of this process to autonomous microsystems can help in simplifying the fabrication and assembly process. For example, the latest version of the Smart Dust sensor motes[16], shown in Fig. 7-1, could be realized with only two die instead of the current four. The solar cell arrays, corner-cube retroreflector and accelerometer could all be fabricated together on one die.

Although this process has been demonstrated, there are a number of areas which would benefit from further optimization. The area which would benefit the most from further development is the circuitry. Better transistor characteristics would allow more sophisticated circuits to be built, which could potentially eliminate the need for a separate, CMOS control chip for simple devices. Higher breakdown voltages would enable the use of higher drive voltages for the actuators.

Another element of the design which can be developed is the SOI handle wafer. Thinning the handle wafer would reduce the size and mass of the final devices or etching it would allow devices to be placed on both the front and back sides of the wafer.

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APPENDIX - TSUPREM-4 OUTPUT FILES

The output files from the TSUPREM-4 models are given below. The header from the output files has been removed from the outputs in order to save space. The header is the following:

```
*****************************************************************
***                      TSUPREM-4 (TM)                       ***
***          Version 6.6.0, System H (HP: HP-UX)              ***
***          Unpublished Copyright (C) 1988-1998              ***
***               Avant! Corp. and TMA, Inc.                  ***
***                  All Rights Reserved                      ***
***    Avant! Corporation Proprietary and Confidential        ***
***                                                           ***
***   Your use of this program and its documentation are      ***
***  covered by a license agreement, a copy of which may      ***
***   be found in the file "license.txt" located in the       ***
***  install directory.  Your use of this program is your     ***
***    consent to be bound by its terms and conditions.       ***
***                                                           ***
***      Use of copyright notice is precautionary and         ***
***        does not imply publication or disclosure.          ***
***                                                           ***
***    Use, duplication or disclosure by the Government       ***
***       is subject to restrictions as set forth in          ***
***       subparagraph (c) (1) (ii) of the Rights in           ***
***     Technical Data and Computer Software clause at        ***
***                    DFARS 252.227-7013.                    ***
***                                                           ***
***          Technology Modeling Associates, Inc.             ***
***            is a wholly owned subsidiary of                ***
***                   Avant! Corporation                      ***
***                 46871 Bayside Parkway                     ***
***                   Fremont, CA 94538                       ***
***                                                           ***
***        Unpublished - Rights reserved under the            ***
***                 copyright law of the U.S.                 ***
*** TSUPREM-4 is a trademark of Avant! Corp. and TMA, Inc.    ***
*****************************************************************
```

01. Process Version 1: N- Region

```
 Entering source file n-.inp.

$ TSUPREM-4 -- n- simulation
$ 1-d model of n- region of SOI solar cell
```

```
OPTION          DEVICE=CL/POSTSCRIPT PLOT.OUT=n-.ps

$ Use automatic grid generation with defined grid
LINE Y          LOCATION=0.0 SPACING=0.005 TAG=SITOP
LINE Y          LOCATION=3.0 SPACING=0.005 TAG=OXTOP
INITIALIZE      <100> BORON=8E16
** Automatic X grid generation:  lines at X=0 and X=1 micron.
   2 lines in the x direction.
   601 lines in the y direction.

$ Implantation of boron
IMPLANT      PHOSPHOR DOSE=8.4E13 ENERGY=25 DAMAGE

*** Warning:  PD.TRANS model enabled to simulate effects of implant damage.


$ Grow thermal oxide, providing drive-in
DIFFUSION     TIME=172 TEMPERAT=1050 DRYO2

SELECT          Z=log10(DOPING) LABEL=LOG(CONCENTRATION) TEMPERAT=25
PLOT.1D         BOTTOM=14 TOP=20 RIGHT=2.5 LINE.TYP=1 COLOR=1
** Plotting along X.VALUE=0.


ELECTRICAL


************************ STRUCTURE INFORMATION ************************
LAYER    MATERIAL THICKNESS REGION DIFTYP THICKNESS       TOP    BOTTOM

    2       oxide    0.1503                  0.1503   -0.0851    0.0653
    1     silicon    2.9347      2       n    1.2847    0.0653    1.3500
                               1       p    1.6450    1.3550    3.0000

***********************************************************************


 Bias step   1:    0.00 (Volts)

     ********************************************************************
       Material    Thickness   Type   Junction Depth   Sheet Resistance
     --------------------------------------------------------------------

          oxide      1500 A
        silicon      2.93 um     N           1.28 um       326   ohm/sq
                                 P           2.93 um      1.62 K ohm/sq

     ********************************************************************


 Exiting source file n-.inp.
```

02. Process Version 1: N+ Region

```
 Entering source file n+.inp.

$ TSUPREM-4 -- n+ simulation
$ 1-d model of n+ region of SOI solar cell
OPTION          DEVICE=CL/POSTSCRIPT PLOT.OUT=n+.ps

$ Use automatic grid generation and adaptive grid
LINE Y          LOCATION=0.0 SPACING=0.005 TAG=SITOP
LINE Y          LOCATION=3.0 SPACING=0.005 TAG=OXTOP
INITIALIZE           <100> BORON=8E16
** Automatic X grid generation:  lines at X=0 and X=1 micron.
   2 lines in the x direction.
   601 lines in the y direction.

$ Implantation of boron
IMPLANT          PHOSPHOR DOSE=3.2E15 ENERGY=25 DAMAGE

*** Warning:  PD.TRANS model enabled to simulate effects of implant damage.


$ Thermal oxide growth
DIFFUSION     TIME=172 TEMPERAT=1050 DRYO2

SELECT          Z=log10(DOPING) LABEL=LOG(CONCENTRATION) TEMPERAT=25
PLOT.1D         BOTTOM=14 TOP=20 RIGHT=2.5 LINE.TYP=1 COLOR=1
** Plotting along X.VALUE=0.


ELECTRICAL


************************ STRUCTURE INFORMATION ************************
LAYER    MATERIAL THICKNESS REGION DIFTYP THICKNESS       TOP    BOTTOM

    2       oxide    0.1752                  0.1752   -0.0990    0.0762
    1     silicon    2.9238      2      n    1.9888    0.0762    2.0650
                                 1      p    0.9300    2.0700    3.0000

***********************************************************************


 Bias step   1:    0.00 (Volts)

     ***************************************************************
       Material    Thickness   Type   Junction Depth   Sheet Resistance
     ---------------------------------------------------------------

          oxide      1750 A
         silicon     2.92 um     N          1.99 um        23   ohm/sq
                                 P          2.92 um      2.92 K ohm/sq

     ***************************************************************
```

```
 Exiting source file n+.inp.
```

03. Process Version 1: P+ Region

```
 Entering source file p+.inp.

$ TSUPREM-4 -- p+ simulation
$ 1-d model of p+ region of SOI solar cell
OPTION          DEVICE=CL/POSTSCRIPT PLOT.OUT=p+.ps

$ Use automatic grid generation and adaptive grid
LINE Y          LOCATION=0.0 SPACING=0.005 TAG=SITOP
LINE Y          LOCATION=3.0 SPACING=0.005 TAG=OXTOP
INITIALIZE <100> BORON=8E16
** Automatic X grid generation:  lines at X=0 and X=1 micron.
   2 lines in the x direction.
   601 lines in the y direction.

$ Implantation of boron
IMPLANT BORON DOSE=4E15 ENERGY=25 DAMAGE

*** Warning:  PD.TRANS model enabled to simulate effects of implant damage.


DIFFUSION TIME=172 TEMPERAT=1050 DRYO2

SELECT          Z=log10(DOPING) LABEL=LOG(CONCENTRATION) TEMPERAT=25
PLOT.1D         BOTTOM=14 TOP=20 RIGHT=2.5 LINE.TYP=1 COLOR=1
** Plotting along X.VALUE=0.


ELECTRICAL


************************ STRUCTURE INFORMATION ************************
LAYER    MATERIAL THICKNESS REGION DIFTYP THICKNESS       TOP    BOTTOM

    2       oxide    0.1499                  0.1499   -0.0848    0.0651
    1     silicon    2.9349      1      p    2.9349    0.0651    3.0000

***********************************************************************


 Bias step   1:    0.00 (Volts)

     ********************************************************************
       Material    Thickness   Type   Junction Depth   Sheet Resistance
     --------------------------------------------------------------------

          oxide      1500 A
        silicon      2.93 um     P           2.93 um        41   ohm/sq
```

```
     ********************************************************************

 Exiting source file p+.inp.
```

04. Process Version 2: N- Well

```
 Entering source file cmosn1.inp.

$ TSUPREM-4 -- cmos soi solar+ simulation
$ implant and drive-in of n- region

$ Use automatic grid generation and adaptive grid
LINE Y          LOCATION=0.0 SPACING=0.005 TAG=SITOP
LINE Y          LOCATION=3.0 SPACING=0.005 TAG=OXTOP
INITIALIZE      <100> BORON=8E16
** Automatic X grid generation:  lines at X=0 and X=1 micron.
   2 lines in the x direction.
   601 lines in the y direction.

$ Implantation of phosporus
IMPLANT PHOSPHOR DOSE=8.4E13 ENERGY=25 DAMAGE

*** Warning:  PD.TRANS model enabled to simulate effects of implant damage.


$ Two step drive-in
DIFFUSION TIME=30 TEMPERAT=1100 DRYO2
DIFFUSION TIME=180 TEMPERAT=1100 INERT

$ Remove oxide
ETCH      OXIDE ALL

SAVEFILE OUT.FILE=cmosn1.save

ELECTRICAL


************************ STRUCTURE INFORMATION ************************
LAYER    MATERIAL THICKNESS REGION DIFTYP THICKNESS       TOP    BOTTOM

    1     silicon    2.9704      2      n    1.5704    0.0296    1.6000
                                 1      p    1.3950    1.6050    3.0000

********************************************************************


 Bias step   1:    0.00 (Volts)

     ********************************************************************
       Material    Thickness   Type   Junction Depth   Sheet Resistance
     --------------------------------------------------------------------
```

```
        silicon      2.97 um     N           1.57 um       312   ohm/sq
                                 P           2.97 um      2.10 K ohm/sq

     ************************************************************************

OPTION          DEVICE=CL/POSTSCRIPT PLOT.OUT=cmosn1.ps
SELECT          Z=log10(DOPING) LABEL=LOG(CONCENTRATION) TEMPERAT=25
PLOT.1D         BOTTOM=14 TOP=20 RIGHT=2.5 LINE.TYP=1 COLOR=1
** Plotting along X.VALUE=0.


 Exiting source file cmosn1.inp.
```

05. Process Version 3: N+ Region

```
 Entering source file cmosn2.inp.

$ TSUPREM-4 -- cmos soi solar+ simulation
$ implant and drive-in of n+ region

$ Use automatic grid generation and adaptive grid
LINE Y          LOCATION=0.0 SPACING=0.005 TAG=SITOP
LINE Y          LOCATION=3.0 SPACING=0.005 TAG=OXTOP
INITIALIZE      <100> BORON=8E16
** Automatic X grid generation:  lines at X=0 and X=1 micron.
   2 lines in the x direction.
   601 lines in the y direction.

$ Implantation of phosporus
IMPLANT      PHOSPHOR DOSE=1E15 ENERGY=25 DAMAGE

*** Warning:  PD.TRANS model enabled to simulate effects of implant damage.


$ Wet drive-in
DIFFUSION       TIME=150 TEMPERAT=850 STEAM

ELECTRICAL


********************** STRUCTURE INFORMATION **********************
LAYER    MATERIAL THICKNESS REGION DIFTYP THICKNESS       TOP    BOTTOM

    2       oxide    0.2458                 0.2458   -0.1386    0.1073
    1     silicon    2.8927      2      n    0.5677    0.1073    0.6750
                                 1      p    2.3200    0.6800    3.0000

************************************************************************


 Bias step   1:    0.00 (Volts)
```

```
     ********************************************************************
       Material    Thickness   Type   Junction Depth   Sheet Resistance
     --------------------------------------------------------------------

          oxide      2460 A
         silicon     2.89 um     N          0.57 um        77   ohm/sq
                                 P          2.89 um      1.01 K ohm/sq

     ********************************************************************

OPTION          DEVICE=CL/POSTSCRIPT PLOT.OUT=cmosn2.ps
SELECT          Z=log10(DOPING) LABEL=LOG(CONCENTRATION) TEMPERAT=25
PLOT.1D         BOTTOM=14 TOP=20 RIGHT=2.5 LINE.TYP=1 COLOR=1
** Plotting along X.VALUE=0.


 Exiting source file cmosn2.inp.
```

06. Process Version 2: N+ Region in N- Well

```
 Entering source file cmosn3.inp.

$ TSUPREM-4 -- cmos soi solar+ simulation
$ implant and drive-in of n+ inside n- well

LOADFILE        IN.FILE=cmosn1.save

$ Implantation of phosphorus
IMPLANT      PHOSPHOR DOSE=5E14 ENERGY=25 DAMAGE

$ Wet drive-in
DIFFUSION     TIME=150 TEMPERAT=850 STEAM

ELECTRICAL


************************ STRUCTURE INFORMATION ************************
LAYER    MATERIAL THICKNESS REGION DIFTYP THICKNESS       TOP    BOTTOM

    2       oxide    0.2200                  0.2200   -0.0944    0.1255
    1     silicon    2.8745      2      n    1.4945    0.1255    1.6200
                               1      p    1.3750    1.6250    3.0000

***********************************************************************


 Bias step   1:    0.00 (Volts)

     ********************************************************************
       Material    Thickness   Type   Junction Depth   Sheet Resistance
     --------------------------------------------------------------------
```

```
          oxide      2200 A
        silicon      2.87 um     N           1.49 um       110   ohm/sq
                                 P           2.87 um      2.14 K ohm/sq

     ***********************************************************************

OPTION          DEVICE=CL/POSTSCRIPT PLOT.OUT=cmosn3.ps
SELECT          Z=log10(DOPING) LABEL=LOG(CONCENTRATION) TEMPERAT=25
PLOT.1D         BOTTOM=14 TOP=20 RIGHT=2.5 LINE.TYP=1 COLOR=1
** Plotting along X.VALUE=0.


 Exiting source file cmosn3.inp.
```

07. Process Version 2: P+ Region

```
 Entering source file cmosp1.inp.

$ TSUPREM-4 -- cmos soi solar+ simulation
$ implant and drive-in of p+ region

$ Use automatic grid generation and adaptive grid
LINE Y          LOCATION=0.0 SPACING=0.005 TAG=SITOP
LINE Y          LOCATION=3.0 SPACING=0.005 TAG=OXTOP
INITIALIZE      <100> BORON=8E16
** Automatic X grid generation:  lines at X=0 and X=1 micron.
   2 lines in the x direction.
   601 lines in the y direction.

$ Implantation of boron
IMPLANT      BORON DOSE=5E14 ENERGY=25 DAMAGE

*** Warning:  PD.TRANS model enabled to simulate effects of implant damage.


$ Wet drive-in
DIFFUSION     TIME=150 TEMPERAT=850 STEAM

ELECTRICAL


************************ STRUCTURE INFORMATION ************************
LAYER    MATERIAL THICKNESS REGION DIFTYP THICKNESS       TOP    BOTTOM

    2       oxide    0.1795                  0.1795   -0.1014    0.0781
    1     silicon    2.9219      1      p    2.9219    0.0781    3.0000

***********************************************************************


 Bias step   1:    0.00 (Volts)
```

```
     ********************************************************************
       Material    Thickness   Type   Junction Depth   Sheet Resistance
     --------------------------------------------------------------------

          oxide      1790 A
         silicon     2.92 um     P          2.92 um       214   ohm/sq

     ********************************************************************

OPTION          DEVICE=CL/POSTSCRIPT PLOT.OUT=cmosp1.ps
SELECT          Z=log10(DOPING) LABEL=LOG(CONCENTRATION) TEMPERAT=25
PLOT.1D         BOTTOM=14 TOP=20 RIGHT=2.5 LINE.TYP=1 COLOR=1
** Plotting along X.VALUE=0.


 Exiting source file cmosp1.inp.
```

08. Process Version 2: P+ Region in N- Well

```
 Entering source file cmosp2.inp.

$ TSUPREM-4 -- cmos soi solar+ simulation
$ implant and drive-in of p+ inside n- well

LOADFILE        IN.FILE=cmosn1.save

$ Implantation of boron
IMPLANT      BORON DOSE=5E14 ENERGY=25 DAMAGE

$ Wet drive-in
DIFFUSION     TIME=150 TEMPERAT=850 STEAM

ELECTRICAL


************************ STRUCTURE INFORMATION ************************
LAYER    MATERIAL THICKNESS REGION DIFTYP THICKNESS       TOP    BOTTOM

    2       oxide    0.1799                   0.1799   -0.0720    0.1079
    1     silicon    2.8921      4      n     0.0071    0.1079    0.1150
                               3      p     0.6450    0.1200    0.7650
                               2      n     0.8500    0.7700    1.6200
                               1      p     1.3750    1.6250    3.0000

***********************************************************************


 Bias step   1:    0.00 (Volts)

     ********************************************************************
       Material    Thickness   Type   Junction Depth   Sheet Resistance
     --------------------------------------------------------------------
```

```
          oxide      1800 A
        silicon      2.89 um     N              93 A      > 100 K ohm/sq
                                 P            0.66 um       406   ohm/sq
                                 N            1.51 um      1.24 K ohm/sq
                                 P            2.89 um      2.15 K ohm/sq

     ****************************************************************

OPTION           DEVICE=CL/POSTSCRIPT PLOT.OUT=cmosp2.ps
SELECT           Z=log10(DOPING) LABEL=LOG(CONCENTRATION) TEMPERAT=25
PLOT.1D          BOTTOM=14 TOP=20 RIGHT=2.5 LINE.TYP=1 COLOR=1
** Plotting along X.VALUE=0.



 Exiting source file cmosp2.inp.
```

09. Process Version 3: N- well

```
 Entering source file ic1.inp.

$ TSUPREM-4 -- soi solar+ simulation
$ n- region
OPTION DEVICE=CL/POSTSCRIPT PLOT.OUT=ic1.ps

$ Use automatic grid generation and adaptive grid
LINE Y           LOCATION=0.0 SPACING=0.005 TAG=SITOP
LINE Y           LOCATION=4.0 SPACING=0.005 TAG=OXTOP
INITIALIZE       <100> BORON=2.5 RESISTIV
** Automatic X grid generation:  lines at X=0 and X=1 micron.
   2 lines in the x direction.
   801 lines in the y direction.

$ Implant n- region
IMPLANT           PHOSPHORUS DOSE=6E12 ENERGY=25 +
          IMPL.TAB=tr.phosphorus DAMAGE

*** Warning:  PD.TRANS model enabled to simulate effects of implant damage.



$ Drive-in n- region
DIFFUSION        TIME=40  TEMPERAT=1100  DRYO2
DIFFUSION     TIME=720 TEMPERAT=1100 INERT

ETCH           OXIDE ALL

$ Grow gate oxide
DIFFUSION     TIME=85 TEMPERAT=1050 DRYO2

SAVEFILE     OUT.FILE=ic1.save
```

```
ELECTRICAL


************************ STRUCTURE INFORMATION ************************
LAYER    MATERIAL THICKNESS REGION DIFTYP THICKNESS       TOP    BOTTOM

    2       oxide    0.0952                 0.0952   -0.0185    0.0767
    1     silicon    3.9233      2      n    2.4683    0.0767    2.5450
                               1      p    1.4500    2.5500    4.0000

***********************************************************************


 Bias step   1:    0.00 (Volts)

     ***********************************************************************
       Material    Thickness   Type   Junction Depth   Sheet Resistance
     -----------------------------------------------------------------------

          oxide       952 A
        silicon      3.92 um     N           2.47 um      1.71 K ohm/sq
                                 P           3.92 um      30.7 K ohm/sq

     ***********************************************************************

SELECT          Z=log10(DOPING) LABEL=LOG(CONCENTRATION) TEMPERAT=25
PLOT.1D         BOTTOM=14 TOP=20 RIGHT=4.0 LINE.TYP=1 COLOR=1
** Plotting along X.VALUE=0.




 Exiting source file ic1.inp.
```

010. Process Version 3: P+ Region in N- Well

```
 Entering source file ic2.inp.

$ TSUPREM-4 -- new soi solar+ simulation
$ 1-d model of n+ on p- region of SOI solar cell
OPTION DEVICE=CL/POSTSCRIPT PLOT.OUT=ic2.ps

LOADFILE     IN.FILE=ic1.save

ETCH          OXIDE ALL

IMPLANT         BORON DOSE=5E15 ENERGY=20 +
                IMPL.TAB=tr.boron DAMAGE

DEPOSIT          OXIDE THICKNESS=1.0

DIFFUSION       TIME=60 TEMPERAT=900 INERT
```

```
SAVEFILE     OUT.FILE=ic2.save

ELECTRICAL


************************ STRUCTURE INFORMATION ************************
LAYER    MATERIAL THICKNESS REGION DIFTYP THICKNESS       TOP    BOTTOM

    2       oxide    1.0000                 1.0000   -0.9233    0.0767
    1     silicon    3.9233      3      p   1.2133    0.0767    1.2900
                               2      n   1.2600    1.2950    2.5550
                               1      p   1.4400    2.5600    4.0000

***********************************************************************


 Bias step   1:    0.00 (Volts)

     ***********************************************************************
       Material    Thickness   Type   Junction Depth   Sheet Resistance
     -----------------------------------------------------------------------

          oxide      10000 A
         silicon      3.92 um     P           1.22 um        37   ohm/sq
                                  N           2.48 um      11.8 K ohm/sq
                                  P           3.92 um      31.2 K ohm/sq

     ***********************************************************************

SELECT          Z=log10(DOPING) LABEL=LOG(CONCENTRATION) TEMPERAT=25
PLOT.1D         BOTTOM=14 TOP=20 RIGHT=4.0 LINE.TYP=1 COLOR=1
** Plotting along X.VALUE=0.


 Exiting source file ic2.inp.
```

011. Process Version 3: N+ Region in N- Well

```
 Entering source file ic3.inp.

$ TSUPREM-4 -- new soi solar+ simulation
$ 1-d model of n+ on p- region of SOI solar cell
OPTION DEVICE=CL/POSTSCRIPT PLOT.OUT=ic3.ps

LOADFILE     IN.FILE=ic1.save

ETCH          OXIDE ALL

IMPLANT         PHOSPHOR DOSE=5E15 ENERGY=35 +
                IMPL.TAB=tr.phosphorus DAMAGE

DEPOSIT          OXIDE THICKNESS=1.0
```

```
DIFFUSION       TIME=60 TEMPERAT=900 INERT

SAVEFILE     OUT.FILE=ic3.save

ELECTRICAL


************************ STRUCTURE INFORMATION ************************
LAYER    MATERIAL THICKNESS REGION DIFTYP THICKNESS       TOP    BOTTOM

    2       oxide    1.0000                  1.0000   -0.9233    0.0767
    1     silicon    3.9233      2      n    2.4783    0.0767    2.5550
                                 1      p    1.4400    2.5600    4.0000

***********************************************************************


 Bias step   1:    0.00 (Volts)

     ********************************************************************
       Material    Thickness   Type   Junction Depth   Sheet Resistance
     --------------------------------------------------------------------

          oxide      10000 A
         silicon      3.92 um     N           2.48 um        20   ohm/sq
                                  P           3.92 um      31.2 K ohm/sq

     ********************************************************************

SELECT          Z=log10(DOPING) LABEL=LOG(CONCENTRATION) TEMPERAT=25
PLOT.1D         BOTTOM=14 TOP=20 RIGHT=4.0 LINE.TYP=1 COLOR=1
** Plotting along X.VALUE=0.


 Exiting source file ic3.inp.
```