



Berkeley
Wireless Research Center

A Heterogeneous SoC for Bluetooth LE in 28nm

Felicia Guo, Nayiri Krzysztofowicz, Alex Moreno, Jeffrey Ni, Daniel Lovell, Yufeng Chi, Kareem Ahmad, Sherwin Afshar, Josh Alexander, Dylan Brater, Cheng Cao, Daniel Fan, Ryan Lund, Jackson Paddock, Griffin Prechter, Troy Sheldon, Shreesha Sreedhara, Anson Tsai, Eric Wu, Kerry Yu, Daniel Fritchman, Aviral Pandey, Ali Niknejad, Kristofer Pister, and Borivoje Nikolic

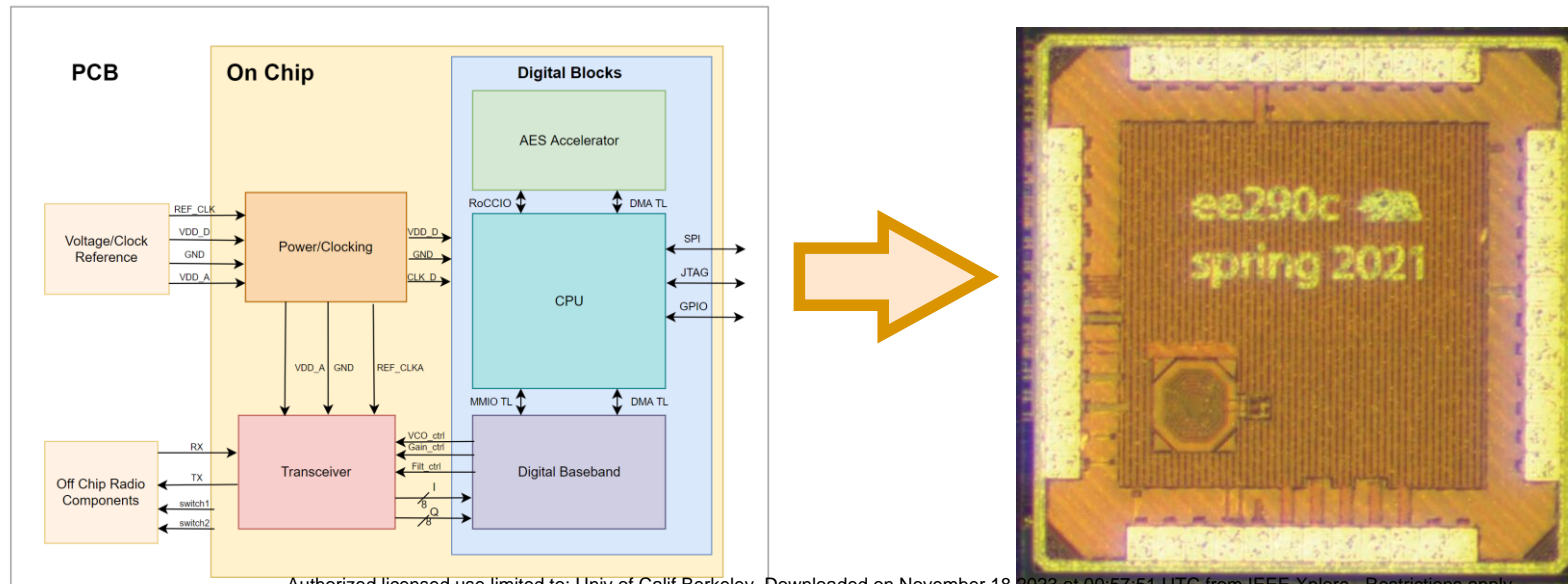
University of California, Berkeley

OsciBear is a system-on-chip (SoC) featuring a RISC-V 32-bit 5-stage in-order scalar processor, AES accelerator, BLE 1M baseband-modem, and a 2.4 GHz radio front end (RFE) transceiver. It was designed in TSMC's 28nm process with a total die area of 1 mm^2 during the course of a 14-week semester by 18 students - 4 Ph.D students, 6 masters students, and 8 undergraduates – enrolled in UC Berkeley's special topics course "28nm SoC for IoT" in Spring 2021. Additionally, a PCB was designed with off-chip reference clocks, bring-up tooling, as well as power amplifiers, RF switch, and an antenna to complete the radio front-end.

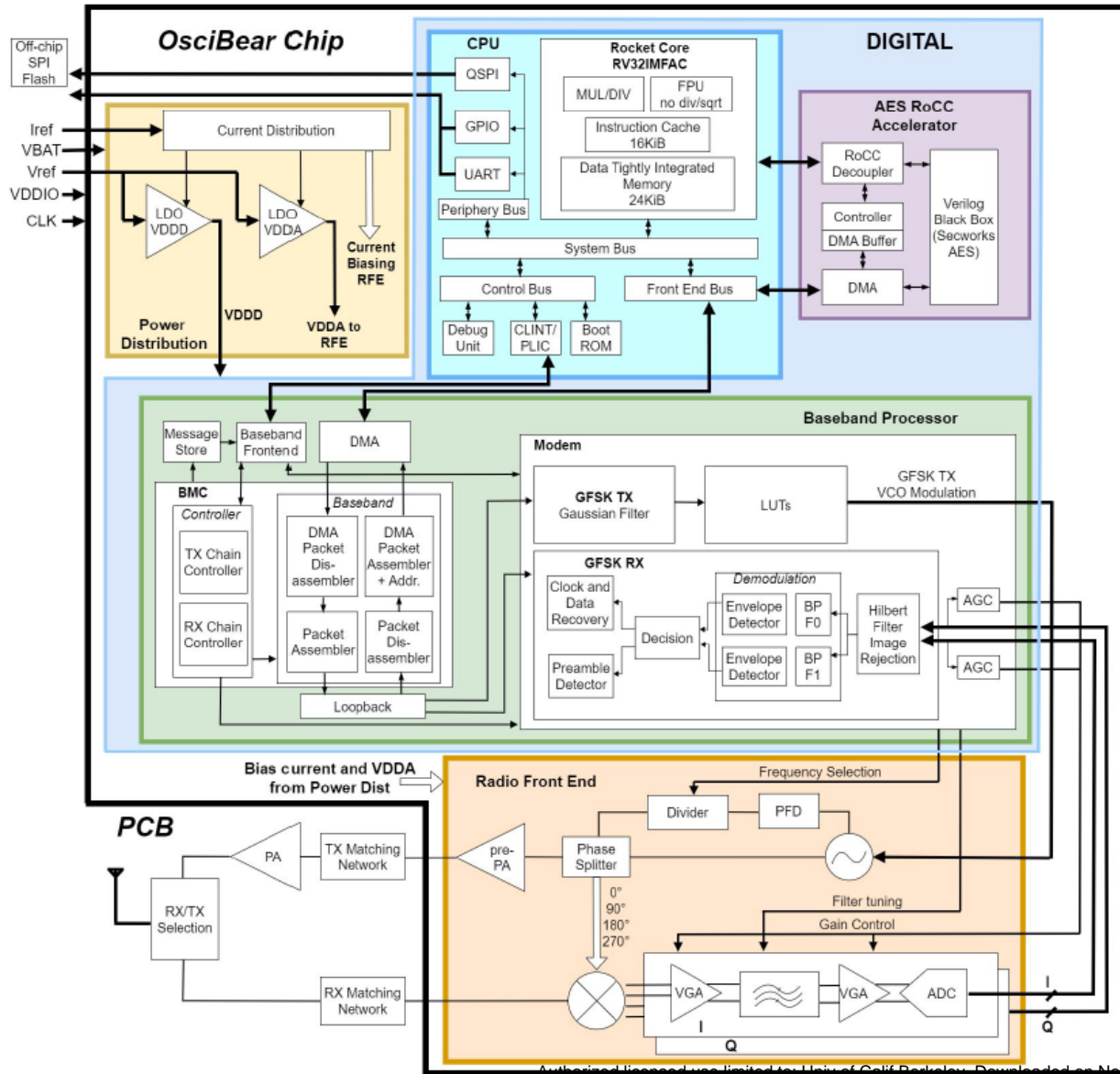
The CPU has been demonstrated to run up to 30 MHz in typical operating conditions. The BLE 1M-compliant PHY layer packet assembly and disassembly has been verified in-hardware through "loopback" testing. Adherence to BLE's PHY FM specifications has also been verified with a commercial BLE receiver. In total, the chip consumes 8.43 mW of static power.

Motivation

- Create a system-on-chip (SoC) (dubbed OsciBear) featuring:
 - RISC-V 32-bit 5-stage in-order scalar processor
 - AES accelerator
 - BLE 1M baseband-modem
 - 2.4 GHz radio front end (RFE) transceiver
 - On chip power regulation and distribution
- Tape out in 14 weeks with 19 students (4 Ph.D students, 6 masters students, and 8 undergraduates)
- Demonstrate Berkeley developed agile hardware tools and flow
- More about UC Berkeley's tapeout course can be found at <https://ucb-ee290c.github.io>

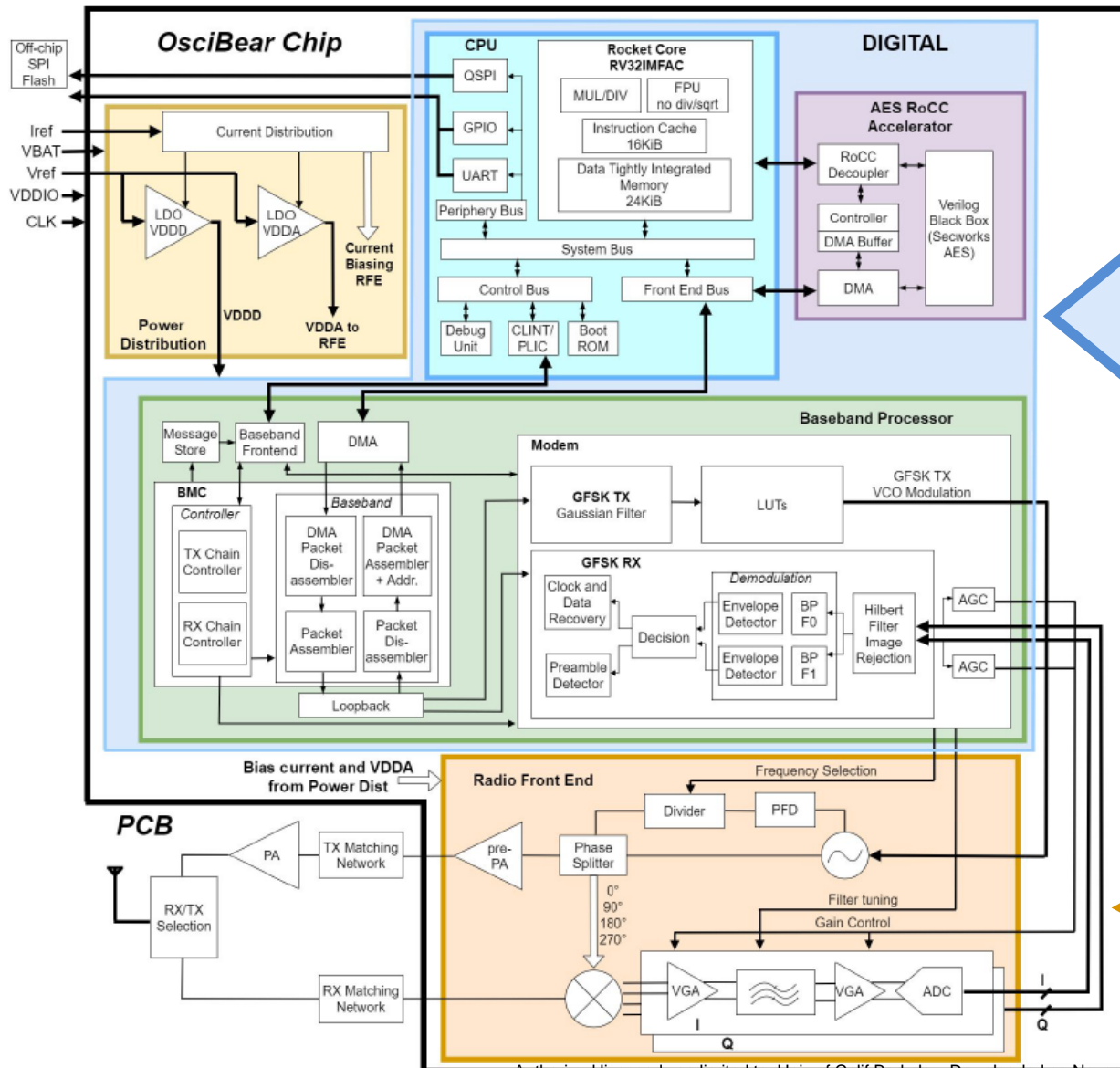


Chip Architecture



- Digital Components
 - Compute
 - RV32IMFAC Core
 - Interrupt Controller
 - UART and TSI peripherals
 - Digital Baseband
 - TX/RX packet control
 - Digital RF tuning constants
- Analog Components
 - Radio Front End
 - Low-IF receiver architecture
 - Transmitter and LO generation through VCO
 - Digital GFSK modulation tuning interface
 - Power Regulation
 - Analog, digital, and I/O domains
 - LDOs for analog and digital domains
- <10mW of static power
- 74% density on digital portion of chip

Research Infrastructure



<https://chipyard.readthedocs.io>



<https://hammer-vlsi.readthedocs.io>



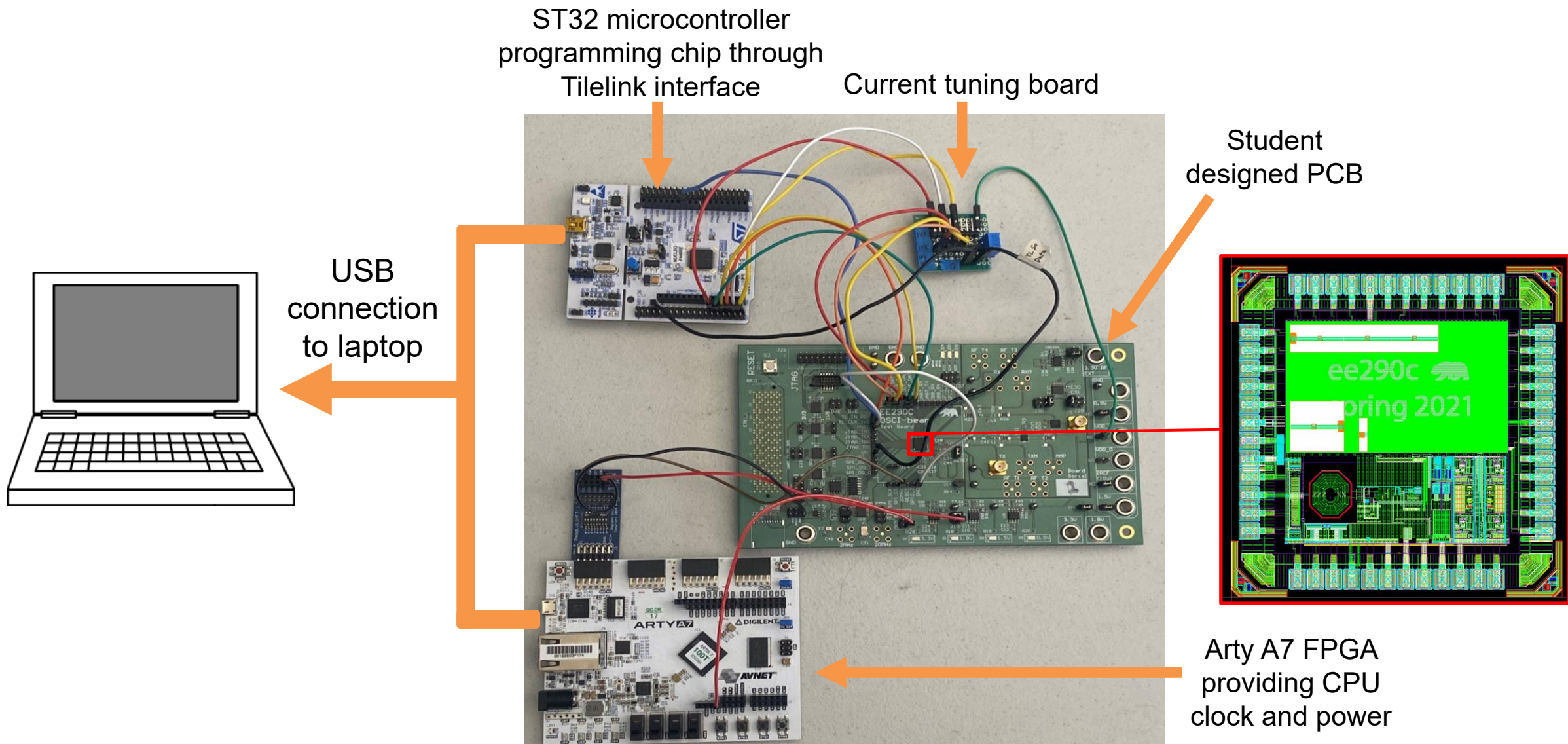
<https://www.chisel-lang.org>

BAG

Berkeley Analog
Generator
(ADC Only)

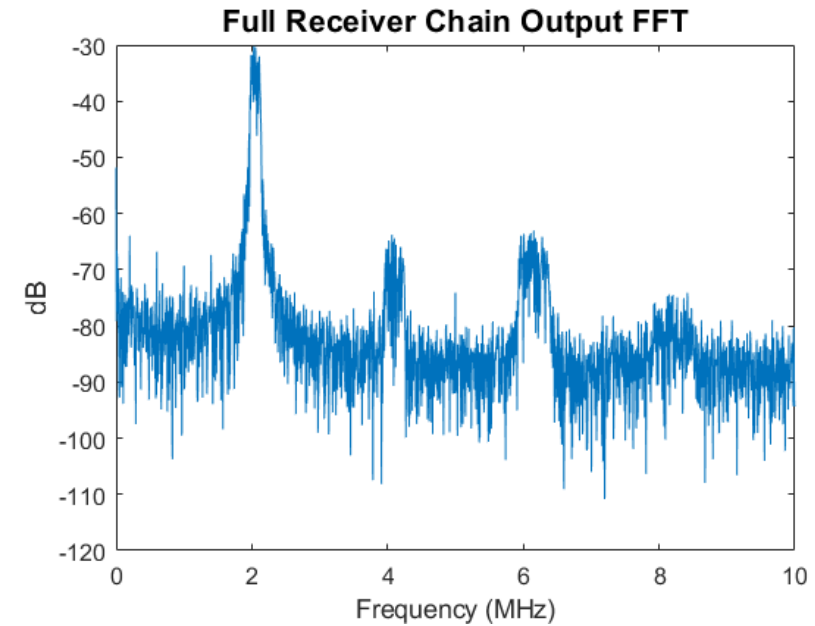
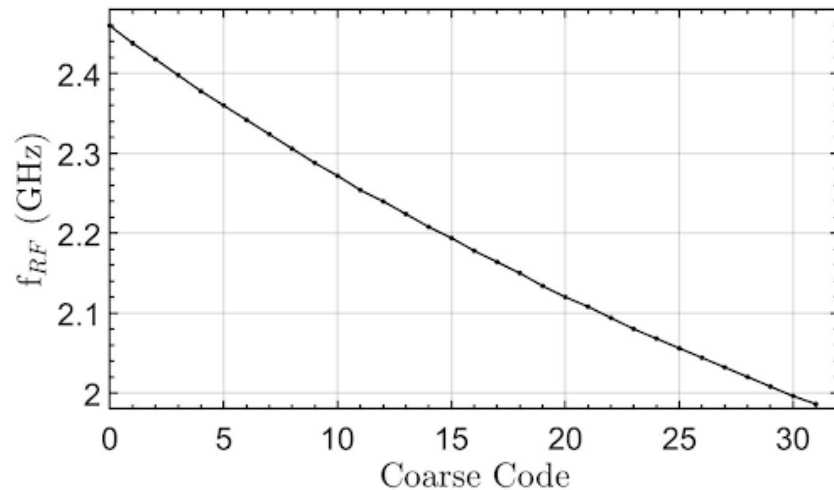
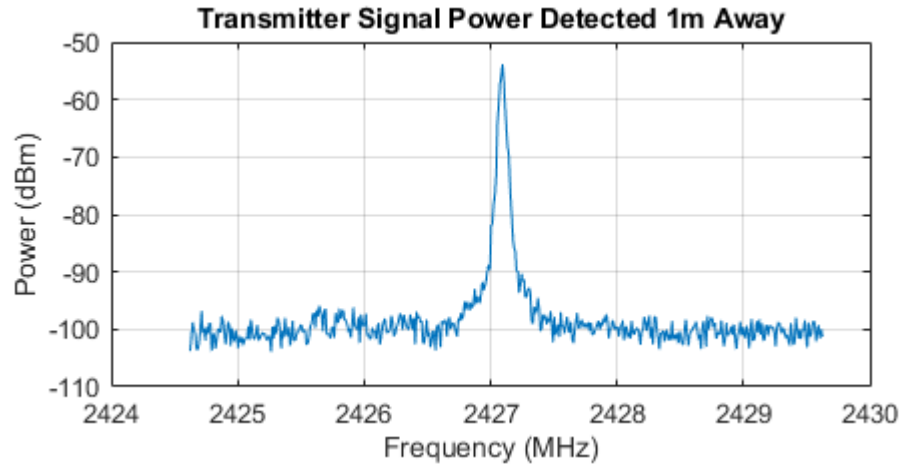
<https://bag3-readthedocs.readthedocs.io>

Verification



BLE Transceiver Analog Measurements

- Receiver tested from PCB antenna port to differential output of final VGA (pre-ADC)
- Transmitter measured using antennas spaced approximately 1 meter away

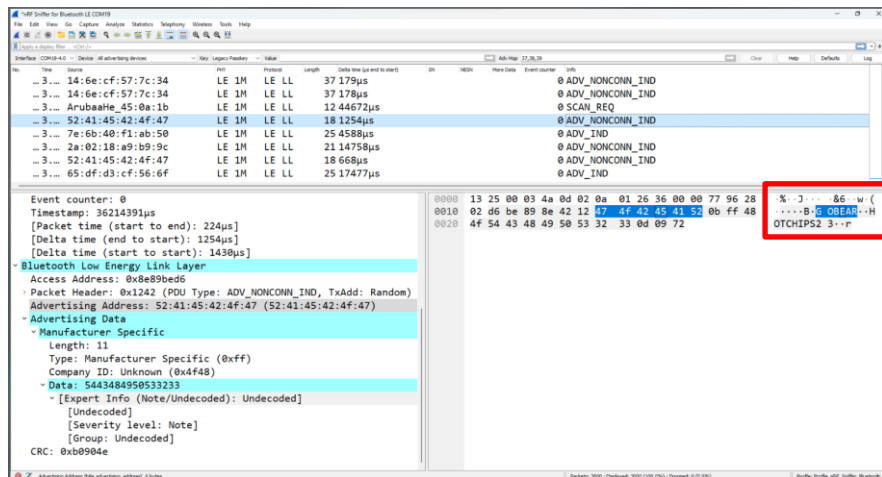


Radio Measurement Summary

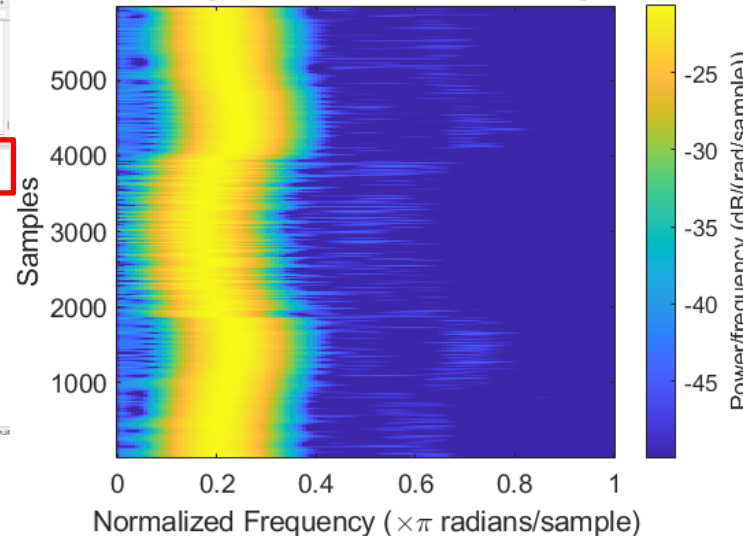
TX Frequency Modulation Range	~250 kHz
TX Power 1 meter away	-55 dBm
RX Chain SNDR (pre-ADC)	24.87 dB

Transmit packet decoding done two ways:

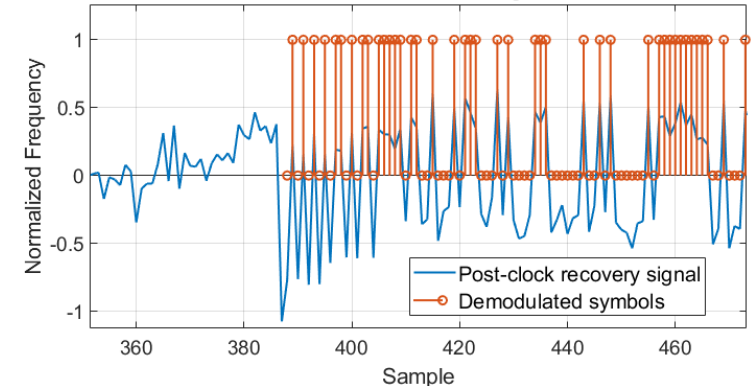
1. Software Testing
 - Transmitted RF signal mixed down off chip
 - IF signal demodulated in software showed preamble, access address, and payload
2. Commercial (Nordic nRF52840 DK) receiver
 - LO calibrated to BLE channel 38 (advertisement)
 - Packet transmitted periodically with commercial receiver configured as sniffer



Spectrogram of GFSK Modulated Signal



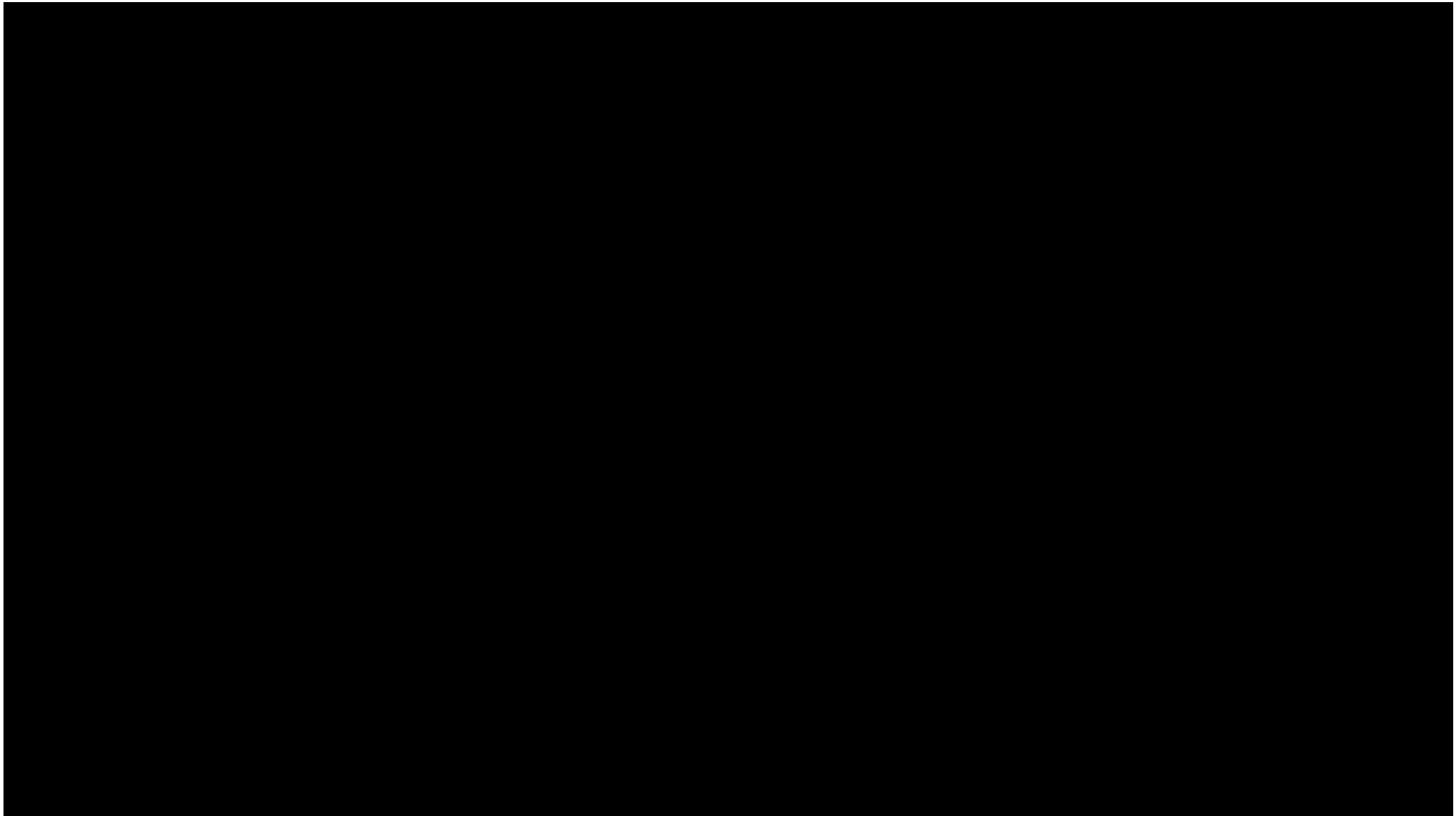
Demodulated GFSK Signal



Demodulation in software

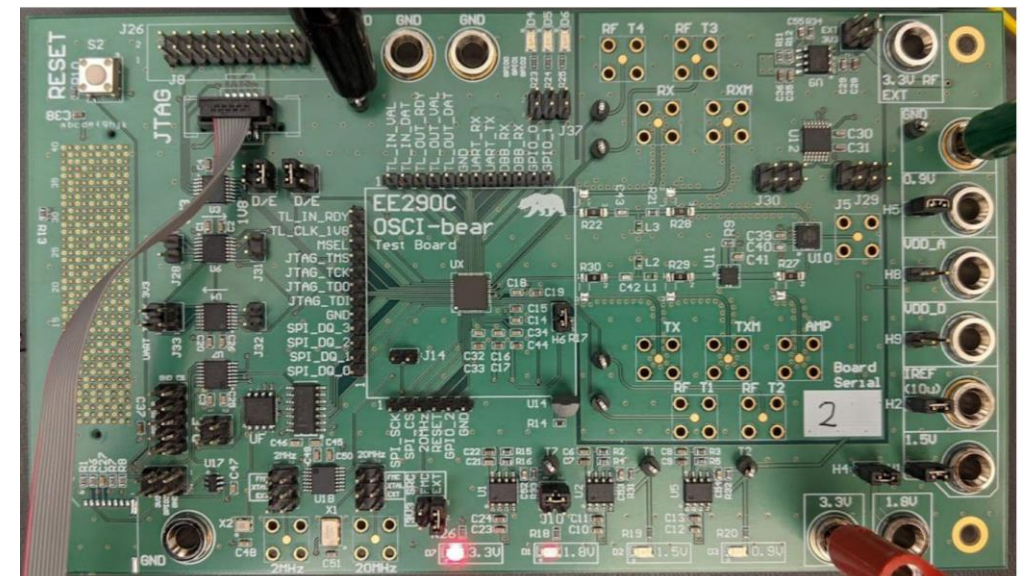
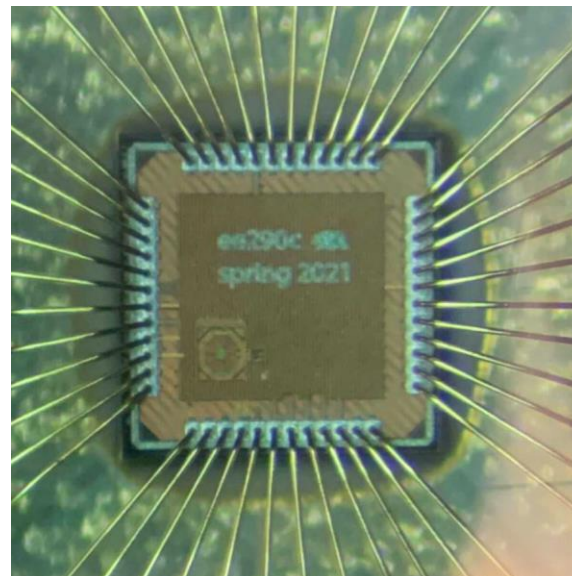
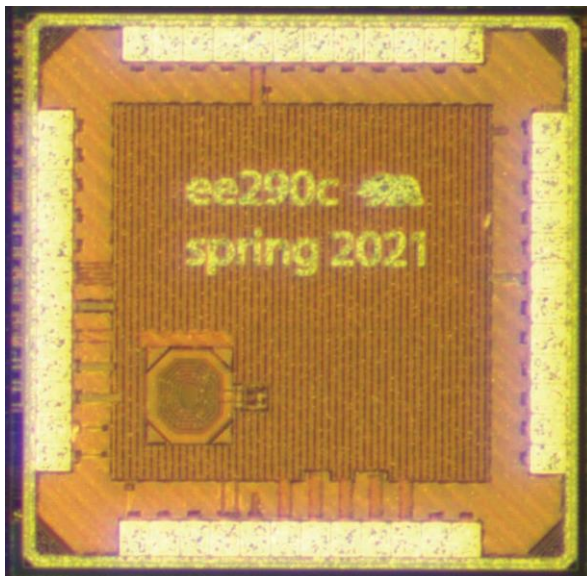
Commercial receiver decoding correctly formed packet sent with "GOBEAR HOTCHIPS23" as payload

Video Demo



Conclusion

- Completely student driven chip design and bringup
- Successfully designed and tested SoC featuring BLE radio, with verified:
 - RISC-V 32-bit IMAC instructions
 - DMA controller
 - BLE 1M Digital Baseband Modem
 - RF Frontend
 - Power distribution with on chip LDO regulation
- More about the design process and this iteration of the course can be found in our prior publication:
[Tape-Out Course: Silicon in a Semester](#)



Acknowledgements

We would like to acknowledge and thank Apple for supporting integrated circuit engineering classes at UC Berkeley EECS department through Apple's New Silicon Initiative program.

This work is also funded by NSF CCRI ENS Chipyard Award #2016662.