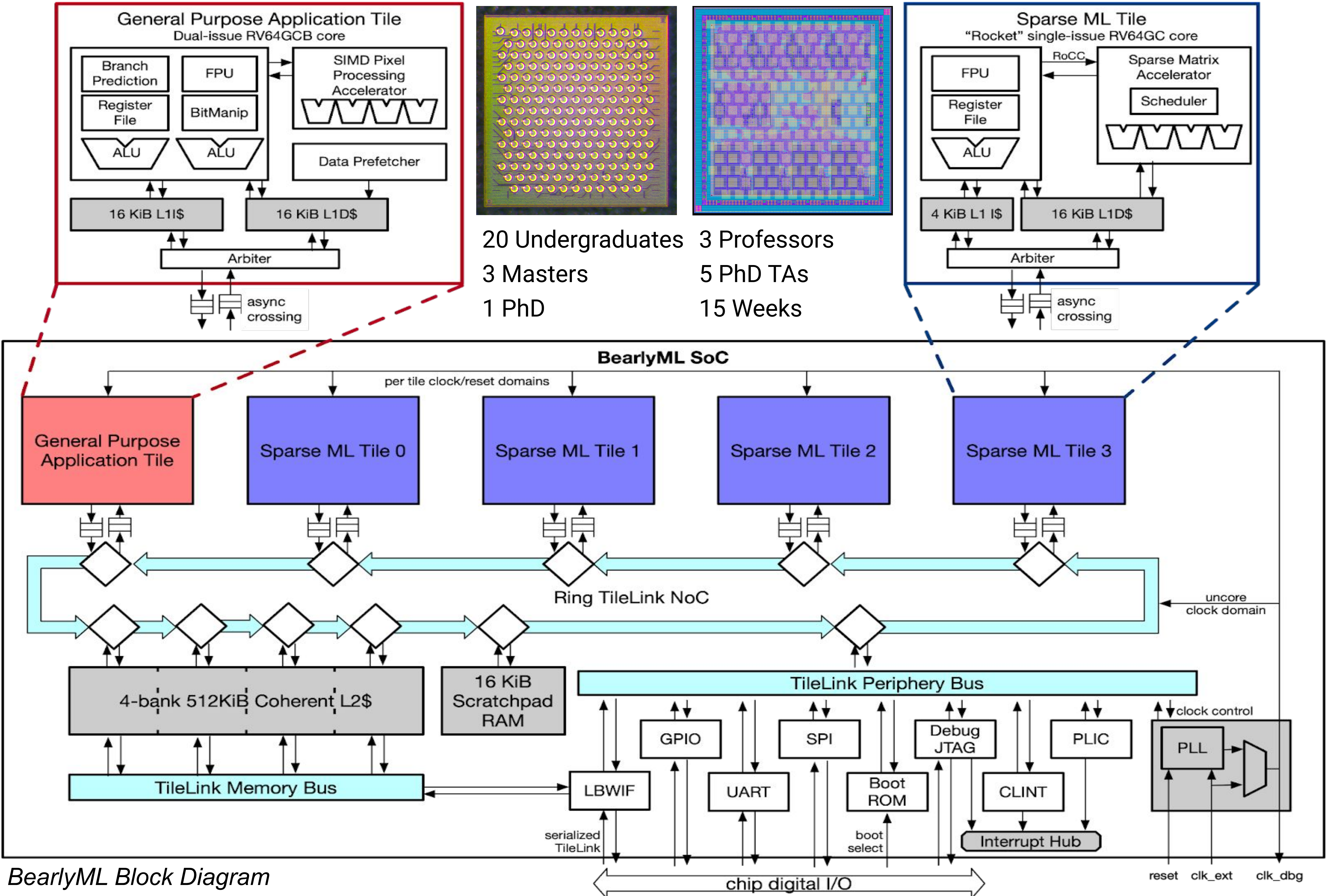


Yufeng Chi, Franklin Huang, Raghav Gupta, Ella Schwarz, Jennifer Zhou, Reza Sajadiany, Animesh Agrawal, Max Banister, Michelle Boulos, Jason Chandran, Jessica Dowdall, Leena Elzeiny, Claire Gantan, Anthony Han, Roger Hsiao, Chadwick Leung, Edwin Lim, Jose Rodriguez, Tushar Sondhi, Mitchell Twu, Rongyi Wang, Mike Xiao, Ruohan Yan, Paul Kwon, Zhaokai Liu, Jerry Zhao, Bob Zhou, Ali Niknejad, Kristofer Pister, Borivoje Nikolić

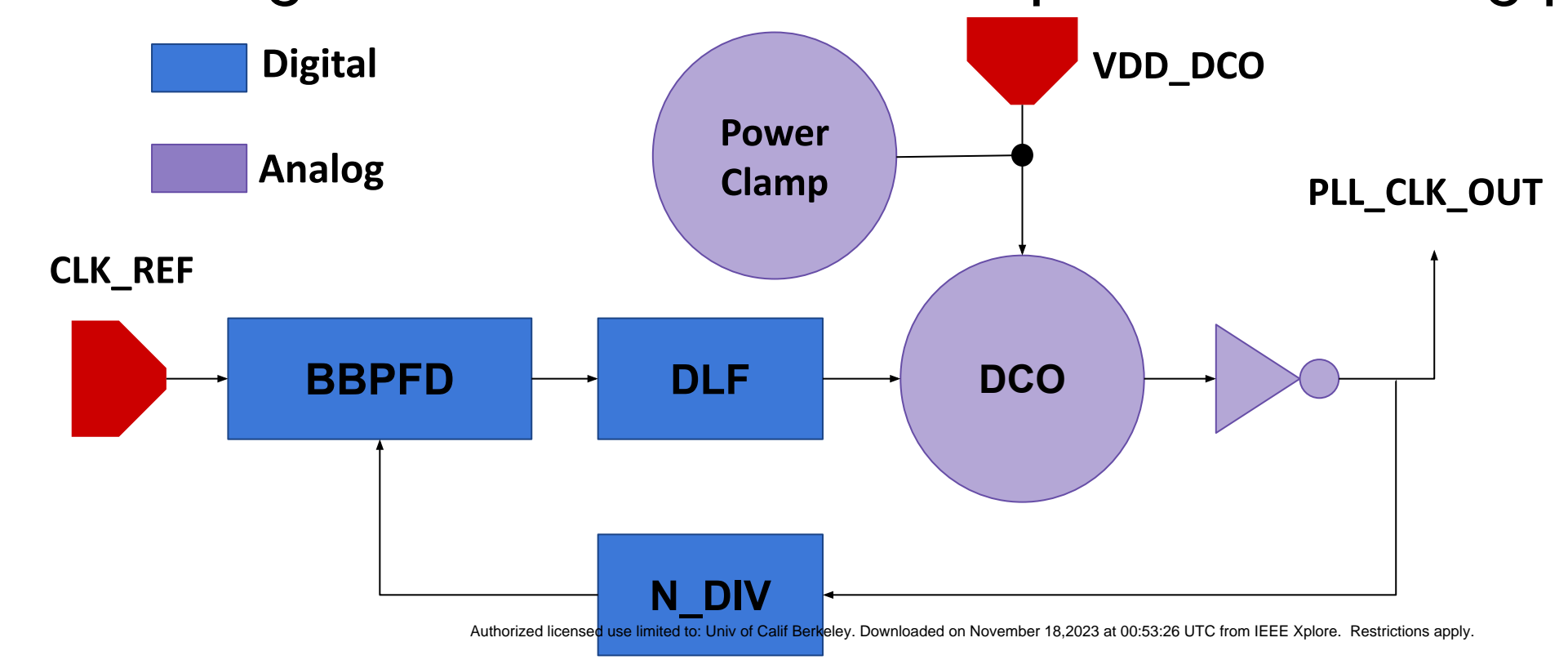
BearlyML



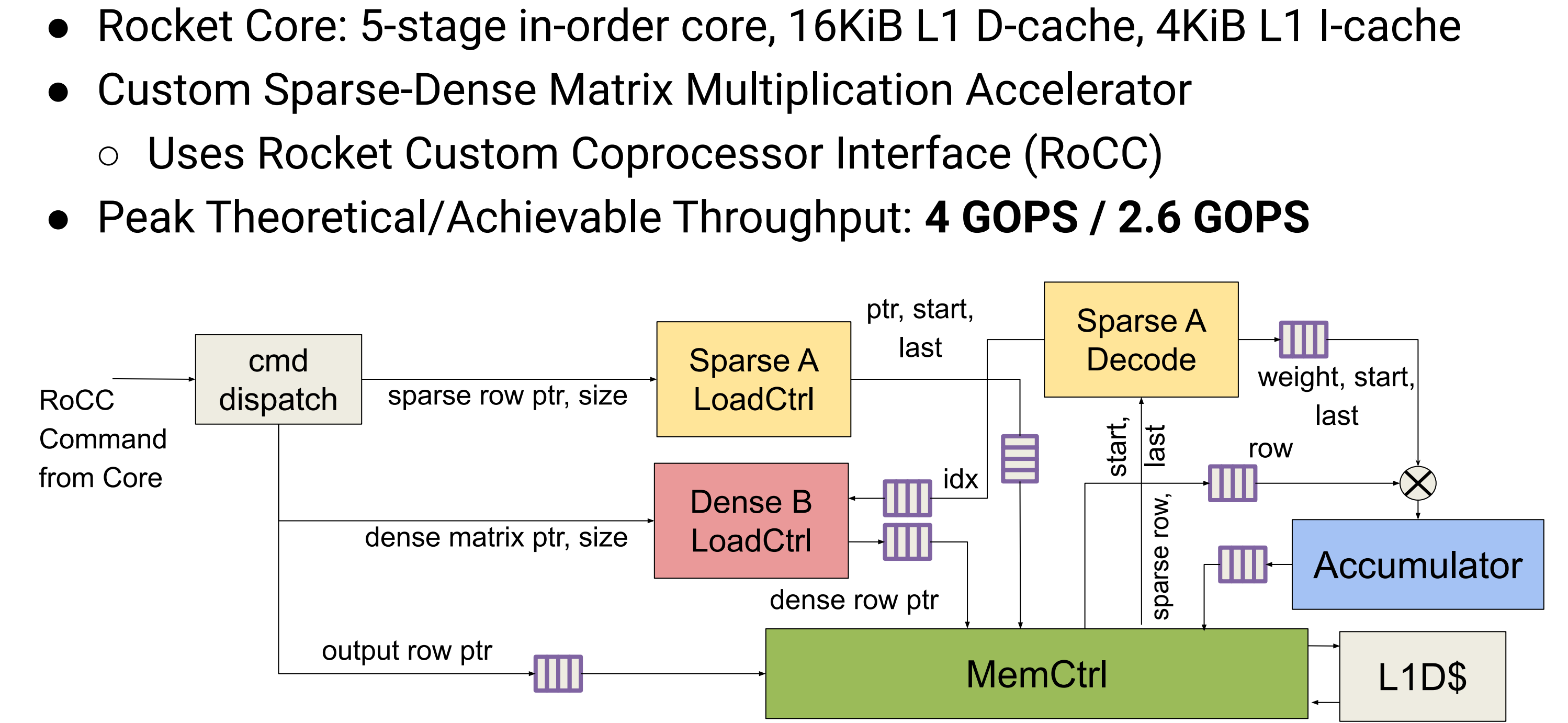
- 2mm x 2mm RISC-V SoC in Intel 16 finFET process
- Network-on-Chip system bus with unidirectional torus topology
 - First tapeout of Chipyard Constellation
- 1 experimental RV64GCB dual-issue core with DSP extensions
 - Prefetcher, Bit-manipulation, Pixel SIMD RoCC (Peak 0.6 GOPS)
- 4 specialized RV64GC Rocket cores
- 512 KiB 8-way-associative second-level cache system (4 banks)
- 16 KiB on-chip scratchpad memory
- Tile-specific clock domain with configurable MMIO clock tree

Clocking

- Off-chip 100MHz clock
- On-chip PLL (0.1~1.2 GHz) with DCO designed by Sean Huang and generated with the Berkeley Analog Generator (BAG)
- Configurable via MMIO and exposed on debug pin



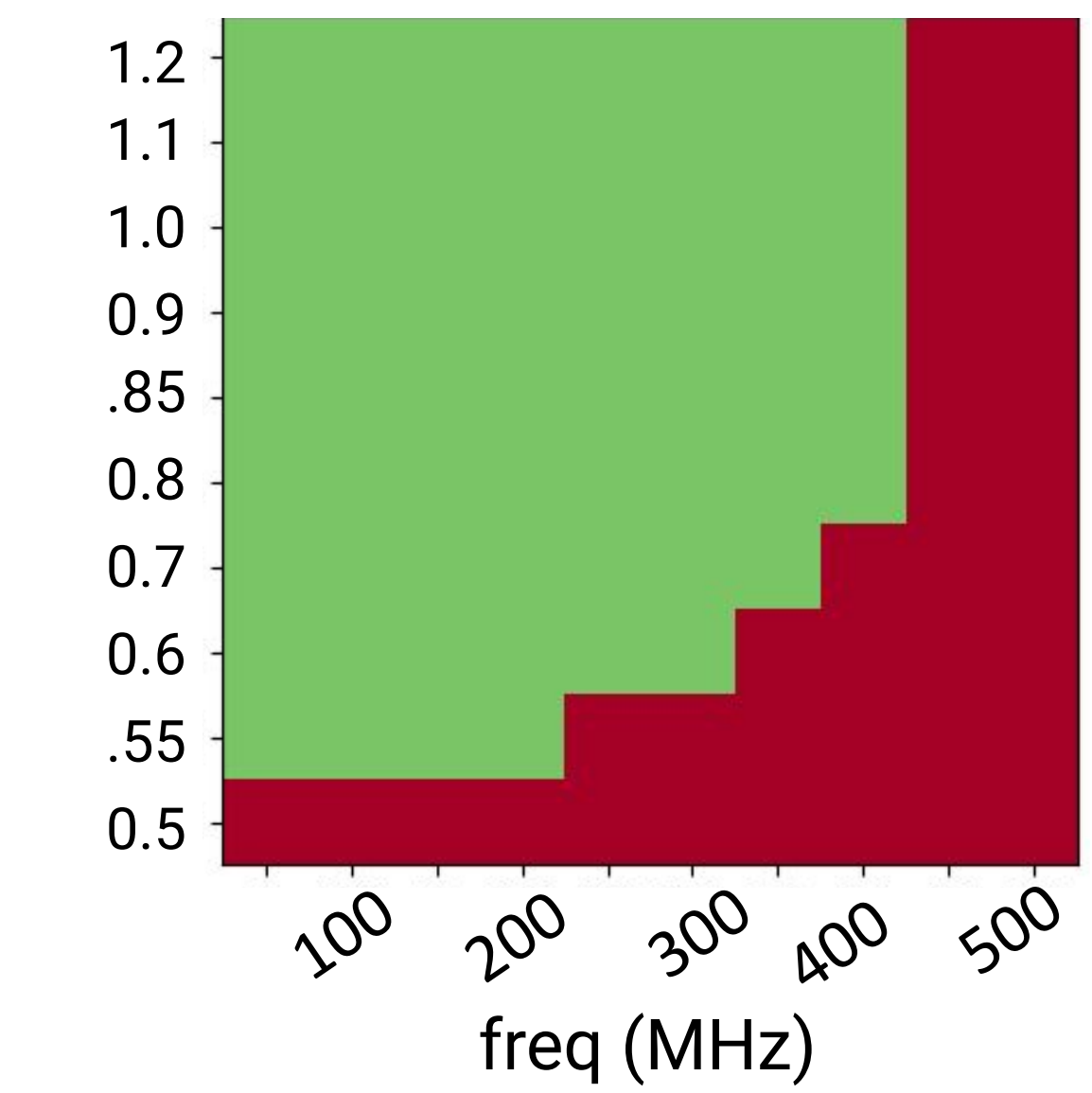
ML Inference Tile



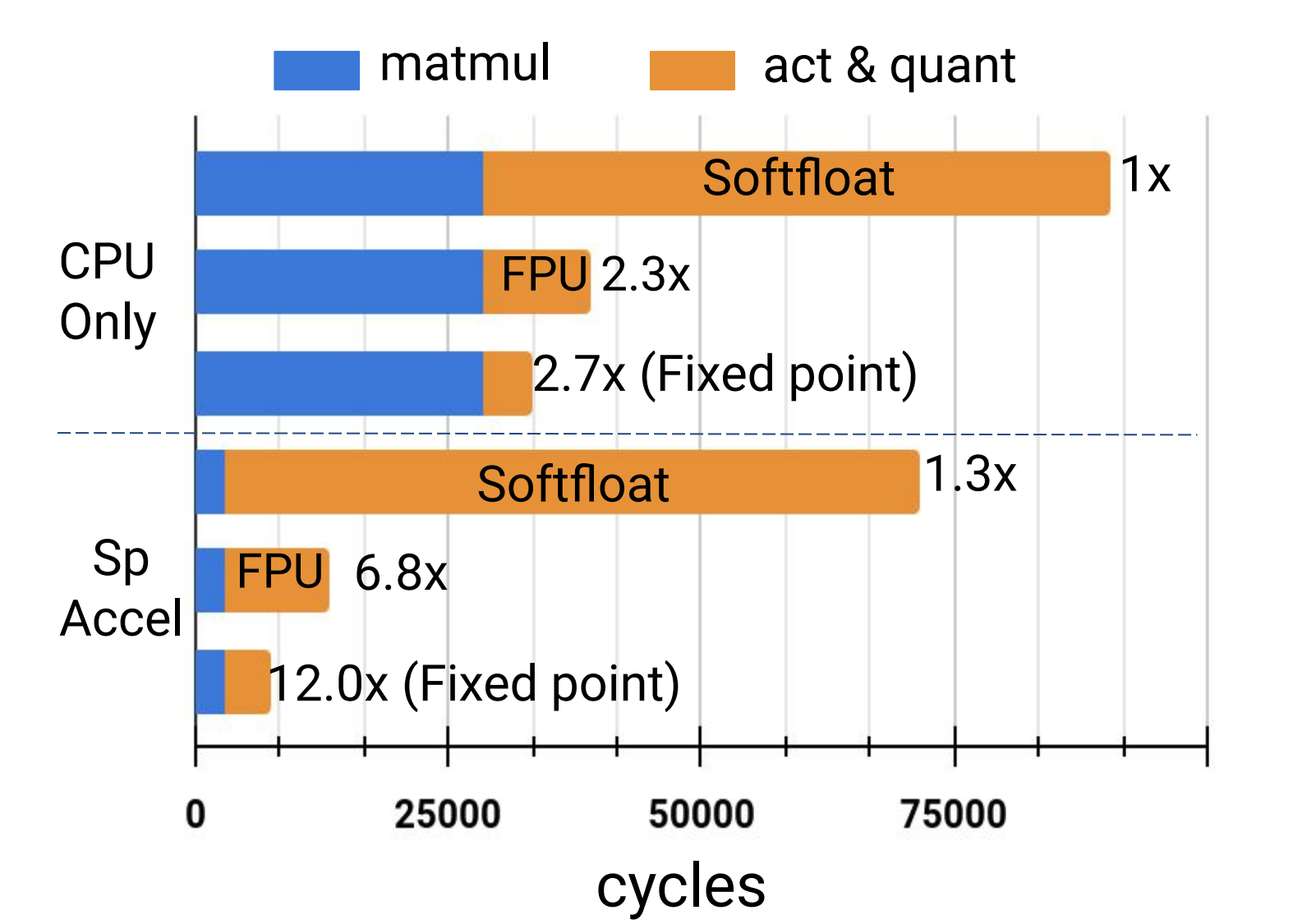
Bringup & Demo

- Test PCB are designed by students in the following bringup class
 - Tested max operating frequency: 400 MHz core clock
- MNIST Demo
 - 32MiB off-chip Flash and 16KiB of on-chip scratchpad
 - 91.23% and 95.42% accurate MNIST, 196x32x10 FC int8 neural net, up to 12x acceleration

Volts BearlyML Shmoo Plot



MNIST Cycle Breakdown



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