A 120-330V, sub-µA, Optically Powered Microrobotic Drive IC for DARPA SHRIMP

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***Abstract*—This work presents a 4-channel, mm-scale, electrostatic and piezoelectric actuator driver that uses < 1 µA total quiescent bias current and can drive actuator loads up to 120-330 V at frequencies over 1kHz. The driver achieves over 99% current efficiency and can operate untethered with an integrated photovoltaic array powered by a collimated or diffuse optical power source. The circuit is demonstrated also as a driver for an off-chip boost circuit, generating over 1.5kV with 85% power efficiency at 45mW load. The system uses a simple 4-bit CMOS logic level interface with 100 kHz clock to actuate high voltage channels; on-chip photovoltaics also power the digital controller, and I/O bus.**

Keywords—microrobotics, MEMs, DC-DC converter

I. Introduction

Micro-robotics and microelectromechanical systems (MEMs) have promising applications in biomedicine, optics, industrial diagnostics, manufacturing, and defense. However, these systems are limited by the need for untethered power delivery and high-voltage electronics that are small, lightweight, and efficient. Micro- and mm-scale mechanical transducers need high voltage to drive electrostatic and piezoelectric actuators, which present as dominant-capacitive loads in the 10pF to 10nF range, [1]. Voltage requirements may be in the range of 30V to a few kV, with drive frequencies between 10Hz–10kHz, [1]–[3]. Wireless power delivery is attractive for MEMs technology, but near-field electromagnetic approaches are limited in range and size. Despite several decades of research in the micro-actuator area, development of power delivery and power management solutions is still nascent and underexplored.

II. Design Overview

This work presents a multi-channel actuator driver in a 650V SOI CMOS process, powered wirelessly by an on-chip (silicon) photovoltaic (PV) array, excited with a collimated (laser) or diffuse light source, or optionally by an off-chip voltage source. Shown in Fig. 1, the system comprises 4 actuation channels, each capable of driving a reactive actuator up to 330V. The system interfaces with an off-chip, low power microcontroller (MCU) which provides a 100 kHz clock and four logic-level CMOS digital control signals. A digital control block conditions the low-voltage signals for a high-voltage level shifter and gate-driver circuit, providing needed deadtime, high-current switching activation, and low-current state-holding modes.

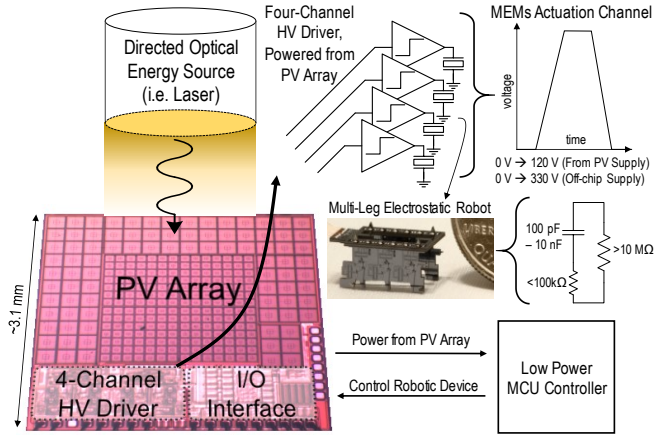

Fig. 1 System block diagram

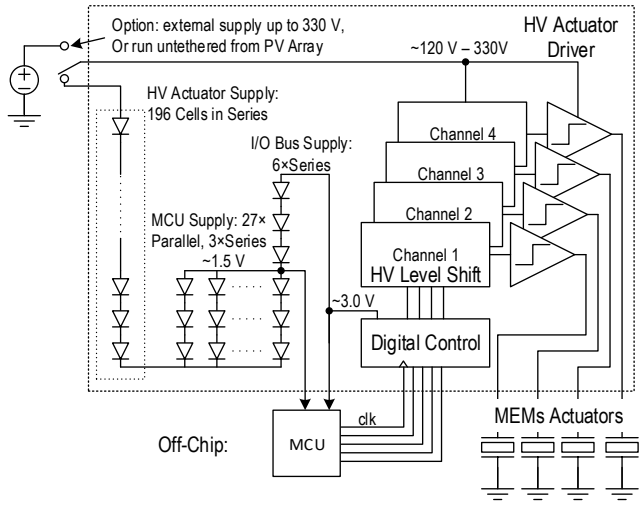

Fig. 2 System detail: on-chip photovoltaics power system control and 4 high-voltage driver channels

Shown in Fig. 2, on-chip solar arrays are used to power on- and off-chip control, the I/O interface, and the high-voltage (HV) actuator channels. The HV array consists of 196 silicon solar cells in series, providing ~120-140V and 0.3-1.7 mW at 1-5 mW/mm^2 optical intensity with measured (~5000K spectrum) optical efficiency of ~11%. The MCU array consists of

3-series × 27-parallel cells with total area ~4mm^2, providing 1.5-1.8V up to 440µW to power an off-chip microcontroller (MCU). A final array is used for the 3.0-3.6V (<1µA) digital I/O bus and controller which uses a stack of three additional cells.

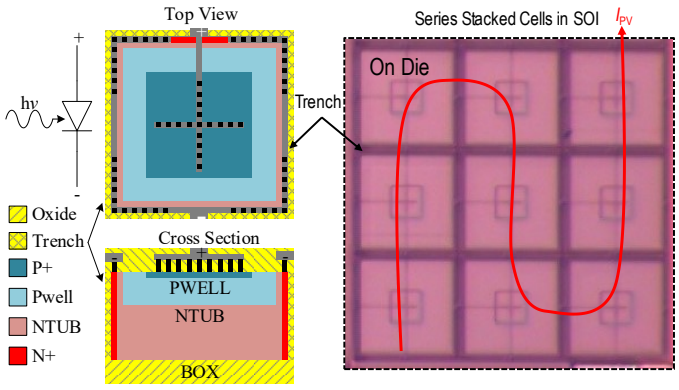

Fig. 3 On-chip photovoltaic cells in 650V trench-isolated SOI CMOS process.

Shown in Fig. 3, PV cells are constructed using SOI trench isolation, such that they can be floated and stacked arbitrarily without junction leakage, similar to the approach in [2]. In the N-well SOI CMOS process, PV diodes are constructed with a lightly doped N- cathode, N+ contacts at the trench edge (N-sinker), a lightly doped P-well anode with P+ contact region; a buried oxide (BOX) completes isolation of the junction. All diffusions and oxides are available in the SOI CMOS process such that no additional pre- or post-CMOS processing is needed.

III. Drive and Interface Circuitry

Key on-chip circuit components include an I/O interface, digital logic and a state machine controller to synchronize pulse driving, a low-power current reference block, and four actuator drive channels. Due to very limited power availability and a desire to use available energy efficiently, each of these circuit components were designed to operate with very low quiescent power overhead. Fig. 4 shows the actuator driver circuit comprising a high-voltage level shift circuit and class-B powertrain. The class-B powertrain uses 330V quasi-vertical DMOS devices; an NDMOS pulls the output low with a gnd-referenced drive signal; a HVPMOS pulls the output high with a drive signal referenced to the high-voltage supply, VDDH.

The HV level shifter works by using a low-voltage, current DAC and floating 'accordion' OTA to control the HVPMOS. The gnd-referenced NDMOS is driven on the I/O bus supply with deadtime to prevent cross conduction in the output stage. To drive the HVPMOS, the current DAC sinks differential current through an NDMOS cascode and a diode-connected, low-voltage PMOS-NMOS pair referenced to the system high voltage (HVDD). The V_{ON}* and V_{OFF}* signals in the diode-connected pairs are amplified through the accordion OTA structure to drive the HVPMOS gate. The current DAC uses two weighted current sources, mirrored from an on-chip 180 nA current reference; the HCon/off gates control a multiplied current source (~900 nA) to switch the HVPMOS gate quickly; the LCon/off gates control a ~90 nA current source which is used to hold the state of the PMOS gate after switching.

A leakage clamp circuit is used to prevent voltage overstress on the current DAC circuit during its 'off' state. The leakage clamp uses diode connected devices between the source and gate of the high voltage NDMOS cascodes. When a respective current sinking branch is 'off,' the clamps provide a path for residual leakage current (<<1nA in the NDMOS) to flow to vdd, and maintaining a reasonable voltage on the current DAC devices.

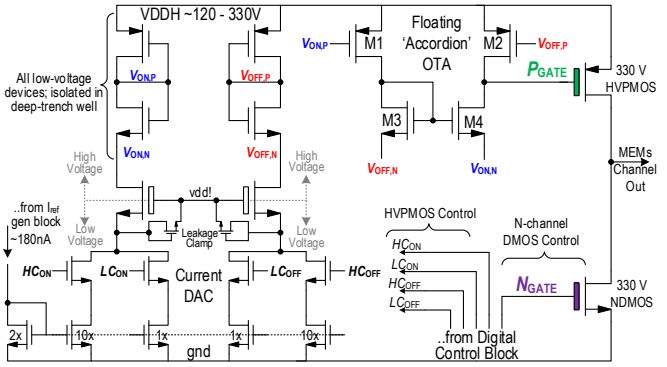

Fig. 4 HV level shift and class B powertrain

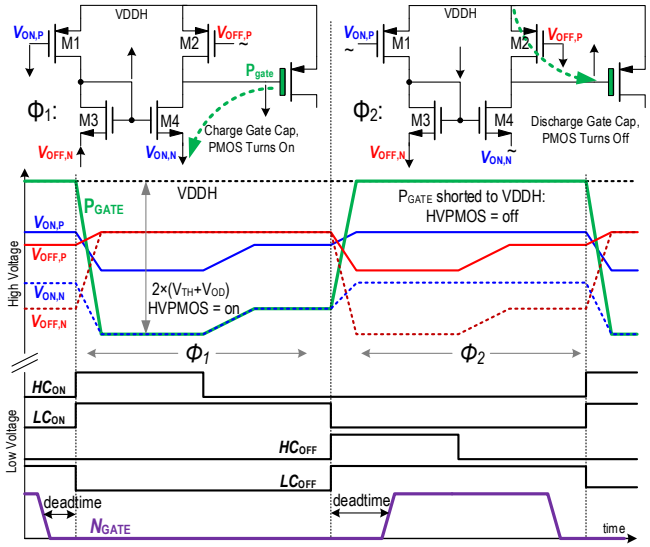

Fig. 5 Representative signals and timing diagram for floating OTA circuit

Shown in Fig. 5, in Φ_1, the HVPMOS is turned on. The HC_{ON} and LC_{ON} signals are high, while HC_{OFF} and LC_{OFF} are low, pulling down nodes $V_{ON,N}$ and $V_{ON,P}$ and floating $V_{OFF,N}$ and $V_{OFF,P}$. Signal $V_{ON,P}$ turns on M1, which pulls up the gate of M3 and M4; this pulls up the source of M3 ($V_{OFF,N}$), and pulls up $V_{OFF,P}$, the gate of M2, turning it off. With $V_{ON,N}$ also pulled down by the current DAC, M4 turns on, allowing the current DAC to pull down P_{GATE} turning the HVPMOS on. In Φ_2, currents and voltages are reversed. $V_{OFF,N}$ and $V_{OFF,P}$ are pulled down, while $V_{ON,N}$ and $V_{ON,P}$ are floated. This pulls down the gate of M4, turning it off; M2 pulls P_{GATE} to VDDH, turning the HVPMOS off.

Cross-coupling of the diode connected signals in the accordion OTA merges the gain of the PMOS differential pair and the NMOS current mirror, increasing gain, slew rate, and rise/fall time. Rather than using a a floating regulator to create a separate voltage domain referenced to VDDH, the HVPMOS drive reference is set by the diode-connected NMOS/PMOS threshold + overdrive, which tracks the HVPMOS over process and temperature. In the HC_{ON} state, the HVPMOS gate is charged at roughly $3\times V_{TH}$ or ~2.4V; in the LC_{ON} state, it is held at 2×VTH or ~1.6V. Thus, the dominant source of power consumption in the circuit is the 90nA quiescent current bias drawn from VDDH during the LCon/off states, and the needed gate charge of the HVPMOS during the turn on/off transitions.

The proposed level shifter has several advantages compared to previous techniques. Most contemporary level shifters use latching structures or simple 'pull down' networks to actuate floating high-voltage devices. Latching structures require multiple cascode stages and (typically) additional voltage rails that must be regulated (i.e. linear regulation stages that require additional quiescent bias current). Pull-down networks (e.g. [2]) often require high quiescent current and it can be challenging maintain a desired pull down voltage level. The proposed level shifter can be viewed as a compromise between these approaches. It achieves high gain through the accordion OTA such that low quiescent current may be used, however no additional voltage references are needed and the design eliminates the second set of cascode devices often required in latching structures.

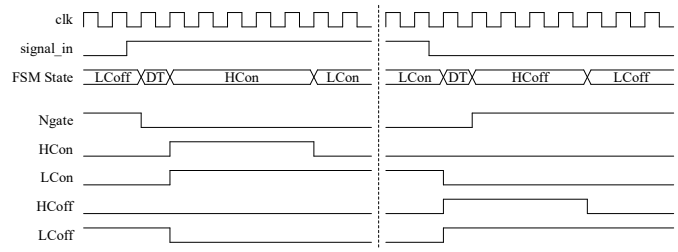

Fig. 6 Timing sequence for I/O and pulse sequencing state machine.

Fig. 6 shows the timing sequence for the I/O interface and synchronous state machine used to construct the drive signals for the circuit in Fig. 5. The I/O channel comprises 4 logic level bits (*signal_in*), each representing the desired state of one of the HV actuation channels, and a single 100 kHz clock. Following assertion of one of the logic level inputs, on a following rising clock edge, the N_{GATE} signal goes low (turning off the low-side NDMOS). On the next rising clock edge (deadtime being one full clock cycle, ~10µs), the HC_{ON} and LC_{ON} bits are asserted to initiate switching the HVPMOS. The HC_{ON} signal is assered for a duration of 5 full clock cycles (~50µs), after which it goes low and switching is presumed to be completed. The LC_{ON} signal remains asserted until *signal_in* goes low, at which time a similar process is completed for the high-low transition. Due to state machine requirements, the maximum drive frequency is limited to $1/6^{th}$ of the clock frequency, however the clock frequency can be adjusted with some benefits for higher or lower frequency operation as needed up to a maximum tested limit of ~1 MHz.

IV. Results and Discussion

Fig. 7 shows the die photo of the prototype. Total area of the chip was just under 10 mm^2, the majority for on-die photovoltaics. The HV array used 196 series-connected cells, each cell being ~120µm×120µm including the dielectric trench. The MCU array (used to power an off chip microcontroller) cells were slightly larger at ~220µm×220µm. Active circuitry, including four HV drive channels, digital control, I/O, current reference circuitry, and on-chip bypass capacitance for the I/O rail was roughly 1.5 mm^2. *The only needed off-chip component is a single off-chip bypass capacitor for the VDDH supply*.

Fig. 8 shows the test setup and example transient operation of the HV driver chip. All low-voltage circuitry was powered by the PV array, which in testing was powered by a white-spectrum fiber light. Two main test configurations were used: one which used the on-chip HV solar array to power the HV actuator drive channels, and one test setup where an external (300-330V) DC voltage supply was used to power the HV drive channels. An example oscilloscope screen shot is shown of a single HV channel driving a 40 pF load at ~125 Vpp and 100 Hz.

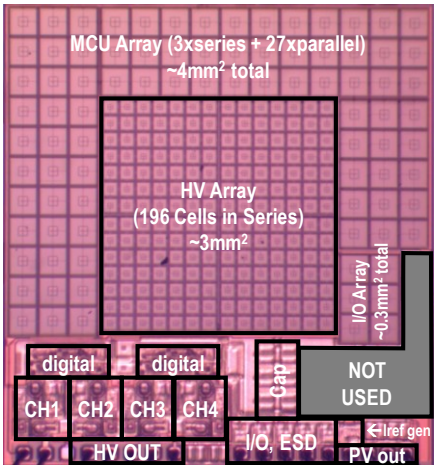

Fig. 7 Die photo: total area ~10 mm^2.

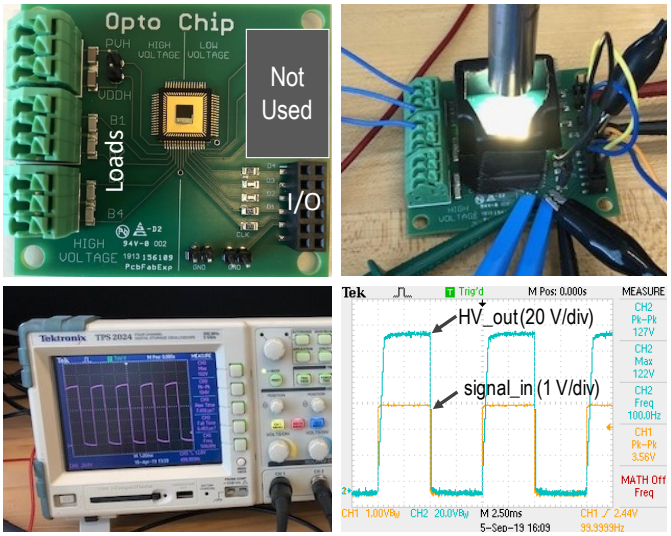

Fig. 8 Test setup and example transient operation with opto power source.

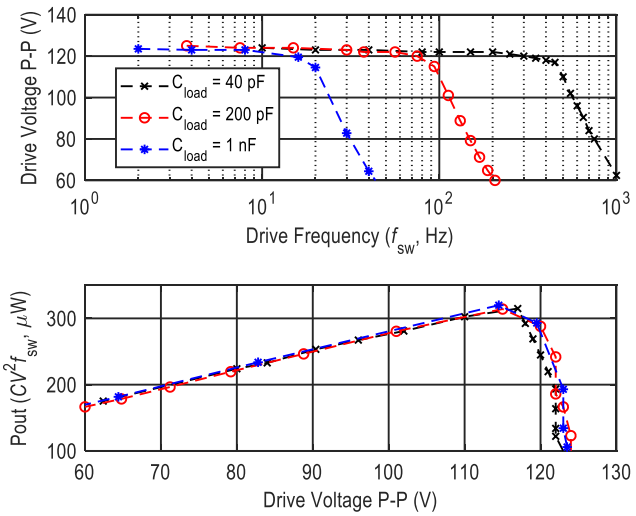

Fig. 9 Measured data with PV power source @1 mW/mm^2: drive voltage peak-peak vs drive frequency with different load capacitance; reactive output power, CV^2f_{sw} vs drive voltage.

Fig. 9 shows measured data for the system operating untethered with an optical power source at ~1 mW/mm^2 (one sun). The HV array provided roughly 125V (open circuit) and up to 330µW maximum power (roughly 11% optical efficiency, which includes area overhead for the trench isolation and metal routing in the array). The peak-peak drive voltage provided to various capacitance loads was ~125V at low frequency; however at higher frequency, the power limitation of the PV array causes this peak voltage to decrease. For example, with a 40pF load, the peak drive voltage remains over 120V up to 300 Hz; for a 1 nF load, the peak drive voltage starts to decrease at around 20 Hz. Plotting the reactive power delivered to these well calibrated capacitive loads vs drive voltage shapes out the power-voltage curve for the HV solar array.

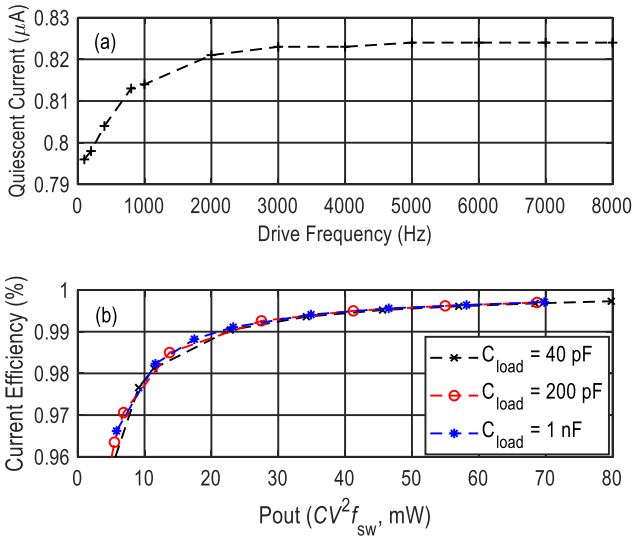

Fig. 10 Measured data with external supply: (a) quiescent current of entire chip (all four drive channels) vs drive frequency, (b) current efficiency versus reactive output power for different load capacitance values.

Fig. 10a shows the measured total quiescent current of the system (all four channels active) vs drive frequency, validating sub-µA operation across the full range. Fig. 10b shows measured current efficiency of the system. Current efficiency is measured as total charge delivered to the reactive load over total current drawn from the VDDH supply (η_I=$C_{load}V_{drive}f_{sw}/I_{total}$). Similar to comparison metrics for linear voltage regulators, this metric was used to highlight the low quiescent power consumption relative to the inherent CV^2f_{sw} losses in the hard switching driver. Current efficiency was measured over ~99.5% for reactive power over 40mW, remaining over 95% down to 5mW.

In addition to operation as a direct actuator-driver, the system was configured and tested as a switching power stage for a high-voltage boost DC-DC converter. Shown in Fig. 6, two-channels of the HV driver were configured to drive the inputs of a 5× differential Dickson voltage multiplier, [4]. The boost stage uses a configuration with small (0402), high-voltage diodes (BAS521LP) and capacitors with increasing voltage rating (all COG dielectric). The boost circuit was off chip on a PCB with size ~5mm × ~14mm (~0.7 cm2).

Fig. 12 shows measured data for the boost converter, powered directly from a ~310V external voltage supply. The converter powertrain operated at ~1kHz to actuate the voltage multiplication stage. The system output voltage achieved levels of ~1.5kV; power conversion efficiency (P_{out}/P_{supply}) was up to 85% at delivered DC power of 45mW. Operating directly from the on-chip PV array with incident optical power of ~5mW/mm^2, the boost circuit achieved voltages up to 600V and peak output power over 1.4 mW.

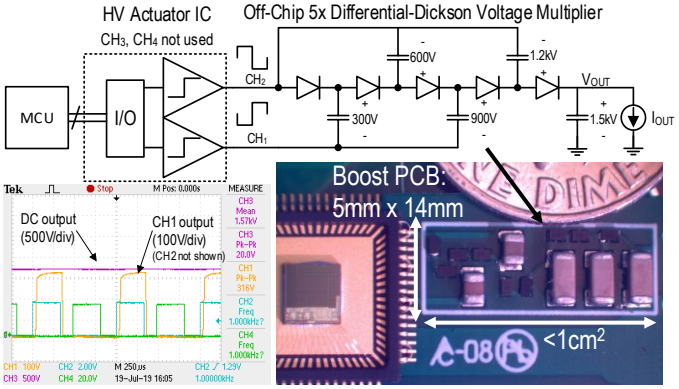

Fig. 11 Circuit, test setup, and oscilloscope screen capture of HV boost circuit.

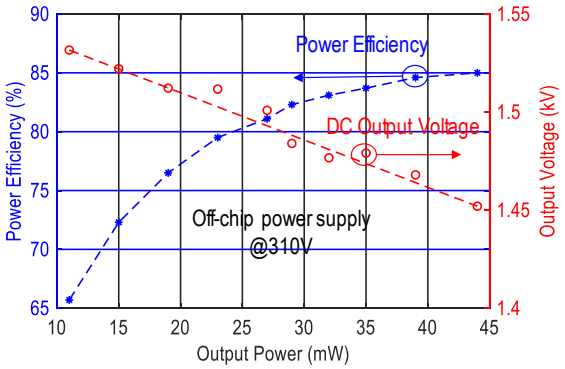

Fig. 12 Measured data for ~300V:1.5kV boost DC-DC operation; ~310V input provided by external voltage supply.

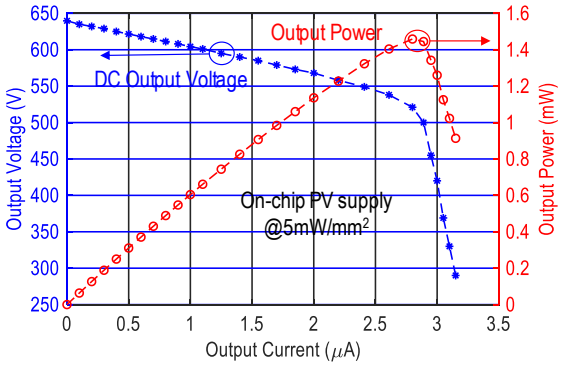

Fig. 13 Measured data for 5× Dickson boost circuit operating from on-chip PV power supply with ~5mW/mm2 incident optical power.

V. Conclusion

This work presented a fully-integrated, optically powered actuator driver for MEMs and micro-robotics. The system used multiple on-chip photovoltaic arrays to power all on-chip circuitry, each of four HV actuation channels, and an off-chip microcontroller. With untethered, 1mW/mm^2 optical power delivery, the system was able to drive capacitive loads up to 125V at frequencies of hundreds of Hz. The system used sub-μA quiescent power to achieve current efficiency over 99% across a wide range. Operated as a half-bridge driver for an off-chip boost circuit, the system provided up to 1.5kV from a ~300V supply at 85% conversion efficiency at 45mW load power. While there has been little past work in the area of power electronics for MEMs and micro-robotics, this work shows a promising direction for future exploration.

VI. Acknowledgements

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VII. References

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