Tapeout class: taking students from schematic to silicon in one semester

David C. Burnett, Brian Kilberg, Rachel Zoll, Osama Khan, Kristofer S.J. Pister
Department of Electrical Engineering and Computer Sciences, University of California Berkeley, Berkeley, CA 94720
Email: {db, bkilberg, rachelzoll, oukhan, pister}@eecs.berkeley.edu

***Abstract*—In the spring of 2017, the UC Berkeley department of EECS introduced an innovative new course: "28nm SoC for IoT." This course went far beyond schematic-level design typical of circuits education and resulted in a chip going out for manufacturing. Ten students with no prior IC experience, nine undergraduate and one graduate, designed and laid out an SoC in ST 28nm FD-SOI CMOS including a 2.4GHz transceiver, baseband filtering, ADC, Bluetooth MAC, a RISC-V CPU, and internal power regulation. The transceiver, baseband, ADC, and power regulation were successfully fabricated. This paper discusses the instructors' experiences and results with this course.**

I. Introduction

A. Motivation

The minimum size of a low-power standalone electronic system is usually dominated, besides its energy source, by the material needed to connect the system's components, e.g., the PCB. This also sets lower parasitic limits, which in turn set a lower bound on power consumption. Interposer advances allow tighter integration of disparate integrated circuits; however, current and future applications demand even further reductions in size. As a result, students intending to go into industry increasingly need to be prepared for extensive on-die design and integration. Present undergraduate and graduate coursework in this area is limited in its "reality" insofar as the vagaries of IC design and manufacturing are concerned.

In order to augment existing IC design coursework at UC Berkeley, we created a course to teach the development of mixed-signal wireless ICs, along with all aspects of IC development often not included in the classroom. The core goal of this course was to design and fabricate a real chip, in a real process, with a real deadline, to provide students with the most realistic SoC design experience possible.

This design experience included both interpersonal and technical elements. On the interpersonal side, we invited students to contribute to a larger team, and to deliver a design for which they alone were responsible. We emphasized clear communication of relevant performance metrics and design challenges through presentations and written documentation, as well as keeping to a semester-long project schedule. On the technical side, students with no past chip experience produced an extremely complex system that would give even accomplished IC veterans pause. Students went beyond their existing circuit education to produce designs which accounted for non-ideal power sources, included on-chip reconfigurability, designed with limitations from the outside world such as ESD and latch-up, and complied with the foundry's design rules. Along the way, we introduced students to industry-standard digital design & synthesis tools from Cadence, Mentor Graphics, and Synopsys in a real production environment which had bugs and inconsistencies; in contrast, polished academic generic process design kits tend to be free of those quirks.

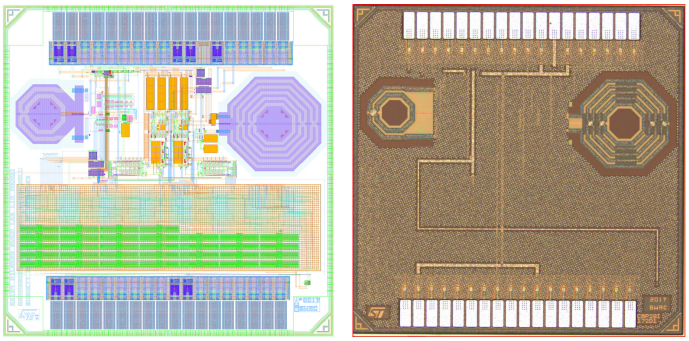

Fig. 1. Final results of class project, measuring 1.1mm x 1.1mm. Left: screenshot of final layout including 2.4GHz transceiver & power regulation in top half, and microprocessor in bottom half. Unfortunately, synthesized digital elements in bottom half were not completed in time for fabrication. Right: photo of die produced from accepted GDS, including transceiver and hand-built scan chain for debugging.

B. Course background

This course was first offered by the University of California, Berkeley, in the Department of Electrical Engineering and Computer Sciences during the Spring 2017 semester. Titled "28nm SoC for IoT," the purpose of the course was to introduce students to the challenges of modern IC development by having them design a complete 2.4GHz transceiver and fully-featured microcontroller in a modern process, verify and integrate functionality, and send the design out to be manufactured. The chip was to be capable of satisfying Bluetooth Low-Energy (BLE) physical (PHY) and media access control (MAC) layer specifications [1] in hardware, and the rest of the BLE stack in software. The course consisted of 10 enrolled students (9 undergraduate, 1 graduate), each of whom had done well in at least one pre-existing electrical engineering undergraduate circuit design course: analog circuit design, digital circuit design, or RF circuit design. Three instructors were involved: David Burnett, graduate student instructor; Dr. Osama Khan, postdoctoral lecturer; and Prof. Kristofer S.J. Pister, faculty advisor.

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By nature, the course was structured differently than a typical electrical engineering course. Instead of assigning every student or small group of students identical labs and projects throughout the semester, the instructors presented a high-level architecture of a wireless system-on-chip (SoC) on the first day of instruction. This architecture included everything necessary for an internet of things (IoT) device: RF components such as impedance match, mixer, and RF oscillator in an architecture based on our group's crystal-free radio work [2]; analog components such as baseband filtering & amplification, digitization, voltage regulators, and bandgap references; and digital components such as clock and data recovery, a Bluetooth Low-Energy MAC core to handle packets (based on Sahar Mesri's IEEE 802.15.4 MAC [3] and the Nordic nRF series BLE MAC [4]), and a microcontroller with RISC-V processor [5] generated with Rocket-chip [6], based on the Freedom E300 platform from SiFive, Inc [7] and written in CHISEL [8]. From the presented architecture, students volunteered to take responsibility for various blocks according to their background and interest. We were lucky: with 5 students choosing analog/RF blocks and 5 students choosing digital ones, there was enough interest and experience to handle the minimum of components to complete the basic system.

The project was initially intended to fit in 1mm x 1mm of multi-project wafer (MPW) silicon sourced from a commercial vendor but, early in the semester, that vendor discontinued their MPW service. Fortunately, STMicroelectronics donated 1.1mm x 1.1mm of silicon in their 28nm fully-depleted silicon-on-insulator (FD-SOI) process [9] for use in the class, in the existing context of their collaboration projects with UC Berkeley. Once the project was completed, the GDS was submitted to ST for manufacturing. The resultant chip is displayed in Figure 1.

II. Overcoming student misconceptions

In a traditional engineering course, the final project is due at the end of the semester and demonstrates your skills as an engineer. In this course, by far the most challenging aspect was convincing students that their individual "project" e.g., the filter, or oscillator, or synthesized digital module, or other block, needed to be ready very early and was only the beginning of a larger integrated whole requiring significant effort to complete. This was one of many misconceptions about engineering work that academia tends to emphasize to students; examples of others are as follows:

- "99.99% is an A": students need to understand that where design rules are concerned, many foundries will simply not accept chips with nonzero design rule check (DRC) errors. We also observed students failing to investigate absolutely all layout-versus-schematic (LVS) errors or even disagreeing with the tool, where poorly-understood LVS errors can be catastrophic.
- "Performance is my only benchmark": students can benefit from a more holistic view of design with more focus on functionality and integration and less on meeting spec perfectly across process corners or accounting for rare or avoidable edge cases. The tendency to spend valuable hours practicing perfectionism resulted in weeks of timeline delays and loss of design integration and verification time.
- "My block is my only concern": it was a distinct challenge to convince students to anticipate interfaces with other blocks, or to demonstrate two or more of their blocks operating together.
- "Late is OK": the fabrication deadline is fixed. "Reduced functionality and on-time" is much more preferable to "late but fully-featured". This is the opposite to how project grading and late penalties are structured in most courses.

Our initial failure to motivate students to avoid these issues led to a severe timeline distortion. The intended design schedule was first upset by needing to change processes. Then, as the semester progressed, students were a little late with each design stage. This lateness compounded and, by the end of the semester, we had barely begun top-level chip assembly. After the end of the semester, the teaching assistant and a few students were able to devote time to the chip between research and internship commitments until it was finally finished. We were lucky that the GDS due date was well after the end of the semester, or the tapeout would have been a total miss.

III. Teaching assistant to project manager

While students needed to approach this course differently, instructors also needed to modify their approach to this course in order to make it successful. This was particularly apparent in the role of teaching assistant (TA). The TA's traditional roles in guiding labs or emphasizing lecture material were replaced with responsibilities such as managing overall schedule, making high-level decisions about chip organization, and forecasting & preventing roadblocks. These roles are more traditionally associated with those of a technical project manager.

The TA was also responsible for using his design experience to advise students about upcoming tapeout steps. As discussed in Section II, students initially focused predominantly on their own blocks to the exclusion of all else. Soon enough, the students began to focus on practical design considerations which most courses don't have time to explore: V_t mismatch, floorplanning, designing with real voltage, current, and frequency sources, defining interfaces and tuning, designing for test, accounting for parasitics, etc. By the end of the course, our students had learned to think about their designs in the bigger picture and to understand that schematic results are just the start of a physically-realizeable circuit.

Most of the TA's unique responsibilities were carried out continuously during the semester through weekly revisions to schedule, reminders about future steps, and emphasis on multi-block integration. Near the end of the semester it became clear that bugs in our digital synthesis tool flow would not be resolved in time. Assuming the IC would lack a microprocessor and digital peripherals, the TA led implementation of backup

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plans to allow testing of what had already been successfully put down in layout.

The most significant new TA challenge was a lack of expertise in the course material. The diversity of subsystems that go into a wireless SoC makes it unlikely to find a single person qualified to advise on all design aspects. Instead, the TA tapped resources outside of the course, usually other graduate students, to advise design of a particular block. We were grateful to find 11 such individuals, enumerated in the Acknowledgement section, to provide their expertise to our students.

IV. Results

Our students put an incredible amount of effort into this class and it showed: at the end of the semester, we successfully taped out and submitted the design to the foundry. Issues with our digital synthesis toolchain led to synthesized components not making it in time for this semester's fabrication deadline. A screenshot of the layout including synthesized digital components is shown on the left side of Figure 1 and a photo of the manufactured design, lacking synthesized digital, is shown on the right. A block diagram of the project's final form, though lacking detail on the digital components, is given in Figure 2. The components successfully taped out include:

- 2.4GHz Bluetooth low-energy compliant transceiver
  - RF frontend matched to off-chip antenna
  - Power amplifier
  - Differential IQ passive mixer & 4.8GHz LC tank
  - Low-IF baseband amplification, filtering, and ADC
- Power management of entire chip from a single unregulated supply
- Microcontroller w/ custom digital peripherals in CHISEL (DRC & LVS clean but not fabricated)
  - 32-bit RISC-V processor & 64kB SRAM
  - Bluetooth packet handling
  - GFSK oscillator modulator
  - Clock & data recovery

At time of writing, preliminary tests of the chip indicate the power regulation is functioning. Testing is ongoing.

A. For future tapeout courses

As we reflect on the strengths and weaknesses of the semester, we have a few specific future recommendations. It is our hope that these recommendations will help future courses like this one, including our own.

- More meetings: partway through the semester, we devoted an hour each week to coordination meetings for analog and digital teams. Progress markedly improved. These meetings should have begun on the first week.
- Foster collaboration: students will seldom meet on their own but, when called together by instructors, will stick together and continue working well after the called meeting. We fostered this tendency by scheduling the aforementioned one hour analog or digital coordination meetings but reserving the room for two hours. After the instructors left, students continued to hammer out their designs.
- Devote in-class time to progress presentations: about halfway through the semester, every student was expected to present for at least 5 minutes per week, every week. This was essential for keeping everyone up to speed on project development, while motivating students to make progress. Early in the semester, we spent a lot of time giving lectures and assigning homework in pursuit of fostering a better understanding of wireless communication. However, because all enrolled students had already demonstrated proficiency in one of the foci necessary to enable this project, much of this background was not necessary to start individual block design. In the future, theory lectures can likely be moved to later in the semester and early lectures should focus on giving students a thorough system overview.
- Grading structure: We were, perhaps, too reliant on students' intrinsic motivation and placed a low emphasis on assigning tasks with clear grades attached. Future courses should include frequent graded milestones with stiff penalties for lateness to emphasize the need for a quick, "good enough," solution instead of a late, better, one. In general, grading emphases should resemble performance reviews in industry, including timeliness, communication responsiveness, and cooperation.
- Demand deliverables: there are a few specific milestones which students should be made to take seriously via grading structure. Every student should produce:
  - System-level considerations & design: all interfaces for their block, including power, and must either terminate at a pad or match an adjacent student's interface exactly,
  - System block diagram: their concept of the whole system and where theirs fits in,
  - Design review: this semester, several blocks escaped a critical eye by accident. All should be reviewed by an expert before progressing too far in design, and
  - Performance measurements: make sure students demonstrate their block works as advertised.
- Hide buffer time in the schedule: we were able to manufacture a chip in large part because we never discussed the foundry's true due date with students. Instead we opted to build tolerance into the schedule and kept students aiming for an earlier deadline.

Regarding curriculum, as noted above, we attempted to teach wireless communication background early in the course. We speculate that early lectures could be better spent teaching ICs from the outside in to introduce the real-world issues students will need to consider in their designs. These include the voltage levels and communication protocol (commonly JTAG) of the test equipment , mechanical design considerations of the PCB, parasitics of wirebonds and pads, ESD prevention and input/output pad drivers, high-voltage IO MOSFETs vs core voltage MOSFETs, and prevention of latchup and antenna

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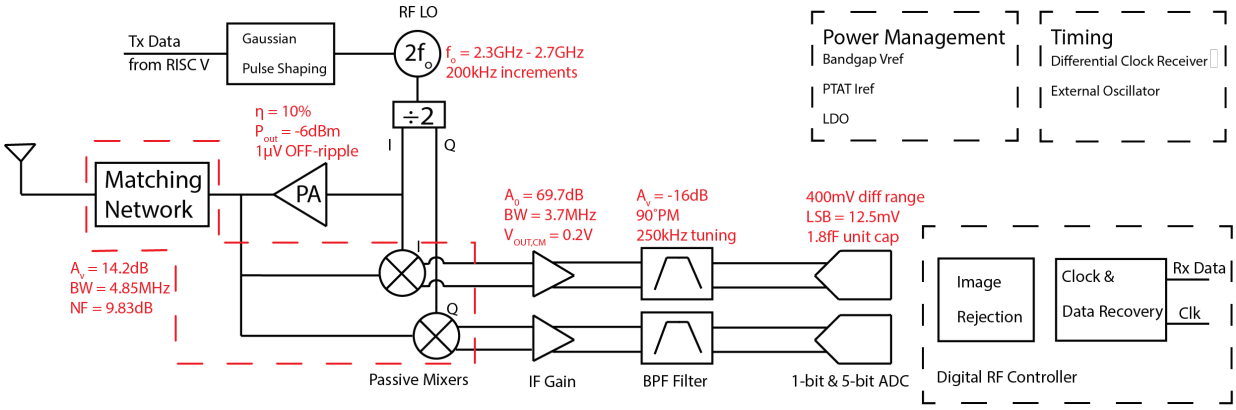

Fig. 2. Block diagram of class project including simulated performance annotations in red. Digital blocks not pictured: RISC-V microprocessor, memory, DMA, and BLE MAC. Also included on chip but not pictured: clock receiver, courtesy of Pi-Feng Chiu.

violations.

B. Feedback

The course has generated a significant amount of interest (and initial skepticism) from the local UC Berkeley community. We had approximately 10 extra graduate students auditing it off-and-on throughout the semester. It has since been a popular subject of conversation among the graduate and undergraduate communities, and has been added to the department's Master of Engineering program as a capstone project course for the Physical Electronics and Integrated Circuits track.

We surveyed the students at the end of the semester and asked for their anonymous feedback. First, we asked them to rate the necessity of various elements of the course from 1 (could be removed next year) to 5 (absolutely necessary). Our recommendations in Section IV-A were in line with these student survey results, which were read only after Section IV-A was written: weekly in-class presentations and analog/digital coordination meetings, which were rated 97% necessary and 93% necessary, respectively, were seen as much more necessary than assignments and lectures which were rated 70% and 50%, respectively.

We asked, "if you had more time on this chip, what would you do?" Responses centered around testing, fixing the design, and learning more about the tools.

Unsurprisingly, responses to "how would you change things next year?" and "what will you do differently on your next chip?" were almost exclusively about getting organized sooner and completing individual block design earlier.

Lastly, there were a couple of good student statements that summarize the technical and non-technical outcomes of this course:

> "I learned how to bridge circuit design to system design. I also learned how to design a chip, not just a circuit."
>
> "[I learned about] communication across function-sets of the chip, learning to set expectations, just saying no when things are unreasonable, making a decision even when the direction isn't clear (you just need *a* decision, not *the* decision)"

V. Conclusion

We have taught the first iteration of a unique new design course, pooling talented students successful in prior RF, analog, and digital design courses, to create a cohesive team to design and fabricate a 2.4GHz wireless sensor node.

Many educational institutions already have access to industry-standard semiconductor tools and, even without donated silicon, could offer a similar course on a modest budget. For instance, MPW space in 350nm is on the order of US$1000 per mm^2. It is our hope that any institution wishing to offer a tapeout class will benefit from our experience to more efficiently teach this material.

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