Narrowband communication with free-running 2.4GHz ring oscillators

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***Abstract*—Ring oscillators have area and power advantages over LC tanks, but conventional wisdom is that rings must be locked to a high-Q external reference to be useful in RF communications. In this paper we explore performance of a 2.4GHz receiver incorporating only a free-running ring as a local oscillator. Using a simple technique to compensate for frequency error, we find that a minimum-size ring fabricated in 65nm CMOS and consuming only 105μW is able to demodulate 75% of received 802.15.4 packets and, if the FSK tone deviation is doubled from 802.15.4 spec, packet receive rate exceeds 99.8%.**

I. Introduction

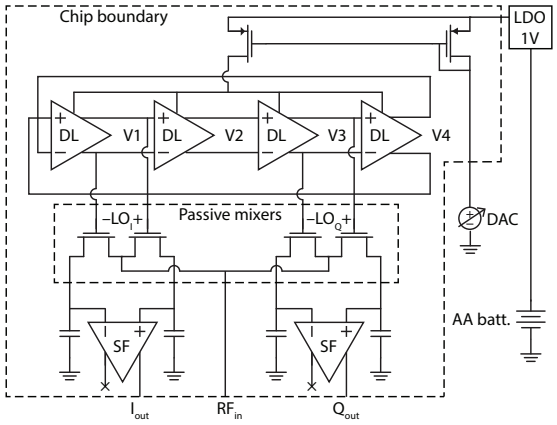
As CMOS communication circuits move from being manufactured as standalone components to being integrated alongside ASICs to add wireless communication functionality, die area and power comes at an increasing premium. Digital components benefit in area and cost from process scaling while analog and RF seldom do. This is owed partially to the large size of the passives analog and RF blocks must utilize. Often, RF designs will save area by using a ring oscillator to generate local RF signals in lieu of a large inductor as part of an LC tank. Removing the filtering capabilities of the resonant tank comes at a significant phase noise cost. Standard wisdom is that a ring oscillator's frequency error is so significant that communication is impossible unless the ring is locked to a high-quality reference via PLL, which requires off-chip references and greatly increases system complexity. In this paper we explore capabilities of a 2.4GHz FSK receiver using neither a resonant tank to reject noise nor an off-chip reference to correct it. Instead, our receiver simply uses a free-running ring oscillator to generate the local RF signal. Furthermore, we investigate narrowband & high spectral efficiency communication performing 1-2Mbit (or Mchip, in our specific case) communication in a bandwidth of a few MHz. Our primary application is satisfying, to the maximum extent possible, the IEEE 802.15.4 specification [1] but these results can be applied to any modulation involving binary frequency shift keying (BFSK). This includes the 802.15.4 standard's offset-quadrature phase shift keying with half-sine shaping (OQPSK-HSS), which is equivalent to minimum shift keying (MSK) [2] as well as Bluetooth Low-Energy's Gaussian frequency shift keying (GFSK) [3].

A. CMOS circuit

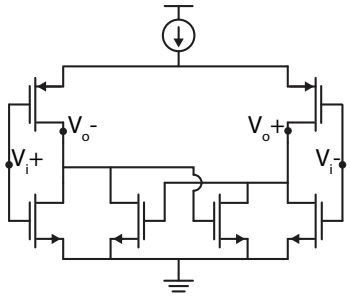
B. Free-running ring oscillators for RF communications

Design of ring oscillators themselves is well-studied, [4], [5] and some standards-compliant frequency synthesizer designs have been based on free-running rings [6]. In wireless sensor nodes, free-running rings or other relaxation oscillators are often used to satisfy timekeeping requirements [7], [8], [9], [10] while some ring designs have been specifically targeted for wireless communications [11], [12]. Radios incorporating free running LC tanks have been demonstrated to demodulate OOK [13], [14] and standards-compatible FSK [15] signals, but lack the compactness and scaling benefits of ring oscillators.

When rings serve as the RF oscillator and left free-running, the radios that incorporate them tend to fall into two modulation categories. The first is OOK [16], [17], [18] incorporating



(a) Overall Circuit



(b) Delay Cell

Fig. 1. Experimental oscillator & NMOS passive mixer structure, as fabricated in a 65nm bulk process, diagrammed in (a). Minimum-size ring oscillator containing 4 differential delay cells (DL) in (b) drives single-balanced passive mixers downconverting RF signal provided by test equipment. Mixed-down intermediate frequency passes into source followers (SF) with high drive strength to pass signal off-chip. Not shown: kick-start circuit to prevent even number of ring stages from latching at power-on.

strategies to compensate for an uncertain LO frequency and typically serves the role of always-on wakeup radio for a higher performance 2.4GHz transceiver. The second is FM-UWB [19], [20] and is usually a complete standalone FSK transceiver but with very wide modulation. Both types of radios have wide IF bandwidths, leading to low sensitivity which must be augmented by significant coding gain and therefore have low data rates. By contrast, our work aims to demonstrate FSK in a bandwidth of a few MHz which can enable higher sensitivities, commercial standards compatibility and, by connecting this ring to a transmitter, symmetric communication.

II. Background

A simple experimental ASIC in 65nm bulk CMOS was designed and fabricated consisting only of mixer, output buffers, and the oscillator under test as illustrated in Figure 1(a). No LNA and no baseband filtering or amplification was included. The oscillator is a 4-stage differential ring oscillator; topology was chosen with an eye toward use in a differential IQ receiver. Each of the ring's four delay cells contained a pair of inverters with cross-coupled NMOS, as drawn in Figure 1(b), to provide additional gain and enforce opposite sides to have opposite phases. Transistors were sized at minimum (PMOS devices at 2x minimum size to account for differences in carrier mobility). Minimum size was chosen to give worst-case phase noise behavior at best-case current consumption, with the knowledge that the measured phase noise results could be improved with increased width & power [21]. The ring drives the NMOS mixer gates with approximately 800mV swing at 1V VDD and 105μA input current. The ring can be tuned over a range of about 1.6GHz to 2.6GHz, limited by the current mirror devices. In the vicinity of 2.4GHz, frequency can be adjusted by 100kHz by changing the current mirror bias by 101nA (or 84μW). The resultant 2.4GHz signals were connected directly to passive mixer gates. This yielded what we believe to be the absolute minimum practical power consumption for a ring of this topology in 65nm CMOS.

A. Simulation

Analytical derivation of phase noise profile is dependent on enough process-specific parameters that an accurate phase noise estimate for a given ring oscillator is impractical [22]. Hence, we move directly to simulation to get a good idea of the ring's performance. A transient simulation, including noise, of the complete circuit in Figure 1(a) was performed for 1ms of simulated time. A histogram of this simulation is given in the left half of Figure 2. The presence of frequency-independent white noise and 1/f flicker noise will result in a phase noise spectrum in the shape of a Voigt profile [23], but for the purposes of using standard tools in this estimate we will approximate it as a Gaussian.

B. CDF prediction

To obtain an initial estimate of performance, we first assume the Gaussian profile represents the frequency distribution when

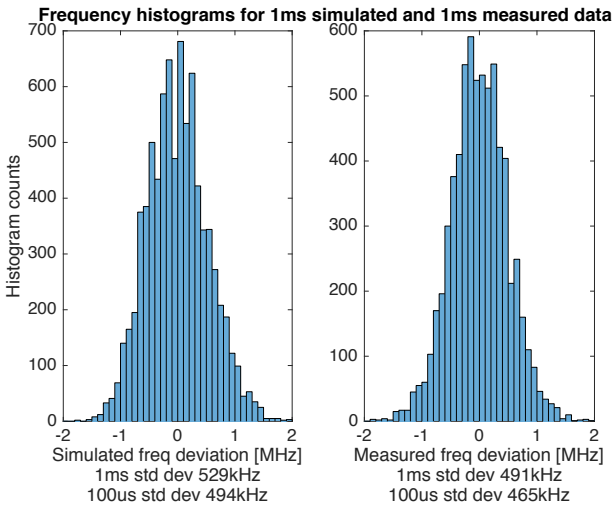


Fig. 2. Frequency histograms for 1ms of simulated data (determined by computational limitations) and a 1ms portion of a 16ms oscilloscope capture. Both frequency distributions were obtained from nominally 8MHz intermediate frequencies resultant from an RF input derived from ideal source (simulation) or test equipment (measurement) mixed with a free-running ring oscillator. Standard deviations, or jitter, indicate that simulation and measurement are in good agreement. Standard deviation value for 1ms is calculated over full histogram period. Standard deviation value for 100μs is mean of jitter over 10 non-overlapping 100μs windows. Note: time-series of frequency data forming measured histogram on right is displayed in top half of Figure 7.

the ring is tuned to a particular frequency. By shifting the mean of that Gaussian a particular distance (to a higher or lower frequency) and overlapping it with an un-shifted one, we can build an estimate of frequency distribution over time. These Gaussians were generated from statistics in Figure 2 and are displayed with frequency distribution from an example data set in Figure 3. These statistics were calculated over time periods of 1ms, whereas each bit decision is made every 1μs (1Mcps) or 0.5μs (2Mcps), both of which will have smaller standard deviations. Hence they will yield somewhat pessimistic estimates, but they nonetheless allow us to obtain a reasonable starting point with which we can compare experimental results.

We assume the ring spends about half of its time tuned to either frequency, which is a good assumption given IEEE 802.15.4 DSSS coding. The cumulative distribution function (CDF) can then give us the probability of incorrectly selecting the wrong bit (i.e., the estimated chip error rate) based on the overlap of the two Gaussians. The 802.15.4 specification defines the sensitivity as the received power which yields a 1% packet error rate (PER) for a 20 byte (or "octet" in the parlance of the specification) packet with 6 byte overhead at a tone spacing of IF+/-0.5MHz or 1MHz total tone separation. A 1% PER can be shown as equivalent to 6.5% chip error rate (CER) [24]. Using this tone separation and setting the CDF decision point to halfway between the two, our simulated standard deviation yields CER=17.2%, implying that no level of RF input power will yield a 1% PER. This is consistent with the data presented later in this paper. Solving for frequency separation instead, we find our simulated ring

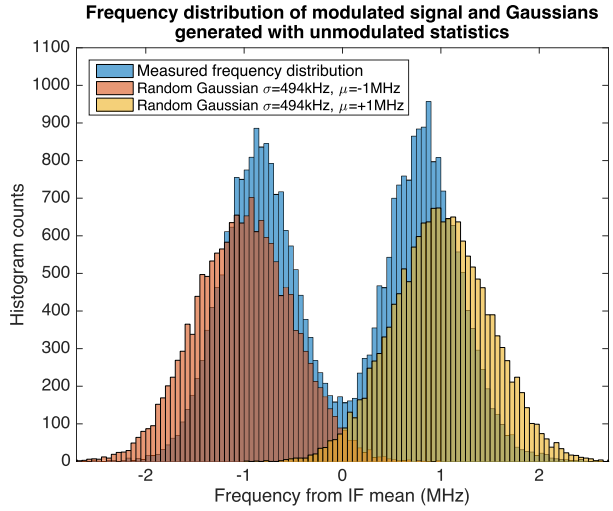


Fig. 3. Distribution of measured frequency for 2Mchip/s and +/-1MHz tone separation. Also plotted are two normally-distributed random values with measured standard deviation 494kHz, as displayed in Figure 2, and means of +/-1MHz. Experimental data has been post-processed to subtract the windowed average described in Section IV and displayed in Figure 4. This subtraction was necessary to expose the two groupings of high and low frequency per FSK modulation. Without, the measured histogram appears homogeneous. The subtraction is likely responsible for the reduction in standard deviation and frequency shift, which is about 375kHz and +/-0.87MHz for each of the two modalities.

oscillator frequency distribution can meet 6.5% CER if FSK frequency shifts are increased to IF+/-0.80MHz or 1.60MHz total separation. Again, this is consistent with experimental data.

III. Experimental Methods

A. Setup

The RF input in Figure 1(a) was connected to a signal generator set to a frequency in the 2.4GHz band such that the intermediate frequency would be in the vicinity of 8-12MHz. Exact tuning of the IF was not possible due to the random frequency changes of the free-running oscillator. Neither signal generator nor ring oscillator frequency (i.e., ring oscillator current mirror bias) were adjusted over the several hours during which data was taken and the IC was kept in an open air lab environment. This mimics a one-time calibration of the LO. Data was collected during several of these multi-hour sessions over the course of several days. The signal generator was set to produce enough input power to ensure the IF voltage waveform was approximately 25mV amplitude when captured. The desired intermediate frequency was determined through experimentation to be lowest possible while still ensuring a low likelihood of the ring's instantaneous frequency jumping across the incoming RF signal. A low IF was desired to maximize period measurement accuracy of the captured signal. The IF was captured by oscilloscope at 2.5GSamp/s for 16ms.

The ring's current source was biased off-chip. The frequency of a current-starved ring oscillator is controlled by its current, so any noise on the current being mirrored to the ring will directly result in additional phase noise. Initial attempts were made to generate current via SMU and dedicated current source IC but both were found to add an unsatisfactory amount of noise to the output. An appropriately-sized resistor to bias the current mirror was found to result in the narrowest practical ring frequency spectrum. Voltage was supplied by an IC LDO powered by two AAA batteries. Later a 16-bit precision DAC powered by FPGA was found to produce practically equivalent frequency variation while being much more experimentally flexible.

Initial tests were performed in a shielded room but those results were not significantly different than an open lab environment.

B. Procedure

The signal generator in use required its modulation signal to be provided in the form of in-phase and quadrature inputs. Minimum frequency shift keying (MSK) has an easy representation in the IQ domain [2], [25], but general FSK does not. Weaver's 3rd method [26], [27] was employed to generate equivalent IQ modulation for any tone spacing not half of its data rate. Data was transmitted at 1Mchip/s and 2Mchip/s over a variety of FSK tone spacings.

The IEEE 802.15.4 specification defines sensitivity in terms of 1% packet error rate for a packet containing a 20B "PHY service data unit" (PSDU) or data payload [1]. Packets were constructed per that spec, of size 26B total including 4B preamble, 1B start symbol, 1B length, and 20B of randomly-generated data. We did not attempt to build a PSDU conforming to 802.15.4 MAC spec. These packets were encoded using standard 4-to-32 DSSS chip sequences for a total of 1664 chips per packet. The chips modulated the RF input signal using FSK at 2Mchip/s at a variety of tone separations. Packets were modulated at 1Mchip/s but due to test hardware limitations those packets were 14B: 2B preamble, 1B start symbol, 1B length, and 10B random data for a total of 896 chips.

The digitized IF output was analyzed for mean voltage crossings to determine cycle periods and then per-period frequencies. At the data period, the mean of these frequencies were compared to the nominal intermediate frequency and a 0 or 1 was stored. A step of clock recovery was included in data processing to ensure frequency of the IF was measured during one whole bit period instead of measuring frequency partly during one bit and partly another. This array of recovered chips was also correlated with the standard 802.15.4 DSSS chip sequences to find the 32-chip symbols the chip stream best matched.

IV. Results

The ring oscillator frequency varied by 1-2MHz over the course of a given 16ms oscilloscope capture. Were we to simply set a frequency as a high/low or 1/0 decision point, as described in Section II-B, this would have yielded poor results. Instead, we established a high/low decision frequency based on a windowed average of the last several frequency measurements to track the slow frequency changes of the ring.

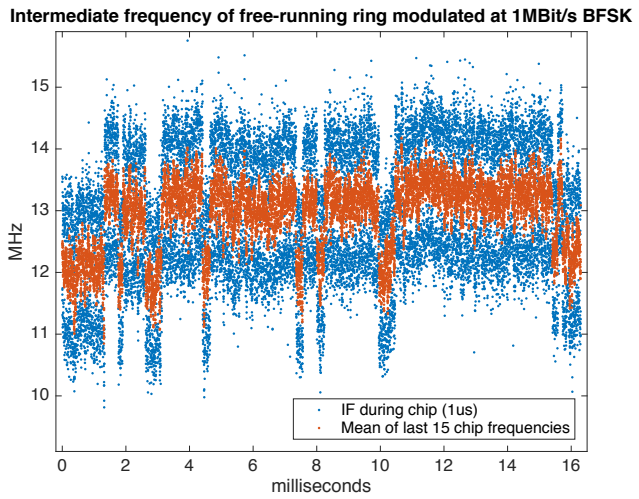


Fig. 4. Instantaneous frequency of FSK modulated signal (blue, appearing as top and bottom traces) measured via voltage zero-crossing period over time. Also displayed: windowed average of frequency (orange, middle trace). Windowed average tracks slow frequency changes as ring oscillator drifts, sometimes abruptly, and provides decision point by which to judge high or low frequency shift. In this particular data set, the 896 chip test packet is repeated 18 times with 2MHz FSK frequency spacing. Random, abrupt, ring frequency shifts move the ring center freq by approximately 1MHz.

It was found that a 15-point window recovered chips most accurately. Up to 50-point windows were tested with negligible change in recovery rate. A sample set of frequencies during a capture is plotted in Figure 4 with a moving average overlaid. Readers will notice the abrupt changes in frequency in addition to the more Gaussian-spreading of frequencies evident in any given segment of time. These shifts are as yet unexplained, but the techniques presented successfully compensate for them. Clock and data recovery, taking place after the frequency high/low decision is made, is anticipated to be unaffected by these large jumps in frequency.

Unmodulated intermediate frequencies were first captured to establish the frequency statistics of the ring oscillator without needing to directly capture RF cycles. These data are shown in the left half of Figure 2 and indicate that simulation from Section II-A and experiment are in good agreement, giving support that our design was fabricated as intended. Experimental data has slightly better standard deviation over 1ms. This is likely due to chance; the full capture is plotted in the top half of Figure 7 and indicates that the measured frequency has more variance on longer time scales.

Results are displayed in Figure 5 with chip error rate 6.5% line superimposed. While the 802.15.4 frequency spacing of 1MHz results in greater than 6.5% CER, relaxing tone separation requirements to 2MHz does meet error rate spec. Alternatively, if the application using a free-running ring receiver can tolerate higher packet error, the standard frequency separation will still result in the majority of chips being successfully received.

These results in comparison to other free-running ring oscillator designs are displayed in Table I and indicate that

TABLE I
COMPARISON TO OTHER PUBLISHED WORK

	This work	[17]	[18]	[16]	[19]	[20]
Frequency	2.4GHz	2.4GHz	2.0GHz	2.4GHz	4.0GHz	4.0GHz
Process	65nm	130nm	90nm	65nm	90nm	65nm
VCO power	105uW	233uW @33kbps	6uW	13uW	280uW	140uW
Ring topology	4-stage differential	Not reported	3-stage single	3-stage single	3-stage single	2-stage differential
Data rate	up to 2Mcps	up to 33kbps	100kbps	250kbps	100kbps	100kbps
Modulation	FSK	OOK	OOK assumed	OOK	FM-UWB	FM-UWB
Noise bandwidth	∼5MHz	100MHz estimated from [28]	100MHz	54MHz	500MHz	300MHz

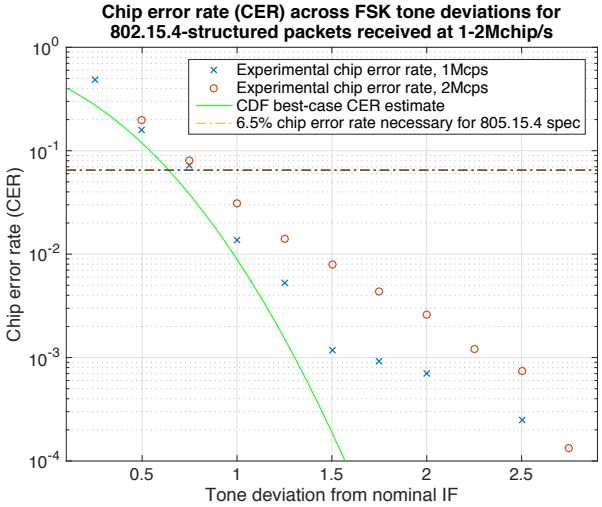


Fig. 5. Ratio of chips successfully recovered over a variety of FSK tone deviations (tone deviation is +/-Δf; total tone separation is 2x axis label). Chips were received by circuit at 1 or 2 Megachips/s (Mcps) for 16ms, for a total of 16000 or 32000 chips per data point. Free-running ring does not meet average 1% packet error rate (6.5% chip error rate) at +/-0.5MHz and 2Mcps as required by 802.15.4 spec, but does at +/-1MHz and wider. Not pictured: A freq deviation of +/-3MHz (tone separation of 6MHz) and 1Mcps results in 100% of chips recovered during test.

our work is capable of communicating in a uniquely narrow bandwidth compared to other free-running radios while still consuming a comparable amount of power and communicating at a comparable rate. Reference [16] deserves particular mention for its data rate vs power but is still restricted to OOK and thus lacks the potential for more higher sensitivity via reduced receiver bandwidth and advanced receiver features such as I/Q demodulation.

A photo of the die is shown in Figure 6.

A. *Packet error rate*

A 16ms capture represented 16000 or 32000 chips, depending on data rate, which yielded a good statistical source on which to base the results of 5. However, at 896 or 1664 chips per packet, this means only 18 whole packets were contained in each data set. Nonetheless, we correlated the chip stream,

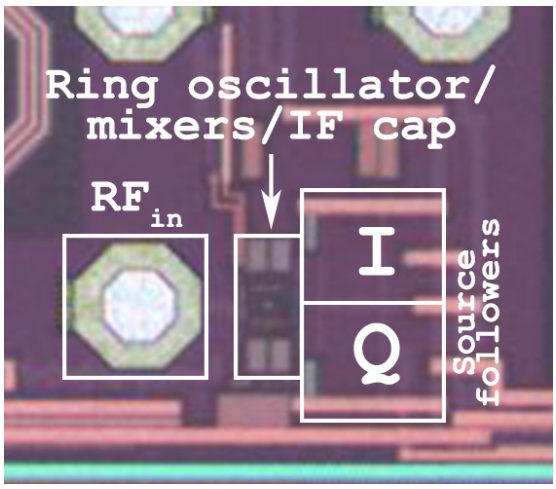


Fig. 6. Photo of section of IC containing circuits under test. Displayed IC section is 450um wide by 400um tall. Our 4-stage differential ring oscillator is the white dot inside the box labeled to contain ring, mixers, and IF capacitors. Not shown: pads for power, current mirror bias, and IF I & Q out.

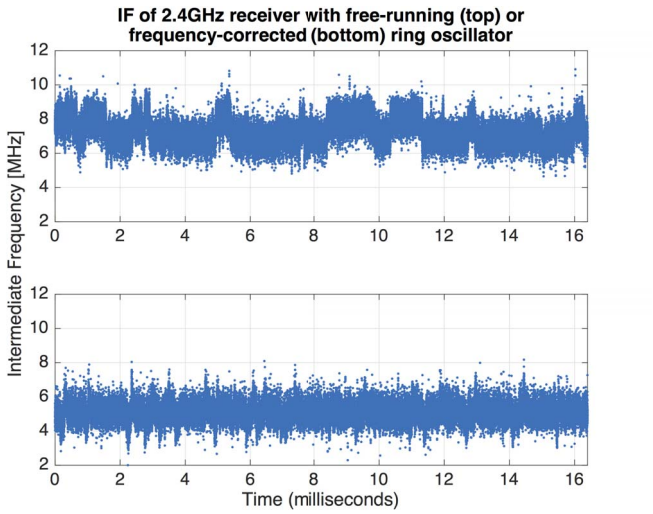


Fig. 7. Top: IF of free-running ring mixing down an unmodulated tone showing large random frequency changes. Standard deviation is 718kHz. Bottom: IF of ring with frequency correction, based on cycle counts, applied every 100ns to center IF at 5MHz. Large random disturbances evident in any free-running time series have been corrected out. Some frequency disturbances still exist due to inconsistent cycle counter behavior. Standard deviation is 537kHz. Note: first 1ms of top plot forms basis of histogram for right-side histogram in Figure 2.

found preambles and start symbols, and despread the chips to recover data. All 18 packets were perfectly recovered in all frequency spacings aside from +/-0.5MHz and +/-0.75MHz, which recovered 14/18 and 15/18 respectively. At +/-1MHz tone spacing a longer capture was taken, at only 100MSamp/s for a total of 410ms of acquisition time. After recovering chips and converting to bits, and 487/488 packets were recovered perfectly for a PER of 0.2% or successful packet recovery rate of 99.8%. These results reflect only IEEE 802.15.4 DSSS codes but, were this high-noise recovery method employed with an encoding scheme with higher coding gain, we expect proportionally better PER with closer frequency spacing or higher noise.

B. Effect on noise bandwidth

This investigation focused entirely on the effect of high phase noise on received chip/packet error rate. This means the IF is unfiltered and the experiment was designed with high SNR to avoid confounds from other sources of noise. In a real system, maximizing SNR to maximize sensitivity is a high priority. An effective way to limit noise is to limit bandwidth. In MSK-based systems, the null-to-null width of a modulated tone is 1.5x the data rate [25], so a signal modulated at 2Mchip/s as in 802.15.4 can limit its noise bandwidth to about 3MHz. In this work, the ring oscillator's noise profile results in a large range of intermediate frequencies. This full range must be accommodated by an IF band-pass filter to recover as much received data as possible. A free-running capture is plotted in the top half of Figure 7 as an example, indicating approximately 5MHz to capture the majority of received power. A review of other data yields worst-case bandwidth of about 8MHz. This worst-case is observed in both 16ms and 400ms captures. Increasing IF bandwidth to 8MHz would result in SNR of about 4.3dB worse than the null-to-null required for MSK.

Much of the frequency distribution in the top half of Figure 7 is due to low-frequency wander of the ring oscillator. The ring was biased by precision DAC, so a feedback system was built to count IF cycles over periods of 100ns and correct the DAC code appropriately. The 100ns timer was derived from a divided FPGA clock. The intended effect was to correct slow frequency variations and reduce necessary bandwidth. The results are displayed in the bottom half of Figure 7 and indicate a bandwidth of only around 2MHz is needed to capture the majority of received power. Some larger frequency deviations are still present on account of inconsistent cycle counter behavior. This plot displays an unmodulated IF, so additional bandwidth is dependent on FSK tone spacing. We speculate that this distribution added to an identical one shifted 1MHz away, as in the time spacing for MSK at 2Mchip/s, would add another 1MHz of required bandwidth for a total of 3MHz, just as in typical 802.15.4.

Such a feedback system requires high initial bandwidth. A system could be devised to start with wide bandwidth to find the incoming carrier while receiving preambles, enable 100ns (for example) correction of the local oscillator, and switch in a narrower filter to reduce noise bandwidth while receiving data. Prior work has described efficacy of this concept [29]. Care must be taken with system design, as this method is susceptible to locking on to the highest-power signal in the IF bandwidth including strong interferers.

V. Conclusion

We have demonstrated that, contrary to popular belief, narrowband communication is possible with a 2.4GHz free-running ring oscillator burning only 105μA. A receiver using

such a ring for a local oscillator is capable of recovering packets transmitted by an IEEE 802.15.4-compliant transmitter, but recovering around 75% of received packets. Alternatively, if the FSK specification were widened from +/-0.5MHz to +/-1MHz, about 99.8% of packets can be received perfectly.

We speculate that we could improve performance by two different methods. The first is by putting the RF oscillator in feedback: the loop need only have bandwidth $\sim$10x beyond the frequency of the random jumps, or only about 100 kHz. The magnitude of the frequency jumps is on the order of 10%, so an RC oscillator with typical $\sim$0.1% jitter could serve as a loop reference. With a loop bandwidth in excess of 10MHz, one could correct IF variance as well. This is above the modulation rate and one would use the VCO feedback control signal to demodulate instead of sampling the IF. Given the IF variance is over 6%, we speculate that an RC oscillator would also suffice here. The second method to improve performance is by simply burning more current in a moderately larger ring to bring variance down, effectively shifting the data in Figure 5 down or left. Either method is likely to push the performance of this free-running receiver over the edge of 1% packet error rate as prescribed by the 802.15.4 specification.

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