A 915MHz Integrated FSK Receiver Front-End and a CMOS Ring Oscillator PLL Built with Standard Cells

Richard Su, Steven Lanzisera, Kristofer S. J. Pister
BSAC, University of California, Berkeley, USA
E-mail: yukuwan@eecs.berkeley.edu

***Abstract*—This paper demonstrates a fully integrated frequency shift keying (FSK) receiver built with standard cells in .18µm CMOS without any off-chip components. Building a receiver with standard cells dictates that an inverter-based ring oscillator, rather than an LC oscillator, will be used for LO generation. This approach reduces the effort required when re-designing the receiver in a different process. Additionally, an inverter-based ring oscillator takes up much less area compared to an LC oscillator. A .18µm standard CMOS receiver prototype occupies only 500µm x 350µm of area, has a sensitivity of -76dBm at 10kbps data rate, and consumes 6mW from a single 1.8V supply while operating in 915MHz ISM band.**

I. INTRODUCTION

RF Transceivers available today are designed to be high-performance devices. These radios require careful design by experienced and skilled RF IC designers, more expensive RF processes, and large chip areas for RF passives. The resulting cost of these devices approaches the dollar level without the off-chip components, and the careful design required makes integration of these radios with other circuits (microprocessors, sensors, etc.) an expensive proposition. Radios that require limited design skills while still having reasonable performance will enable widespread use of wireless technologies.

The primary goal of this work is to create a fully integrated radio topology that does not require any off-chip components, takes up a small chip area, and can be moved from process to process, layout to layout with a minimum of effort. The radios of interest operate at sub-GHz frequencies, and have reasonable sensitivity and wide-band linearity. Power is a concern with these devices, but ease of design is the primary objective. The goal of process portability dictates that passives other than capacitors cannot be used. The main challenge for this design paradigm is the poor phase noise of the inverter-based ring oscillator as binary FSK with ±200kHz frequency deviation is chosen to allow reasonable spectral efficiency. To provide improved phase noise performance, this design uses an integer-N phase-locked loop (PLL) with a bang-bang phase detector.

In this prototype, the receiver is built entirely with standard cells, with the only exception being current sources for controlling low-noise amplifier gain and ring oscillator frequency. A high level block diagram of the prototype is shown in Fig. 1. Section II describes the receiver, which includes a low-noise amplifier and a passive mixer. Section III covers the all-digital PLL used in this prototype to suppress phase noise of a digitally controlled ring oscillator, which drives the passive mixer. Section IV and V discuss measurement results and the conclusions of this work, respectively.

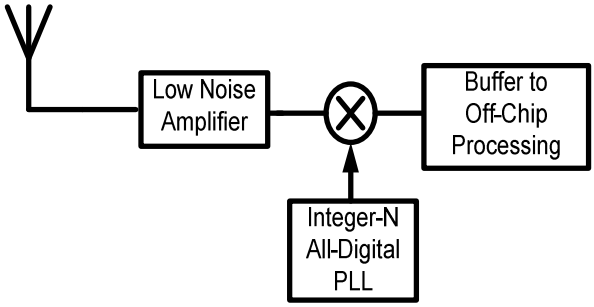

Fig. 1. Receiver Block Diagram

II. RECEIVER (RX)

Even though direct conversion receivers inherently provide image rejection, they are also known for their issues related to quadrature paths, DC offset, I/Q mismatch, and flicker noise [1]. To avoid these issues, low-IF receiver architecture is chosen. In this prototype, the IF frequency is 1MHz. The signal is directly digitized for demodulation at the IF, without second step of down conversion. The frequency deviation of the FSK in this receiver is ±200kHz, and this is chosen based on the configuration at the transmitter. The RF front end has noise figure (NF) of 10dB, which matches well with the simulation results.

Fig. 2 illustrates the receiver circuits. The low-noise amplifier (LNA) is a self-biased inverter [2]. LNA is biased with pass-transistor logic. M3 in Fig. 2 functions as a resistor. A passive mixer follows the LNA. The mixer is driven by a 910MHz ring oscillator locked to a 10MHz reference frequency through a PLL. The LNA converts the input voltage to current, which is alternately driven to one of two output capacitors by a pair of passive switches. In other words, the switches in the mixer sample the RF input voltage at the LO frequency. This LNA provides maximum gain, 20dB, at low power supply, and its NF can be estimated as:

$$\text{NF} = \frac{1}{(g_{m1}+g_{m2})\times 50} + 1 \quad \text{(Assuming } \gamma = 1) \qquad (1)$$

Simulation shows that the NF of this LNA is 5.5dB at 915MHz band, which matches well with the estimate from

978-1-4244-8499-7/11/$26.00 ©2011 IEEE

Equ. 1. The mixer contributes noise by converting noise from the image band as well as all odd harmonics down to baseband, and the NF of the mixer is 4.1dB from simulation. The total NF from simulation is 9.6dB which matches well with the 10dB measured from the test chip.

This receiver architecture provides great wide-band linearity by suppressing wide-band interferers at the intermediate RF node between the LNA and the mixer [3]. Since the intention is to demonstrate a fully integrated receiver without any off-chip components (inductors or filters), this wide-band linearity is critical in desensitizing the LNA to wide-band interferers that would otherwise drive the LNA transistors into triode.

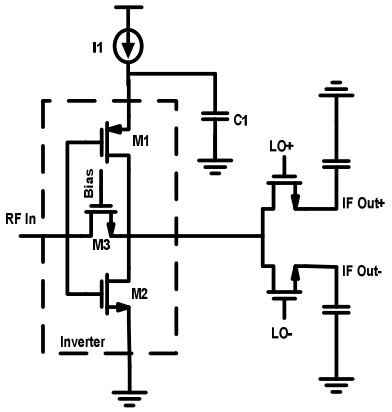

Fig. 2. LNA and mixer Circuit

III. ALL-DIGITAL PHASE-LOCKED LOOP

Commercial radios are often built with LC oscillators to achieve superior phase noise compared to inverter-based ring oscillators. One critical component in an LC oscillator is an inductor. An on-chip inductor takes up a large chip area, whereas an off-chip inductor increases the cost and complexity of packaging. To build a fully integrated receiver with standard cells, we provide the LO signal using a ring oscillator, which occupies much less chip area compared an on-chip LC oscillator. However, to achieve successful demodulation using a ring oscillator, an all-digital phase-locked loop (ADPLL) is included in our design to improve the phase noise of an inverter-based ring oscillator. This ADPLL is also built with standard cells to demonstrate a complete digital-friendly system.

A bang-bang phase detector (BBPD) is commonly used in integer-N PLLs for its simpler design and lower power consumption compared to a multi-bit time-to-digit converter (TDC). For a PLL with a BBPD, there exists a tradeoff between the magnitude of limit cycle and the loop bandwidth. However, it has been shown that a PLL with a BBPD can be designed to match the performance of a linear PLL if the phase and frequency steps are chosen correctly [4]. As a result, in this prototype, a BBPD and a programmable gain loop filter are used. The exact architecture is shown in Fig. 3. The output signal, after being divided down, is compared with the reference signal through a BBPD. The BBPD output then controls the DCO through a loop filter.

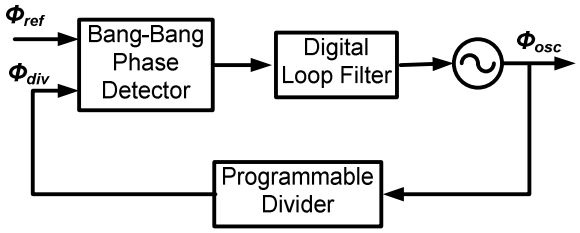

Fig. 3. ADPLL Architecture

A. Digitally-Controlled Ring Oscillator

The digitally-controlled ring oscillator (DCO) is implemented differentially in this design because differential signals are required to drive the mixer. Latches using minimum sized inverters given in standard cells are inserted between two chains of larger inverters to assure the differential nature of the structure. To ensure the larger inverters have enough drive strength to overpower the latches and also to have fast enough rising/falling edges, the size ratio is 4:1 as shown in Fig. 4. The number of stages in this DCO is chosen after taking into account the delay per stage, current consumption, and the magnitude of the final output swing for driving the next stage. The outputs of this DCO go through a pair of cross-coupled NAND-gates to deliver two-phase non-overlapping LO signals for the mixer.

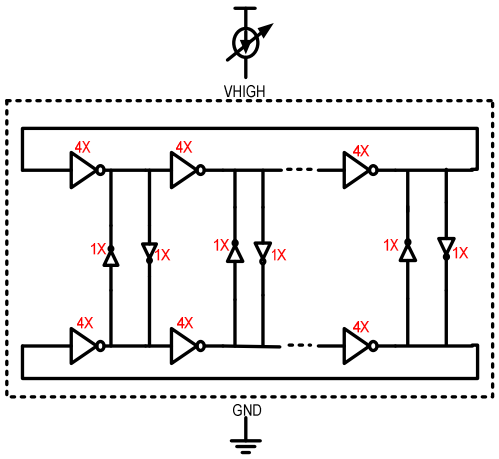

Fig. 4. Differential DCO

For DCO frequency control, there are six bits of control from a binary array digital to analog converter (DAC), five bits through a unitary array, and an additional five bits through a current source controlled by a sigma-delta modulator. The unitary array is chosen to ensure monotonicity, whereas the sigma-delta modulator is used to gain finer frequency steps in the DCO tuning [5]. This DCO has finest frequency step of 30kHz, and it can operate from 400MHz to 1.3GHz. A detailed diagram is shown in Fig. 5.

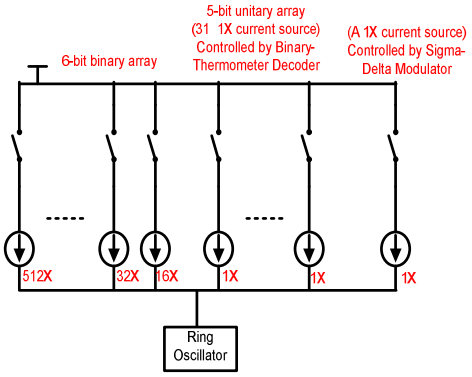

Fig. 5. Current DAC

B. *Programmable Divider*

To lock the DCO to different frequencies in order to demonstrate a receiver with multiple channels, a programmable divider, rather than a fixed divider, is implemented. This programmable divider consists of a prescaler, which divides the 910MHz clock signal down by a factor of 10 or 11, as well as a programmable counter and a swallower counter that each may be reset [6]. A circuit diagram of this programmable counter is shown in Fig. 6. The prescaler is a chain structure, and it divides the oscillator output by 10 or 11 depending on whether the ctrl signal from the swallow counter is high or low. The sole purpose of the swallow counter is to swallow up one additional count from the oscillator cycle to achieve a total division factor other than a multiple of 10.

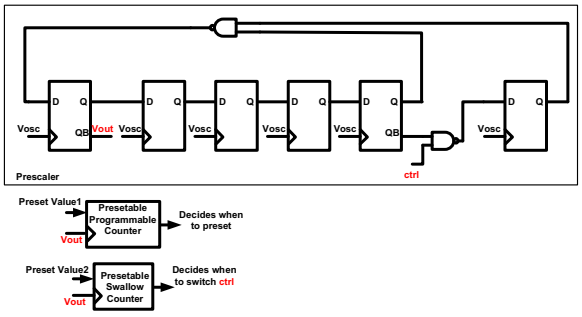

Fig. 6. Programmable Counter

As an example to illustrate the operation of this programmable counter, when dividing a 910MHz clock signal down to 10MHz, the programmable counter is preset to 9 whereas the swallow counter is preset to 1. Since the swallow counter is preset to 1, the ctrl signal into the prescaler will initially force the prescaler to swallow up one additional oscillator cycle. After that, the prescaler will go back to divide oscillator frequency by 10. The final division will therefore be 91.

C. *Bang-Bang Phase Detector*

The BBPD in this prototype is similar to the popular phase frequency detector (PFD) commonly used in analog PLLs. A simplified circuit diagram of this BBPD is shown in Fig. 7. In a PFD, the two outputs from the two DFFs are used to turn on switches for two current sources in an analog PLL. In this BBPD, the two outputs are sent into a latch followed by a metastability filter made of two inverters cross-coupled through their supplies [7]. The final output of this BBPD then decides whether the DCO should speed up or slow down.

The outputs of these two DFFs are normally low, forcing the outputs of the NAND-gates to be high and outputs of the metastability filter to be low. If the rising edge of the V_{ref} arrives before V_{div}, V_q and V_qb_final will be driven low, whereas V_qb and V_q_final stay high. The reset signal will be raised through additional circuitry not shown here after V_{ref} and V_{div} both rise high and output of the metastability filter has settled.

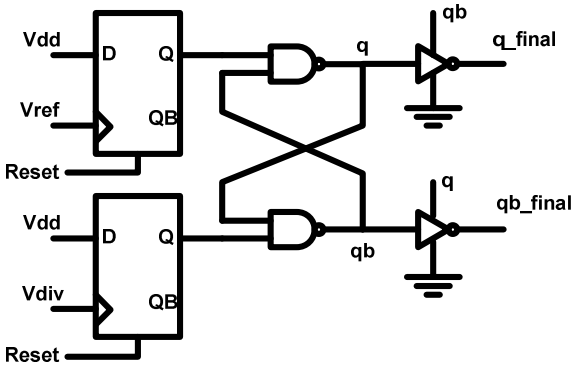

Fig. 7. BBPD Circuit

D. *Loop Filter*

The loop filter is a digital proportional and integral (PI) controller. The integral path ensures that the loop will not settle until the phase offset reaches zero, and the proportional path is added to help stabilize the system, as the DCO and the integral path each contribute a zero to the transfer function at DC [8]. This PI controller runs on the reference clock and takes in the output from the BBPD. The proportional and integral coefficients are adjustable through a serial interface.

IV. Measurement Results

This prototype receiver was fabricated in a 1P6M standard .18µm CMOS without any options. Fig. 8 is a die photo of this test chip. The entire active area occupies 500µm x 350µm including a serial interface, whereas the CMOS ring oscillator PLL portion only takes up 500µm x 200µm. A single multi-turn spiral inductor in a 2.4GHz LC oscillator in [3] takes up 330µm X 330µm of chip area by itself, which is roughly equivalent to the area taken up by the entire frequency synthesizer in this prototype. At a sub-GHz frequency, a similar design will require an even larger inductor. Additionally, while inductors do not scale with technology, an inductor-less design as demonstrated in this paper scales with technology.

Fig. 9 is a phase noise plot of the DCO free running versus locked through the ADPLL over a 2MHz band surrounding the center frequency. As can be seen from Fig. 9, it is unlikely

to demodulate FSK signal with ±200kHz frequency deviation using a free-running DCO, because the energy of the DCO spread almost equally within the entire 2MHz band centered at 910MHz. Fig. 10 is a log scale phase noise plot taken from an Agilent E4440A PSA Series Spectrum Analyzer. The phase noise of the ADPLL is -80dBc/Hz at 1MHz offset from center frequency, while the reference spurs at multiple of 10MHz offset are not worse than -85dBc/Hz. Table I is a summary of results from this 915MHz receiver.

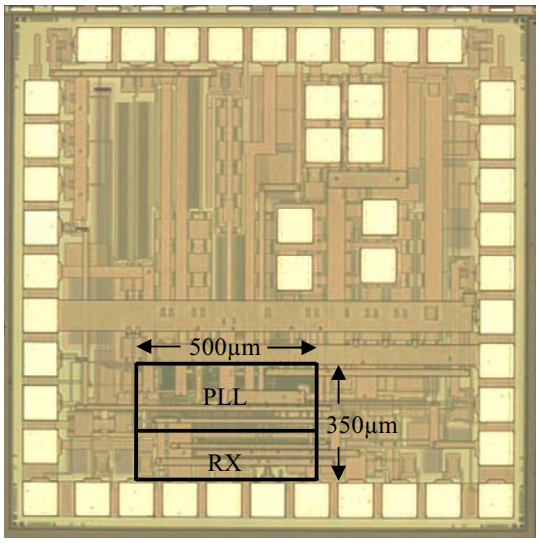

Fig. 8. Die Photo

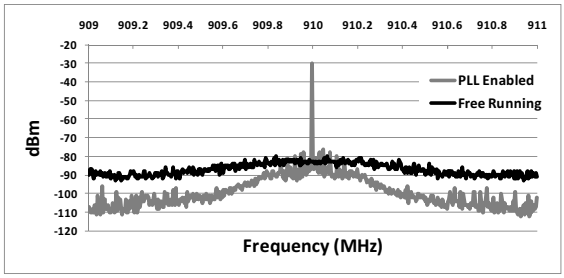

Fig. 9. Phase Noise Measurement with RBW=1Hz

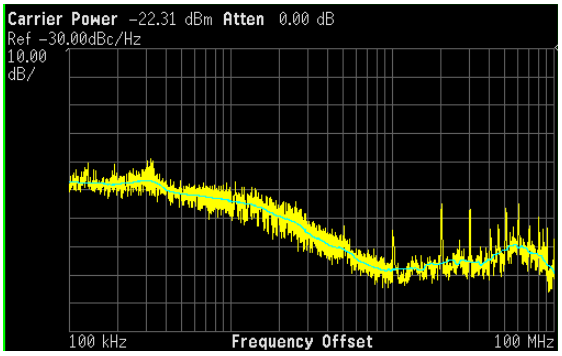

Fig. 10. Phase Noise Plot with PLL Enabled

From our measurement, this prototype receiver has sensitivity of -76dBm (BER of 10E-3) when receiving at 10kbps.

CMOS Technology	0.18µm
Power Supply	1.8V
RX front-end Power Consumption	1mW
RX front-end NF	10dB
PLL Power Consumption	5mW
PLL Phase Noise at 1MHz Offset (F_{ref} = 10MHz)	-80dBc/Hz
Sensitivity at 10kbps	-76dBm
Area (RX + PLL)	500µm X 350µm

Table I. Receiver Summary

V. Conclusion

The chip area of an inverter-based ring oscillator is much smaller than an LC oscillator when operating at sub-GHz frequency. An on-chip inductor for a sub-GHz LC oscillator can easily occupy an area that is equivalent to that of the entire frequency synthesizer in this prototype. This 915MHz fully integrated FSK receiver that is built with a ring oscillator and is highly based on standard cells have reasonable spectral efficiency, sensitivity, and wide-band linearity. Additionally, as more advanced CMOS technology becomes available, this design can be ported to a newer technology to achieve active area in the order of a few bond pads without much added design effort.

References

[1] B. Razavi, RF Microelectronics, Prentice Hall, NJ, 1998, pp129-138

[2] A. Molnar, B. Lu, S. Lanzisera, B. Cook, and K.S.J. Pister, "An Ultra-low Power 900 MHz RF Transceiver for Wireless Sensor Networks," *CICC*, Oct. 2004.

[3] B. Cook, A. Berny, A. Molnar, S. Lanzisera, and K.S.J. Pister, "An Ultra-Low Power 2.4GHz RF Transceiver for Wireless Sensor Networks in 0.13µm CMOS with 400mV Supply and an Integrated Passive RX Front-End," *ISSCC*, Feb. 2006

[4] J. Crossley, E. Naviasky, and E. Alon, "An Energy-Efficient Ring-Oscillator Digital PLL," *CICC*, Sep. 2010.

[5] R.B. Staszewski, K. Muhammad, D. Leipold, et al., "All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130-nm CMOS," *IEEE JSSC*, Dec. 2004.

[6] M. Krishna, M. Do, K. Yeo, C. Boon, and W. Lim, "Design and Analysis of Ultra Low Power True Single Phase Clock CMOS 2/3 Prescaler," *IEEE Transactions on Circuits and Systems-I:Regular Papers*, Jan. 2010.

[7] J. Tierno, A. Rylyakov, and D. Friedman, "A Wide Power Supply Range, Wide Tuning Range, All Static CMOS All Digital PLL in 65 nm SOI," *IEEE JSSC*, Jan. 2008.

[8] J. Kim, M.A. Horowitz, and G. Wei, "Design of CMOS Adaptive-Bandwidth PLL/DLLs: A General Approach," *IEEE Transactions on Circuits and Systems-II:Analog and Digital Signal Processing*, Nov. 2003.