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Theoretical and Practical Limits to Sensitivity in IEEE 802.15.4 Receivers

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Abstract- **This paper addresses the performance limits of the IEEE 802.15.4 standard 2.4 GHz PHY for wireless personal area and sensor networks. As designers start considering the addition of power amplifiers to improve link margin, other methods that do not increase power significantly are of high value. Minimizing power consumption is the key goal of 802.15.4 systems, and improvements in sensitivity can be traded for power savings. The limits from communication theory are compared to the performance of common system topologies, and methods for improving system performance without significant cost are discussed and verified through simulation. Approximately 6.6 dB of sensitivity is shown to be commonly sacrificed, and 5.8 dB is recoverable without large increases in design complexity.**

I. INTRODUCTION

Wireless personal area networks (WPAN) and wireless sensor networks (WSN) have received significant attention in recent years. These devices are designed with power consumption and device cost as the primary considerations, and sacrifices are made in performance and reliability in order to meet these objectives. The IEEE 802.15.4 standard 2.4 GHz wireless physical layer (PHY) was designed for WPAN and WSN systems which require moderate data rate communication capabilities while meeting these stringent power and cost constraints [1]. The standards body created a PHY description that enables system designers to produce simple devices while maintaining good performance in additive white Gaussian noise (AWGN) channels and reasonable spectral efficiency. In order to improve performance in noisy environments, a block direct-sequence spread spectrum (DSSS) code is used to spread the signal across a wider bandwidth and achieve both coding and processing gain. The transmitter modulates the carrier using offset quadrature phase shift keying with half-sine shaping (OQPSK-HSS); this modulation scheme achieves a high degree of spectral occupancy while having very little spectral leakage outside the signal band. These choices should result in a system with excellent sensitivity, little interference to other users in the spectrum, and low power implementations. Commercially available and published radio implementations do not achieve the theoretical sensitivity limits due to sacrifices in design in the name of power and complexity savings, but the savings achieved are not always worth the trade in link margin. In order to improve link margin, designers are starting to include power amplifiers in their design at a high power cost [2]. By exploring the theoretical sensitivity limits and the impact design decisions have on sensitivity, the design trade offs can be evaluated on the system level to reveal where the sacrifices are valuable. By improving receiver sensitivity, improvements in system link margin and/or reductions in power are possible.

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This paper will discuss the sensitivity enhancements included in the standard and how common system implementations impact the overall sensitivity. Section II will discuss the performance limits of an ideal 802.15.4 receiver. Section III will discuss common implementation choices for 802.15.4 radios and the effect of these tradeoffs, and section IV will discuss methods to regain some of the lost performance.

II. PERFORMANCE LIMITS

The fundamental sensitivity limit of IEEE 802.15.4 in AWGN channels can be characterized by considering standard link margin calculations that include the signaling characteristics, coding gain, and processing gain of the standard. The sensitivity of a receiver, P_{min}, is defined to be the minimum signal power at the antenna that results in the specified error performance,

$$P_{\min} = kT \cdot W \cdot n_f \cdot SNR_{\min} \tag{1}$$

where k is Boltzmann's constant, T is absolute temperature, W is the communication bandwidth, n_f is the noise factor of the receiver, and $SNR_{\min}$ is the minimum baseband signal power to noise power ratio at the demodulator. $SNR_{\min}$ is given by

$$SNR_{\min} = \frac{(E_b/N_o)_{\min}^{OQPSK\_HSS}}{C \cdot P} \tag{2}$$

where $(E_b/N_o)_{\min}^{OQPSK\_HSS}$ is the minimum energy per bit to noise ratio required for the OQPSK-HSS modulation scheme, C is the coding gain, and P is the processing gain. Calculating the value of the $SNR_{\min}$ term in (1) is the primary focus of this section. Each component of the standard that impacts noise performance will now be considered.

The $SNR_{\min}$ value depends on the required error rate tolerated by the standard, and this error rate is given as a maximum allowable packet error rate (PER) of 1% for a reference packet with 20B (Bytes) of payload and 6B of overhead. These 26B are encoded into 52 symbols of k = 4 bits each [1]. A single symbol error causes a packet error to occur from which the required symbol error rate (SER) can be calculated to be

$$SER = \frac{PER}{symbols/packet} = \frac{1\%}{52} = 1.9 \times 10^{-4}. \tag{3}$$

The SER can be used to estimate the average BER of a system. A single symbol error does not correspond to a single bit error in the typical case because a single symbol error can result in up to k bit errors. On average approximately $k/2$ bit errors occur for each symbol error resulting in a required BER of 9.5×10^{-5}.

The performance of the signaling characteristics is the first component impacting $SNR_{\min}$ to consider. Shannon's limit shows that the minimum E_b/N_o required for error free communication is -1.6 dB, but this limit can only be achieved by coding over an infinitely long data set (resulting in infinite latency). Non-ideal modulation and detection schemes along with the finite number of bits coded across result in higher E_b/N_o requirements. Figure 1 shows the bit error performance of OQPSK-HSS as a function of E_b/N_o for different detection methods. The best case is to use coherent detection of OQPSK-HSS where the required E_b/N_o is 8.8 dB to achieve 9.5×10^{-5} BER.

To determine the coding gain available from the symbols, the degree of orthogonality for the code set must be understood. When one code word, r_1, is compared to the set of template code words $R = \{r_1, ..., r_M\}$, the number of chip flips required to change r_1 to any r_i is called the Hamming distance between the code words. For a DSS code, the coding gain of R is calculated by finding the mean Hamming distance of the code set, $\bar{d}$. Given the code set for 802.15.4, $R_{15.4}$, the maximum, mean and minimum distances are 20, 17, and 12

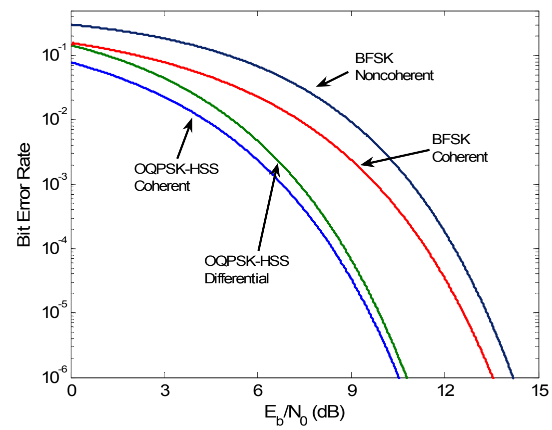

Figure 1. Bit error performance for varying detection schemes

respectively. For DSSS code sequences, an approximate expression for coding gain is

$$C \approx k\left(\frac{\bar{d}}{n} - \frac{\ln 2}{E_b/N_o}\right) \tag{4}$$

where n is the length of the code [3]. For the BER rate required and $R_{15.4}$, the coding gain is approximately 2 dB which directly reduces the required E_b/N_o. The value of C in (2) is an average across all codes in $R_{15.4}$ meaning that some symbols will have better or worse properties according to their Hamming distance to other codes and the errors that occur.

The performance of the $R_{15.4}$ code set is limited by the moderate orthogonality of the code words, but the minimum distance for a code set is bounded by

$$d_{\min} \le n(1 - k/n) + 1. \tag{5}$$

No binary codes achieve equality in (3), but it is useful to note that the coding gain increases exponentially with d. Figure 2 shows the coding gain for different values of d suggesting that using improved codes could improve sensitivity significantly [3].

The processing gain of a code is set by the ratio of the number of chips transmitted per bit of information. Therefore the processing gain is

$$P = n/k = 9\,dB. \tag{6}$$

The processing gain does not reduce the energy per bit required because it is just a measure of how much more energy per bit is used in detection compared to the energy per chip.

The $SNR_{\min}$ can be calculated from the application of (2): $SNR_{\min} = 8.8\,dB - 2\,dB - 9\,dB = -2.2\,dB$. Using the sensitivity equation in (1), the best case sensitivity can be calculated to be

$$P_{\min} = kT \cdot W \cdot n_f \cdot SNR_{\min} = -174\,dBm + 63\,dB + 0\,dB - 2.2\,dB = -113.2\,dBm. \tag{7}$$

III. COMMON IMPLEMENTATION PENALTIES

Due to system level decisions, common implementations sacrifice sensitivity so that the $P_{\min}$ of the system is higher than expected from (7). Due to power constraints, the n_f of the receiver is greater than unity, but this term does not account for all of the lost sensitivity. A recent implementation demonstrated a n_f of 5.7 dB with a sensitivity of -101 dBm [4]. An additional 6.5 dB is lost in this implementation that is unaccounted for by n_f, and the demodulation and detection techniques used are the primary sources of this sensitivity reduction.

Demodulation of OQPSK-HSS can be through a variety of techniques at a zero IF or at a non-zero IF. Converting to a zero IF enables the user to use coherent demodulation (the receiver has a good phase estimate of the carrier) as OQPSK-HSS which typically is reported to provide a 3 dB performance improvement as compared to noncoherent demodulation techniques. A zero-IF noncoherent alternative is to use the differential phase encoding inherent in the signal to perform demodulation, and the sensitivity penalty is only 0.9 dB for OQPSK-HSS at the required of E_b/N_0 as shown in figure 1. This differential phase technique can be thought of as using the prior chip as the carrier phase estimate for the current chip, so it is a technique somewhere between coherent and noncoherent techniques resulting in the reduced penalty. Both of these techniques require a linear baseband chain with conversion to baseband either through direct conversion or through a super heterodyne architecture. Binary FSK detection at a non-zero IF is attractive because it can be performed using a simple low-IF architecture. This requires that OQPSK-HSS be detected as minimum-shift keying (MSK), a type of binary frequency shift keying (BFSK), and the performance penalty due to this change is much larger. Non-coherent detection of MSK at a non-zero IF requires 4.6 dB higher E_b/N_0 for the same BER than coherent detection of OQPSK-HSS. Using coherent MSK detection at a non-zero IF reduces this loss to 3 dB (see figure 1). The most common implementation uses non-coherent MSK demodulation at a non-zero IF, however, and the reference design in [4] uses this common architecture.

After demodulation, the resulting chip estimates are correlated against the template codes to determine which symbol the received signal is most likely to be. The processing gain associated with this technique is $P = n/k$ but this assumes that the correlation uses chips that are continuous valued (soft decisions) rather than limited to discrete values of ±1 (hard decisions). To evaluate the penalty associated with using hard decisions, a calculation of the error probabilities in each case is required. The calculation of the loss in sensitivity is challenging and is computed numerically, and the reader is referred to [3] where the loss in sensitivity is found to be $\pi/2$ or 2 dB for the general set of digital communication codes.

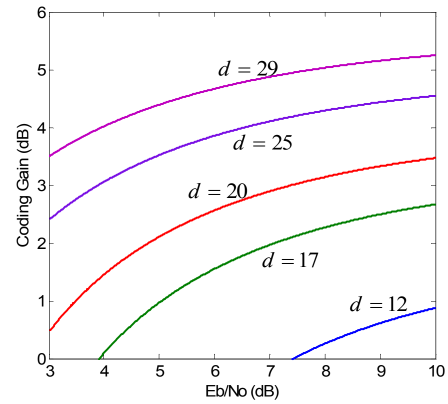

Figure 2. Coding gain for a k=4, n=32 block code with varying distance between code words

The combination of non-ideal demodulation and hard decision detection shows a sensitivity sacrifice of 6.6 dB. This number is only 0.3 dB off from the unexplained sensitivity degradation reported in [4] demonstrating that demodulation and detection can account for significant losses in system sensitivity.

IV. RECLAIMING LOST GROUND

Contributions from the system noise figure, non-ideal detection, and non-ideal correlation all contribute to lost sensitivity observed in implemented systems. Each one of these values can be adjusted by the designer at some cost, and it is important to understand the costs involved in reducing these values.

A. Reducing Noise Figure

The noise figure is largely determined by the LNA of the design. This block has a characteristic where the noise factor of the LNA is approximately

$$n_f \approx 1 + \alpha / P_{LNA} \qquad (4)$$

where α is a topology and process dependent parameter and P_{LNA} is the power consumed by the LNA [5]. Clearly for values of n_f approaching 1, the power consumed increases rapidly. The reference design has $\alpha = 13\,mW$ and a total receiver power of 26 mW [4]. Therefore, moving from a n_f of 6 dB to 3 dB results in a 33% increase in total receiver power budget, and other system changes may yield similar improvements at lower cost.

B. Improving Demodulation Efficiency

The potential improvement in demodulation efficiency is 4.7 dB by moving from non-coherent FSK demodulation to coherent OQPSK-HSS demodulation, but this requires a carrier phase tracking loop to be implemented. Performing differential phase detection, however, can achieve 3.8 dB of the improvement without requiring the phase tracking loop. This improvement in sensitivity comes at the cost of design challenges, however, because conversion to a zero-IF is more problematic than a low-IF architecture. Recent results in the literature, however, show success in low power, narrowband direct conversion receivers [6,7]. Using the more complicated super-heterodyne architecture also moves the signal to baseband, and it can also alleviate the noise and DC problems by allowing more gain at frequencies dominated by thermal noise and reducing linearity concerns before conversion to baseband.

C. *Improving Correlation Efficiency*

The 2 dB that is lost by using single bit correlators at the chip level can be reduced without significant increases in power or complexity. Many demodulator topologies provide an intermediate output that is a multi-bit representation of the current state of the IF or baseband signal, and this output can be used for the chip level correlations. Typical implementations provide 2-5 bits of resolution on the demodulated output before the result is thresholded to obtain the single bit value. The 1 bit correlator is simply an xor gate, and the full correlation is of the form

$$R = \sum_i y_i \oplus x_i \tag{5}$$

where the correlation value is R, the received single bit chip estimate is y_i and the single bit template is x_i. The standard solution for a full correlation is

$$R = \sum_i y_i \times x_i \tag{6}$$

where the multiplication can be implemented simply as an inversion conditioned on the single bit value of the template x_i. The xor in (5) is therefore replaced with a multi-bit addition in (6). More complicated soft decision algorithms have been proposed and implemented [8]. Figure 3 shows the efficiency improvement achieved for different numbers of bits on the demodulator and correlator, and using 3 bits achieves nearly all of the possible 2 dB of improvement.

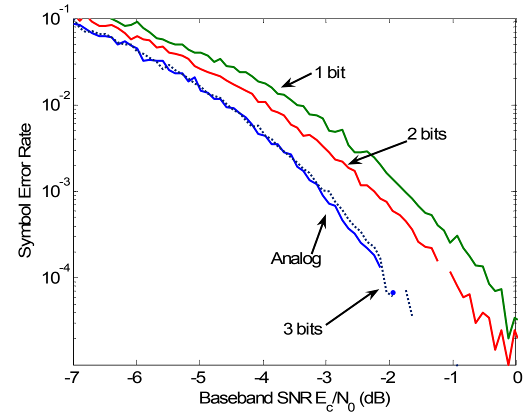

Figure 3. Simulated correlator efficiency vs number of bits.

V. CONCLUSIONS

The sensitivity of 802.15.4 receivers has been reported to be lower than expected by the basic theory. We have shown how using non-ideal system components can account for the lost sensitivity. For a given noise figure, approximately 5.8 dB of the possible 6.6 dB of sensitivity improvement is achievable without significantly changing the power consumption of the receiver if the demodulation and detection methods are improved. Using differential phase detection provides a 3.8 dB improvement in sensitivity, and soft decision detection of the DSSS code achieves a 2 dB improvement. These significant improvements can be used to achieve excellent performance even at very low power consumptions.

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REFERENCES

[1] IEEE 802. 15.4-2003 Standard: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs). URL: http://standards.ieee.org/getieee802/download/802.15.4-2003.pdf

[2] Dust Networks, "M2135 Product Brief." URL: http://www.dustnetworks.com

[3] J. Proakis, *Digital Communication*, 3rd Edition, Chapters 5-8, McGraw Hill, 2001.

[4] W. Kluge et al., "A Fully Integrated IEEE 802.15.4 Compliant Transceiver for Zigbee Applications," IEEE J. of Solid-State Circuits, vol. 41, no. 12, Dec. 2006.

[5] B.W. Cook, S. Lanzisera, K.S.J. Pister, "SoC Issues for RF Smart Dust," Proc. of IEEE, Vol. 94, Issue 6, June 2006.

[6] [DCB] G. Chang et al., "A direct-conversion single-chip radio-modem for Bluetooth" ISSCC Digest of Technical Papers, Feb. 2002.

[7] B.W. Cook, A. Berny, A. Molnar, S. Lanzisera, K.S.J. Pister, "Low-Power 2.4-GHz Transceiver With Passive RX Front-End and 400-mV Supply," IEEE J. of Solid-State Circuits, Vol. 41, Issue 12, December 2006, Pages: 2757-2766.

[8] M. Fossorier, S. Lin, "Computationally efficient soft-decision decoding of linear block codes based on ordered statistics," IEEE Trans. on Information Theory, Pages: 738-750, Vol. 42, Issue 3, May 1996.