Low-Power 2.4-GHz Transceiver With Passive RX Front-End and 400-mV Supply

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***Abstract*—An ultra low power 2.4-GHz transceiver targeting wireless sensor network applications is presented. The receiver front-end is fully passive, utilizing an integrated resonant matching network to achieve voltage gain and interface directly to a passive mixer. The receiver achieves a 7-dB noise figure and −7.5-dBm IIP3 while consuming 330 μW from a 400-mV supply. The binary FSK transmitter delivers 300 μW to a balanced 50-Ω load with 30% overall efficiency and 45% power amplifier (PA) efficiency. Performance of the receiver topology is analyzed and simple expressions for the gain and noise figure of both the passive mixer and matching network are derived. An analysis of passive mixer input impedance reveals the potential to reject interferers at the mixer input with characteristics similar to an extremely high-Q parallel *LC* filter centered at the switching frequency.**

***Index Terms*—Low-power radio, low-power RF, passive gain, passive mixer, RF CMOS, sensor network, Smart Dust.**

I. Introduction

MESH NETWORKS of wireless sensor nodes have emerged as a commercially viable technology. Each wireless sensor node contains one or more sensors, hardware for computation and communication, and a power supply. Motes are assumed to be autonomous, programmable, and able to participate in multi-hop mesh communication.

The vast majority of sensor networks today rely on a costly wired infrastructure for power and communication. In the near term, wireless networks are simply replacing existing wired networks, dramatically reducing installation costs. Applications for these networks demand lifetimes of multiple years without battery replacement. With currently available hardware, multi-year lifetimes are only possible by running the system at very low duty cycle or using large batteries. Deep duty cycling limits wireless sensor networks to applications requiring low data throughput.

The radio is typically the most power-hungry block on a sensor node, making extension of the lifetimes and application space of these networks largely dependent on reducing the energy consumed by the RF circuits. Energy consumption per ADC conversion or microprocessor instruction of just a few tens of pJ [1]–[4] has been demonstrated, whereas even the lowest power transceivers designed for short range communication typically require tens to hundreds of nJ to transmit and receive a single bit [5]–[9]. Here we demonstrate a 2.4-GHz transceiver achieving 1 nJ per received bit and 3 nJ per transmitted bit with 300-μW transmit power and 7-dB receiver noise figure.

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II. Architecture

The transceiver block diagram is shown in Fig. 1 and a simplified front-end schematic is shown in Fig. 2. A 400-mV supply was chosen for this system to accommodate a single solar cell as the power source. In sunlight the entire transceiver could operate continuously from a 2.6 mm × 2.6 mm solar cell [10]. Because of the reduced supply voltage, all circuits in the transceiver are made differential to increase available swing. Symmetric, center-tapped inductors tie both voltage-controlled oscillator (VCO) and power amplifier (PA) outputs to the supply, doubling available headroom by allowing their outputs to swing above the supply rail. The PA and mixers are driven directly from the VCO's high-Q *LC* tank without buffering both to save power and to improve performance by making use of the VCO's doubled output swing.

This transceiver uses binary FSK with a relatively increased tone separation, effectively trading spectral efficiency for a simplified low-power architecture [7], [11]. The constant envelope nature of binary FSK permits use of an efficient nonlinear PA in the transmitter and 1-bit quantized demodulation in the receiver. Large FSK tone separation relaxes phase accuracy specs for the transmitter and decreases the receiver's sensitivity to phase noise and LO pulling—which can be an issue when driving the mixer directly from the VCO tank.

The relatively large FSK tone separation chosen for this system stands in contrast to the modulation schemes employed in Bluetooth and 802.15.4 [12], [13] in which tone separation is only 1/3 to 1/2 the modulation rate so as to minimize occupied bandwidth. Sacrificing spectral efficiency for reduced power and system complexity is particularly favorable for wireless sensor network applications wherein data rates below 1 Mb/s are the norm and 85 MHz of unlicensed spectrum is available in the 2.4-GHz ISM band.

A. Receiver

At the receiver input, an integrated passive *LC* network is used to achieve impedance matching and voltage gain. The output of this network connects directly to double balanced passive mixers for downconversion. A programmable capacitor at the passive mixer output places a low-pass *RC* corner at about 1 MHz to filter out wideband interferers before any active gain stages. The capacitor is made programmable to account for the dependence of the mixer output resistance on the amplitude

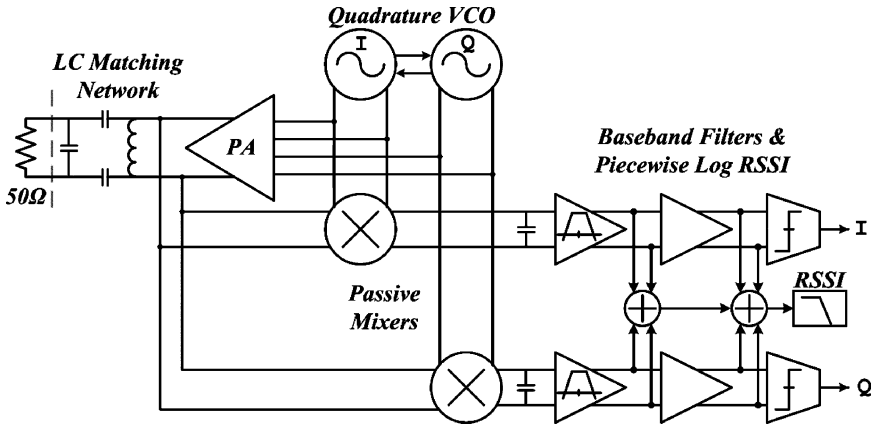

Fig. 1. Transceiver block diagram.

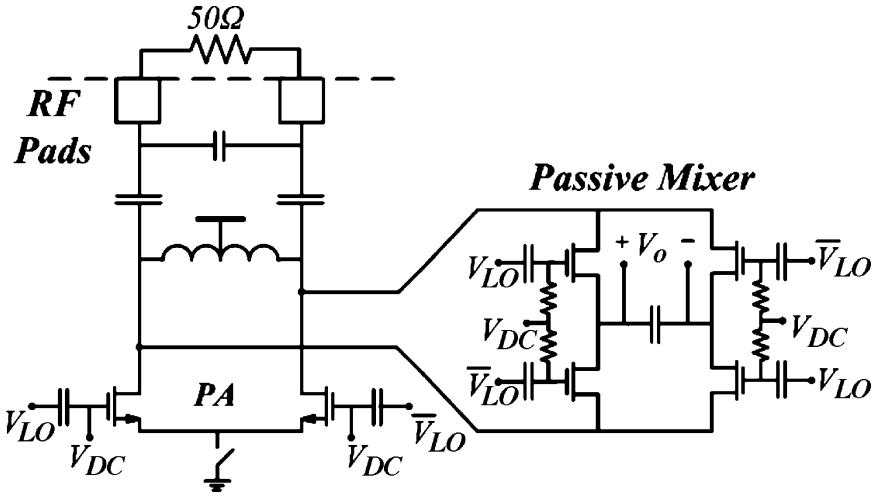

Fig. 2. Simplified transceiver front-end schematic.

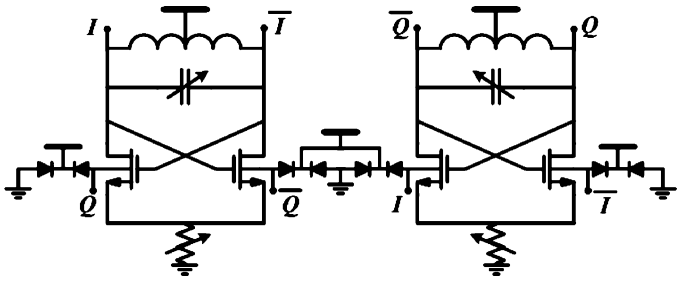

Fig. 3. Quadrature VCO utilizing back gate coupling.

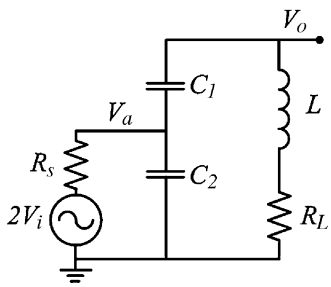

Fig. 4. Circuit model for tapped-capacitor resonator.

and DC level of the VCO signal driving the switches. The mixer outputs differentially drive a bandpass filter comprising a pair of linearized CMOS inverters. The filter outputs feed into a piecewise logarithmic RSSI that hard-limits the signal, providing a square voltage waveform for demodulation.

In its default mode, the receiver uses a low-IF architecture sacrificing image rejection in exchange for cutting power in half. The factor of two lower power in low-IF mode is due to the fact that only a single phase of the VCO is needed and the current of the baseband chain is also halved. When necessary however, a back-gate coupled quadrature VCO generates I & Q signals (Fig. 3) [14] and two matching BB chains can be enabled. The back-gate coupled VCO architecture was used here because it produces quadrature outputs without the additional current requirements of coupling transistors. In this mode, the receiver uses direct-conversion, achieving DC suppression via the bandpass response of the baseband filters.

1) LC Input Network: A single *LC* matching network is used for both the receiver and transmitter, making a front-end switch unnecessary and reducing inductor count. This network is a tapped capacitor resonant transformer (Fig. 1, upper left). The purpose of this network is to boost the PA load impedance in the transmitter and to achieve substantial passive voltage gain in the

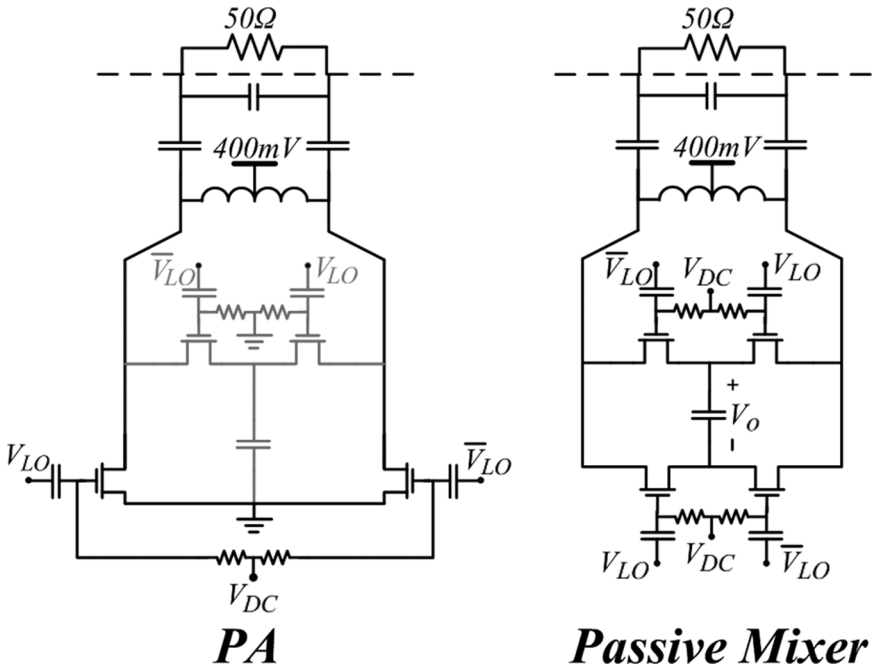

Fig. 5. Reconfigurable PA/mixer topology. Sharing transistors of the PA and mixer substantially reduces parasitic loading on the input *LC* network and the VCO tank.

receiver front-end while presenting a large real impedance to the mixer input. In this design, the voltage gain from receiver input to the mixer output is about 17 dB and the PA load impedance is boosted from 50 Ω to about 1 kΩ.

The tapped capacitor resonator presents both series and parallel resonant modes to the receiver input port. Impedance matching from the input port to a real impedance at the output is achieved at the parallel resonance. On-chip resonant networks have typically not been used to achieve large passive voltage gain because the noise contributions of the low-Q passive components increases with gain. However, as the achievable Q of integrated inductors rises, this noise-gain tradeoff improves. Here we examine the effect of finite inductor Q on the matching, noise, and voltage gain of the network.

The simplified *RLC* network shown in Fig. 4 is used in the following analysis. The source driving the RF port has magnitude 2 V_i to account for the voltage dropped across R_S. If the input impedance of the network is matched to R_S, then $V_{\rm a} = V_i$. Note that there is some parasitic capacitance in parallel with the inductor due to both finite inductor self resonance frequency (SRF) and the transistors of the PA and mixer which attach directly to the network.

A reconfigurable PA/mixer topology was developed to minimize the parallel capacitance contributed by the front-end transistors by reducing transistor count. In essence, a single quad of transistors can be configured as a PA or mixer, depending on bias voltages and the states of a couple switches. Fig. 5 illustrates this reconfigurable topology. Since both PA and mixer are driven directly from the VCO's *LC* tank, this topology has an added benefit of substantially reducing capacitive loading on the VCO.

From the output port, the matching network appears as a simple parallel *LC* tank with a lossy capacitor and inductor. The lossy capacitor consists of elements C_1, C_2, and source resistance R_S and its effective Q (QC) is set by R_S and the ratio of capacitors C_2 and C_1. The overall network Q at the parallel resonance is a parallel combination of the inductor Q (Q_L) and Q_C. Q_C may assume a wide range of values, permitting design flexibility, while the Q_L is limited by process constraints. Q_C is defined as

$$Q_C = \omega R_S \frac{C_2}{C_1}(C_2 + C_1) + \frac{1}{\omega R_S C_1}. \tag{1}$$

The output impedance of the network at resonance is real and its magnitude is

$$R_o|_{\omega=\omega_o} = \omega_o L \frac{Q_C Q_L}{Q_C + Q_L}. \tag{2}$$

Noise at the output is contributed by both R_S and R_L. If Q_C is very large, then the overall Q is limited by the inductor and most noise at the output will come from R_L, leading to high noise factor. On the other hand, the network has the lowest noise factor when Q_C is much smaller than Q_L because losses and output noise are dominated by R_S. To quantify the relationships between L, Q_L, and Q_C, we first determine the voltage gain of a noise voltage source at both R_L and R_S to the output, denoted A_{VL} and A_{VS}, respectively:

$$|A_{VL}(\omega_o)| \approx \frac{2Q_C Q_L}{Q_C + Q_L} \tag{3}$$

$$|A_{VS}(\omega_o)| \approx \frac{2Q_C Q_L}{Q_C + Q_L}\sqrt{\frac{\omega_o L}{R_S Q_C}}. \tag{4}$$

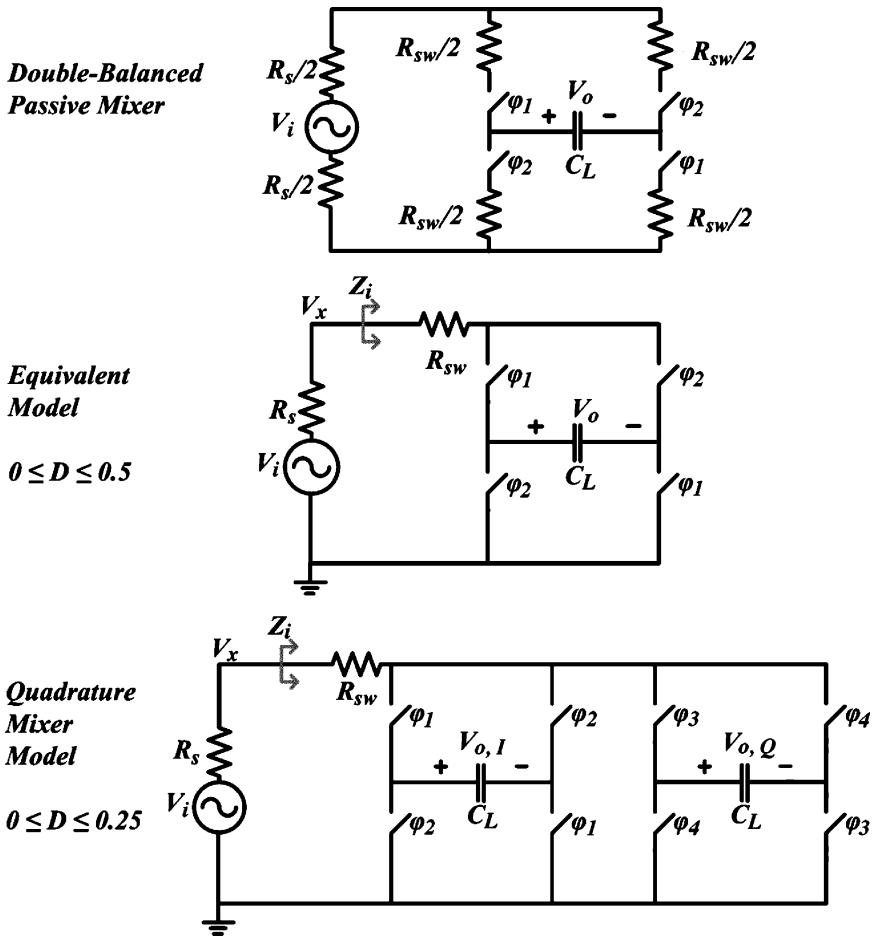

Fig. 6. Passive mixer circuit models. Top: double balanced passive mixer. Middle: equivalent model valid for $0 < D < 1/2$. Bottom: equivalent model for quadrature mixer when $0 < D < 1/4$.

Therefore, the noise factor (F) of the network at resonance becomes

$$F|_{\omega=\omega_o} = 1 + \frac{R_L}{R_S}\left(\frac{|A_{VL}(\omega_o)|}{|A_{VS}(\omega_o)|}\right)^2 = 1 + \frac{Q_C}{Q_L}. \quad (5)$$

The maximum gain is achieved when the source impedance is perfectly matched to R_L. This is an intuitive result because all power delivered to the network must be dissipated in R_L and the output voltage is largest when the current through R_L is maximum. Matching occurs when Q_L and Q_C are equal. Thus, from (5), the noise factor is 2 when matched. The voltage gain of the network when matched is

$$|A_{VS}(\omega_o)|_{\max} \approx \frac{2\omega_o L}{\sqrt{R_S R_L}}. \quad (6)$$

2) Passive Mixers: At the output of the *LC* network, passive mixers downconvert the RF signal. The mixers must present a relatively high impedance to the matching network to avoid reducing its gain. In this section, the input impedance, conversion gain, and noise factor of passive mixers are related to the switch on-resistance and characteristics of the driving waveform. The circuit model for the passive mixer used in the following analysis is shown in Fig. 6.

As mentioned, the nMOS switches in the passive mixer are driven directly from the VCO's high-Q tank to save power and achieve large gate drive. The driving signal is approximately sinusoidal and, since conductance of a MOSFET in the triode region is linear with V_{gs}, the resulting switch conductance waveform resembles a rectified sine wave. To simplify the following analysis, we approximate the conductance waveform as a pulse train with a variable duty cycle as in [15]. For sinusoidal drive, variation of the conductance duty cycle is realized by varying the DC level of the driving waveform relative to the switch threshold (Fig. 7).

The conversion gain of the passive mixer at 0 Hz offset can be derived by considering sampling a sinusoid at the input that is perfectly in-phase with the conductance waveform. The output voltage is simply the average of the input voltage while the switch is conducting. For calculating gain at 0 Hz offset, the switch resistance can be ignored since the output voltage will have an infinite number of cycles to settle to a DC value. The switch resistance and load capacitance determine the time constant with which the output voltage can change, but do not affect 0 Hz offset voltage gain. The output voltage is dependent on the phase of the input wave but, since the average of an orthogonal

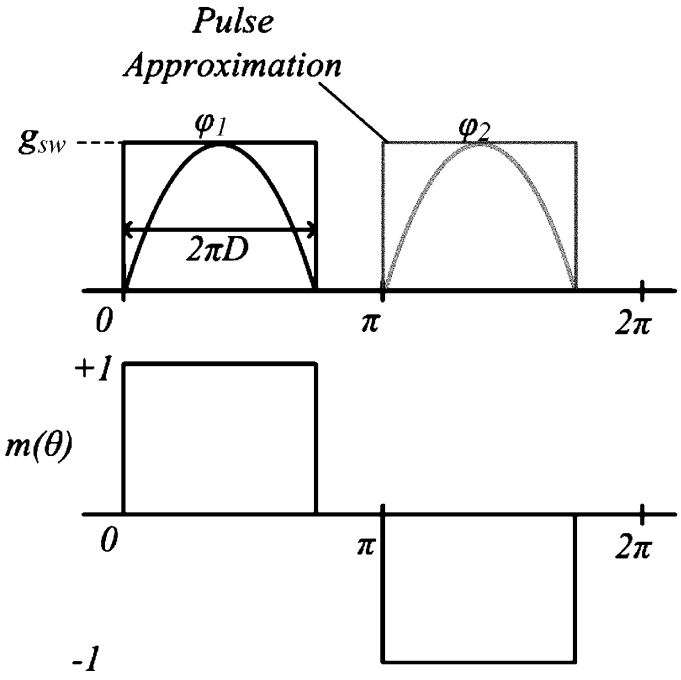

Fig. 7. Top: illustration of sinusoidal switch conductance waveform and pulsed conductance approximation used in this analysis. Bottom: corresponding mixing function using pulsed approximation.

input wave (90° out of phase) during one conduction cycle is zero, we may ignore its contribution in the gain calculation and consider only the in-phase signal. The gain is expressed below:

$$G_{\mathrm{Conv}} = \frac{1}{2}\left(\frac{1}{2\pi D}\int_{-\pi D}^{\pi D}\cos\theta d\theta - \frac{1}{2\pi D}\int_{\pi-\pi D}^{\pi+\pi D}\cos\theta d\theta\right) = \frac{1}{2\pi D}\int_{-\pi D}^{\pi D}\cos\theta d\theta = \frac{\sin\pi D}{\pi D}. \quad (7)$$

The quantity D is the conduction duty cycle, thus D can assume values from 0 to 1. Equation (7) is valid for $0 < D < 1/2$. For very small D, the gain approaches 1 and gain decreases monotonically to $2/\pi$ when $D = 1/2$. As frequency offset increases, the gain will roll off due to the low-pass filter formed by C_L, R_S, and R_{SW}. The value of this output pole is

$$\omega_p = \frac{1}{R_o C_L} = \frac{2D}{(R_S + R_{SW})C_L}. \quad (8)$$

The mixer also has gain at odd harmonics of the switching frequency. The conversion gain for each odd harmonic is

$$G_{\mathrm{Conv}}(n \cdot f_o) = \frac{\sin n\pi D}{n\pi D}, \text{ for odd } n. \quad (9)$$

With proper choice of D, the gain at a particular harmonic can be rejected. For instance, if $D = 1/3$, the gain at the third harmonic is 0.

Next, we calculate the input impedance of the mixer for signals both at 0 Hz offset and at large frequency offset from the LO. Consider the case of an input sinusoid at 0 Hz offset. If C_L is sufficiently large such that the mixer output pole (ω_{p}) is a much lower frequency than the RF input signal, we can assume the mixer output voltage holds a quasi-static value over a single conduction period. Thus, the mixer output capacitor is modeled as an ideal voltage source for this calculation with a DC value equal to the average of the input voltage during the sampling period. Since this circuit model contains no imaginary components, the resulting input impedance is real. To calculate R_{IN}, we first integrate the power delivered from the source to find the energy transferred over one period:

$$E_{\mathrm{in}} = \frac{|V_{\mathrm{in}}|^2}{2(R_S + R_{\mathrm{in}})}\cdot 2\pi = \frac{|V_{\mathrm{in}}|^2}{R_S + R_{SW}}\cdot\left(\int_{-\pi D}^{\pi D}\left(\cos\theta - \frac{\sin\pi D}{\pi D}\right)^2 d\theta + \int_{-\pi D}^{\pi D}(\sin\theta - 0)^2 d\theta\right). \quad (10)$$

Then the input resistance at 0 Hz offset becomes

$$R_{\mathrm{in}}|_{\Delta f=0} = \frac{R_{SW} + R_S}{2D\left(1 - \left(\frac{\sin\pi D}{\pi D}\right)^2\right)} - R_S \quad 0 \le D \le \frac{1}{2} \quad (11)$$

Now consider the input impedance for the case of an input signal whose frequency *offset* is much greater than ω_{p} and thus, the input signal has nearly zero gain to the output. Again, we assume C_L is large enough that the mixer output voltage is quasi-static over one cycle, but here we further assume the output voltage is independent of the input signal. In this case, the mixer output is modeled as a short to ground and we integrate power to find the energy transferred from the source over one period:

$$E_{\mathrm{in}} = \frac{|V_{\mathrm{in}}|^2}{2(R_S + R_{\mathrm{in}})}\cdot 2\pi = \frac{|V_{\mathrm{in}}|^2}{R_S + R_{SW}}\cdot\left(\int_{-\pi D}^{\pi D}(\cos\theta)^2 d\theta + \int_{-\pi D}^{\pi D}(\sin\theta)^2 d\theta\right). \quad (12)$$

Then the input impedance far from the carrier frequency is real and its value is

$$R_{\mathrm{in}}|_{\Delta f \gg f_p} = \frac{R_{SW} + R_S}{2D} - R_S, \quad 0 \le D \le \frac{1}{2}. \quad (13)$$

If $D = 1/2$, then the input impedance at large frequency offsets is just R_{sw}. The input impedance for a quadrature passive mixer can be calculated in a similar fashion and the results are shown below:

$$R_{\mathrm{in}}|_{\Delta f=0} = \frac{R_{SW} + R_S}{4D\left(1 - \left(\frac{\sin\pi D}{\pi D}\right)^2\right)} - R_S, \quad 0 \le D \le \frac{1}{4} \quad (14)$$

$$R_{\mathrm{in}}|_{\Delta f \gg f_p} = \frac{R_{SW} + R_S}{4D} - R_S, \quad 0 \le D \le \frac{1}{4}. \quad (15)$$

Fig. 8 is a plot of the mixer input impedance versus frequency offset for a quadrature mixer with $D = 1/4$. The input impedance closely resembles that of a very high-Q parallel *LC*

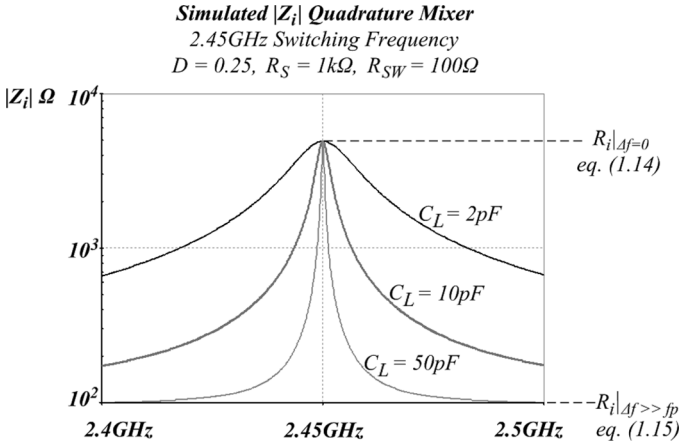

Fig. 8. Input impedance of quadrature passive mixer versus frequency.

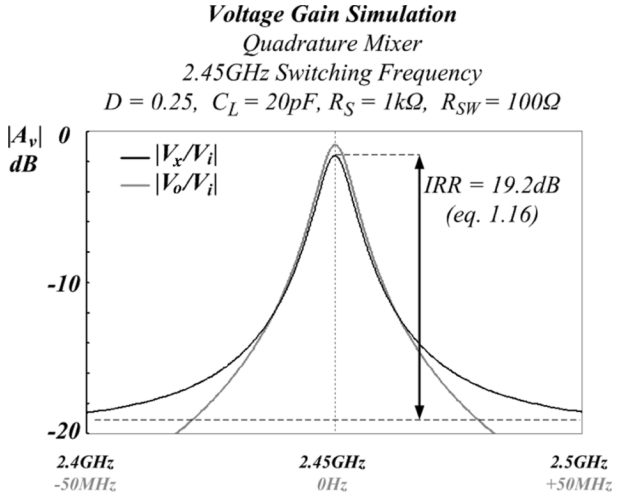

Fig. 9. The sharp mixer input impedance profile attenuates far-out interferers at both the mixer input and output. Refer to Fig. 6(bottom) for equivalent circuit model and node variables.

tank with center frequency set by the VCO and 3-dB bandwidth equal to twice the mixer output pole frequency from (8). Thus, the passive mixer can be designed to present a very low impedance to signals far from the carrier while remaining high impedance in a narrow band around the switching frequency. The result is that signals at small frequency offsets are passed while those at large offsets are strongly attenuated not only at the mixer output, but at the mixer input as well (Fig. 9).

The voltage gain from V_i to the mixer input node $V_{\rm x}$ (A_{Vx}) is easily derived from the voltage divider formed with the R_s and $R_{\rm in}$. The interference rejection ratio (IRR) is the ratio of A_{Vx} at 0 Hz offset to A_{Vx} at large offset. Maximum rejection is achieved for $D = 1/4$ in the quadrature mixer and at $D = 1/2$ for the single phase case. IRR is 19.2 dB under the conditions listed at the top of Fig. 9.

$$\max\{\mathrm{IRR}\}_{\mathrm{I\&Q}} = \left.\frac{A_{Vx}|_{\Delta f=0}}{A_{Vx}|_{\Delta f\gg fp}}\right|_{D=0.25} = 1+\frac{R_S}{R_{SW}}\left(\frac{8}{\pi^2}\right). \tag{16}$$

Finally, we analyze the noise performance of a differential passive mixer with both single-phase and quadrature driving signals. As mentioned previously, the mixer downconverts signals and thermal noise near the switching frequency and all odd harmonics with a gain given in (9). Therefore, the total mixer output noise power density at 0 Hz is given by an infinite summation:

$$\frac{\overline{V_n^2}}{\Delta f} = 4kT(R_S+R_{SW})\sum_{\substack{m=-\infty\\ n=2m+1}}^{\infty}\left(\frac{\sin n\pi D}{n\pi D}\right)^2. \tag{17}$$

The gain terms at each harmonic are closely related to the Fourier series of the mixing function $m(\theta)$ (Fig. 7), which is

$$\Im\left(m(\theta)\right) = \sum_{\substack{m=-\infty\\ n=2m+1}}^{\infty} 2D\frac{\sin n\pi D}{n\pi D}. \tag{18}$$

Therefore, we can use Parseval's relation to find the sum of the noise power at all harmonics and thus the total mixer output noise:

$$\frac{1}{2\pi}\int_{-\pi}^{\pi}|m(\theta)|^2 d\theta = 2D = \sum_{\substack{m=-\infty\\ n=2m+1}}^{\infty}\left(2D\frac{\sin n\pi D}{n\pi D}\right)^2 \quad \text{(Parseval)}. \tag{19}$$

From (17) and (19), the total noise density at the mixer output is

$$\frac{\overline{V_n^2}}{Hz} = 4kT\frac{R_S+R_{SW}}{2D}. \tag{20}$$

Given the signal gain and total output noise, we can derive the SNR at the output and hence, the noise factor of the passive mixer:

$$NF = \frac{R_S+R_{SW}}{R_S}\cdot\frac{1}{2D}\cdot\left(\frac{\pi D}{\sin\pi D}\right)^2, \quad 0\le D\le\frac{1}{2}. \tag{21}$$

Taking the derivative of (21) with respect to D and setting to zero, we find that there exists an optimal D delivering best noise factor:

$$\frac{\partial NF}{\partial D} = 0 \Rightarrow \frac{\tan\pi D}{2\pi D} = 1 \Rightarrow D_{\rm opt}\approx 0.375. \tag{22}$$

For quadrature downconversion, both I & Q mixers are connected to the same input node and overlap in the switching waveforms of the two mixers must be avoided. Since overlap is avoided, the thermal noise at sampling instants of the I and Q mixers is uncorrelated, but the output signals are correlated. The noise factor for a quadrature passive mixer is

$$F_{\mathrm{I\&Q}} = \frac{R_S+R_{SW}}{R_S}\cdot\frac{1}{4D}\cdot\left(\frac{\pi D}{\sin\pi D}\right)^2, \quad 0\le D\le\frac{1}{4}. \tag{23}$$

The best case noise factor for the passive mixer with quadrature downconversion occurs at $D = 1/4$ and its values is given below:

$$F_{\mathrm{I\&Q}}|_{D=0.25} = \frac{R_S+R_{SW}}{R_S}\cdot\frac{\pi^2}{8}. \tag{24}$$

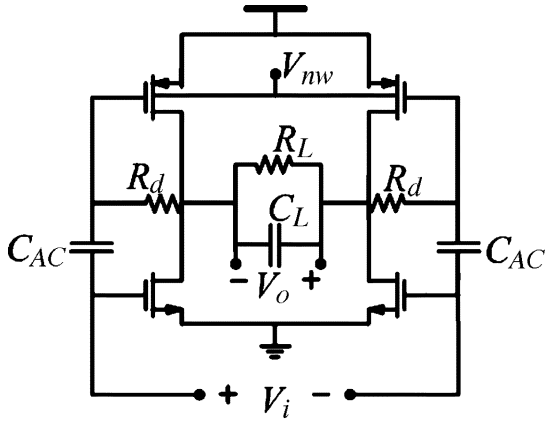

Fig. 10. First baseband amplifier stage following the passive mixer.

Given the noise-folding properties of the mixer, it is possible to improve upon its noise performance by filtering out noise from R_s at odd harmonics of the switching frequency. The tapped-capacitor resonator at the input of the receiver discussed here does effectively remove source noise at odd harmonics. However, the thermal noise from R_{sw} still comes through unfiltered at all odd harmonics and the *LC* network contributes its own noise, as previously discussed.

3) Baseband Chain: The first baseband stage following the mixer is a bandpass filter with a lower cutoff below 100 kHz and a programmable upper cutoff frequency. The schematic is shown in Fig. 10. At very low frequencies, the amplifier has a gain of about 1 because the input signal only appears at the nMOS gates and these devices drive diode connected pMOS loads with similar g_m. The combination of C_{AC} and the Miller-gain reduced R_d create a high-pass filter with a corner well below 100 kHz, passing the input signal to the gates of the pMOS devices in the passband. Thus, the current required to meet noise constraints is reduced because the amplifier utilizes the g_m of both N and P devices in the passband. The *RC* corner set by C_L and R_L defines the upper end of the passband.

Forward-body biasing of the pMOS devices is used to set the common-mode level of the first baseband stage at midrail. The output of this stage drives the pMOS inputs of the subsequent stage which shares the same n-well. The DC gain through the baseband chain is approximately 1. There are four baseband stages and a limiter which delivers a square waveform for demodulation at the output. The outputs of each baseband stage drive single transistor amplitude detectors and the currents of these detectors are summed to create a piecewise logarithmic RSSI signal which gives a "linear in dB" estimate of the input from about -100 to -20 dBm.

B. Transmitter

The goal for the transmitter was to achieve reasonable global efficiency with a low-power output in the range of 100–500 μW. The power output target was derived from a system level analysis of link margin versus power consumption based on a generic transceiver model [11]. To maintain high global efficiency at low power output, power hungry upconversion mixers and LO buffers must be eliminated. Furthermore, the severe voltage headroom constraint makes active upconversion mixers impractical.

Since the modulation chosen for this transceiver is tolerant of moderate frequency and phase errors without significant bit error rate (BER) degradation, an extremely simple transmit topology was used. In transmit mode, the VCO and PA are the only RF blocks consuming current and binary FSK is accomplished by directly modulating the VCO tank capacitance. A digital frequency-locking loop (FLL) is necessary to select the channel frequency but, due to time constraints, it was not implemented on this chip. The simulated power estimate for a digital FLL similar to that reported in [7] is about 25 μW.

The differential PA drives the tapped-capacitor resonator analyzed above. Given the large output swing afforded by using a differential design and swinging above the supply rail, the PA could easily put out several milliwatts efficiently. To maximize the efficiency of this class-C PA at the selected power output, it is necessary to boost the PA load impedance so that the PA uses all available voltage headroom. The optimum load impedance for 300 μW power output and 800-mV zero-to-peak differential voltage is around 1 kΩ.

Equation (2) expresses the PA load impedance as a function of the component values. Given the target impedance of 1 kΩ at resonance, the maximum allowable size of the inductor is found by setting $C_2 = 0$ and $R_{\rm o} = 1$ kΩ:

$$L_{\max} = \frac{\sqrt{(R_S + R_L)R_o}}{\omega_o}. \tag{25}$$

Just as losses in the inductor degrade the noise performance of the *LC* network in the receiver, the finite Q_L effectively reduces the network efficiency in the transmitter because some of the PA output power is dissipated in R_L. The efficiency of the network is expressed below:

$$E_{LC} = \frac{P_{R_S}}{P_{R_S} + P_{R_L}} = \frac{Q_L}{Q_C + Q_L}. \tag{26}$$

The best efficiency is achieved when $C_2 = 0$ where Q_C is minimized. The capacitor C_2 was made programmable to accommodate the different optimum capacitance values for the receiver and transmitter.

III. Results

A. Receiver Measurements

Fig. 11 is a plot of noise figure versus total receiver power consumption. The noise figure was measured with a spectrum analyzer using the 1-bit quantized baseband output. There are multiple data points at each receiver power level representing a sweep of the input signal frequency across the passband of the baseband filters. At very low power, the VCO has low amplitude swing and the baseband amplifiers have reduced bias current. As a result, the input referred noise from the amplifiers and the effective R_{sw} is increased. The linearity of the receiver is also degraded due to the reduced VCO swing. As receiver power consumption increases above 300 μW, the VCO swing approaches 400-mV zero-to-peak, improving the mixer noise and linearity.

The receiver achieves a noise figure of 7 dB and an IIP3 of -7.5 dBm at its nominal operating point while consuming

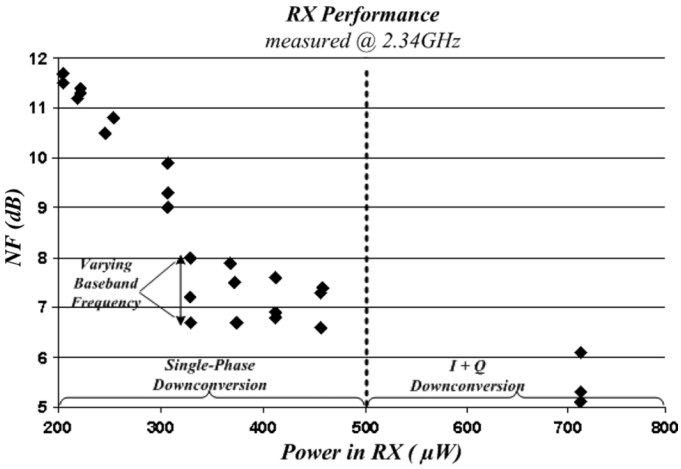

Fig. 11. Receiver noise figure versus power consumption.

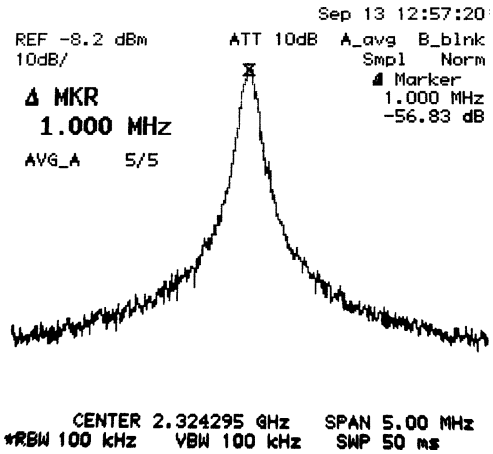

Fig. 12. Unmodulated transmitter output spectrum.

330 μW. Current consumption in the receiver is fairly evenly split between the VCO and the baseband amplifiers. A 5.5-dB noise figure was measured in quadrature downconversion mode. Overlap in the conduction cycles of the I & Q mixers was avoided in quadrature mode by biasing the mixer switches well below threshold. As a result, a full 3-dB noise improvement was not seen because effective R_{SW} is substantially higher. Note that all measurements in the receiver and transmitter are taken at a frequency slightly below 2.4 GHz. The VCO was unable reach the desired band because of improper modeling of the custom designed tank inductance.

B. Transmitter Measurements

An unmodulated transmitter output spectrum is shown in Fig. 12. The phase noise is estimated from this measurement as -106 dBc/Hz at 1 MHz offset. The low output power of -8.2 dBm seen in this measurement reflects the losses in the balun, cables, connectors, and board traces, totaling about 3 dB. Structures were included on the test board to calibrate out the loss in the balun and traces.

Fig. 13 is a plot of global transmitter efficiency and PA efficiency as a function of power output. At 300 μW power output,

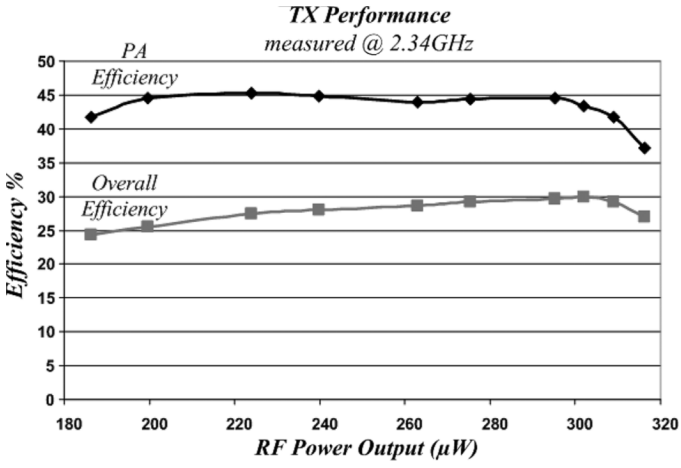

Fig. 13. Transmitter efficiency and PA efficiency versus power output.

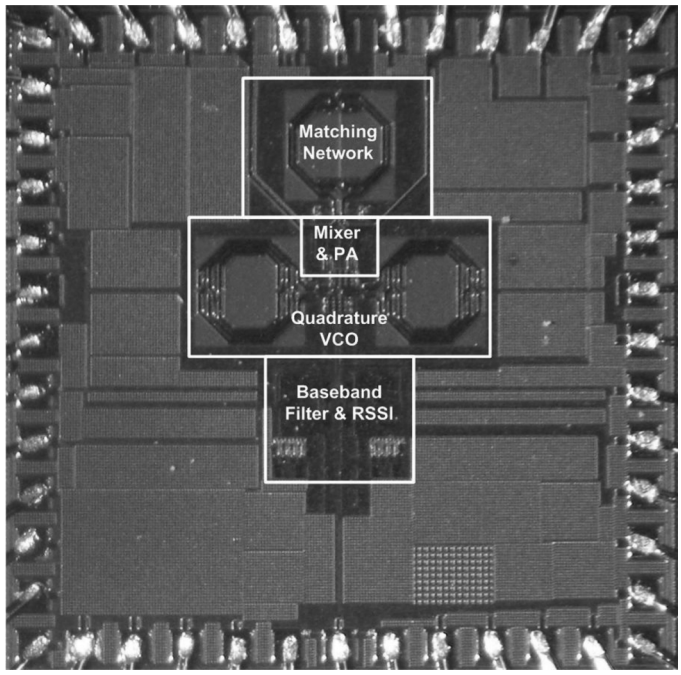

Fig. 14. Die photo of the transceiver. The die size is 2.1 mm × 2.1 mm limited by pad count.

the PA is 45% efficient and the overall efficiency is 30%. The capacitor C_2 is programmed to its minimum value to maximize the efficiency of the *LC* network as described above. The current necessary to provide maximum VCO swing is substantially higher in the transmitter than in the receiver as the VCO is loaded by a PA with large output swing and no cascoding transistors.

IV. Conclusion

An ultra-low-power 2.4-GHz transceiver operating from a 400-mV supply has been demonstrated. The chip was fabricated in a 130-nm RF CMOS process and a die photo is shown in Fig. 14. RF voltage gain in the receiver front-end is achieved with a resonant matching network that interfaces directly to a passive mixer for downconversion. This front-end topology simultaneously achieves good noise figure and IIP3 at low

TABLE I
SUMMARY OF MEASURED PERFORMANCE

Overall		**Value**
Supply Voltage	Min/Typ/Max	360/400/600 mV
2-FSK Deviation	Min/Max	300/1000 kHz
RX		
Power Consumption	Min/Max	200/750 µW
Noise Figure	Min/Max	5.1/11.8 dB
IIP3	Typ.	-7.5 dBm
TX		
Power Consumption	Min/Max	700/1120 µW
Output Power	Min/Max	140/320 µW
PA Efficiency	200<P_{OUT}<300 µW	>44 %
VCO		
Power Consumption	$Min_{I\ Only}/Max_{I+Q}$	160/700 µW
Frequency	Min/Max	1.95/2.38 GHz
Quadrature Mismatch	Meas. ΔΦ at I&Q Mixer Out	|ΔΦ-90| < 5 deg
Phase Noise @1MHz	@ P_{VCO} = 270 µW	-106 dBc/Hz

voltage and low power. The measurement results for the transceiver are summarized in Table I.

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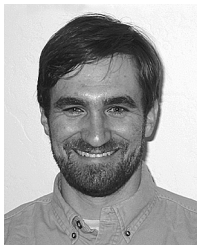

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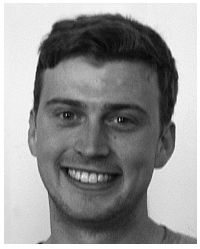

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