Low Power RF Design for Sensor Networks

Invited Paper

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Abstract — **Design of RF circuits for short-range, low-power wireless communication is discussed. A derivation of optimum link range and transceiver power budget is presented based on simple models for indoor path loss and power vs. performance tradeoffs in a generic transceiver. Design techniques aimed at efficiently reaching these parameters are discussed for individual circuit blocks. Finally, some published transceivers are discussed with respect to the optimization and design techniques presented.**

Index Terms — **Low power RF, RF CMOS, sensor network, Smart Dust.**

I. Introduction

Wireless sensor networks consist of a collection of small, cheap, independent nodes sensing various properties of their environment. Each node includes a microprocessor, memory, power source, sensor(s), an ADC, and wireless communication. Typically, nodes gather data continuously over a period of time and intermittently transmit that data to a base station through single or multi-hop wireless communication. In many target applications, thousands of nodes will be deployed for periods of months or years, so individual nodes must be designed for minimum cost and maximum lifetime.

The limits of communication range are fundamentally tied to power consumption in the RF circuits, making communication a node's most expensive operation. An optimized sensor network minimizes the global power consumption within these fundamental limits, and makes use of circuits designed to approach these limits within practical constraints.

II. Power Limits of Wireless Communication

Consider the power required to send a single message from one node to a base station far away through a series of RF links. By making some basic assumptions about propagation conditions and transceiver performance vs. power consumption, one can find an optimum link distance and power distribution between receiver and transmitter.

In an ideal, time synchronized network, each link requires both a transmitter and receiver to be on for equal amounts of time. Power consumed in the transmitter, P_{TX},

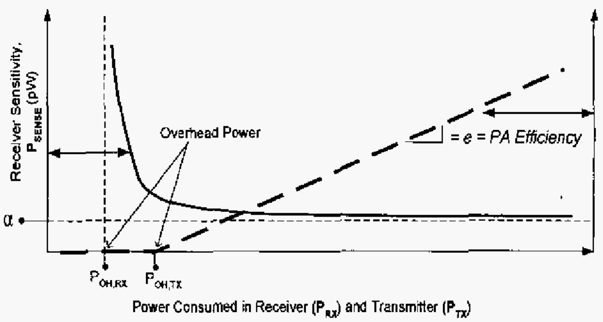


Fig. 1. Graphical representation of the simple model for transceiver performance versus power consumption

consists of the power consumed in the PA (P_{PA})plus an overhead power ($P_{OH,TX}$) associated with generating and modulating the RF signal. For simplicity, we assume $P_{OH,TX}$ and PA efficiency (e) are independent of power output. Receiver power (P_{RX}) consists of the power consumed in the first amplification stage (P_{LNA}) plus an overhead ($P_{OH,RX}$) associated with RF signal generation, channel selection, and demodulation.

$$P_{LINK} = P_{TX} + P_{RX} = P_{OH,RX} + P_{OH,TX} + P_{LNA} + P_{PA} \quad (1)$$

For a CMOS receiver, the LNA is best implemented with a MOSFET biased in saturation. Assuming that this amplifier dominates system noise factor (NF) one may derive sensitivity (P_{SENSE}) as a function of power consumption in the LNA. See figure 1 for a graphical representation of this model.

$$P_{SENSE} = \left(SNR_{\min}\right)\left(BW\right)\left(kT\right)\left(NF\right) = \alpha NF \quad (2)$$

$$NF = 1 + \frac{1}{g_m R} = 1 + \frac{V_{DSAT} V_{DD}}{2 P_{LNA} R_{ANT}} = 1 + \frac{\gamma}{P_{LNA}} \quad (3)$$

$$P_{SENSE} = \alpha \left(1 + \frac{\gamma}{P_{LNA}}\right) \quad (4)$$

Using the indoor path loss model from [4], the link range (r) of a node is given by:

$$r = \sqrt[\beta]{\left(\lambda/4\pi\right)^2 \cdot \frac{P_{OUT}}{P_{SENSE}}} = \sqrt[\beta]{\left(\lambda/4\pi\right)^2 \cdot \frac{e}{\alpha} \cdot \frac{P_{LNA} P_{PA}}{P_{LNA} + \gamma}} \quad (5)$$

The value of β, the path loss coefficient, depends on the environment, but is between 2 and 4 for most situations of interest [4]. Substituting $P_{PA} = P_{SUM} - P_{LNA}$, and solving for the optimal P_{LNA} given P_{SUM}, leads to:

$$\frac{\delta r}{\delta P_{SUM}} = 0 \Rightarrow P_{LNA,OPT} = \sqrt{\gamma^2 + \gamma P_{SUM}} - \gamma \qquad (6)$$

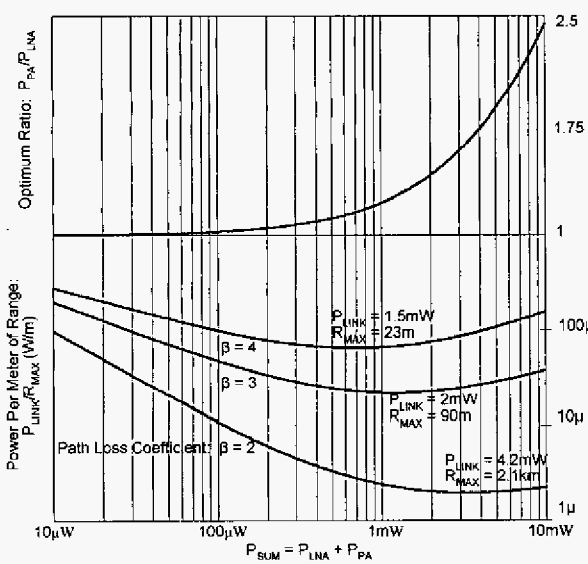
Power per meter of link range (P_{LINK}/R_{MAX}) is the value to be minimized over P_{SUM}, where $P_{SUM} = P_{PA} + P_{LNA}$:

$$\frac{P_{LINK}}{R_{MAX}} = \frac{P_{OH,RX} + P_{OH,TX} + P_{SUM}}{\sqrt[\beta]{\left(\lambda/4\pi\right)^2 \cdot \frac{e}{\alpha} \cdot \left[P_{SUM} + 2\gamma + \frac{\gamma P_{SUM} - 2\gamma^2}{\sqrt{\gamma^2 + \gamma P_{SUM}}}\right]}} \qquad (7)$$

P_{LINK}/R_{MAX} is plotted against P_{SUM} on the bottom of figure 2 for β=2–4. The assumed values of R_{ANT}, $P_{OH,TX}$, $P_{OH,RX}$, V_{DSAT}, and e are shown. With these assumptions, for β = 2 – 4, the optimum P_{LNA} = .3 – 1.3mW and P_{PA} = .4 – 2.1mW.

III. Low Power Transmitter Design

Transmitters perform three basic functions: generate an RF signal, modulate it, and drive it onto an antenna with a PA. Methods for increasing PA efficiency at low power output and reducing overhead power ($P_{OH,TX}$) needed for RF signal generation and modulation will now be discussed.



Assumptions: $P_{OH,TX} = P_{OH,RX} = 400\mu W$, e = 40%, f = 1GHz, V_{DSAT} = 200mV
V_{SUPPLY} = 1V, $R_{ANT} = 50\Omega$, BW = 1MHz, SNR = 10

Fig 2. Top: Optimum ratio of P_{PA}/P_{LNA} vs. P_{SUM}. Bottom: Power per meter of range P_{LINK}/R_{MAX} vs. P_{SUM} for β = 2-4.

A. RF Signal Generation

At the core of any RF transmitter is an oscillator that generates the carrier signal to be modulated and radiated. Since oscillator swing and start-up gain are proportional to bias current and resonator impedance $|Z_L|$, $|Z_L|$ must be maximized if bias current is to be minimized. For a parallel LC tank:

$$|Z_L| = \omega_o \cdot L \cdot Q_{tank} \qquad (8)$$

Q_{tank} is usually limited by the inductor, and the product $\omega_o \cdot L$ cannot be increased indefinitely due to both parasitic and tuning capacitance included in the oscillator. On-chip inductors typically have a lower L·Q product than discrete components, thus, previous low-power radios have used an off-chip inductor [1-3]. Rather than using an LC tank, a mechanical RF resonator with extremely high-Q (Q~1200) was used in the oscillator in [5]. Despite the high-Q, the RF impedance at resonance was lower than that possible using an LC resonator with an off-chip inductor.

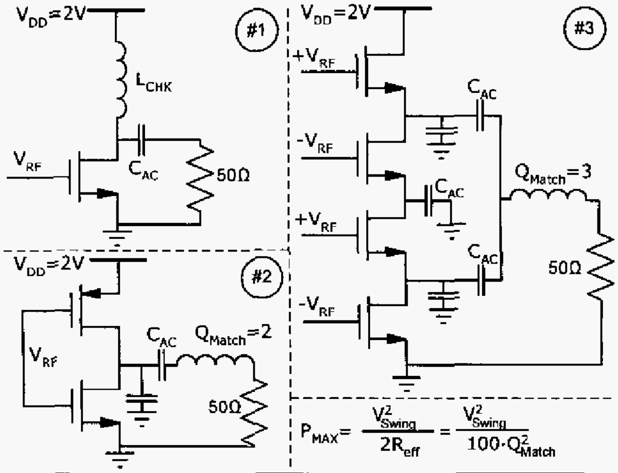
B. Modulation Techniques

Modulation is accomplished by changing the amplitude, phase and/or frequency of an RF signal relative to a stable reference. For a system to approach fundamental channel data capacity limits, precise phase and amplitude control are required. Such control requires additional circuit blocks, such as upconversion mixers, and fast, high-precision PLLs. Hence, spectral efficiency comes at the cost of increased power dissipation.

In contrast to many high-performance systems, sensor networks have drastically reduced communication range, and duty cycle, implying little need for optimal use of bandwidth. A simple modulation scheme that has seen use in sensor networks is OOK, wherein the entire transmitter is turned on only when transmitting a "1". With OOK, the transmitter's bias points and oscillator must settle in less than a single bit period, potentially limiting data rates. An attractive alternative that avoids settling limitations is binary FSK with a large modulation index (m=2-3). The large modulation index relaxes precision requirements so FSK can be accomplished by directly modulating the frequency of the oscillator – leaving only the PA and oscillator running at high frequency. An added benefit of FSK is that its constant envelope, continuous phase nature enables the use of an efficient, nonlinear PA [1], [3].

C. Efficient PA Design with Low Power Output

To avoid wasting power, the active element(s) in a PA should switch on and off completely and have close to 0V across them when strongly conducting – implying rail-to-rail swing is necessary for efficient operation. For a PA with very low power output, either the available voltage



$$P_{MAX} = \frac{V_{Swing}^2}{2R_{eff}} = \frac{V_{Swing}^2}{100 \cdot Q_{Match}^2}$$

PA Topology	V_{Swing}	$R_{eff}=(Q^2)50\Omega$	P_{Max}
#1	2V	50Ω	**40mW**
#2	1V	200Ω	**2.5mW**
#3	0.5V	450Ω	**275μW**

Fig. 3. Impact of PA topology and impedance boosting networks on maximum power output. Each PA will operate efficiently when swinging rail-to-rail and radiating approximately P_{MAX}.

headroom must be small or the PA load impedance must be high. An impedance converting network can be used to boost the PA load impedance by Q^2 at the center frequency. Additionally, stacking techniques may be employed to reuse bias current and reduce available voltage swing – permitting efficient operation with low power output (see figure 3). PA's with efficiencies greater than 40% have been reported with output power from 200μW to 10mW and beyond [1], [3].

IV. Low Power Receiver Design

The functions performed by a receiver can be summarized as: linear, low-noise amplification, channel selection, and demodulation. Several different receiver architectures have been proposed for sensor network applications, the most common ones are shown in figure 4 and described below.

A. Receiver Topology

One simple receiver topology that has seen use is a high gain RF amplifier with an envelope detector. This approach is sensitive to wide band interference or else requires an extremely high-Q channel select filter at RF. Furthermore, since an envelope detector requires 10's of millivolts to operate, substantial RF gain is necessary to achieve reasonable sensitivity.

Super-regenerative receivers create a high gain, extremely narrow band amplifier using an RF oscillator held near the cusp of oscillation. Following this with an envelope detector provides demodulation, resulting in a very simple receiver topology with the potential for low power operation. However, super-regenerative receivers are quite sensitive to pulling by interfering signals and generally suffer from slow settling and so must operate at correspondingly low data rates.

Zero-IF and low-IF receivers amplify incoming RF signals and mix them with an RF VCO to translate them to lower frequencies where voltage gain requires less power and channel selection may be done with on-chip filters. Though the RF VCO increases $P_{OH,RX}$ compared to simpler topologies, such receivers enable multi-channel communication, handle a wide variety of modulation techniques, and resist interference.

Zero-IF receivers require quadrature VCO outputs to differentiate signals at positive and negative frequency offsets from the carrier. All other processing occurs at baseband and can be accomplished for very little power. In a low-IF architecture, the quadrature signal may be dispensed to save power in exchange for a loss of image rejection and 3dB degradation of noise figure.

B. LNA and Mixer Design

Low power LNA's must achieve maximum g_m and voltage gain for a given current to minimize the input referred noise of the receiver front-end. For a CMOS LNA, maximizing g_m leads to large devices with small V_{DSAT} and low f_T. If the LNA drives an LC load, then the device capacitance can be absorbed by the tank and high voltage gain can still be achieved. If LC loads are not used, then the devices should be biased for higher f_T to keep capacitances low and maintain adequate voltage gain.

At low power levels, CMOS LNA's have a large, predominantly imaginary, input impedance. Thus, a high Q impedance boosting network can be used to

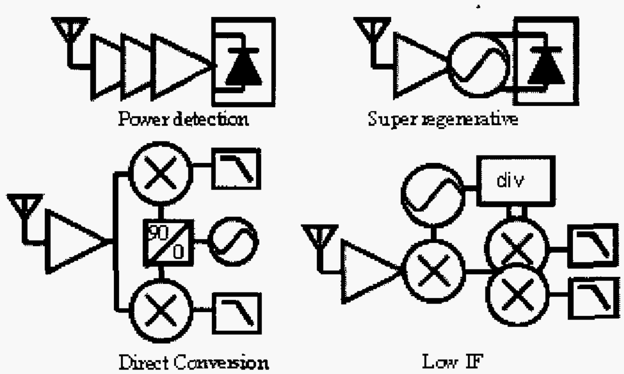


Fig. 4. Receiver Architectures discussed in section IVa. Low-IF is shown without image rejection, as implemented in [1].

simultaneously improve matching and *NF* while providing voltage gain. The effect of boosting impedance on *NF* is evidenced by the R_{ANT} term in (3). However, resistive losses in the matching network can degrade NF substantially.

Low power mixing can be accomplished with either passive or single-balanced active mixers. Active mixers provide gain and present minimal loading to the LNA, but they consume power and generate flicker noise. Passive mixers, on the other hand, consume no power, offer good linearity and do not generate flicker noise, making them attractive for low power designs, particularly with zero-IF.

V. Reported Low Power Transceivers

Only a handful of transceivers targeted at sensor networks have been published. The authors in [2], reported a 433MHz, zero-IF transceiver using binary FSK with a large modulation index, *m*. The VCO used an off-chip inductor and drove a passive, phase shifting network to generate quadrature signals. An off-chip matching network with Q = 4 was used in the receiver, effectively boosting R_{ANT} to 800Ω. The LNA and active mixers were stacked into one structure at just a 1.2V supply. This receiver achieved -95dBm sensitivity at 24kbps while consuming 1mW. The transmitter put out 10mW into 50Ω while burning 25.4mW.

In [1], a 900MHz, low-IF transceiver utilizing binary FSK with large *m* was reported. An off-chip inductor was used in the VCO, and the PA and mixer input capacitances were absorbed into its high Q LC tank – substantially reducing power overhead. To reduce cost, a 3V Lithium battery was chosen as the power supply. Modulation was performed open-loop by toggling switched capacitors in the VCO tank. To reduce $P_{OH,RX}$, this design utilized extensive stacking to re-use bias currents and did not generate quadrature or perform image rejection. While consuming only 1.25mW each, the receiver achieved -93dBm sensitivity at 100kbps and the transmitter put out 250μW into 50Ω. A 20m indoor link obstructed by two concrete walls was demonstrated between two of these transceivers, indicating $\beta = 3.3$, for these conditions.

In [5], a 1900MHZ, transceiver using OOK was reported. The receiver was super-regenerative, employing a Pierce oscillator stacked below a PMOS LNA. A high-Q (Q≈1200), off-chip, film bulk acoustic resonators (FBAR) was employed to perform channel selection and mitigate the inherent sensitivity to frequency pulling. The receiver consumed 400μW from a 1V supply and achieved a sensitivity of -100.5dBm at 5kbps. The transmitter employed an oscillator consuming only 220μW, and an inductively loaded PA radiating 375μW into 50Ω. The transmitter consumed 1.6mW total.

VI. Discussion

Table 1 compares the transceivers in [1], [2-3] and [5] with respect to the optimization performed in section II. The link power (P_{LINK}) reported in each design approaches the calculated optimum value fairly closely. Various techniques aimed at reducing power overhead were employed in [1] and [5], resulting in just a few 100μW overhead in both transmit and receive modes. Hence, the optimum link power for each is correspondingly lower.

In [2], a much higher $P_{OH,TX} = 7.5$mW, resulted in an optimum link power an order of magnitude greater than in [1] and [5]. The optimum P_{PA}/P_{LNA} value is also much higher, due to the boosted R_{ANT} in receive mode. Interestingly, the reported value for P_{PA}/P_{LNA} greatly exceeds the optimum, possibly due to higher expected duty cycles in receive mode.

REF	P_{LINK} *Reported (mW)*	P_{LINK} *opt. (mW)*	*e (%) PA*	*f MHz*	P_{PA}/P_{LNA} *reported*	P_{PA}/P_{LNA} *Opt*
1	2.5	2.2	40%	900	1.2	1.3
2	26.4	18.3	55%	433	185	9
5	1.2	1.2	27%	1900	6.8	2.5

Table 1. Calculated optimum parameters (with β=3) for transceivers in [1], [2] and [5] based on reported values of: $P_{OH,RX}$, $P_{OH,TX}$, R_{ANT}, *BW*, V_{SUPPLY} *and e*. Transmitter and receiver are assumed to have equal duty cycles.

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