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An Ultra-low Power 900 MHz RF Transceiver for Wireless Sensor Networks

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Abstract

A 900 MHz, ultra-low power RF transceiver is presented for wireless sensor networks. It radiates –6 dBm in transmit mode and has a receive sensitivity of –94 dBm while consuming less than 1.3 mW in either mode from a 3 volt battery. Two of these transceivers have been demonstrated communicating over 16 meters through walls at a bit rate of 20 kbps while using only 4 off-chip components.

Introduction

Wireless sensor networks are a rapidly growing area of research with countless applications in environmental monitoring, inventory tracking, etc. (1). Such networks are made up of small wireless nodes consisting of a suite of sensors, some custom analog and digital circuitry, a microprocessor, a power supply, and a means of communication. Although other methods have been suggested, the primary method of communication is through low-power RF communication.

Very low power sensors, analog circuits(2), and microprocessors (3) have been demonstrated. RF communication, however, has proven difficult to design to be truly low power because it requires efficient radiation and sensitive detection of high frequency signals (but see (4)).

Sensor networks are generally conceived of as being peer-to-peer networks wherein data gathered by one node is transmitted to the end user via a series of hops between nodes. Hence, the range required for nominal radio operation indoors, assuming one node per room, needs to be about 10 meters through at least one wall. The nodes are expected to be deployed for years, powered by a single battery or scavenged ambient energy. In either case, a mean power consumption of about 10 μW (5) is required. Given a reasonably low duty cycle on the order of 1%, radio power consumption must be limited to approximately 1 mW.

We present an ultra low power, 900MHz RF transceiver capable of communicating at 20 kbps at a range of greater than 16 meters while consuming a total link power of less than 2.5 mW in the transmitter and receiver combined. The transceiver consists of an oscillator, transmit antenna driver, high frequency divider and a digital frequency locked loop (FLL) as well as a low-IF receiver and FSK demodulator. The transmitter radiates 250 μW of power with an efficiency of 19% (including oscillator, divider, etc.) The receiver achieves a sensitivity of –94dBm while receiving 20 kbps and consuming approximately 1.2 mW. The transceiver requires only a single off-chip inductor, 32kHz quartz crystal, antenna, and Lithium coin cell battery for full functionality, at a total cost of $1.00.

System architecture

Two primary techniques were used to minimize power consumption in this design. The first was to make maximum use of the 3-volt supply available from a lithium cell battery by stacking multiple circuits in a single bias stack thus reusing bias current. The second was to include a single high-Q, high inductance, off-chip inductor for the resonant core of an LC oscillator and to drive all other RF circuits from the LC core of the oscillator (see figure 1).

For a differential swing of approximately $2V_{th}$ (to drive FET switches strongly on and off), the oscillator requires a power of $2 \cdot V_{th}^2/(Q \cdot L \cdot \omega)$. This oscillator requires a bias current of approximately $V_{th}/(Q \cdot L \cdot \omega)$ and about 1.2 V of headroom. To meet this current requirement while efficiently using available headroom, bias current from the oscillator is reused to supply all of the other RF and analog circuits in the radio.

Power depends critically on Q·L, which is maximized by using a single, off-chip inductor in the oscillator tank. Once a high-Q drive is available, it makes sense to use it to drive any other RF circuits' gates and so tune out those gate capacitances, reducing required power by approximately $1/Q$.

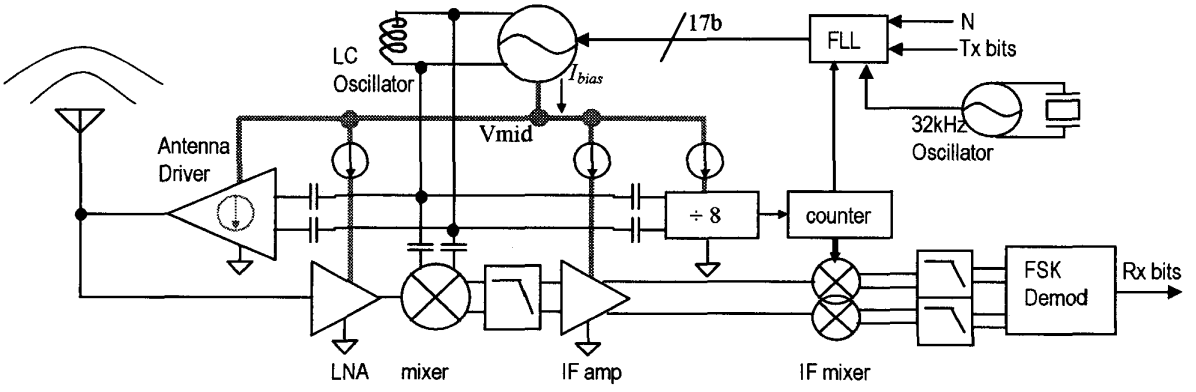

Figure 1. Full transceiver architecture. Bias current is reused by stacking oscillator "above" other RF circuits. The tuned oscillator core is AC coupled to other RF circuits.

Oscillator

The oscillator uses cross-coupled CMOS inverters to provide negative resistance across the single, off-chip inductor and an on-chip, digitally programmable capacitor array. The array is made up of 17 bits of switchable capacitors with sub-binary weighting to cover any mismatch and prevent dead-frequency zones. This array provides enough tuning to cover process and inductor variations while being able to reach the US ISM 900MHz band. Furthermore, the array was designed to maximize Q, achieving a simulated value of about 80 and so guaranteeing that Q was inductor dominated.

Transmitter

The transmitter consists of a buffer circuit driven by the oscillator and designed to efficiently drive low impedance antennas at low power. Frequency modulation is achieved by directly modulating the capacitor setting of the oscillator.

The primary design challenge of the transmitter is to drive a 100-300 μW RF signal onto a 50-200 Ω antenna while efficiently using the 200-300 μA and 1.6 V made available by the oscillator. Efficient use of the voltage headroom implies a peak swing of 1.6V/2, or 800mV. Similarly, efficient use of current implies using the full 250 μA bias current in a 50% duty-cycle push-pull structure, implying peak current swings of 500 μA. These two numbers translate to an ideal output impedance for the buffer of 800mV/500μA, or 1.6 kΩ, radiating 200 μW. Although this is the desired output power level, the impedance matching is far from ideal. Matching can be significantly improved by using two stages of push-pull buffer, stacked for current reuse, but connected in parallel by AC coupling capacitors at RF frequencies, as shown in figure 2. The result is that each stage is capable of 400 mV peak swing and contributes 500 μA, for a combined peak current of 1 mA, implying an impedance of 400 Ω, and output power of 200 μW. This matching is much improved and permits sufficient headroom for higher output power if needed.

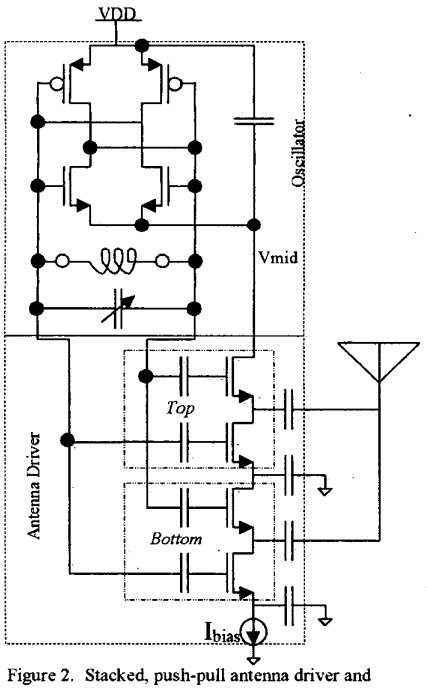

Figure 2. Stacked, push-pull antenna driver and oscillator. Voltage biasing for antenna driver not shown

The NMOS push-pull stages were designed to symmetrically load the oscillator. Devices were sized to optimally balance power dissipated in driving the gate capacitances and the power dissipated in the transistor's channels when they are hard switched. A tail current source was required to guarantee constant current operation to prevent changes in antenna impedance from dramatically changing the bias level and pulling the oscillator. Decoupling capacitors of 10 pF were required at the three intermediate points to reduce bias ripple and efficiently use head-room.

High frequency divider and FLL

For nodes to communicate while avoiding interference, they need to accurately set their local oscillator frequency. Since supply and environmental effects can cause oscillators to shift frequencies, it is necessary to include circuitry to lock the oscillator's frequency to a stable time reference. Sensor network nodes typically require a 32 kHz crystal oscillator as a real time clock (6), and so we included such an oscillator on chip and used it as our reference.

We locked the RF oscillator with a digital FLL as shown in figure 3. The oscillator feeds a continuously running counter, which is sampled each cycle of the reference signal. Subtraction of successive samples yields the frequency ratio between oscillator and reference signal. This ratio is compared to the desired ratio, and errors are accumulated and fed back to the oscillator. Intermediate taps from the counter are used as stable clocks and as the Low-IF of the receiver.

Although FLL circuits can be implemented in standard cell logic, the early stages of the counter will consume a great deal of power. This problem was partially solved by using custom, dynamic logic in early, high frequency stages of the counter. To reduce the input frequency of the counter, a ring divider (7), shown in figure 4, divides the oscillator signal frequency down by 8 before feeding into the counter.

In an N-stage ring divider, a single edge propagates around the loop, advancing by a single flip-flop each cycle of oscillator and so dividing the oscillator frequency by 2N. This structure saves power because only one flip-flop changes state per oscillator cycle. All of the passgates in all of the flip-flops are presented as a load to the local oscillator, whose tank tunes their capacitances out. A four-stage (divide-by-eight) ring divider was chosen to provide the optimal trade-off between reduced digital activity and increased loading in the oscillator. This approach reduces power by a factor of 2 over a simple chain of dynamic T-Flip-Flops.

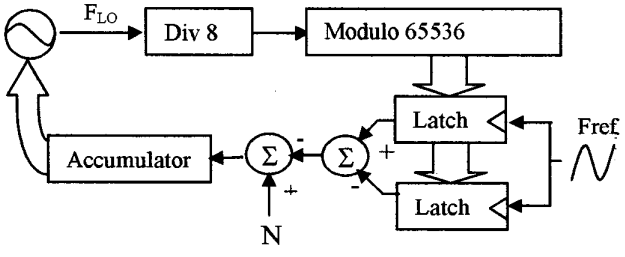

Figure 3. Digital frequency locked loop. $F_{LO} = 8 \cdot N \cdot Fref$

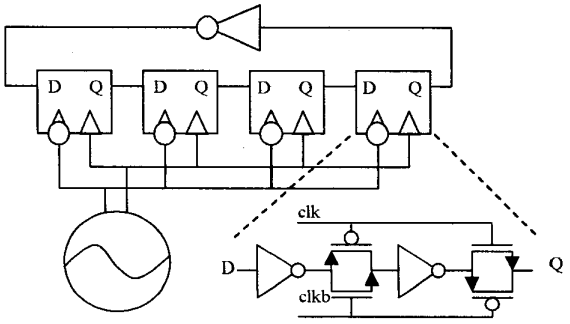

Figure 4. 4 stage ring divider using 8-transistor dynamic flip-flops.

Receiver

As seen in Figure 1, the receiver consists of an LNA, an RF mixer, low pass filtering, an IF amplifier, an IF mixer with IF spur rejection, a baseband chain including 3 poles of low-pass filtering, and an FSK demodulator. The receiver was designed to achieve two performance-related goals while consuming only 250 μA from the 1.6 V available from the oscillator. The first performance goal was to maximize sensitivity, which, along with the output power of the transmitter, dictates the maximum range at which nodes can communicate. The second goal was to minimize the degree to which out-of band interferers degraded sensitivity. This second requirement implies that linearity be maximized in the front-end, that IF and baseband circuits be band-limited to reduce the strength of out-of-band interferers, and that the IF mixer be designed to minimize unwanted mixing spurs.

Sensitivity is best maximized by concentrating gain in the first stage of the receiver. In this case the simplest high-gain circuit that did not require additional off-chip inductors was a self-biased CMOS inverter (see figure 5). The gain of such a stage is $(Gm_{NMOS}+Gm_{PMOS})/(\omega Cp)$, where Cp is the parasitic capacitance on the output of the LNA. In order to maximize gain and minimize input-referred noise in the front-end, most of the current available to the receiver was supplied to the LNA (approximately 200uA). The mixer consists of two NMOS switches driven differentially by the oscillator and sized to minimize noise without significantly increasing Cp. The output of the switching mixer was loaded with a large differential capacitance which interacts with the switching action of the mixer and Cp to form a single-pole switched-capacitor RC structure at the mixer output. Simulations of the front-end showed a gain of 20dB and noise figure of 9dB as well as an outband compression point of −18dBm.

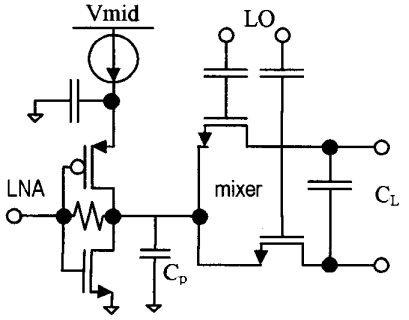

Figure 5. Receiver front-end.

The voltage signal present on the output of the mixer is fed to a differential IF amplifier, which consumes approximately 50 μA and provides an additional 26 dB of gain. The IF amplifier drives an 8-phase sampling mixer. The switches of this structure are turned on in succession by eight, phase split, 12.5% duty-cycle signals at the IF frequency. These switches sample the input signal onto eight capacitors. The sampled signals are then recombined through a pair of 3-input differential amplifiers. Each amplifier takes three 45°-split signals, gains the intermediate signal by 1.4 and sums the signals, passing the fundamental mixing term with a total gain of 2, but canceling the 3rd and 5th-order mixing terms, similar to mixers designed by Weldon et. al. (8). By using two such amplifiers and feeding them signals shifted by 90°, both in-phase and quadrature outputs are generated. These in-phase and quadrature signals are further amplified and filtered before being FSK demodulated (9).

Coupling of RF signals from the oscillator to the LNA input leads to DC offset at the output of the RF mixer. The IF mixer up-converts this DC out-of-band. If the DC is excessive, however, it can saturate the input of the IF amplifier, therefore, a programmable, differential current source was included across the RF mixer output to cancel gross offsets.

Biasing and system level-design

Floating current sources were used in the distribution of current from the oscillator to various blocks (i.e. the LNA, divider and IF amplifier). These sources consisted of high-ratio PMOS current mirrors whose sources drew from the lower bias point of the oscillator and fed current into the highest bias point of their respective circuits.

All bias currents were made programmable, allowing for variable output power in the transmitter, and on-line optimization of power consumption in exchange for sensitivity in the receiver. The IF frequency was programmable from approximately 1.75 MHz to 100 kHz. Correspondingly, IF and baseband bandwidths were made programmable.

The transceiver was designed in a 0.25μm, 2-poly, 5-metal CMOS process. The active die area is 1.1 mm^2 (see figure 6). Bare die were mounted directly on-board for testing.

Results

The oscillator shows a tuning range of 820MHz to 970MHz with a frequency resolution of 3 kHz. Phase noise was

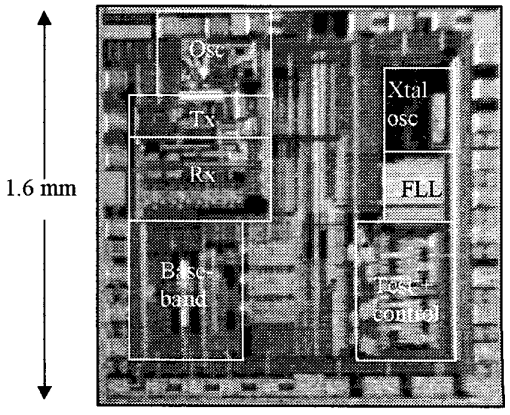

Figure 6. Die photograph

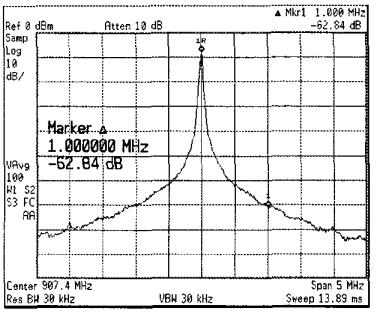

Figure 7. Output spectrum of oscillator. Phase noise at 1MHz offset is –107.6dBc/Hz

measured to be –107.6 dB/Hz at 1 MHz offset (see figure 7). The FLL functions as designed, locking the oscillator to programmed frequencies and maintaining those frequencies under perturbations of bias and supply. The FLL, once locked, has no detectable affect on phase noise.

The transmitter, at a nominal power setting, consumes 1.3 mW while radiating 250 µW, for an efficiency of 19%. Programming the transmitter bias current over a wide range shows that it can radiate anywhere from 60 µW to 380 µW and maintain an efficiency of better than 15% for output powers greater than 150 µW (see figure 8). Output power up to 1 mW is possible by destacking the transmit driver out from under the oscillator and shunting in additional bias current to the oscillator. Efficiency is degraded in this mode to about 13%.

Sensitivity in the receiver was measured by decreasing the power of an in-band monotone signal representing a string of ones until erroneous bits began to appear. For nominal settings this resulted in a sensitivity of –94 dBm while consuming 1.2 mW. Noise Figure was also measured and found to be 12 dB. At lower bias settings, a mildly degraded sensitivity of –90 dBm was measured while consuming only 800 µW from 2.7 V.

Effects of interfering signals were assessed by injecting a -90 dBm signal inband at the same time as an interfering signal. The interfering signal was swept across frequency, and at each frequency its power was ramped up until bit errors began to occur. The results of this test are summarized in figure 10. Far out blockers desense the receiver by 4dB when they reach about –13dBm. Exceptions are those blockers close to the wanted signal, its image, and those matching the 7th, 9th, 15th, and 17th harmonics of the IF, where unwanted

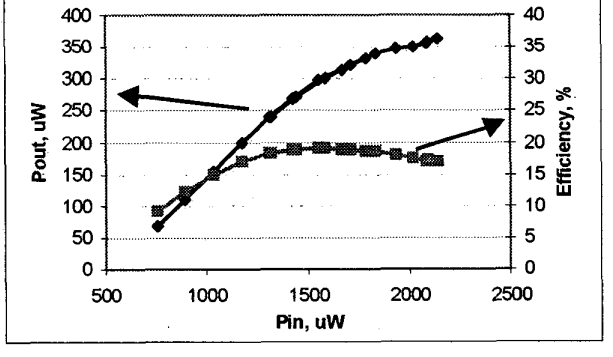

Figure 8. Transmitter power and efficiency vs input power.

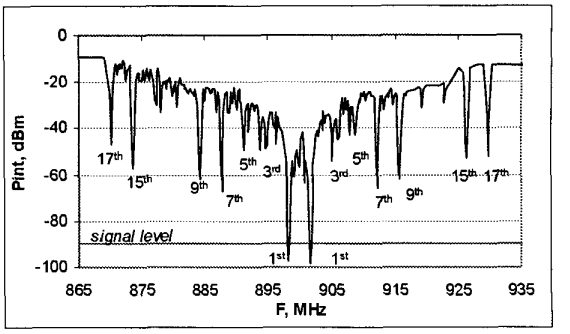

Figure 9. Blocker level required to interfere with a –90dBm signal at 901.6 MHz, vs Frequency. Numbers refer to harmonics of the IF.

mixing products cause the blocker to be down converted into band. It is notable that some desensitization is also present at the 3rd and 5th harmonics, but it is suppressed due to the harmonic cancellation in the IF mixer.

All tests were done using 50Ω RF equipment, with a single 15nH inductor in series with the antenna port, to simulate tuning that could be built into the antenna.

Finally, system-level tests were performed wherein a chip in transmit mode was outfitted with an antenna and driven by square wave modulation. A second chip in receive mode, also outfitted with an antenna, was placed some distance away. Monitoring the receiver's output bits showed that for short range communication, the link could support 100kbps with essentially no errors. For a range of 16 meters indoors, through two concrete walls, the link could support at least 20kbps. Both chips were in nominal bias states.

Conclusion

A transceiver is presented which meets the requirements for cheap, low-power wireless sensor networks. In transmit mode, it consumes 1.3 mW while radiating 250 µW and in receive mode consumes 1.2 mW while maintaining a sensitivity of –94 dBm. Furthermore, this transceiver has been demonstrated to communicate 20 kbps at ranges of greater than 16 meters indoors.

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