

# A 256-Element CMOS Imaging Receiver for Free-Space Optical Communication

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## Abstract

This paper describes a CMOS imaging receiver for free-space optical (FSO) communication links. The die contains 256 parallel receive channels with  $-47$  dBm optical sensitivity and 30 dB optical dynamic range. Arbitration circuitry multiplexes the data to a common bus. The 1.6 M transistor mixed-signal circuit is realized in  $0.25\ \mu\text{m}$  CMOS and measures  $6.5 \times 6.5\ \text{mm}^2$ . Reception at 500 kbps through a 1 km turbulent channel is demonstrated with 10 mW optical transmit power.

## Introduction

Visible light can be collimated to 1 mrad divergence by a mm scale lens, allowing small optical transmitters to achieve antenna gains greater than 60 dB and enabling small low power transceivers to communicate at high data rates over multiple kilometers. At RF wavelengths of a few cm, such antenna gain would require an antenna hundreds of meters in diameter. An additional benefit of such high antenna gain is that transceivers do not interfere with each other when not properly aligned, leading to natural multiple-access through spatial division (SDMA), without the need for code or time division architectures. FSO does have some restrictions, most notably an optical line of sight requirement, and is therefore only suitable for certain applications. The receiver described in this paper is designed for communication between small unmanned aerial vehicles (UAVs), where size and power are tightly constrained, video data rate communication is required over links greater than 1 km, and line of sight is available [1].

In daylight, ambient illumination provides strong dc interference for an FSO receiver. The dc signal itself can be filtered, but it generates wideband shot noise that limits noise performance. Ambient illumination can be reduced with a narrowband optical filter, but this is often insufficient. Further reduction of the ambient signal can be accomplished with an imaging receiver consisting of a lens and a photodetector array as shown in Fig. 1 [2]. Received ambient light is spread across the detector array based on angle of incidence. This reduces the shot noise power at each detector, while one detector ideally receives the full signal. High array resolution is desirable to improve the optical signal-to-noise ratio, but increasing array resolution increases signal processing requirements and makes interconnect between a detector array and external electronics difficult. Integration of the detector array with associated receiver electronics in a single CMOS die provides a way to achieve high array resolution and high data rates simultaneously.

This paper describes a 256-element CMOS imaging receiver with a photodetector and receiver electronics integrated at every element, allowing multiple transmissions to be received simultaneously. The receiver is designed to operate over a link range of 100 m to 5 km, requiring an optical dynamic range of 34 dB and a minimum detectable signal of  $-46$  dBm, with up

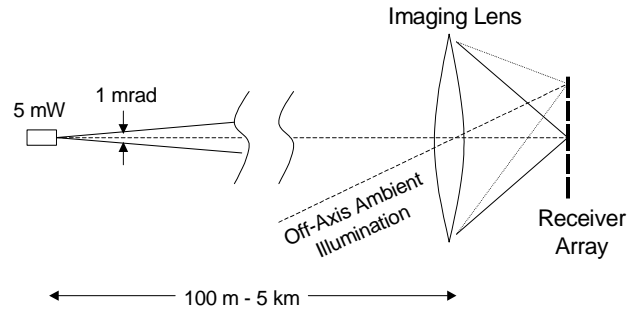


Fig. 1. An imaging receiver uses a lens to divide received light based on angle of incidence, separating the desired signal from most ambient illumination.

to 250 nW ambient illumination at each element. For longer links in this range, atmospheric turbulence leads to time varying channel attenuation on the order of 10 dB at the ms time scale that must be tracked and corrected by the receiver [3]. The following section describes the architecture and circuit implementation designed to accept such wide dynamic range, low power, and time varying signals, with low enough power consumption and complexity to allow for array integration. Mixed-signal issues pertaining to array integration are discussed and performance of the commercially fabricated 256-element imaging receiver confirms the designed sensitivity and dynamic range. Measured results of a 1 km FSO link are presented, demonstrating the ability to correct for time varying turbulent attenuation, and that long range, low power FSO links are realizable with such an imaging receiver.

## Receiver Design and Performance

### A. Front-End Detection

Optical signals are detected by a reverse biased n-well junction diode that generates a current proportional to incident optical power. Measured optical responsivity is  $0.36\ \text{A/W}$  at 660 nm in the process utilized. The  $-46$  dBm minimum detectable optical signal and 34 dB dynamic range specified above translate to a minimum current of 9 nA and a dynamic range of 68 dB (because optical power is converted linearly to signal current), with 100 nA dc ambient interference.

The transimpedance amplifier, shown in Fig. 2a, is a common choice to detect and amplify weak current signals in optical receivers [4]. The transimpedance amplifier can use  $A+I$  times higher resistance than the low impedance topology shown in Fig. 2b with equivalent bandwidth, reducing resistor noise current. However, in this power constrained application, the noise contribution of the amplifier itself must be considered. If the MOS voltage amplifier has a single pole response it can be shown that the amplifier's contribution to the total transimpedance noise power depends on the signal bandwidth  $B$ , the input capacitance  $C_D$ , the closed loop phase margin, and a noise equivalent  $g_m$ , close to the transconductance of the input device. It does not depend on the transimpedance. The input referred noise contribution of the amplifier is given by

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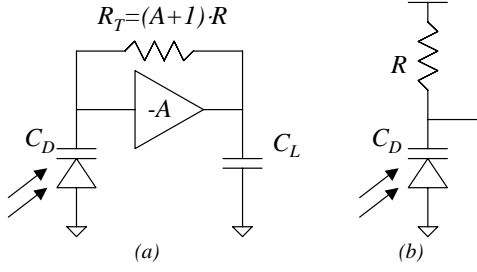


Fig. 2. (a) Transimpedance, and (b) low impedance front ends.

(1), where  $k_m$  is a dimensionless parameter dependent only on the phase margin, approximately 2 for 60° margin.

$$\overline{i_{n,T}^2} \approx 4\pi^2 kT \cdot B^3 C_D^2 \frac{k_m^2}{g_m} \quad (1)$$

In comparison, the input referred noise of the low impedance topology is given by (2).

$$\overline{i_{n,L}^2} = 4\pi^2 kT \cdot B^2 C_D \quad (2)$$

These noise levels are related in (3), which shows that despite arbitrarily low resistor noise, the transimpedance topology requires a minimum transconductance relative to the application dependent admittance  $B \cdot C_D$  in order to achieve superior noise performance. This implies some minimum power consumption, below which the low impedance architecture has lower input noise current.

$$\frac{\overline{i_{n,T}^2}}{\overline{i_{n,L}^2}} = \frac{k_m^2 B \cdot C_D}{g_m} \quad (3)$$

In the receiver described here, power constraints limit  $g_m$  to approximately 100  $\mu$ S, diode capacitance is 0.67 pF, and front-end bandwidth is 2.4 MHz, leading to similar noise performance for the two architectures. However, the low impedance architecture has an advantage in terms of dynamic range since the load impedance can be non-linear or varied over an arbitrarily large range without any stability consideration. Therefore, this receiver uses a low impedance front end with a maximum sense impedance of 100 k $\Omega$ , implemented with a polysilicon resistor, achieving an rms input referred resistor noise of 0.80 nA with a density of 0.41 pA/ $\sqrt$ Hz.

The detected signal is amplified by an LNA based on the circuit shown in Fig. 3b, designed for fixed 10 dB gain and 67  $\mu$ V rms input noise, including flicker noise. With 100 k $\Omega$  sense impedance, this is equivalent to an rms front-end noise

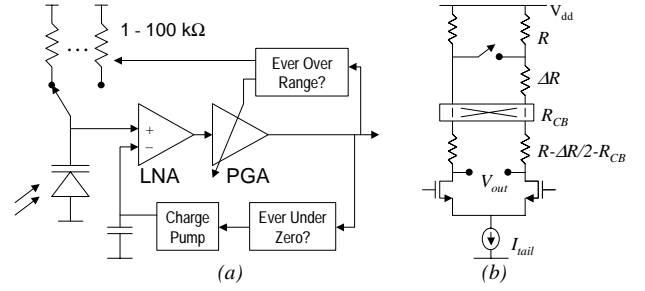


Fig. 3. (a) Gain and offset control architecture based on a 0-33 dB PGA, selectable sense impedance, and a charge pump. (b) LNA and PGA amplifier topology with programmable gain and offset, with only one of three offset control crossbar switches shown.

current of 0.67 nA. Combined with the front-end resistor noise discussed above and 0.34 nA rms shot noise from 100 nA dc ambient signal over a 2.4 MHz bandwidth, the total rms input referred noise is 1.10 nA with a noise density of 0.71 pA/ $\sqrt$ Hz. Fig. 4 shows the measured eye diagram for a 19 nW (-47dBm) optical test pattern applied directly to the receiver, which generates a 7 nA average (14 nAp-p) front-end signal. Ambient illumination was adjusted to generate a 100 nA dc front-end signal in addition to the test signal to include the effect of ambient induced shot noise. The total current is detected with 100 k $\Omega$  sense impedance, the described LNA, and further voltage amplification for off-chip measurement. The dc ambient signal is subtracted by an automatic offset control loop described below.

### B. Gain and Offset Control

Automatic gain control (AGC) is used to achieve wide dynamic range and correct for time varying channel attenuation as shown in Fig. 3a. The AGC loop is based on a 0-33 dB programmable gain amplifier (PGA) with 3 dB step size and selectable front-end sense impedances of 100 k $\Omega$ , 10 k $\Omega$ , and 1 k $\Omega$ . Signals are fully differential, but shown single ended for clarity. AGC feedback is determined by comparing the signal peaks to an over-range threshold. Manchester signal coding guarantees that a data “1” can be observed within any 1.5 bit period window, allowing gain control steps to be performed every 2 bit periods. Logic in the AGC loop automatically adapts to signal conditions, performing a fast two-phase gain search for new signals, and then slew limited gain control to track variations once a signal is recovered. Fig. 5 shows measured AGC loop response for weak and strong incident signals. Worst-case recovery time over the full dynamic range is 14 gain steps, taken in 28 bit periods. Maximum signal power is measured to be 21  $\mu$ W average, 30.4 dB higher than the minimum detectable signal of

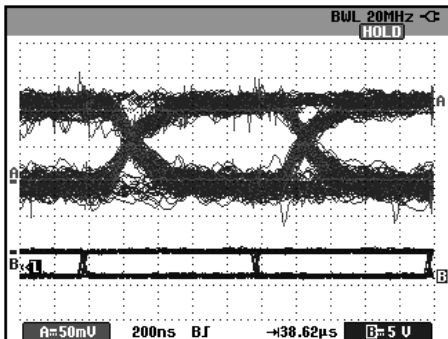
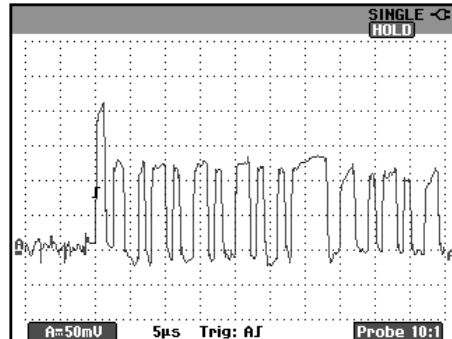
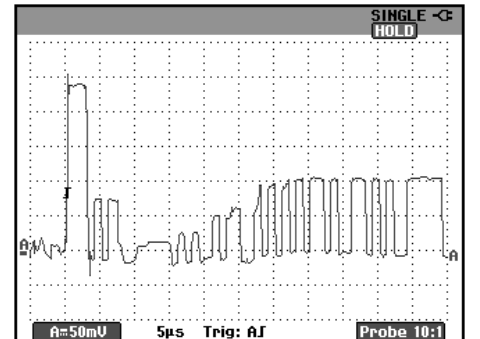


Fig. 4. Measured eye diagram for 19 nW signal with 100 nA dc front-end current.



(a)



(b)

Fig. 5. AGC recovery of new signals for (a) 19 nW average power and (b) 10.1  $\mu$ W average power, which is initially amplifier limited and automatically utilizes a two phase search.

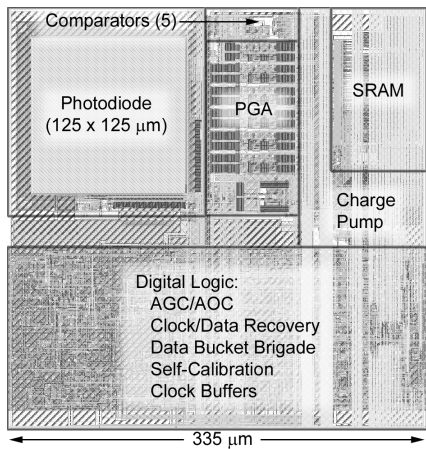


Fig. 6. Single element receiver layout.

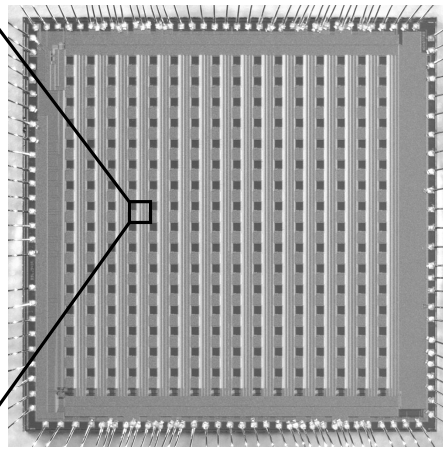


Fig. 7. Micrograph of the  $6.5 \times 6.5 \text{ mm}^2$  die.

19 nW discussed above. This corresponds to a 60.8 dB dynamic range in received signal current.

Fig. 3a also shows the automatic offset control (AOC) architecture used to correct for slowly varying ambient illumination. AOC feedback is determined from the signal minima, as opposed to signal average as in ac coupling. This is so that no immediate offset adjustment is needed when a new signal arrives, as seen in Fig. 5. Thus, the AOC loop runs much slower than the AGC loop without affecting acquisition time. Operating the parallel AGC and AOC loops at different time scales decouples their stability constraints.

The PGA is implemented with a six stage amplifier based on the topology shown in Fig. 3b with one gain control bit and three offset control bits covering an 80 mV range at each stage. The open loop topology is used because on off keyed signals are tolerant of moderate non-linearity. The first five PGA stages are programmed to 0 or 6 dB per stage in a thermometer fashion, and the sixth stage is programmed to 0 dB or 3 dB. Offset errors at each stage contribute to a total input offset that varies with the gain state. Uncorrected, this error is greater than the minimum detectable signal. On-chip foreground self-calibration cycles through all gain combinations, and at each gain recursively corrects the offsets of the amplifiers in the PGA chain. Residual uncorrected offset at any PGA stage is amplified and then included in the correction at the next stage. By dividing the offset trim over multiple stages, an input referred offset error less than 100  $\mu\text{V}$  is achieved without any precision circuits. Offset correction codes are stored in a 128-bit per-pixel SRAM, and applied at the same time as gain updates.

The charge pump for ambient offset control is based on the switched capacitor circuit presented in [5]. The control voltage is applied to a second differential pair in the LNA, generating a current that is summed with the signal at the LNA output. This path has a lower bias and lower gain than the signal path so that it contributes negligible noise. Charge pump step size varies with PGA gain to alleviate the trade-off in stability at high loop gain vs. slew rate at low loop gain.

### C. Receiver Array Design

Layout of the single element receiver described above, as well as necessary clock and data recovery, data framing, and on-chip communication circuits is shown in Fig. 6. The n-well photodiode in the upper left corner fills 14% of the layout

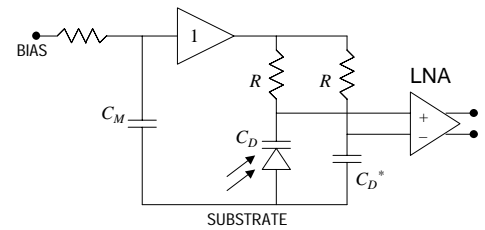


Fig. 8. Substrate noise coupled to the photodiode is converted to a common-mode signal through a replica coupling path and bias compensation.

area. This single element is the basis of the 256-element receiver shown in Fig. 7. A serial bus allows programmability of global registers that control AGC and AOC loop operation and the ability to select various operating windows within the array. The total die size is  $6.5 \times 6.5 \text{ mm}^2$  with a core imaging area of  $28.7 \text{ mm}^2$ . Full array power consumption is 67 mW (56 mW analog, 11 mW digital), excluding I/O.

When a data word up to 16 bits in length is received at any location within the array it is tagged with an address and passed down the column from pixel to pixel in a bucket brigade manner, then across the columns toward a shared off-chip data bus in one corner of the die. Contention for data passing resources can occur when a receiver element and its upstream neighbor simultaneously try to send data downstream. Similar contention arises at the bottom of each column. Synchronized four phase handshaking provides arbitration for such cases, passing one word and then the next in a predetermined order without any possibility of metastability. If two merging data streams exceed the maximum data rate, some data words are arbitrarily dropped.

### D. Mixed-Signal Integration Challenges

Each element in the imaging receiver incorporates an assortment of digital logic as shown in Fig. 6. The complete receiver array shown in Fig. 7 contains over 1.6 M transistors, most of which operate in the digital domain. In the dual well process used, the n-well photodiodes connect directly to the substrate, providing a path for digital interference from these transistors to couple to the LNA inputs. Furthermore, these sensitive analog circuits are thoroughly integrated throughout the array of digital electronics, not isolated in one corner of the die as in many mixed-signal circuits. In addition to the use of an epitaxial wafer with low substrate resistance, circuit techniques are used to minimize substrate noise injection from digital circuits and to provide front-end immunity to any injection that does occur.

Substrate noise is minimized through design of a custom logic library designed for low energy and area, leading to low slew rates, low supply bounce, and small drain junction areas, all of which reduce substrate current injection. This is accomplished at the expense of performance by using near minimum size devices and operating the logic circuits at 1 V, since timing requirements are modest compared to intrinsic logic delays in the 0.25  $\mu\text{m}$  CMOS process utilized.

Two circuit techniques shown in Fig. 8 are used to convert any substrate noise at the photodiode into a common-mode signal at the LNA. The first technique is to connect the negative LNA differential input to the substrate through a replica path. The replica capacitor  $C_D^*$  is not a matched n-well junction diode due to area constraints, resulting in some time constant mismatch for the two paths from the substrate to the LNA inputs. This results in a band pass response from the substrate to the LNA differential mode, with peak magnitude response equal to one half the fractional time constant mismatch at the band edge. Substrate noise is also mirrored to the top of the photodiode bias network with a single stage unity gain amplifier to further reduce feed through to the differential mode. These circuits rely on  $C_D^*$  and  $C_M$  coupling to the same substrate voltage as  $C_D$  within the signal band, which is accomplished by terminating  $C_D^*$  and  $C_M$  to a substrate tap encircling the photodiode.

### Free-Space Link Measurement

Laboratory testing of the fully integrated receiver array was performed by illuminating individual photodiodes with a directly aligned optical fiber with a known exit beam power. Twenty four pixels throughout the array were tested at random without defect. Results discussed in the previous section include a minimum detectable signal of 19 nW (-47 dBm) and 30.4 dB dynamic range, commensurate with the requirements of multi-km FSO links under the size and power constraints of the intended application. To verify this, and demonstrate the ability of the AGC loop to track and correct for time varying channel attenuation, communication over a 1 km free space link was tested.

The free space link was established in Berkeley, CA after sunset, at an average elevation of a few tens of meters above ground level. Testing at night eased practical issues such as link alignment, but did not test immunity to daylight interference. Receiver immunity to 100 nA dc front-end interference with a minimum strength signal was demonstrated in the laboratory as discussed above. Pseudo-random data words were transmitted at 500 kbps with a 10 mW average power 660 nm laser beam with 1 mrad divergence. The imaging receiver was implemented with the 256-element receiver array described above placed at the focal plane of a 1 inch diameter collection lens, oriented such that the received signal was focused onto a known receiver in the array for testing. A typical received waveform at the PGA output for this pixel is shown in Fig. 9. While receiving data in this test, the AGC loop was continuously tracking time varying channel attenuation due to atmospheric turbulence. This is shown in Fig. 10, which shows the mean recovered signal level at a longer time scale, measured by low pass filtering the PGA output. Three visible gain control steps are taken to keep the mean signal level near the data threshold.

Over 99% of data words were received and communicated via the off-chip data bus without any bit errors. This error rate is acceptable for applications that are tolerant of data loss, such as voice communication. In applications that demand lower error rates, forward error correction can be applied at the system level at some expense in bandwidth.

### Conclusion

A 256-element imaging receiver for FSO communication has been integrated in a 0.25  $\mu\text{m}$  CMOS die measuring

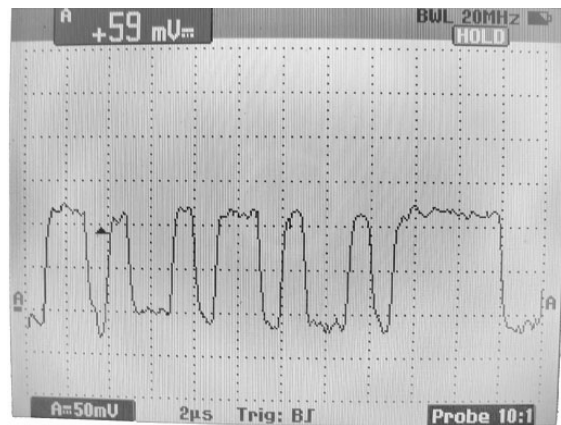


Fig. 9. Recovered signal received over 1 km free-space link.

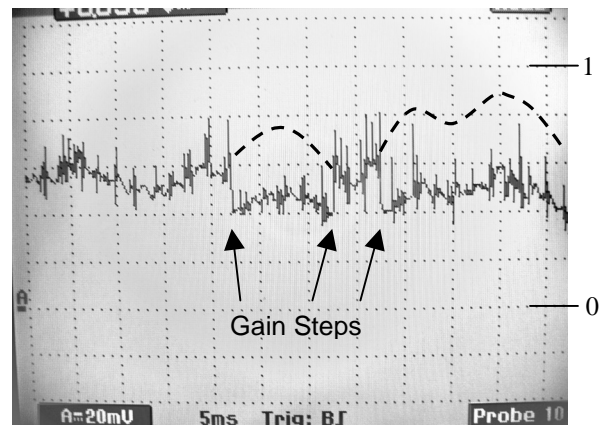


Fig. 10. Mean signal strength over 1 km free space link with automatic gain control. Three discrete gain control steps compensate for varying channel attenuation, keeping the signal mean midway between the indicated 0 and 1 data levels. The dashed line shows the extrapolated trajectory of the signal mean without gain control.

$6.5 \times 6.5 \text{ mm}^2$ . The 1.6 M transistor mixed-signal circuit has a measured minimum optical signal power of -47dBm and a 30 dB dynamic range at 500 kbps with Manchester data coding. Total power consumption is 67 mW, excluding I/O. Communication over a 1 km horizontal path near ground level was demonstrated with a 10 mW, 1 mrad transmission at 660 nm and a 1 inch receiver aperture. This demonstrates the feasibility of long range FSO communication with small low power transceivers, despite the presence of time varying channel attenuation due to atmospheric turbulence. Noise analysis resulting in (3) shows that, despite arbitrarily low resistor noise current, the commonly used transimpedance amplifier topology has higher noise than the low impedance topology in the low power region of the design space. Circuit techniques have been presented to cope with the mixed-signal challenge of sensing weak, substrate-coupled signals throughout a large digital circuit.

### References

- [1] M. Last, et al, "Toward a wireless optical communication link between two small unmanned aerial vehicles", IEEE International Symposium on Circuits and Systems (ISCAS), Bangkok, Thailand, May 2003.
- [2] P. Djahani and J. M. Kahn, "Analysis of Infrared Wireless Links Employing Multi-Beam Transmitters and Imaging Diversity Receivers", *IEEE Trans. on Commun.*, vol. 48, no. 12, Dec. 2000.
- [3] L.C. Andrews and R.L. Phillips, *Laser Beam Propagation through Random Media*, SPIE Optical Engineering Press, 1998.
- [4] J. Franca and Y. Tsividis, *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, 2<sup>nd</sup> Ed., Prentice Hall, 1993.
- [5] G. Wegmann, E.A. Vittoz, and F. Rahali, "Charge injection in analog MOS switches", *JSSC*, vol. SC-22, no. 6, Dec. 1987.