An SOI Process for Fabrication of Solar Cells, Transistors and Electrostatic Actuators

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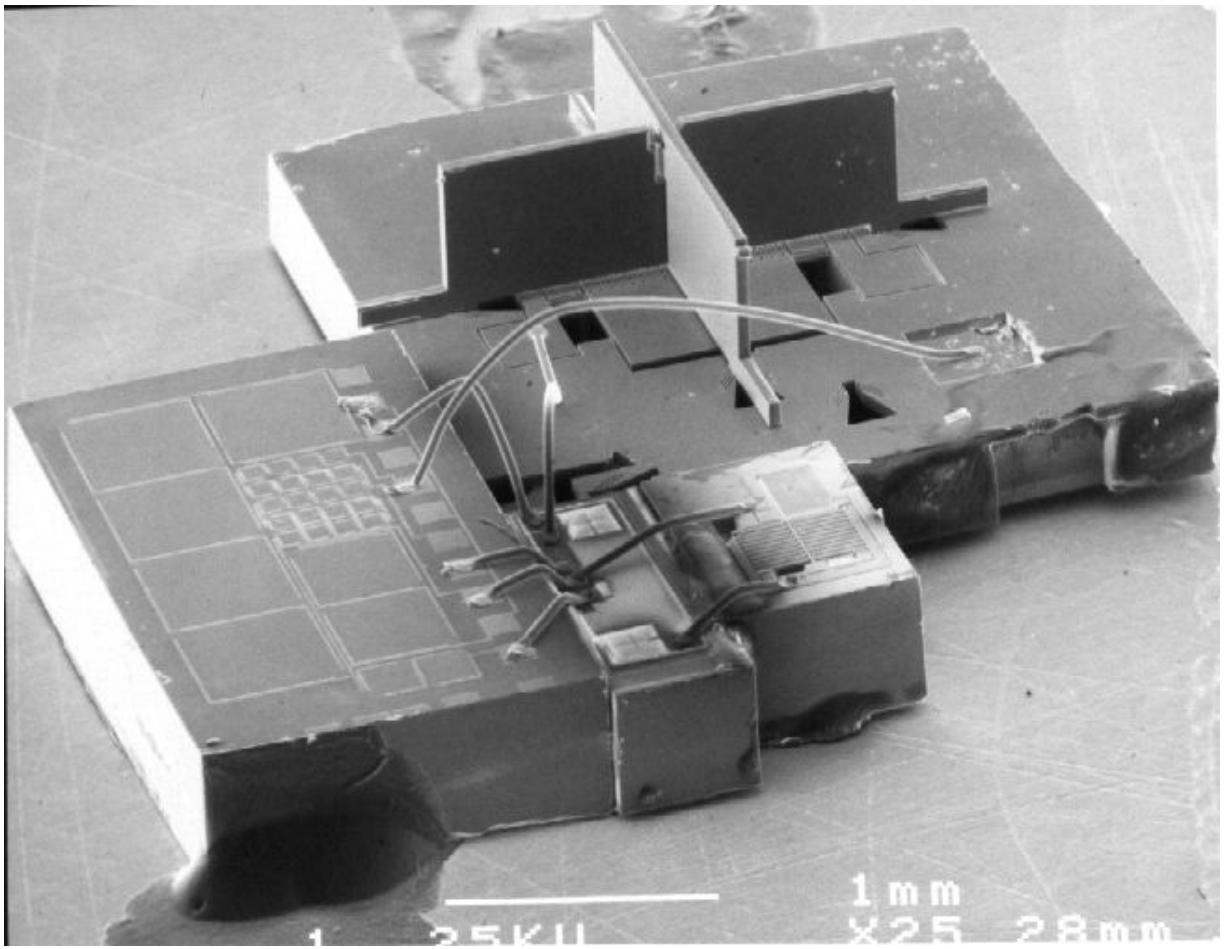
Target Applications

- Autonomous Microsystems
  - Distributed sensor networks - SmartDust
  - Microrobots
- System Components
  - Power sources
  - Circuits
  - Actuators/Sensors

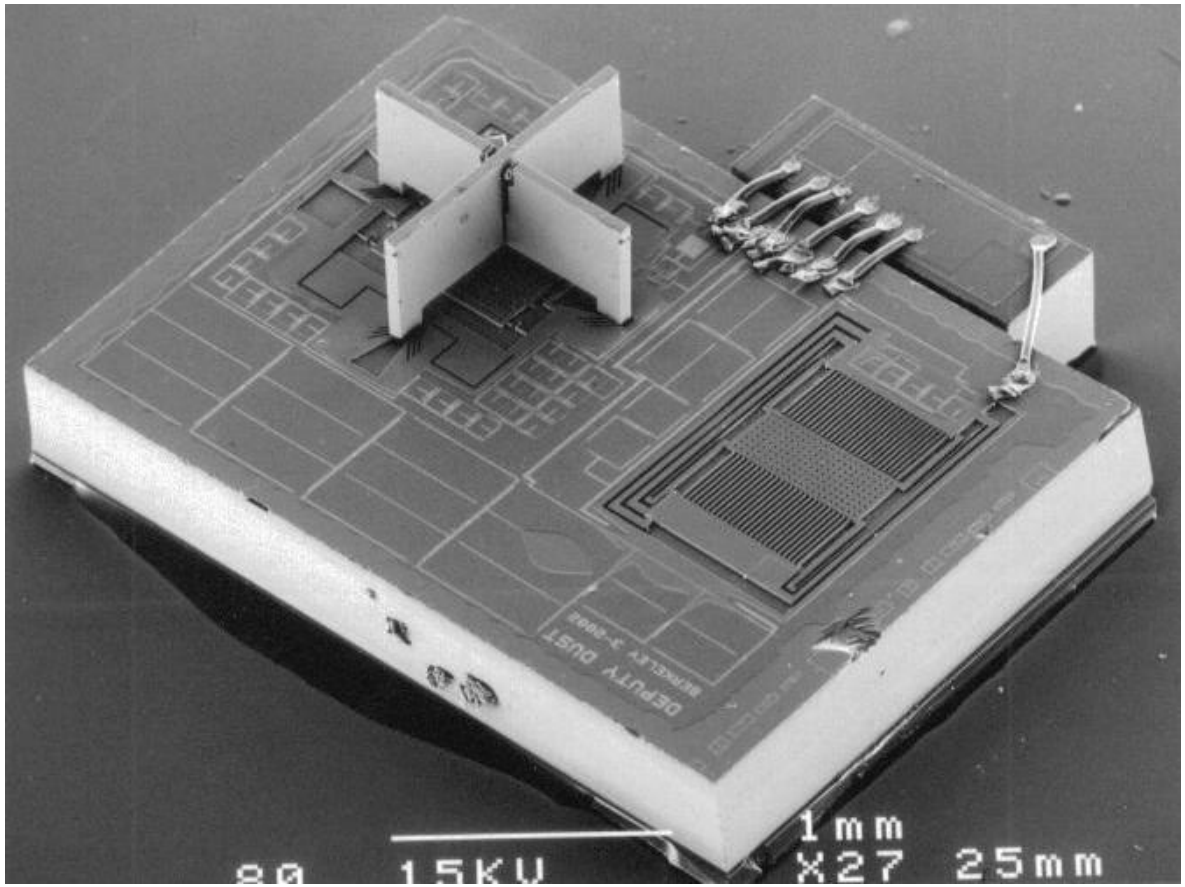
Golem Dust



Process Goals

- Integration - Simplify
  - Reduce the number of separate components
    - Simplify assembly
    - Reduce size
- Solar Power
  - Reduce/eliminate need for stored power
  - Increase life of device
- High-Aspect Ratio MEMS Devices
  - Wide range of possible sensors and actuators

Deputy Dust



System Architecture

- Two chip solution for autonomous MEMS
  - MEMS chip – power and actuation
    - High voltage solar cell arrays
    - Electrostatic actuators and sensors
    - High voltage buffers
  - CMOS chip – control
    - Low voltage, commercial CMOS chip

Selected Technology

- Single crystal silicon
  - Good efficiencies are possible
  - Solar cell performance is stable over time
  - Established processing technology
  - Processing is similar to CMOS processing
  - Requires thicker cells for full power extraction
- Silicon-On-Insulator
  - High-aspect ratio MEMS devices
  - Available means of isolation
    - Back-filled isolation trenches

Summary of Process Features

- Single crystal silicon solar cells
  - Fabricated in the device layer of an SOI wafer
- High-aspect ratio MEMS devices
- Back-filled isolation trenches
  - Connect many solar cells in series to achieve high voltage output
  - Mechanically attached but electrically isolated MEMS devices
- Basic circuits from solar cell processing steps

First generation – NMOS process

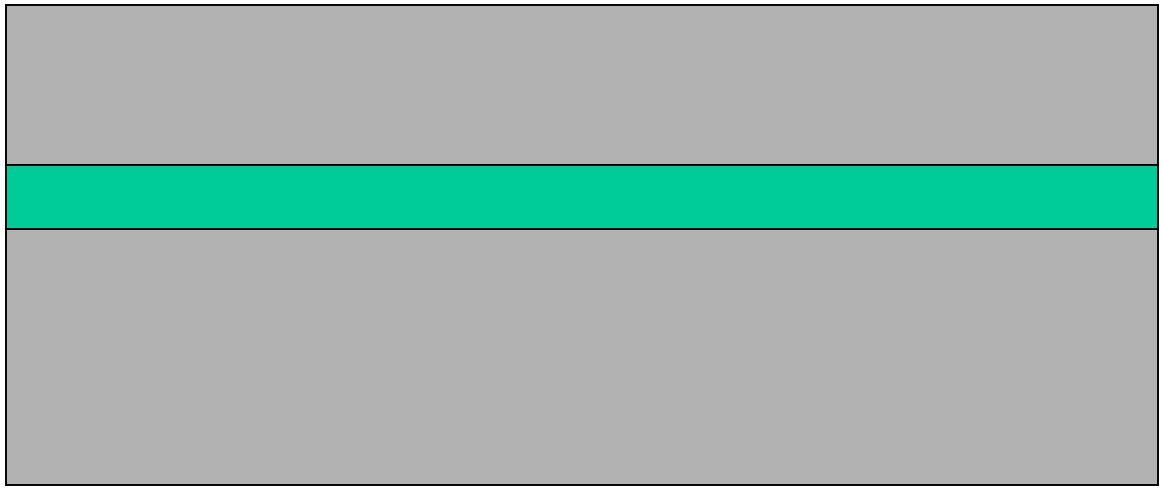
- Design focus – Solar cells
- Circuit capabilities
  - NMOS transistors with metal gates

Process overview

- Four process stages
  - SOI wafer fabrication
  - Isolation trench etching and back-filling
  - Solar cell and circuit fabrication
  - Actuator etch and release

SOI Wafer Fabrication

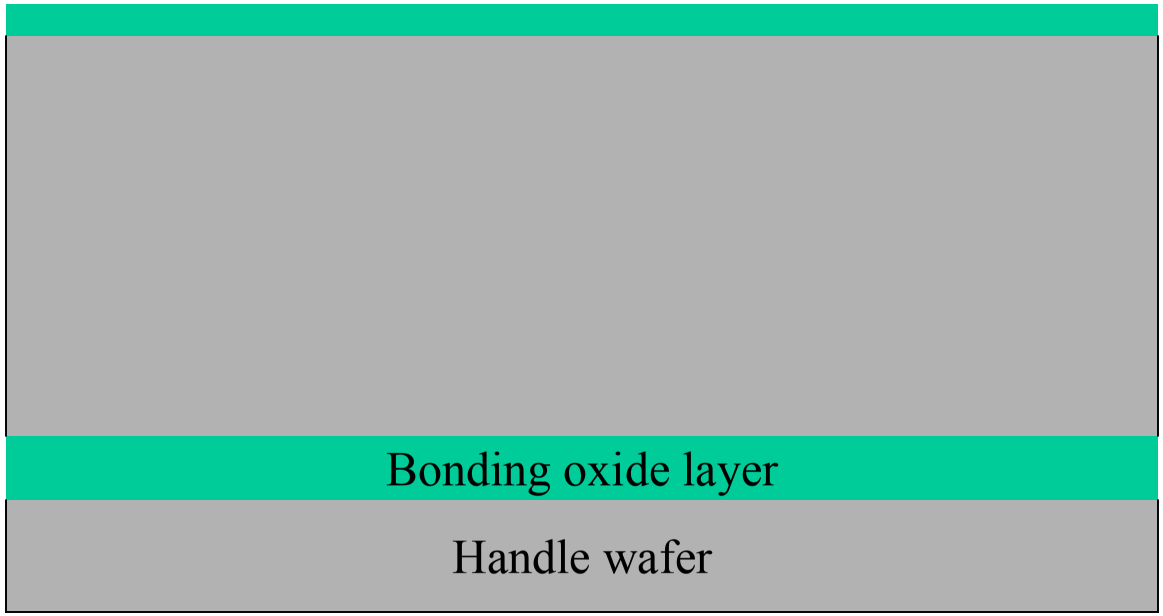
Standard fusion bond of two oxidized wafers followed by grind and polish to desired thickness



Silicon Oxide

Isolation Trench Etching and Back-filling

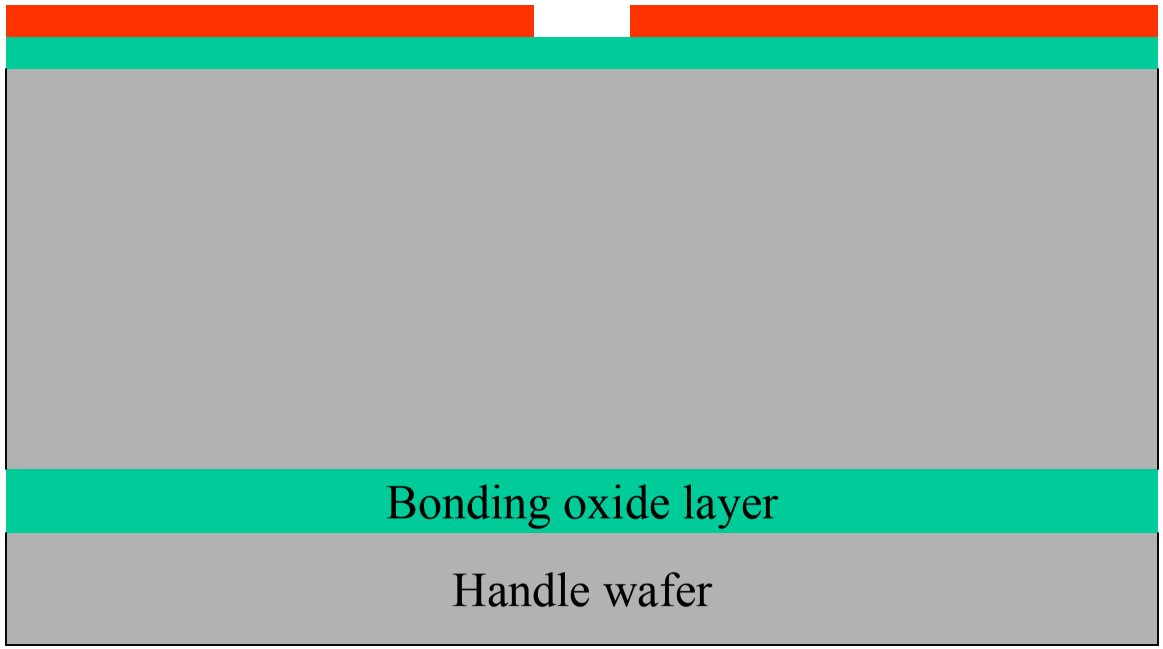
Protective oxide is grown on wafer surface



Silicon Oxide

Isolation Trench Etching and Back-filling

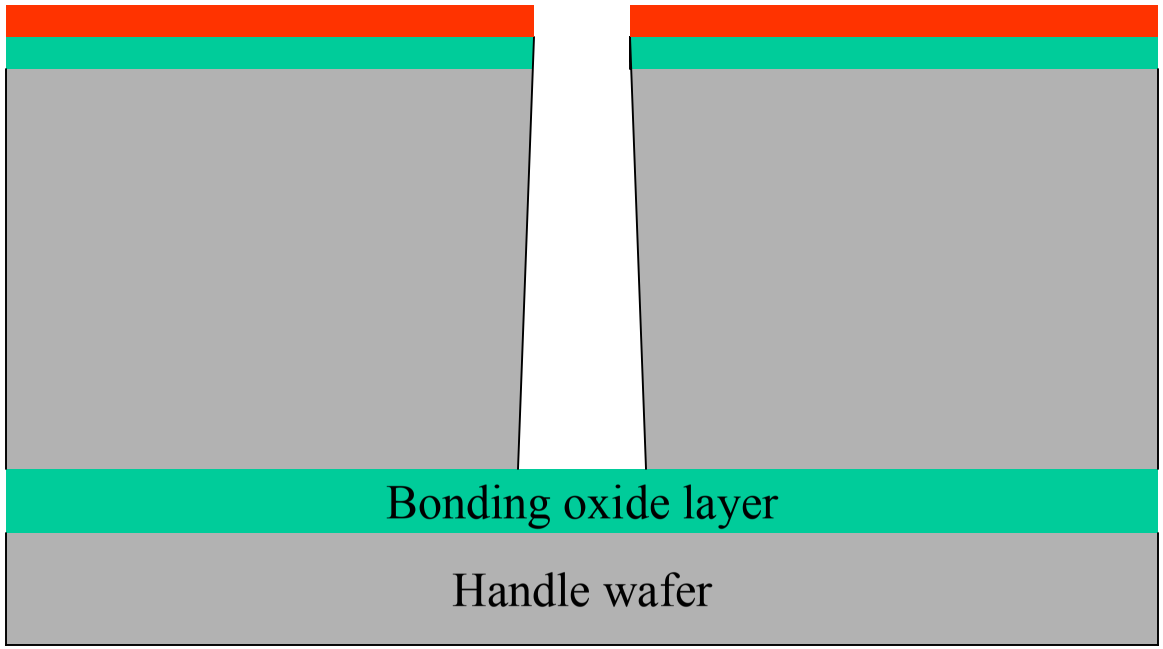
2 μm wide isolation trench pattern is applied



Silicon Oxide Photoresist

Isolation Trench Etching and Back-filling

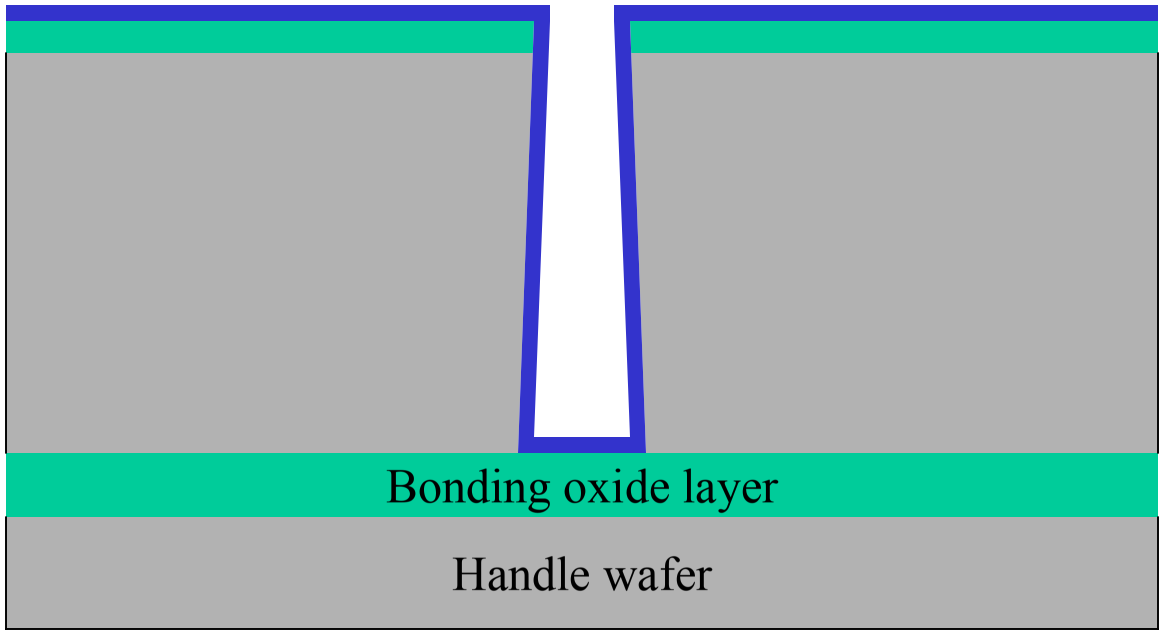
Trenches are etched to bonding oxide layer using DRIE



Silicon Oxide Photoresist

Isolation Trench Etching and Back-filling

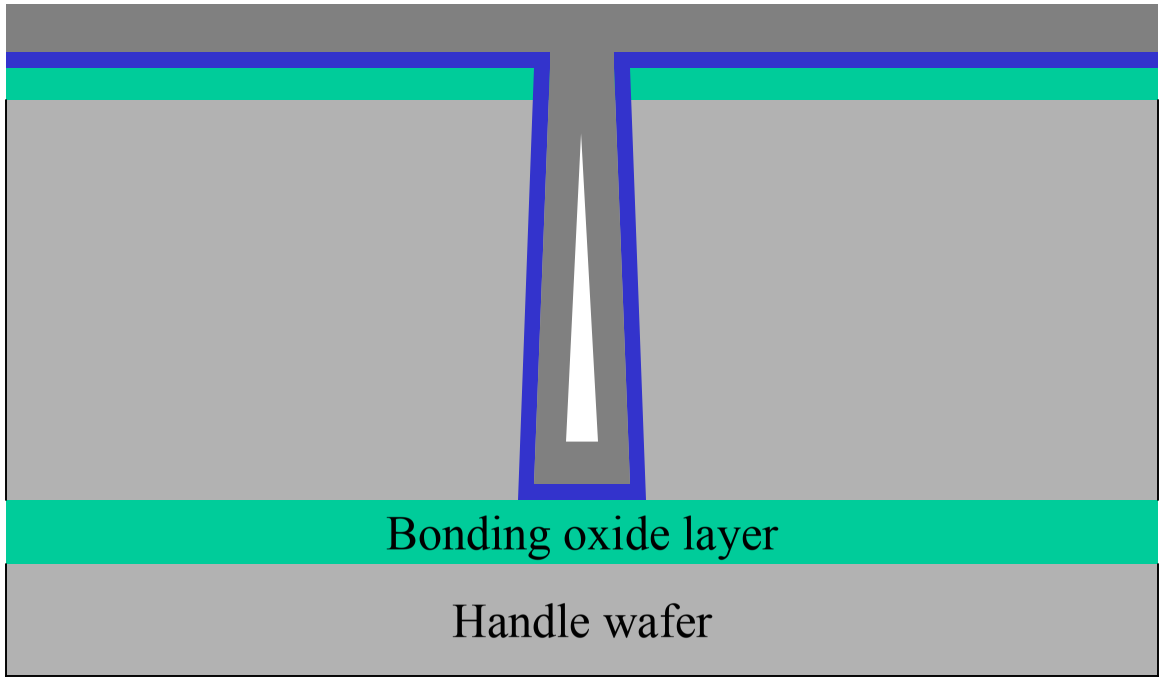
Trenches are lined with silicon nitride



Silicon Oxide Nitride

Isolation Trench Etching and Back-filling

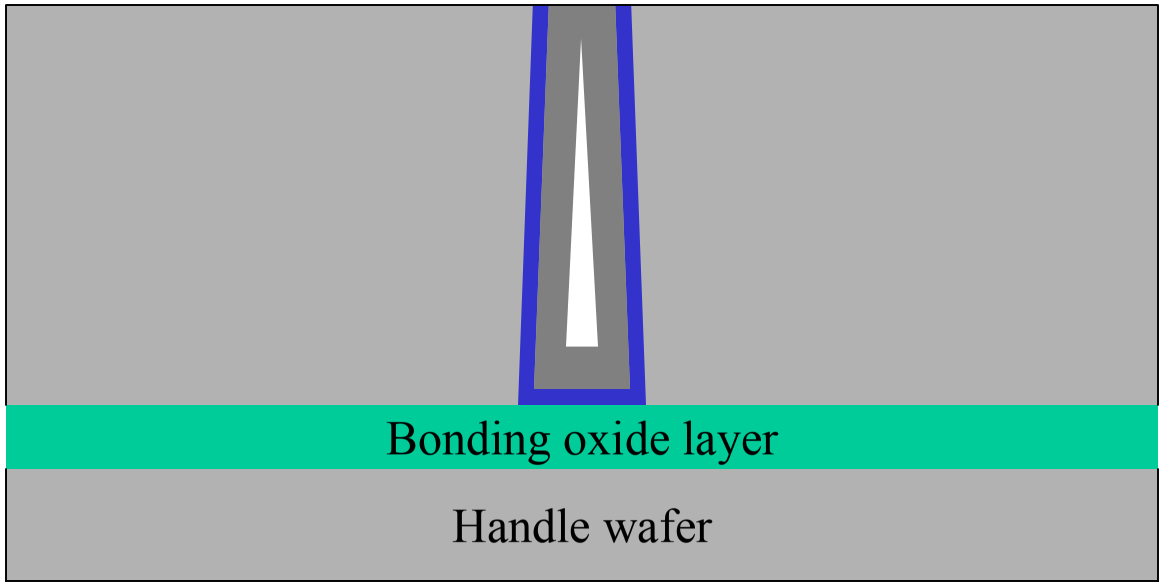
Trenches are filled with undoped polysilicon



Silicon Oxide Nitride Polysilicon

Isolation Trench Etching and Back-filling

Back-fill materials and protective oxide are removed

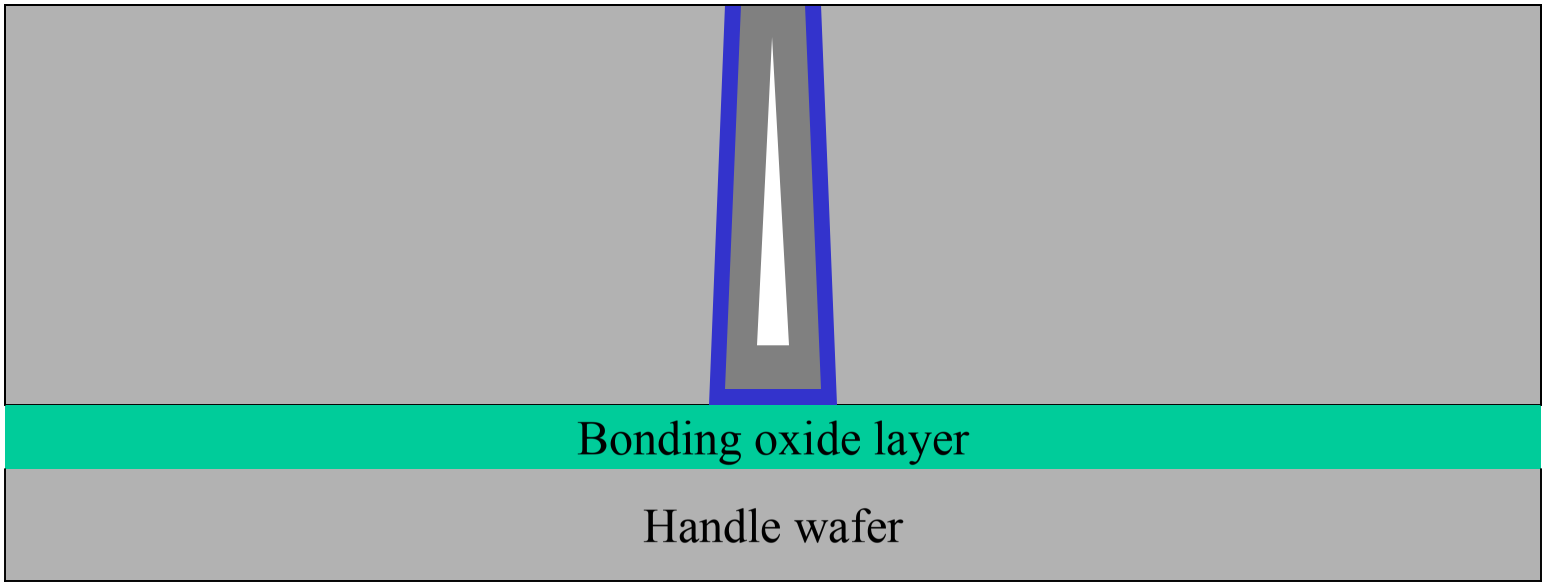


Silicon Oxide Nitride Polysilicon

Solar Cell and Circuit Fabrication

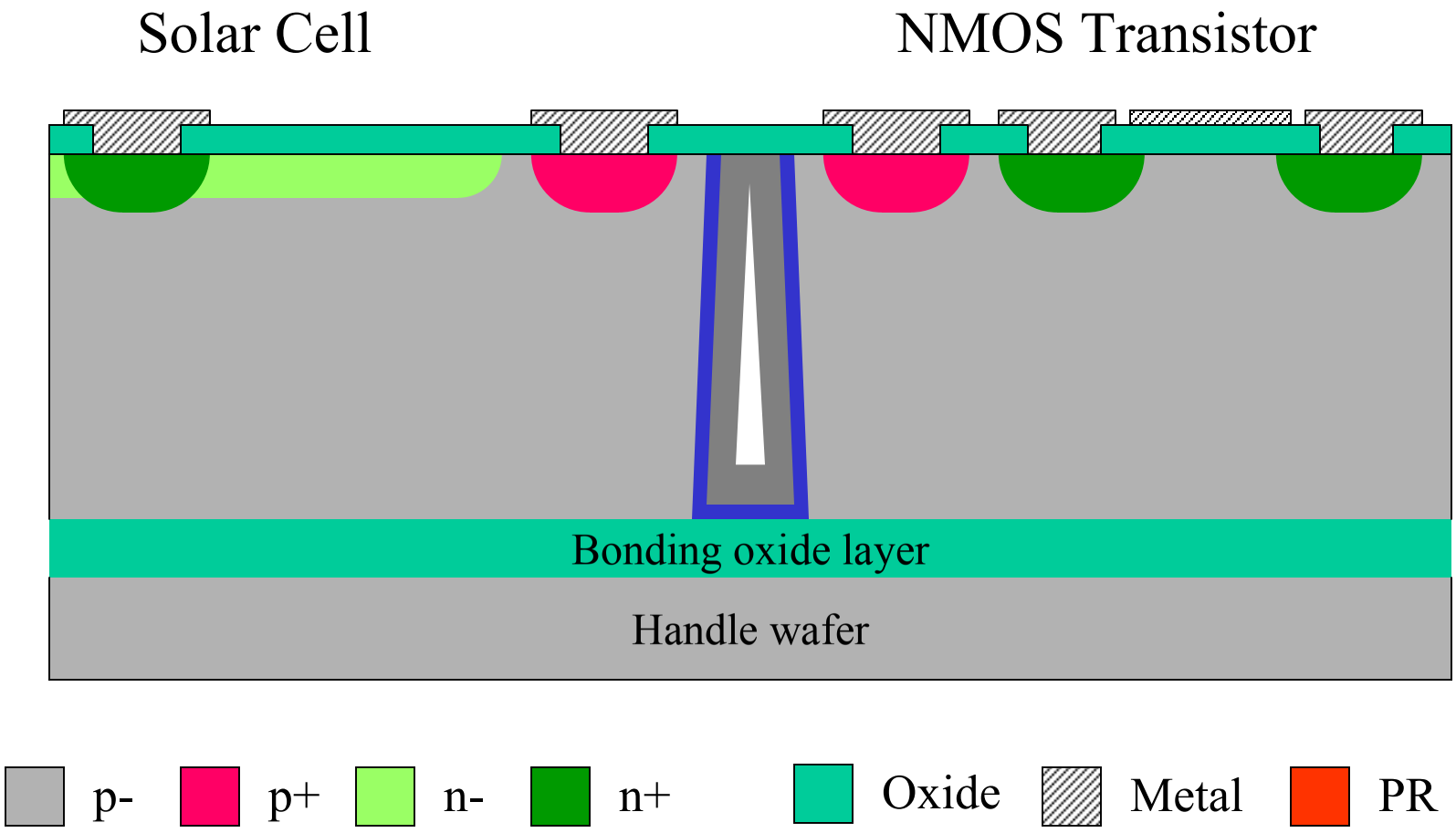
Solar Cell

NMOS Transistor



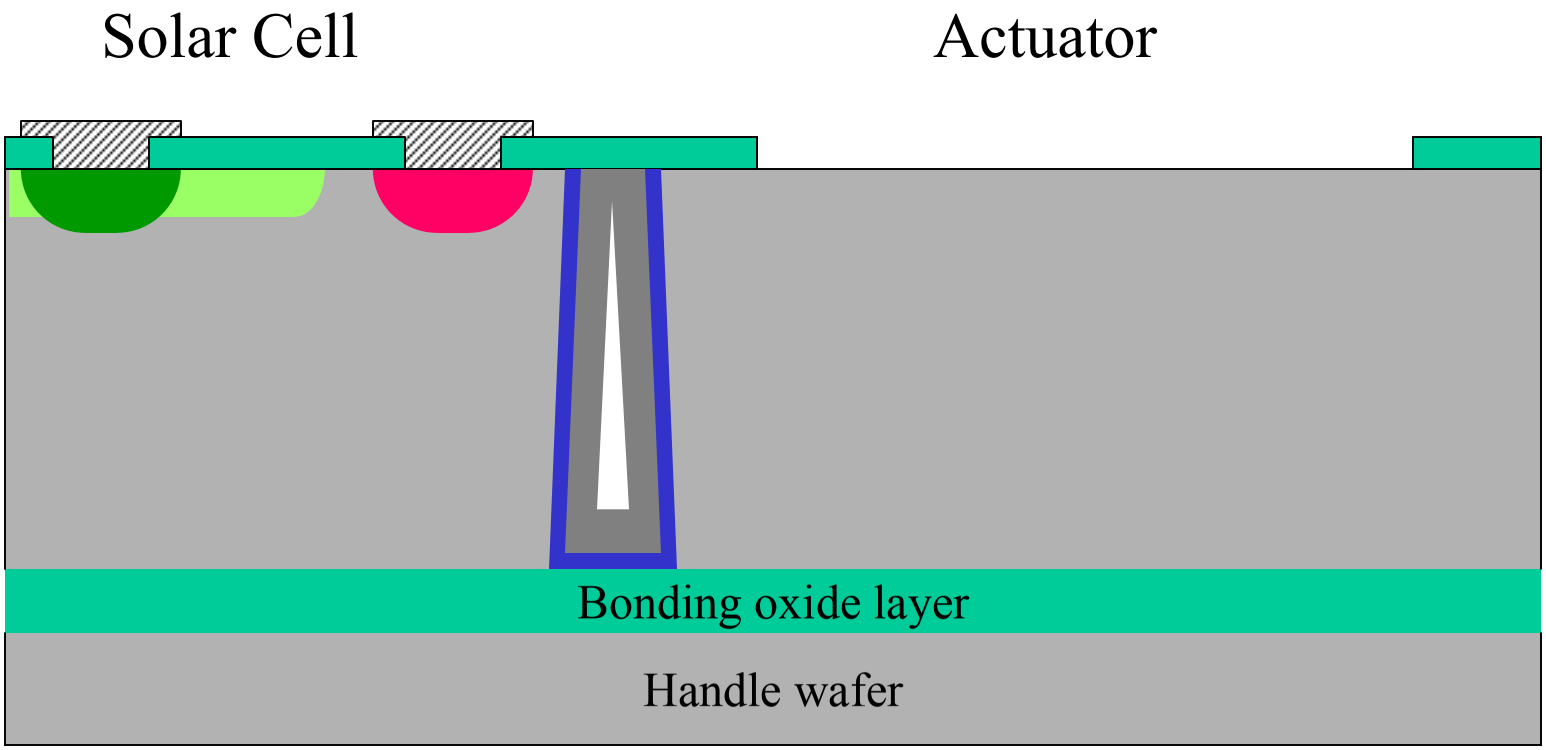
p- p+ n- n+ Oxide Metal PR

Solar Cell and Circuit Fabrication



Actuator Etch and Release

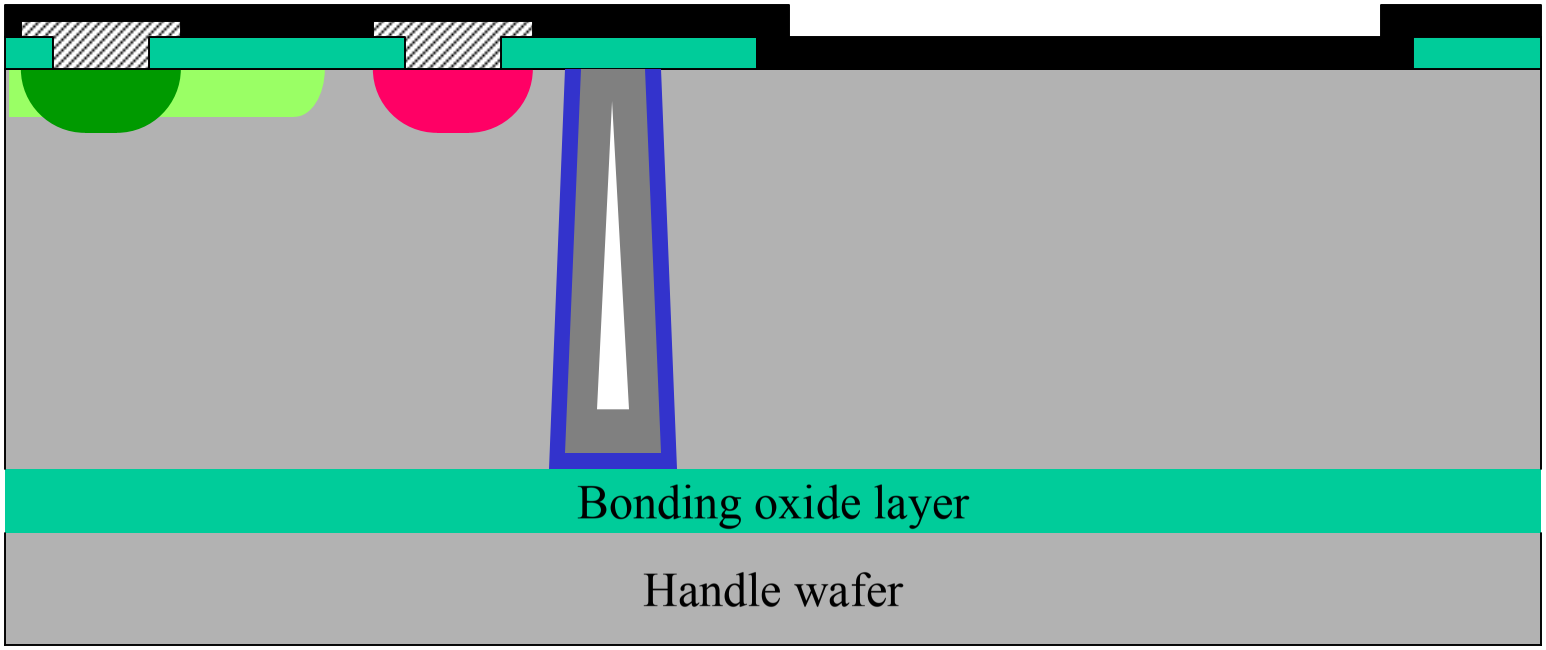
Remove oxide from actuator area



Photoresist Silicon Germanium

Actuator Etch and Release

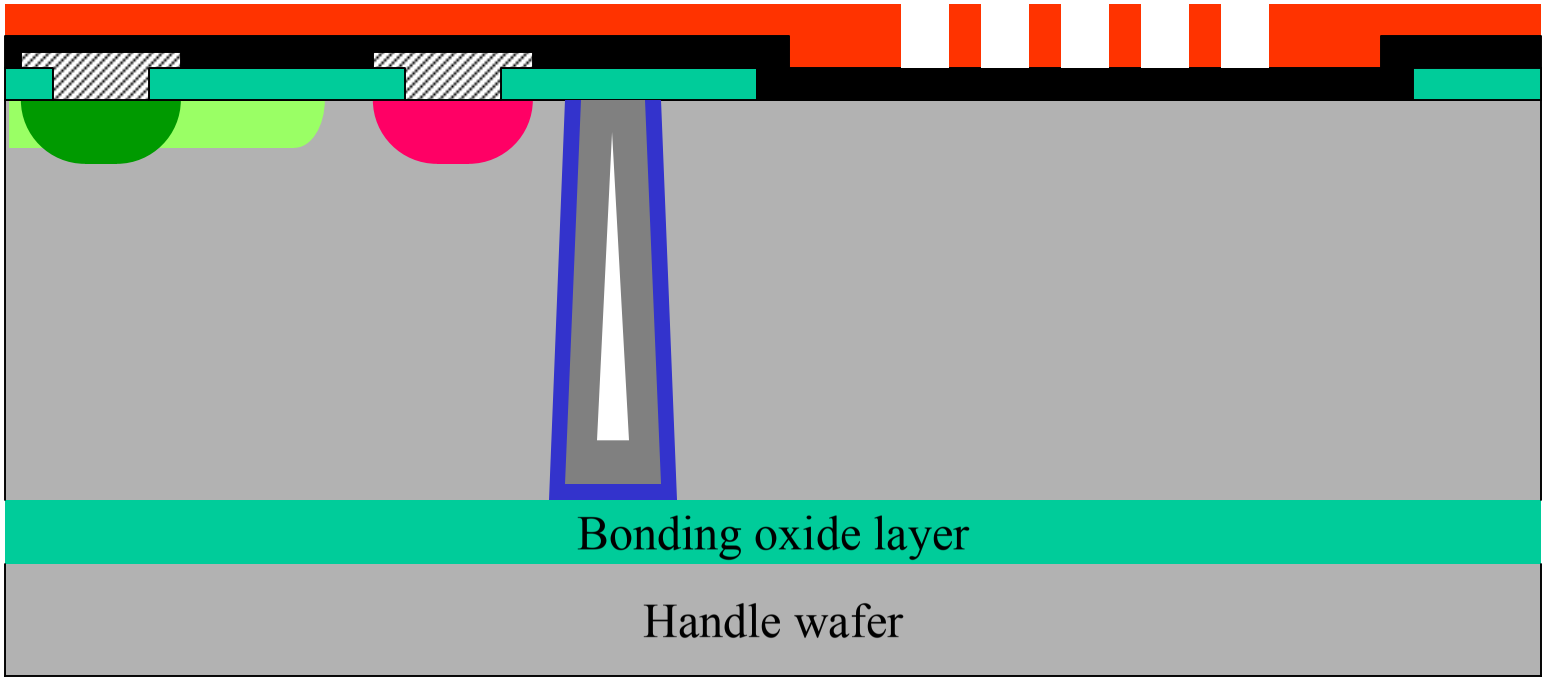
Deposit blanket layer of silicon germanium



Photoresist Silicon Germanium

Actuator Etch and Release

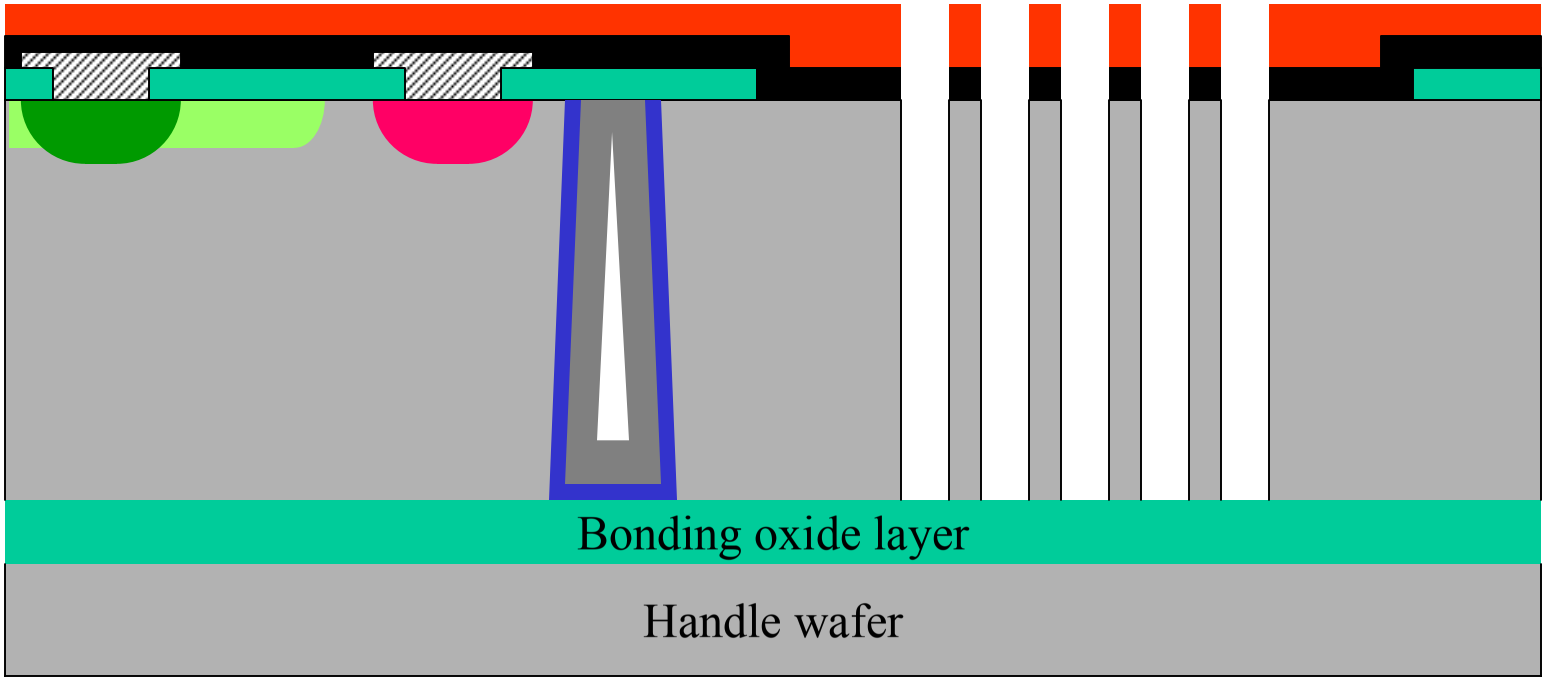
Apply pattern for actuators



Photoresist Silicon Germanium

Actuator Etch and Release

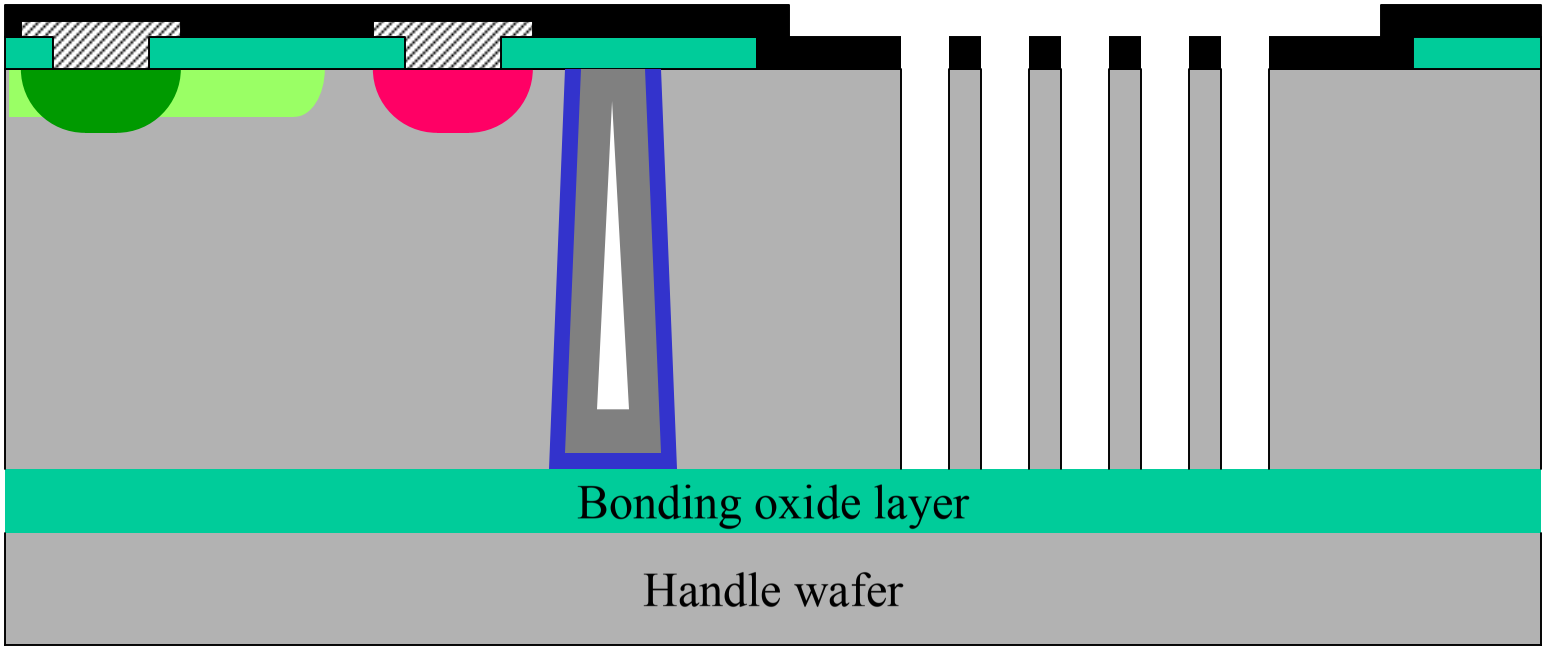
DRIE etch through to the bonding oxide layer



Photoresist Silicon Germanium

Actuator Etch and Release

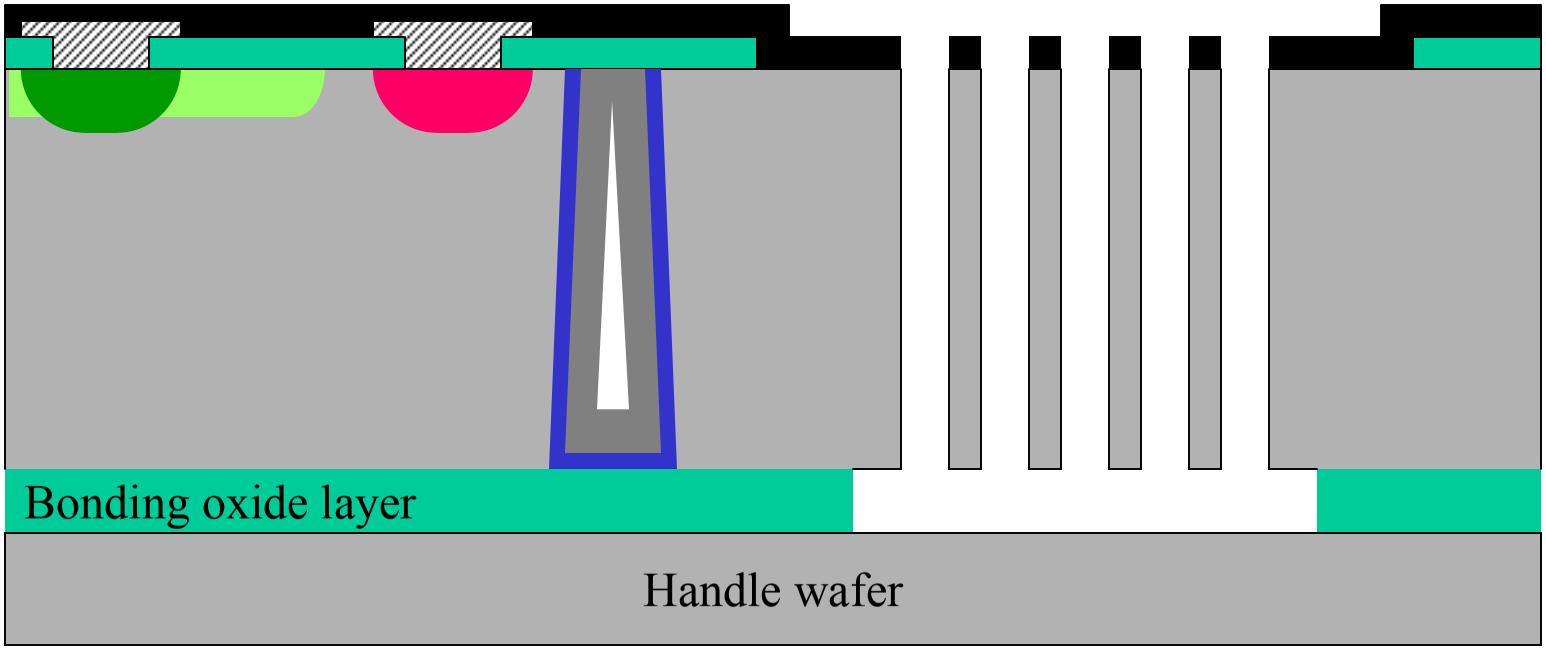
Remove photoresist



Photoresist Silicon Germanium

Actuator Etch and Release

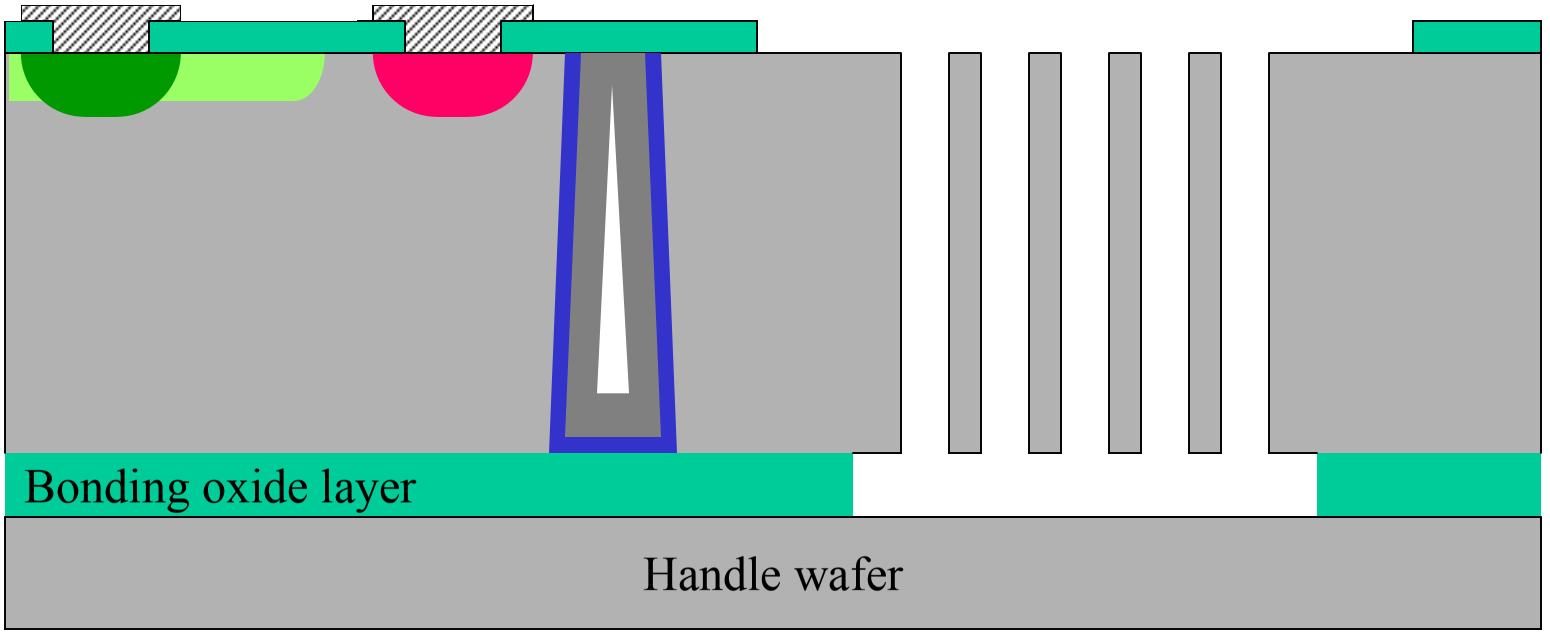
Perform timed etch of bonding oxide layer



Photoresist Silicon Germanium

Actuator Etch and Release

Remove silicon germanium in 90° C H_2O_2
Critical point dry



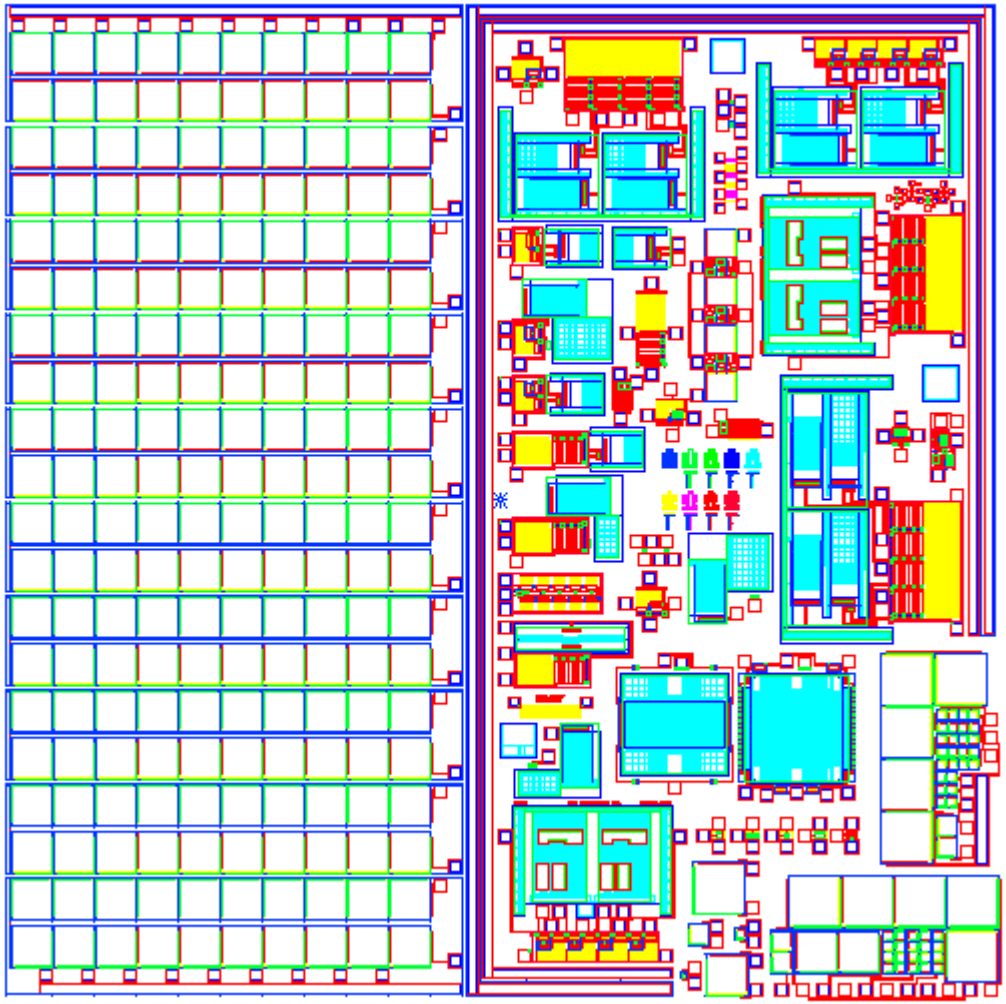
Photoresist Silicon Germanium

Problems with Silicon Germanium and Aluminum

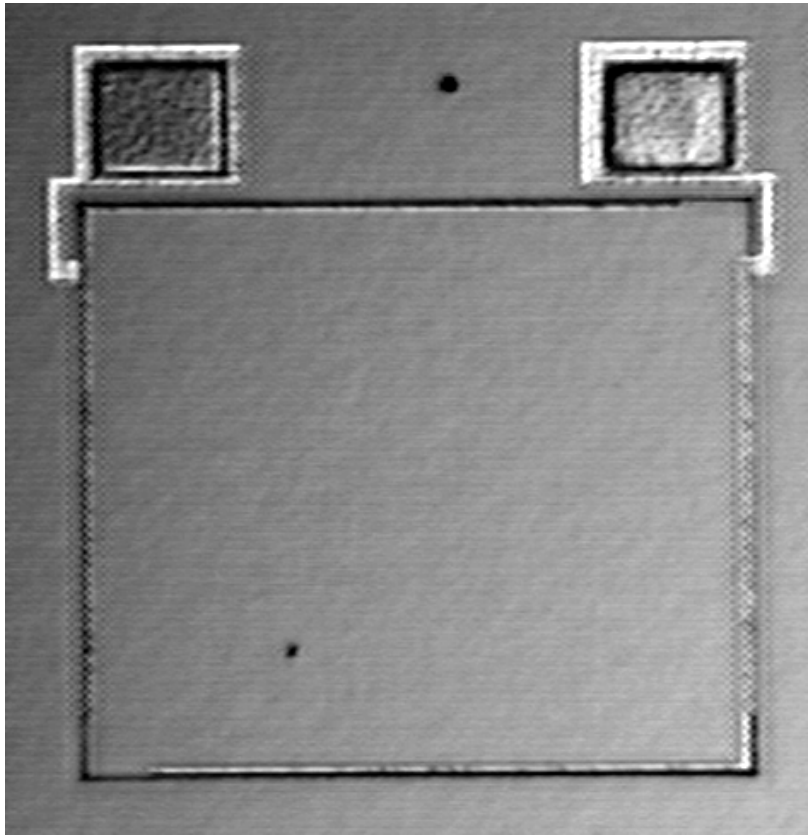
- SiGe will react with any exposed Al during deposition
- Voids form through SiGe layer, exposing Al underneath
- Interaction does not occur with Ti or TiN
- Buried Al is safe but exposed metal replaced with Ti/TiN

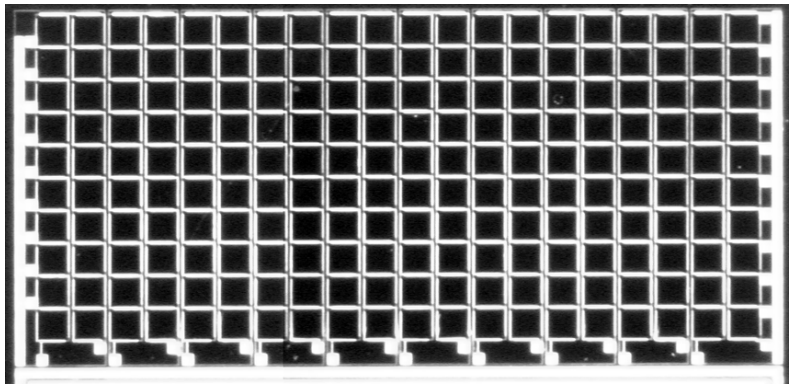
Design

- Configurable solar cell array with 200 cells
- Pre-wired buffer + actuator sets



Solar Cells and Arrays - Design





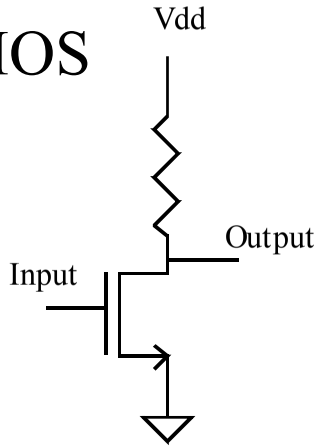
Solar Cell Arrays - Results

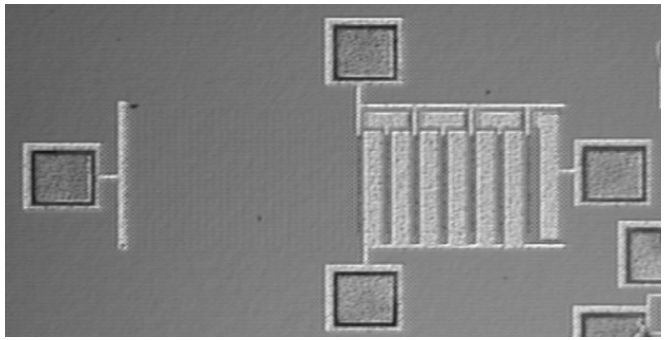
Number of Cells	Short Circuit Current	Open Circuit Voltage	Maximum Power	Efficiency
	uA	V	uW	
20	41.8	8.4	181	7.46%
20	41.7	8.6	190	7.83%
20	41.7	11.1	275	11.33%
20	41.6	11.3	283	11.66%
20	39	11.2	274	11.29%
20	41.6	11.2	281	11.58%
20	41.1	10.7	271	11.17%
20	40.4	9.1	199	8.20%
20	41.5	10.1	255	10.51%
20	41.7	11.3	282	11.62%
200	41.2	88.5	2010	8.28%

Individual cell size = 400μm x 400μm
Solar illumination = ~AM1.71
Incident power = ~758μW/mm^2

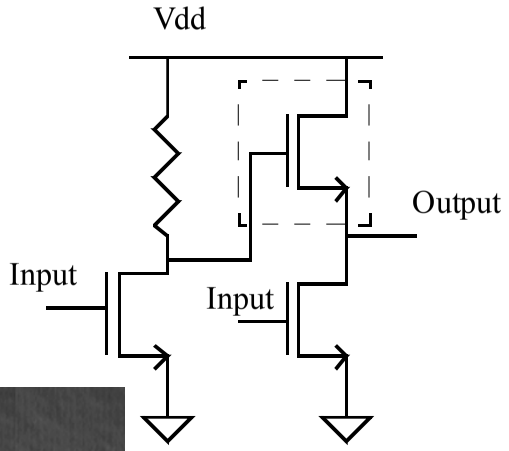
Buffers - Design

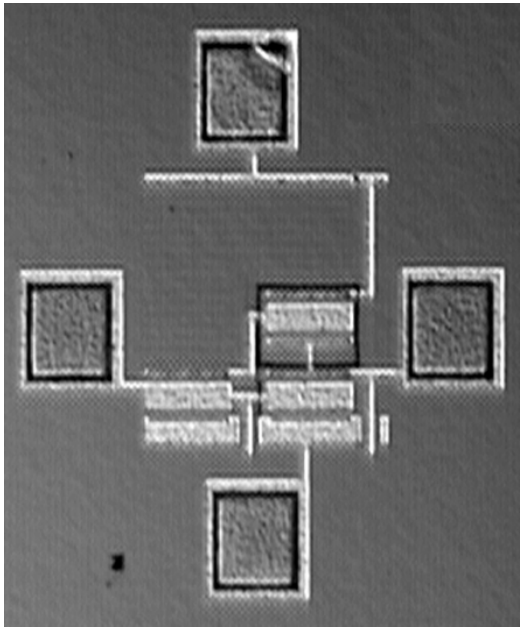
Simple NMOS Inverter





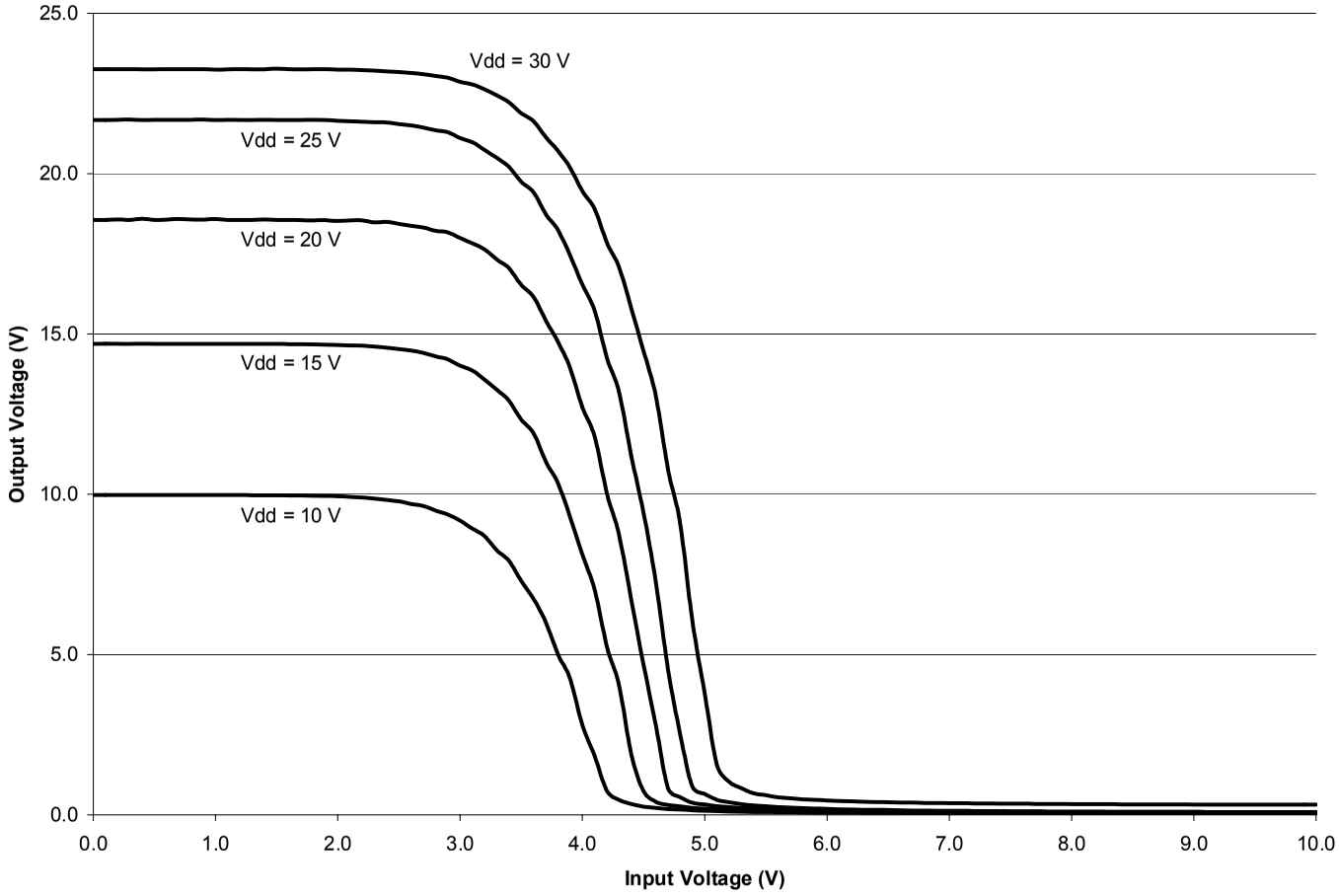
Two Stage Inverter





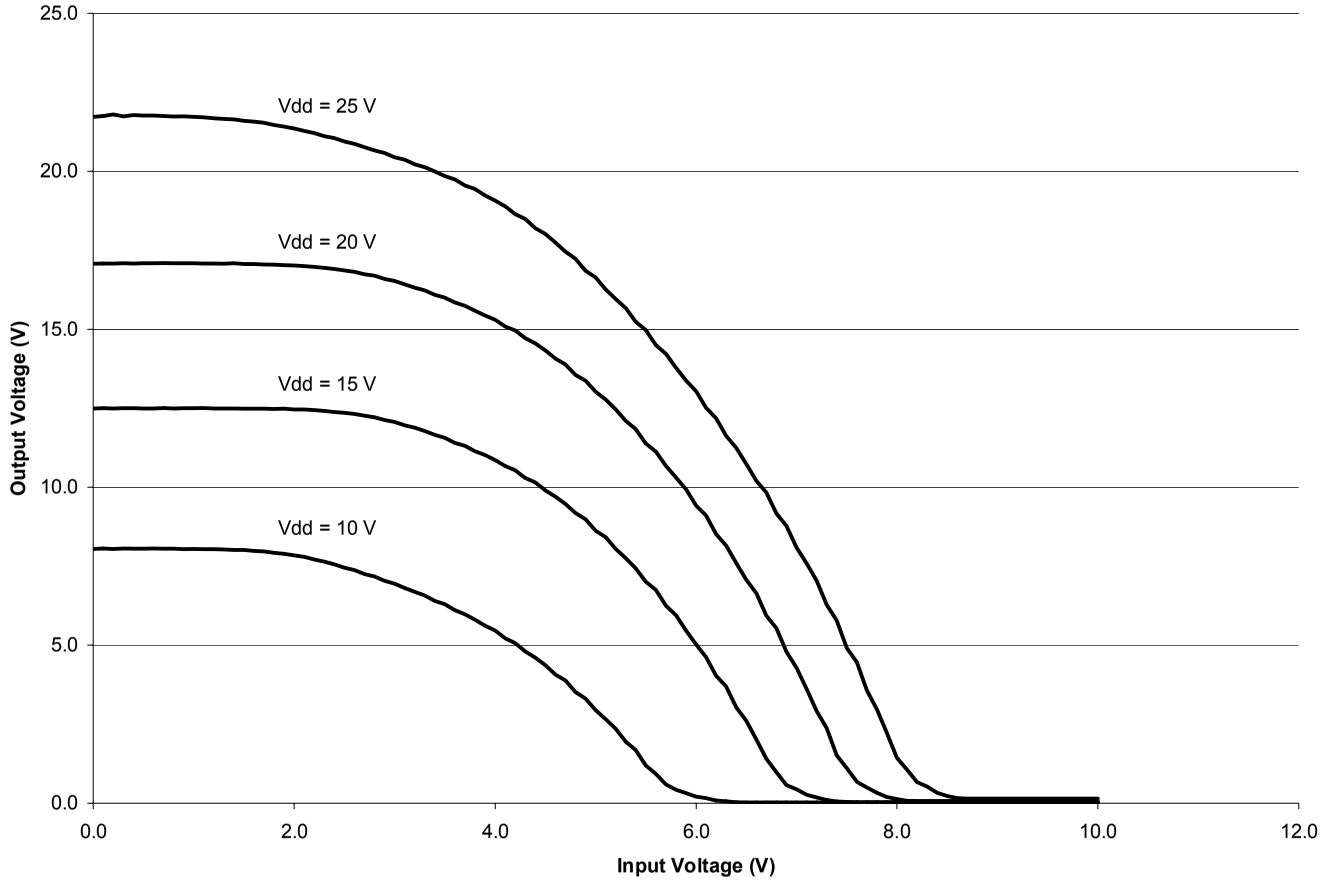
Buffers - Results

Simple NMOS Inverter



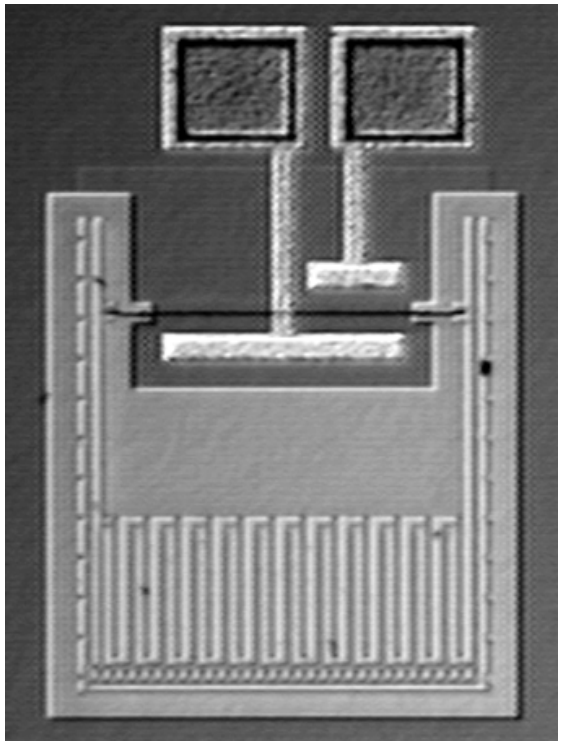
Buffers - Results

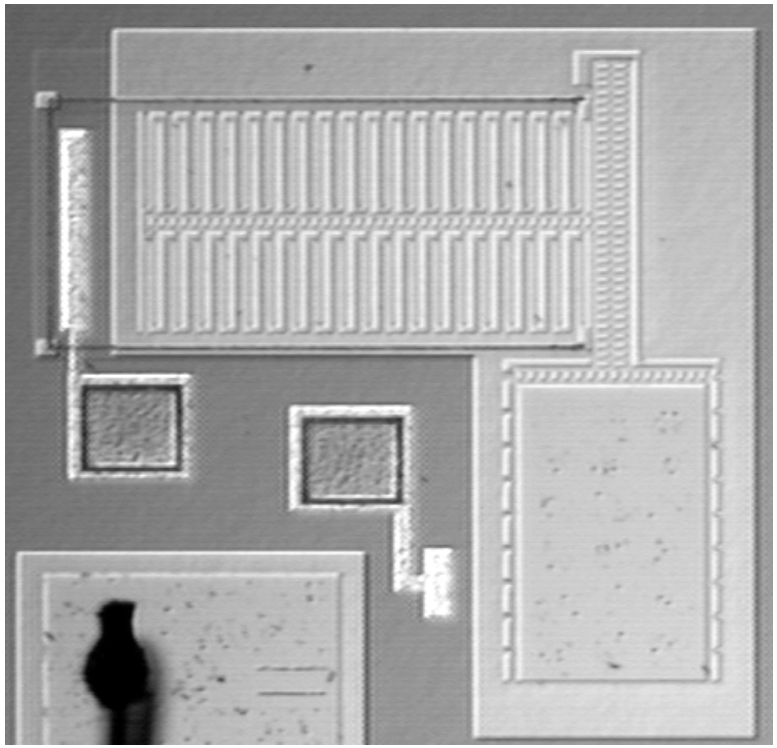
Two Stage Inverter



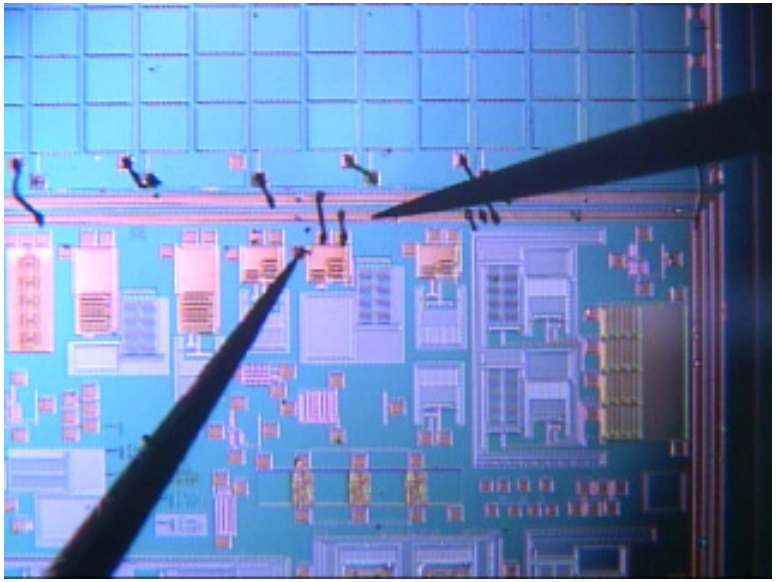
Electrostatic Actuators

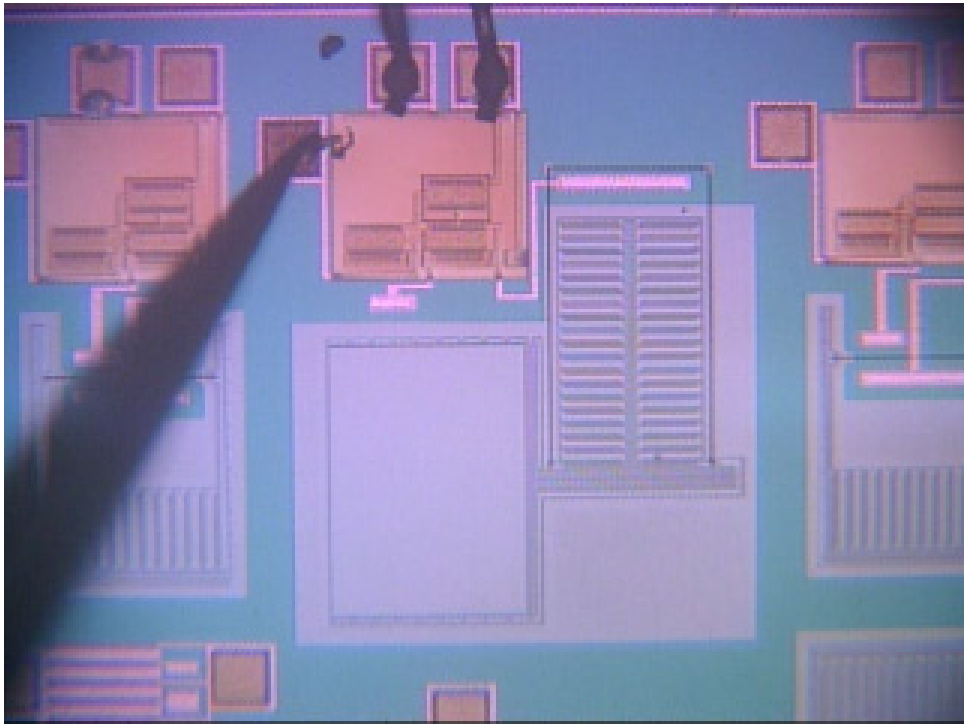
- Test structures – gap closing actuator arrays



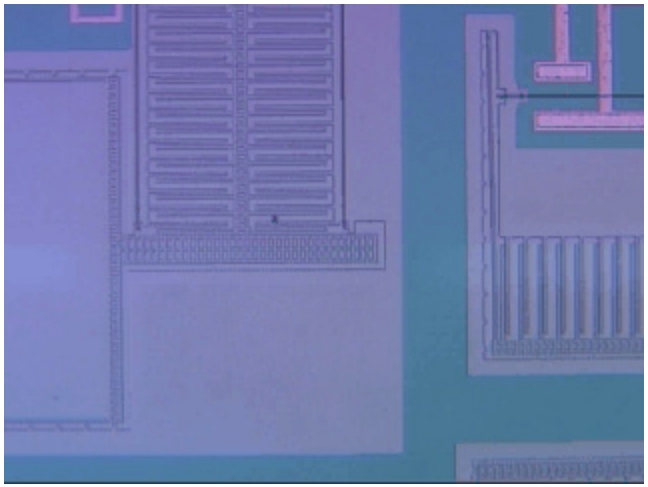


Integrated Device





Integrated Device



Process Limitations

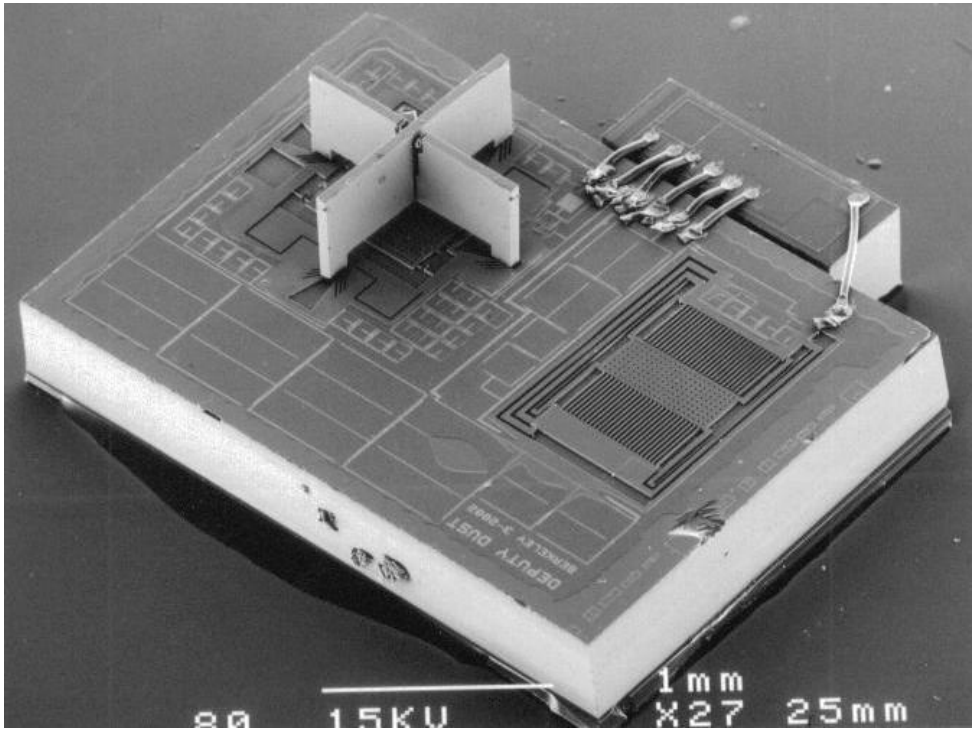
- NMOS only capabilities
- Transistor breakdown voltages ~27 V

Second generation – CMOS process

- Design focus
  - Improved circuit performance
    - Self-aligned, polysilicon gates
    - CMOS circuit capabilities
    - Higher breakdown voltage
    - Better control of threshold voltages
    - Isolation trenches etched and back-filled after solar cell and circuit fabrication
  - Meet specific project needs

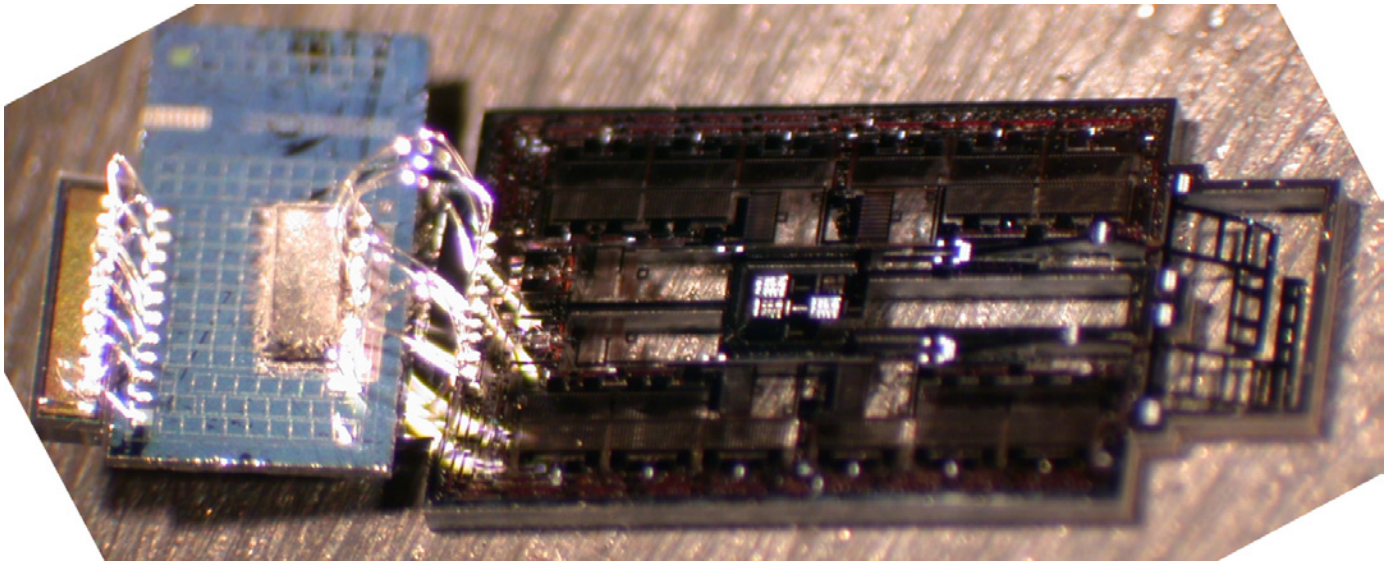
Second generation – CMOS process

- SmartDust
  - Integrated solar cell arrays and electrostatic actuators



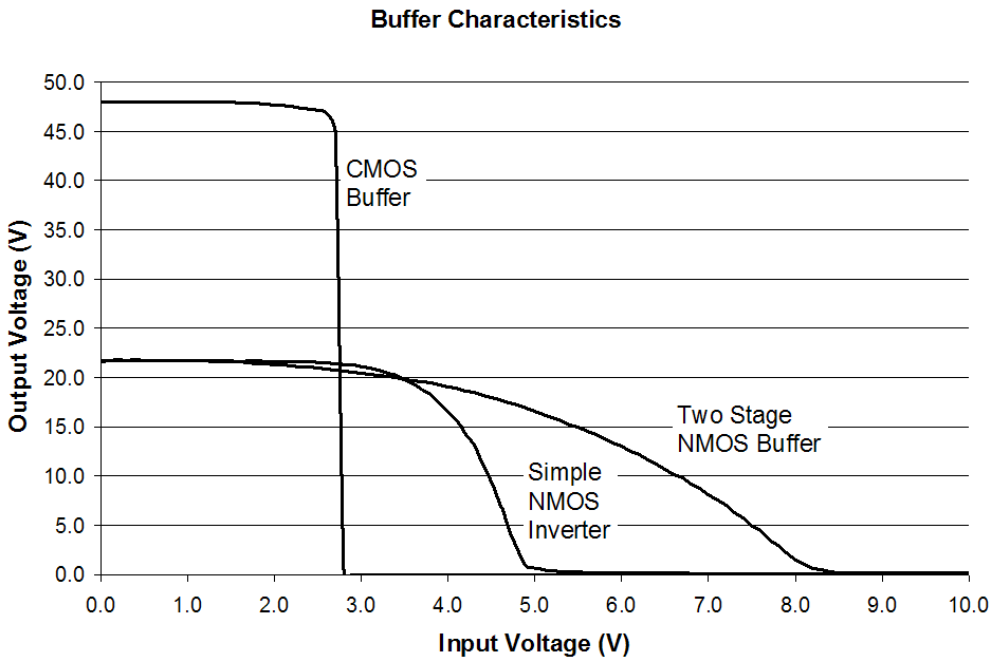
Second generation – CMOS process

- Microrobots
  - Integrated solar cell arrays and high-voltage buffers



Results

- CMOS capabilities allow for more sophisticated buffers
  - Voltage translator circuit using a variant of a cross coupled inverter



Conclusions

- Integrated process has been developed including
  - High voltage solar cell arrays
  - High aspect ratio electrostatic actuators
  - High voltage buffers
- Integrated device fabricated in the process has been demonstrated
- Second generation process has been developed solving the most significant process limitations

Acknowledgements

- SmartDust and Microrobot projects at UC Berkeley
- Prof. A.P. Pisano
- Prof. K.S.J. Pister
- Staff of the Berkeley Microfabrication Laboratory