An Ultralow-Energy ADC for Smart Dust

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***Abstract*—A low-energy successive approximation analog-to-digital converter (ADC) targeted for use in distributed sensor networks is presented. The individual nodes combine sensing, computation, communications, and power into a tiny volume. Energy is extremely limited, forcing the nodes to operate with very low duty cycles. This paper describes the design and implementation of an ADC to meet the unique requirements of sensor networks. The ADC reported here consumes 31 pJ/8-bit sample at 1-V supply and 100 kS/s, with a standby power consumption of 70 pW. This energy consumption is one of the lowest ever reported.**

***Index Terms*—Analog-to-digital converter (ADC), charge redistribution, CMOS, energy, low power, sensor networks, Smart Dust, successive approximation.**

I. Introduction

IN THE PAST decade, much of the research on analog-to-digital converters (ADCs) has focused on increasing sampling rate and resolution. While there are many applications that demand such advances, other emerging applications do not require high performance but do place very stringent requirements on energy consumption. This paper focuses on a portion of the ADC design space that has received comparatively little attention—moderate resolution and speed, but ultralow power.

Such ADCs are critical components in large-scale wireless sensor networks. The vanishing size and cost of the individual nodes in these sensor networks will allow them to interact with the environment in far less intrusive ways than previous networked sensor systems. Potential applications range from smart building environments, tracking wildlife populations, monitoring crops and livestock, and measuring and predicting weather patterns. The energy consumption of the nodes will determine both the lifetime of the individual nodes and the scope of possible applications.

The ADC is the interface between the sensed environment and the sensor network as a whole, so its performance and flexibility are critical. Low active and standby power is paramount, but there are other considerations as well. The remainder of this paper describes the design and implementation of an ADC to meet the unique requirements of distributed sensor networks. While targeted for sensor networks, the ADC presented here is also well suited for other energy-constrained systems, such as low-resolution CMOS imaging systems [1] or microrobotic systems [2].

The organization of this paper is as follows. Section II introduces the target application for the ADC and details the design specifications. Sections III and IV summarize the architecture and circuit design, and Section V presents measured results. The energy consumption of the ADC is considered at the system level in Section VI, and some concluding remarks are provided in Section VII.

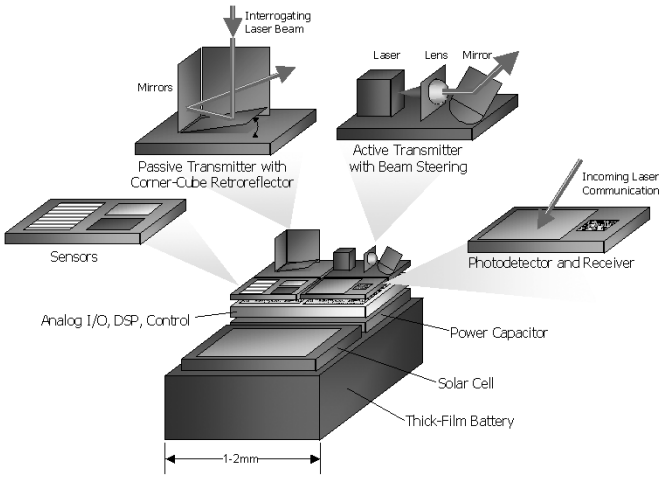

Fig. 1. Smart Dust concept. Tiny sensor nodes will combine sensing, computation, communications, and power.

II. Smart Dust System Overview

The core of the sensor network is a self-contained node capable of operating for a long period on very little energy. Leveraging CMOS device scaling and MEMS technologies for decreased cost and increased levels of integration, each sensor node combines sensing, computation, communications, and power into a volume on the order of 1 mm^3. A typical network may contain thousands of these "Smart Dust" [3] nodes (or "motes").

A conceptual diagram of such a mote and its subcomponents is shown in Fig. 1. The core control of the system is provided by a custom low-power microprocessor (μP). This μP interfaces with the ADC, coordinates uplink and downlink communications, and provides active power control for the system. The mote has an integrated power source, which could be a millimeter-scale battery, solar cells and storage capacitor, or even an energy-harvesting device to scavenge from the environment. Program data, digitized sensor readings, and application data are stored in a small (a few kilobytes) integrated SRAM. The mote is reprogrammable via the downlink communications link, allowing a single mote platform to be used for any variety of application.

The ADC presented here (first reported in [4]) was designed for use in the Smart Dust mote [5] shown in Fig. 2. This mote is controlled with a finite state machine (FSM) instead of a full microprocessor and, as such, it cannot be reprogrammed. The

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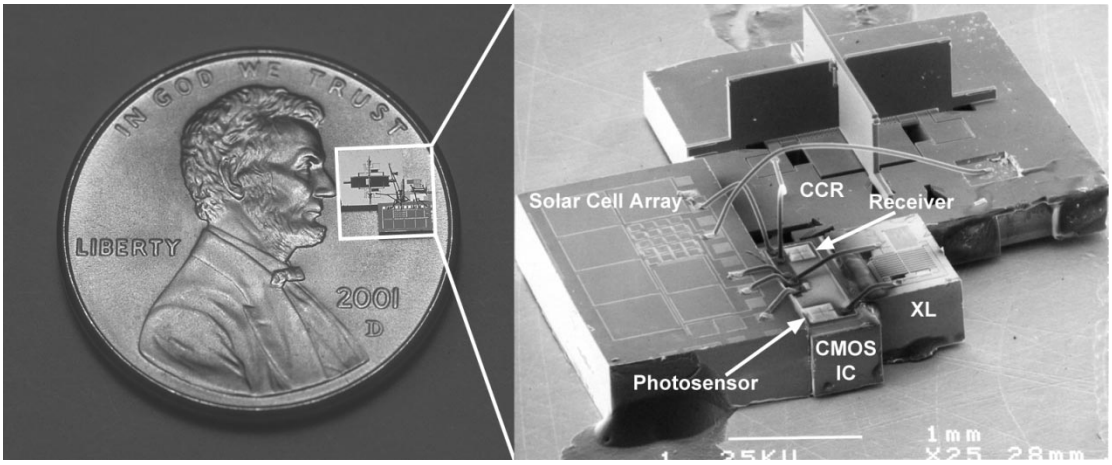

Fig. 2. Latest generation Smart Dust mote, consisting of a corner-cube retroreflector, MEMS accelerometer (not functioning), a CMOS die (with optical receiver, ADC, light sensor, and controller), and a MEMS solar array. Total circumscribed volume is 16 mm^3.

ADC resides on the CMOS chip along with a photosensor, the FSM, and an optical receiver for downlink communications. A second sensor in the form of a capacitive MEMS accelerometer can also be multiplexed by the FSM to the ADC input. Uplink communications for the mote are accomplished via a four-quadrant corner-cube retroreflector (CCR) [6]. Power is supplied to the system by a MEMS solar cell array. Trench isolation allows any number of solar cells to be connected in series, providing multiple variable supply voltages that are isolated from one another. The mote shown in Fig. 2 uses separate supplies for the FSM (1 V, two cells), ADC, photosensor and accelerometer (1 V), optical receiver (2.5 V, five cells), and CCR (10 V, 20 cells). Prototypes of this mote (without the accelerometer) have previously been demonstrated [5].

The ADC design specifications can be roughly grouped into two categories. There are certain *system-level* constraints based on the construction of the sensor node itself, and *application-level* constraints that arise from the potential uses of the sensor network. The most important system constraints for the ADC are:

- energy consumption less than 1 nJ/8-bit sample;
- low-power standby mode—low duty cycle typical (e.g., node mostly sleeps);
- supply voltage of ∼1 V—derived from two series solar cells.

By studying potential applications for large sensor networks [7], the critical application constraints were determined to be:

- resolution of 8 bits or greater;
- maximum sampling rate of at least 10 kHz;
- rail-to-rail conversion range—accommodate a variety of sensors;
- algorithmic flexibility—reduced resolution samples, data thresholding (e.g., $V_{\text{in}} > X?$), data binning (e.g., $X < V_{\text{in}} < Y?$).

III. Successive Approximation Architecture

A survey of ADC architectures reveals that both algorithmic [8] and successive approximation [9] ADCs are well suited to meet the required design specifications. These architectures can be realized using very low power due to the minimal amount of analog hardware required. However, the successive approximation architecture offers greater flexibility to perform general operations on the input. Shown in Fig. 3, the successive approximation architecture uses only one comparator, along with simple digital logic and a switching network to implement the search algorithm. Assuming a binary search, reduced resolution samples can be obtained by simply ending the search algorithm early. Thus, an N-bit successive approximation ADC can produce outputs ranging from 1 to N bits of resolution with no circuit modifications, using less energy for less resolution.

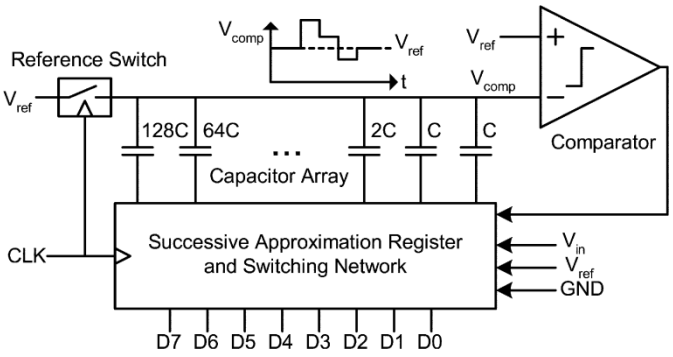

Fig. 3. Successive approximation ADC architecture (shown for an 8-bit converter).

While algorithmic ADCs also provide this feature, the successive approximation architecture offers an additional layer of flexibility through direct modification of the successive approximation register (SAR) itself. In the Smart Dust system, the SAR is implemented by a custom microprocessor, and can be reconfigured easily. For example, the microprocessor (which now acts as the SAR) could change the search to simply threshold the input, bin the input into an arbitrary number of bins, or start the search at the value of the last output code. By implementing these SAR modes with dedicated hardware in the microprocessor, the energy overhead is minimized. This arbitrary control is programmable by the user at the application level, making the successive approximation ADC extremely flexible.

The operation of the ADC is as follows. First, the input voltage is sampled onto the capacitor array. Next, the SAR generates an approximation, which is converted to a voltage at $V_{\rm comp}$ by the capacitor array and compared to $V_{\rm ref}$ by the comparator. The SAR uses the comparator result to compute its next approximation for the digital code. A standard binary search algorithm leads to an N-bit output available after the Nth comparison.

IV. ADC Circuit Design

As seen in Fig. 3, the successive approximation architecture requires a reference voltage to charge the capacitors during the conversion cycle. Often this reference voltage is derived from a bandgap circuit, and therefore requires power. To avoid on-chip reference generation, the reference voltage was chosen to be the supply voltage, which is already present on-chip. In addition to saving power, this choice has a number of additional benefits. First, it allows the use of simple pMOS devices for switching the reference onto the capacitors. Second, the comparator now operates with a threshold voltage $V_{\rm ref}$ equal to the supply voltage $V_{\rm dd}$. This allows the comparator to be realized with a conventional nMOS differential pair input, despite the relatively low 1-V supply. Finally, this sets the input conversion range of the converter to be rail-to-rail.

One potential difficulty with choosing $V_{\rm ref} = V_{\rm dd}$ is the power-supply rejection (PSR) of the converter. As $V_{\rm dd}$ (and, hence, $V_{\rm ref}$) varies, the output codes adjust accordingly. The problem is aggravated because the supply voltage is derived from solar cells that vary substantially with the ambient light. Fortunately, many sensors (e.g., bridge sensors) are ratiometric with $V_{\rm dd}$, which means that the overall sensor-ADC subsystem maintains reasonable PSR despite large absolute variations in supply. For nonratiometric sensors, however, poor supply rejection is inherent and must be tolerated at the application level.

A. Capacitor Array

The accuracy of the converter is dependent upon the matching and noise in the capacitor array. Random process variations in the capacitors were dominant over thermal noise in this ADC. Poly–poly capacitors were used with the top plates acting as the common plate. This minimizes parasitic capacitance at the comparator input (see Fig. 3), which attenuates the signal voltage. Considering random variations along with an additional safety factor, a unit capacitance of 12 fF was chosen to achieve 8-bit resolution. The total resulting array capacitance is then approximately 3 pF excluding bottom-plate parasitics.

The layout for the array utilized a common-centroid structure and dummy capacitors on the edges of the array. Further protection against systematic matching errors was provided by a grounded metal shield over the entire array with one hole per unit capacitor to access each bottom plate. The binary weighted capacitors were built by connecting unit capacitors with routing above the shield as shown in Fig. 4. While adding extra parasitic capacitance from both the bottom plates and the top common plate to ground, the shielding made the weighted capacitors insensitive to routing parasitics. The only effect of the extra parasitics is to slightly increase the total energy consumption because they must be charged and discharged along with the desired array capacitors.

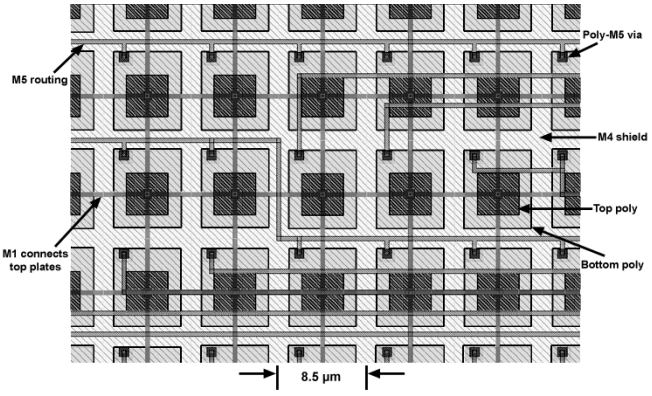

Fig. 4. Layout detail showing the parasitic shielding used in the capacitor array.

B. SAR and Switch Network

Control of the ADC is provided by the SAR and switch network. In Smart Dust, the microprocessor (or FSM in the prototype of Fig. 2) will control the ADC directly. For testing of the ADC standalone, however, a binary search SAR was implemented based on designs presented in [10]. The schematic for the SAR is shown in Fig. 5. The total signal transitions are kept low in this SAR and, hence, the energy consumption is minimized.

The switch network was built with simple nMOS devices for the ground reference, pMOS for the supply reference, and CMOS switches for the input signal. No gate boosting was used despite the low supply voltage because the speed and input bandwidth requirements were modest. Charge injection is not a major problem in the ADC because most capacitive nodes are actively driven during all phases of the conversion cycle. The only charge injection event during the conversion cycle is the opening of the reference switch at the end of the input sampling period. The resulting error voltage is very small as the charge is injected onto the entire array. Moreover, the error is systematic because the reference switch always has the same terminal voltages, resulting in an overall offset to the ADC. This offset varies with the clock slope [11], but is always less than 0.1 LSB.

C. Reference Switch

Choosing $V_{\rm ref} = V_{\rm dd}$ presents a problem for the initialization switch on the $V_{\rm comp}$ node (labeled Reference Switch in Fig. 3). During the first stage of the conversion cycle, this switch initializes $V_{\rm comp}$ to $V_{\rm ref}$ ($V_{\rm dd}$). In the comparison cycles that follow, the $V_{\rm comp}$ node may swing above $V_{\rm ref}$ as depicted in Fig. 3. For a binary search, $V_{\rm comp}$ reaches a worst-case maximum voltage of $1.5{\rm V}_{\rm ref}$ for $V_{\rm in} = 0$ V. The reference switch must then remain strongly off even when one side of the switch is at $1.5{\rm V}_{\rm ref}$. A simple pMOS switch cannot be used if its threshold voltage $V_{\rm tp}$ is near or less than $0.5{\rm V}_{\rm ref}$, a condition that is true in this design and indeed nearly all CMOS circuits.

To combat this problem, a switch employing a single-cycle charge pump was implemented. A schematic of the improved

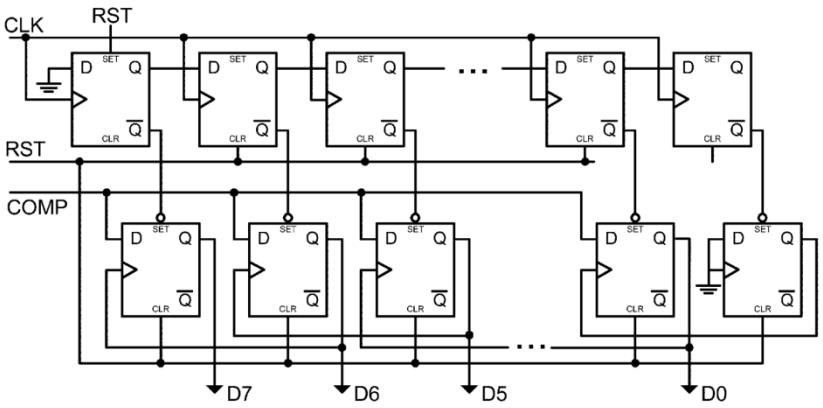

Fig. 5. SAR schematic. The top flip-flops form a shift register that controls the custom bottom register.

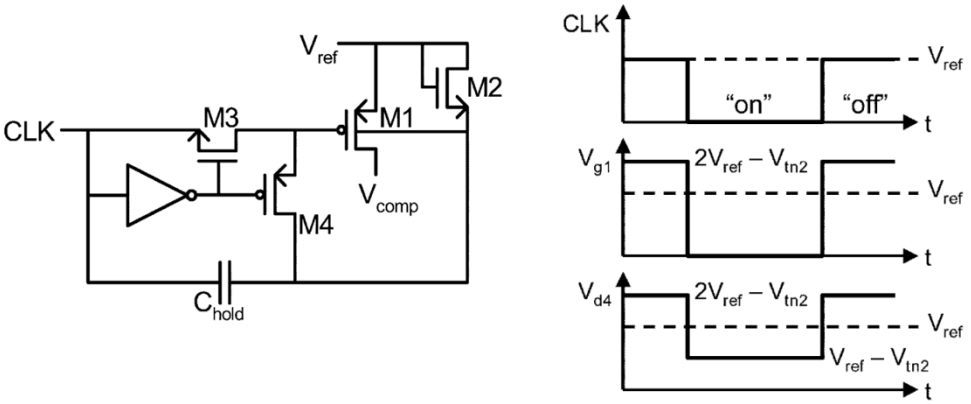

Fig. 6. Charge pump switch circuit schematic and associated signal waveforms.

switch and associated signal waveforms are shown in Fig. 6. By boosting the gate (and body) of the switch to approximately $1.5V_{\rm ref}$ during the off state, the circuit guarantees that the switch will remain strongly off when the drain voltage equals $1.5V_{\rm ref}$. When CLK is low, the switch is on and $V_{\rm comp}$ is forced to $V_{\rm ref}$ through M1. Device M4 is off, and M2 charges the body of M1 and drain of M4 to $V_{\rm ref} - V_{\rm tn2}$. When CLK goes high, the switch transitions to the off state. Device M3 is off, M4 is on, and the gate and body of the pMOS switch M1 are overdriven to $2V_{\rm ref} - V_{\rm tn2}$ by the charge previously pumped into $C_{\rm hold}$.

It should be noted that this circuit does not eliminate charge leakage for arbitrary search algorithms. The maximum voltage at $V_{\rm comp}$ is $2V_{\rm ref}$ for an arbitrary search, and the worst-case off state M1 source-to-gate voltage is $V_{\rm tn2}$. This will be approximately equal to $V_{\rm tp1}$, and device M1 will leak charge off the array. Fortunately, this worst-case scenario is unlikely to occur with any regularity because arbitrary searches are only beneficial when information about the input is known *a priori*. Leakage occurs when the input is low but the initial SAR approximation is high. However, in this case, if the input was assumed low, then the initial SAR approximation would also be low and there is no leakage problem.

D. Comparator

The comparator circuit (shown in Fig. 7) is based on a circuit reported by Peluso *et al.* [12]. During the reset phase (RST low), nodes V_{o+} and V_{o-} are forced to $V_{\rm dd}$ by M5 and M6. When

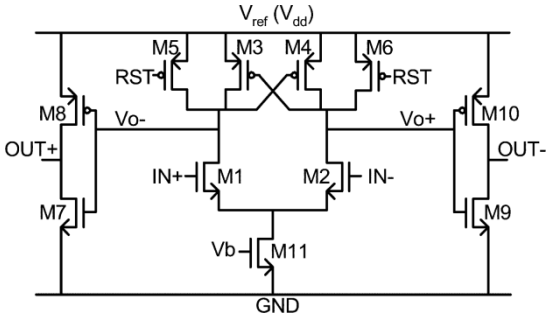

Fig. 7. Comparator circuit schematic.

RST goes high, a comparison operation is initiated and V_{o+} and V_{o-} slew toward ground at unequal rates due to the differential input voltage. When these nodes are low enough, the pMOS positive feedback load devices M3 and M4 activate and latch the comparator. The output inverters restore the comparator outputs to logic levels.

The bias current in M11 is the critical design variable for the comparator. Noise, speed, and power consumption of the comparator are determined by this current. The tradeoff is between choosing a small bias current for low power consumption and a larger value to minimize noise and maximize the comparison speed. The designed value of 1 μA for the tail current results in approximately 0.05 LSB of input referred noise and a comparison time of about 100 ns. For this current, comparator noise

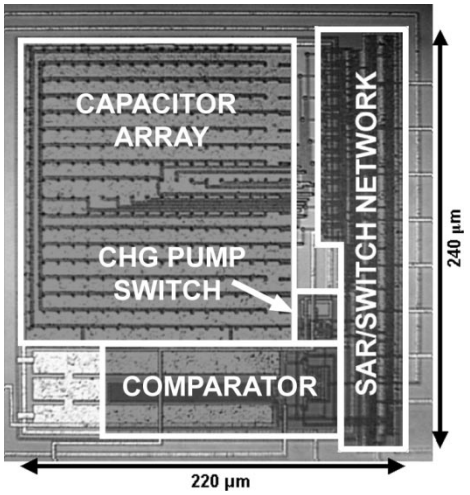

Fig. 8. Annotated ADC micrograph. Note that only the active circuit area is shown.

does not limit the ADC resolution, and speed is more than sufficient for a 10-kHz sampling rate.

Comparator offset voltage adds directly to the total ADC offset. The offset is dominated by V_t mismatch in M1 and M2, which is a few LSB. Offset cancellation techniques were avoided to maintain low power dissipation, particularly because a single sample offset calibration can be performed by the microprocessor if desired.

One consequence of designing the comparator for constant bias current is that the ADC consumes static power during the conversion cycle. As such, the conversion should be completed in as little time as possible to minimize the total energy consumed during the conversion. Note that this conversion time is not necessarily related to the overall sampling rate because the ADC powers down after every conversion. Thus, there is no practical minimum sampling rate (consistent with the system duty-cycle constraints), but a short conversion time is desired for minimum energy consumption. In this ADC, the minimum conversion time is dominated by the input sample-and-hold settling and is approximately 10 μs, allowing for a maximum continuous sampling rate of 100 kHz.

V. ADC Measurement Results

The ADC was fabricated in a 0.25-μm two-poly five-metal CMOS process. An annotated die micrograph of the standalone ADC chip (active area only) is shown in Fig. 8. The core circuitry as shown measures 0.053 mm^2, which is dominated by the capacitor array. To illustrate the relative size of the ADC in relation to the other components in Smart Dust, Fig. 9 shows an annotated layout of the CMOS die for the mote in Fig. 2. The ADC occupies a small portion of the total CMOS die area and is hardly significant compared to the size of the MEMS components in the system.

Fig. 10 shows typical plots for the low-frequency differential nonlinearity (DNL) and integral nonlinearity (INL) error of the ADC at 1-V supply. The major errors in DNL and INL occur at output codes 64 and 192, which correspond to transitions of the 64C capacitor. This is due to the routing of the 64C capacitor, and the error is correctable in future iterations of the ADC.

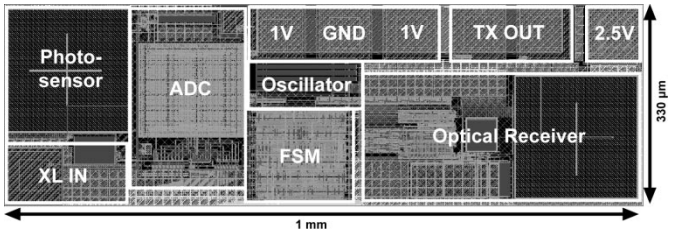

Fig. 9. Layout of CMOS IC showing the relative size of the components.

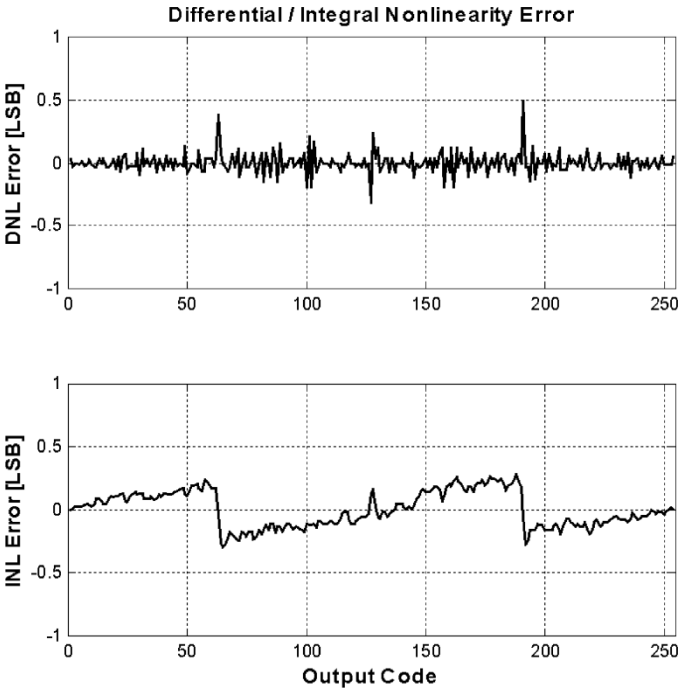

Fig. 10. Typical low-frequency DNL and INL error plots for 1-V supply.

Fig. 11 shows the effective number of bits (ENOB) of the ADC output with a full-scale input sinusoid, defined as

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02} \tag{1}$$

where SNDR is the total signal-to-noise-and-distortion ratio of the output in decibels. ENOB is plotted as a function of input frequency for 100-kHz sampling rate and varying supply voltage. The input sample-and-hold limits the bandwidth of the ADC. The CMOS switches used exhibit very high resistance for mid-rail inputs due to the low supply voltage. (The threshold voltages for the process were both approximately 0.5 V.) This bandwidth limiting is seen in Fig. 11 by comparing the curves for the different supply voltages. At low input frequency, linearity is very high for all supply voltages. However, as input frequency is increased, bandwidth improves with increased supply, tracking the sample-and-hold bandwidth. For bandwidth critical applications, the ADC could simply be supplied by three series solar cells (about 1.5 V), resulting in a modest increase in energy consumption.

A typical low-frequency fast Fourier transform (FFT) output spectrum at 1-V supply is shown in Fig. 12, for a full-scale input at 1.67 kHz, sampling rate of 100 kHz, and 10 000 data samples. The spurious free dynamic range (SFDR) is approximately 60 dB and ENOB is 7.7 for this input frequency.

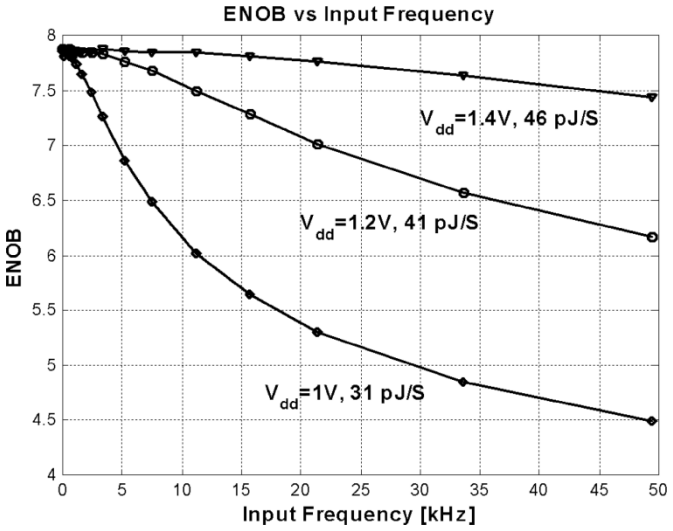

Fig. 11. ENOB versus input frequency and supply voltage ($f_s = 100$ kHz).

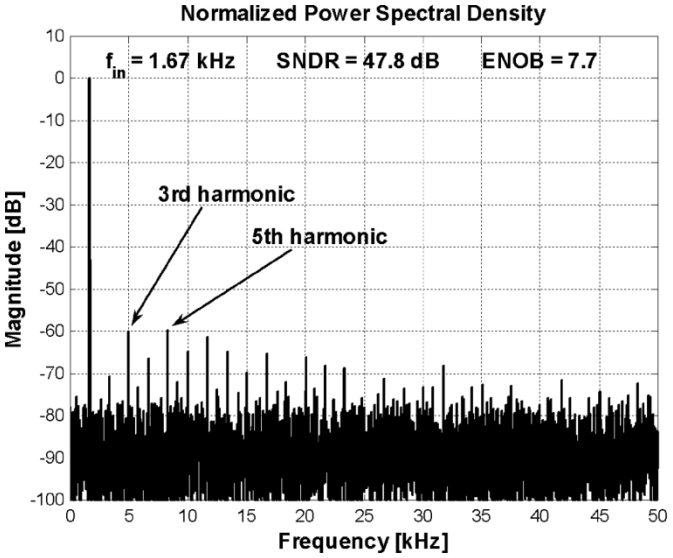

Fig. 12. Typical FFT (10 000 samples) for an input frequency of 1.67 kHz and supply voltage of 1 V.

The most important metric for the ADC is the energy per sample, defined as the total energy consumed in one full conversion cycle. Table I summarizes the energy consumption and standby power (at room temperature, with the comparator disabled) of the ADC for several supply voltages and 100-kHz sampling rate. The energy per sample of this ADC is significantly lower than several recently published moderate-resolution moderate-speed converters [12]–[14]. In particular, the energy consumption at 1 V is over 200 times lower than a very similar recently published ADC [13]. The overall performance of the ADC is summarized in Table II.

TABLE I
ENERGY AND STANDBY POWER OF THE ADC

Supply Voltage	Energy per Sample	Standby Power (T = 25°C)
1.0 V	31 pJ	70 pW
1.2 V	41 pJ	81 pW
1.4 V	46 pJ	96 pW

TABLE II
SUMMARY OF ADC PERFORMANCE

Performance Metric	Value
Voltage supply	1 V (nominal)
Input range	Rail-to rail
Sampling rate	100 kHz
Unit capacitance	12 fF
DNL	< ± 0.5 LSB typical
INL	< ± 0.5 LSB typical
ENOB (1V)	7.9 (DC), 7.0 (4.61 kHz)
Power dissipation (1V)	3.1 μW
Energy per sample (1V)	31 pJ
Standby power (1V)	70 pW
Die area (active)	0.053 mm^2
Process	0.25 μm CMOS (2P5M)

VI. System Energy Considerations

It is interesting to analyze the energy consumption of the ADC in the context of the target application of Smart Dust. The simulated energy consumption at 1 V and 100 kHz is 30.7 pJ, in very good agreement with the measured value of 31 pJ. Most of this energy is consumed in the comparator (17.5 pJ), while the SAR and switching network use 8.7 pJ, and the remaining 4.5 pJ is consumed in charging and discharging the capacitor array.

The lower bound on energy for the ADC is set by the total capacitance of the array assuming the ADC is matching limited (which is the case for this work). This is approached when the comparator, SAR, and switching network consume negligible energy compared with the energy to charge the capacitor array. While the total energy consumed in the capacitor array is input signal dependent, the worst-case lower bound (for zero input voltage) is a fundamental limit on energy per sample given by

$$E_{\min} = C_{\text{total}} \cdot V_{\text{ref}}^2 \tag{2}$$

where C_{total} is the total capacitance of the array (including parasitics). For the ADC presented here, C_{total} is 4.5 pF and V_{ref} is 1 V, and thus $E_{\min} = 4.5$ pJ, compared with the measured average energy of 31 pJ. A self-timed [15] or dynamic comparator along with custom digital logic in the SAR is necessary to approach this limit.

To put these energy numbers into perspective, Table III lists the energy required for the various Smart Dust operations. As seen in the table, an ADC sample, computation, and communication all require comparable amounts of energy. The last two columns list examples of just how many operations are possible assuming a fixed total energy source of 1 J (approximately

TABLE III
SUMMARY OF SMART DUST ENERGY CONSUMPTION

Operation	Energy/Op.	Ops./Joule	Translates to*
ADC Sample (8-bits)	31 pJ	37 billion	10 samples/s for over 100 years
Computation (μP instruction)	10 pJ (simulated)	100 billion	100 operations/s for over 30 years
Receive/Transmit (1-bit)	69 pJ/2 pJ	14 billion/500 billion	1 8-bit packet in and out per second for over 50 years

* Given a 1 Joule total energy budget and ignoring standby power

10 000 times less energy than an alkaline AA battery) and neglecting standby power. Including the standby power, this ADC could take ten samples per second for over 40 years from a 1-J energy budget (down from 100 years when neglecting leakage).

VII. Conclusion

An 8-bit 100-kS/s 1-V ADC was presented for use in sensor network applications. After introducing the target application and resulting design constraints, the actual ADC design was detailed. An energy consumption of 31 pJ per sample was achieved using a charge redistribution successive approximation architecture. Analysis of the full sensor node energy constraints showed that this ADC sample energy was comparable to the energy cost of the other relevant system operations. Example scenarios illustrated the extraordinary number of operations possible for these energy efficient sensor nodes even with very little total energy available over the node lifetime.

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