Micromachining Technology for Lateral Field Emission Devices

Veljko Milanović, *Member, IEEE*, Lance Doherty, *Student Member, IEEE*, Dana A. Teasdale, Siavash Parsa, and Kristofer S. J. Pister

***Abstract*—We demonstrate a range of novel applications of micromachining and microelectromechanical systems (MEMS) for achieving efficient and tunable field emission devices (FEDs). Arrays of lateral field emission tips are fabricated with submicron spacing utilizing deep reactive ion etch (DRIE). Current densities above 150 A/cm^2 are achieved with over $150 \cdot 10^6$ tips/cm^2. With sacrificial sidewall spacing, electrodes can be placed at arbitrarily close distances to reduce turn-on voltages. We further utilize MEMS actuators to laterally adjust electrode distances. To improve the integration capability of FEDs, we demonstrate batch bump-transfer of working lateral FEDs onto a quartz target substrate.**

***Index Terms*—Deep reactive ion etch, field emission device, MEMS, micromachining, vacuum microelectronics, vacuum tubes.**

I. Introduction

THE RESEARCH field of vacuum microelectronics strives to combine the best features of highly advanced solid-state fabrication technology and vacuum tube electronics [1], [2]. The goals and potential applications vary from high-temperature and high-radiation amplifiers, RF oscillators and amplifiers and field emitter displays [2]–[5], to a variety of sensors such as ion gauges [6]. To date, the proposed and fabricated field emission devices (FEDs) have been largely divided into two groups: vertical and lateral structures. Vertical FEDs were frequently fabricated with the use of silicon or Spindt-type metal tips to obtain currents of 100 mA [5]. To our knowledge, the achievable currents per tip with silicon as the emitting material have been limited to below the order of 1 μA. While a device fabricated by Temple *et al.* [2] had emission currents in excess of 20 mA, it was composed of an array of 28 074 tips and averaged 700 nA per tip. In most proposed applications, large field emitter arrays (FEAs) of up to tens of thousands of tips are required to achieve milliamps of electron current. Significantly higher currents have been achieved with the use of metals with lower work functions [5]. FEAs are commonly characterized by turn-on voltages above 60 V.

Lateral field emission devices (LFEDs) [7]–[9] may have many advantages in high-speed and RF applications owing to the simple fabrication, precise control of electrode distances, and lower capacitance. They have been demonstrated with relatively high current densities and turn-on voltages as low as 22 V [9]. Lateral silicon emitters with currents on the order of tens of microamps per tip have been demonstrated.

Utilization of micromachining technology presented in this work allows for more than an order of magnitude increase in achievable current for each individual device than in the previous work with silicon emitters. With the use of deep reactive ion etch [10], [11] (DRIE), which cyclically alternates between etch and deposition steps forming scalloped sidewalls, each fabricated lateral device can consist of dozens of tips vertically stacked with <0.5 μm distance. The methodology is very simple and requires only 1 mask and 1 trench etch with DRIE. It also provides for very accurate electrode distance control via photolithography, oxidation self-alignment, or sacrificial sidewall spacer self-alignment. These are discussed in detail in Section III. Diodes with turn-on voltages between 25 and 40 V emitting currents up to 400 μA were fabricated in a 2 μm process.

The new approach provides direct integration with MEMS actuators which provide a *mechanical tuning* feature. Electrodes can be placed at closer, arbitrary distances by lateral actuation using comb drive, gap-closing, or thermal actuators as described in Section IV.

Finally, the approach provides further integration capability for these types of devices by implementing batch-transfer methodology for fully fabricated diodes and triodes. This methodology, described in detail by Maharbiz *et al.* [12] has the advantage of decoupling circuit and MEMS processes. In our case, CMOS fabrication can therefore be completed independently of FED fabrication on separate wafers and in separate, optimized processes. After completion of both processes, FEDs are batch-transferred onto the CMOS wafer for integration with sense/drive and digital circuits. The methodology and results are detailed in Section V.

II. Theoretical Background

Emission of electrons from a cold metal cathode is characterized by the Fowler–Nordheim tunneling equation [13]. In most cases the equation closely approximates current–voltage characteristics for relatively highly doped semiconductors and is frequently used to extract physical parameters such as cathode sharpness, material work function, and field enhancement factor. We utilize an approximation by Spindt *et al.* [4] of the current I in terms the operating voltage V, work function

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ϕ [eV], emission area α [m^2] and the local field conversion factor β [m^{-1}]

$$I = aV^2 \exp(-b/V) \tag{1}$$

where

$$a = \frac{\alpha A \beta^2}{1.1\phi} \exp\left(\frac{1.44 \times 10^{-7} B}{\phi^{1/2}}\right)$$
$$b = 0.95 B \phi^{3/2}/\beta \tag{2}$$

and A and B are dimensionless constants, $A = 1.54 \times 10^{-6}$ and $B = 6.87 \times 10^7$. The parameter β can be expressed as the ratio of field enhancement to the cathode-anode distance

$$\beta = \frac{\kappa_{\text{tip}}}{d_{\text{cathode-anode}}}. \tag{3}$$

The dimensionless κ_{tip} represents the geometrical enhancement of electric field E [V/m] at the emitter tip due to its small radius of curvature, $\kappa_{\text{tip}} = E/(V/d)$. In the high voltage regime, the exponential term in the current equation may be neglected and current is simply $I = aV^2$. Integration of FEDs with MEMS actuators allows for electrode distance adjustment and modulation. To understand these effects on current, we differentiate current in high voltage regime with respect to d, yielding

$$\frac{\partial I}{\partial d} \approx V^2 \cdot \frac{\partial a}{\partial d} = \frac{2\alpha\beta A V^2}{1.1\phi} \exp\left(\frac{1.44 \times 10^{-7} B}{\phi^{1/2}}\right) \frac{\partial \beta}{\partial d}$$
$$= -\frac{2\alpha A V^2}{1.1\phi} \exp\left(\frac{1.44 \times 10^{-7} B}{\phi^{1/2}}\right) \frac{\kappa_{\text{tip}}^2}{d^3}. \tag{4}$$

As evident in the equations above, there are five physical ways of increasing the emitted current:

1) increasing voltage;
2) decreasing inter-electrode distance;
3) decreasing material work function by increasing the dopant concentration in the n-type silicon or by changing materials;
4) increasing the effective field at the tip through sharpening;
5) increasing the number of tips in a given area, i.e., tip density.

Our fabrication efforts, as detailed in Section III, are directed at simple and low-cost ways of optimizing 2), 4), and 5).

III. Device Fabrication and Characterization

A. Deep Reactive Ion Etch for Tip Fabrication

This method of tip fabrication is based on the cyclical nature of the time multiplexed inductively coupled plasma etch (DRIE) [10], i.e., the Bosch process [11]. The process etches deep, high aspect ratio trenches in silicon by alternating an SF_6 plasma etch with a teflon-like C_4F_8 deposition. As a consequence, trench sidewalls are not smooth, but feature periodic sidewall scallops, as illustrated in Fig. 1(b) and also shown in scanning electron microscope (SEM) images of Figs. 2 and 3. The scallop is commonly an undesired property of DRIE for microelectromechanical systems applications. However, when the mask layout defines an acute angle as shown in Fig. 1(a), two scalloped sidewalls meet at the corner of the structure and form

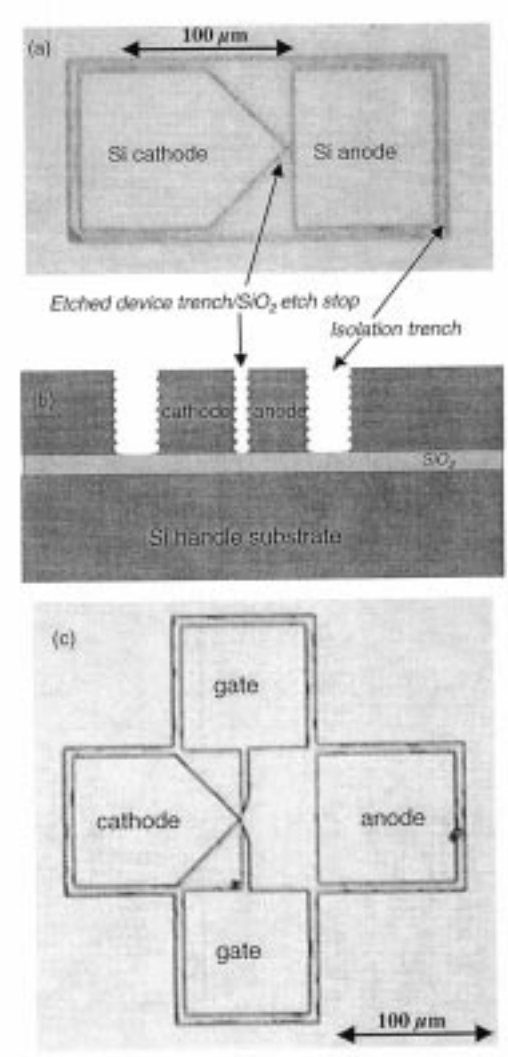

Fig. 1. Fabrication of LFEDs by DRIE etching of SOI wafers: (a) microphotograph of the top view of a diode test structure, (b) schematic cross section of the SOI wafer, (c) microphotograph of the top view of a triode test structure.

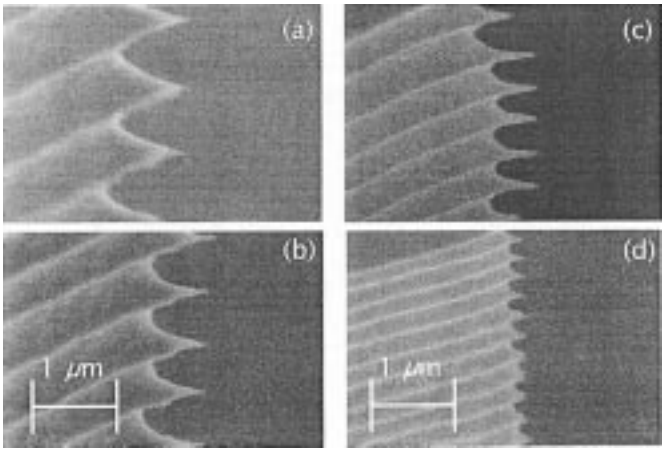

Fig. 2. Four SEM images taken at the same magnification after DRIE etch: (a) low density tips, (b) standard density tips, (c) high density tips, and (d) very high density tips. The corresponding anodes are outside the field of view.

relatively sharp tips. Therefore, with a simple layout as shown in Fig. 1(a) and a single etch of an silicon-on-insulator (SOI) wafer down to the oxide etch-stop, a field-emission diode [or

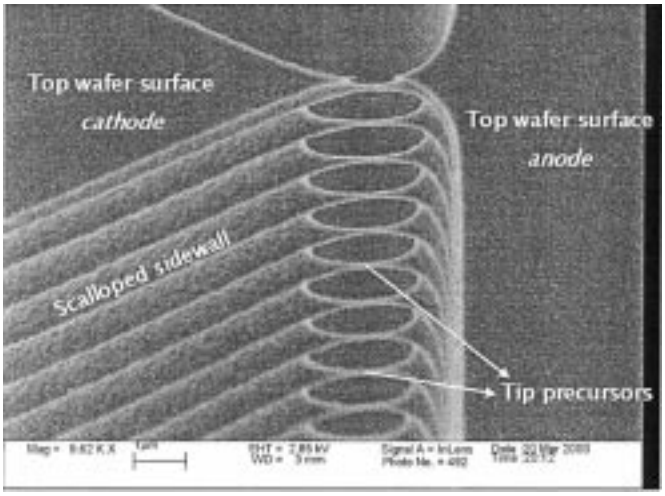

Fig. 3. Silicon nanowires extend between blocks overlapping in layout. DRIE alone does not result in tips with submicron spacing.

TABLE I
DETAILS OF DIFFERENT DRIE TIP RECIPES. IN ALL RECIPES, THE OVERLAP TIME BETWEEN ETCH AND DEPOSITION IS 0.5 s. QUANTITIES ARE FOR LAYOUT OF 60° TIPS. IN THREE LOWER CASES, COIL POWER = 600 W, PLATEN POWER = 120 W, AND SF_6 FLOW = 130 sccm. TOP RECIPE PLATEN POWER = 80 W, AND SF_6 FLOW = 100 sccm

DRIE tip recipe	SF_6 etch time [s]	C_4F_8 dep. Time [s]	Vertical tip dens. [μm^{-1}]	Tip Depth [nm]
Very high density	5 (lower flow, power)	5	4.4 - 4.6	240 ± 60
High density	6	5	2.9 - 3.1	350 ± 70
Std. density	9	7	2.0 - 2.2	510 ± 50
Low density	14.3	11	1.3 - 1.5	700 ± 100

triode as shown in Fig. 1(c)] is obtained with dozens of tips vertically stacked at submicron distances. Varying etch and deposition time in the periodic DRIE cycle results in varying vertical tip density. The latter is also a function of platen power and gas pressure. Four of the recipes used were characterized in a SEM and yielded the results listed in Table I. The highest vertical tip density achieved to date is 4.6 tips/μm. When mask layout includes many such devices at small lateral spacing, extremely high overall tip density is achieved. If, for example, a 50 μm thick SOI wafer is used, each edge includes $\sim$225 tips (for 4.5 tips/μm), and since there would be 5000 such edges/cm length at 2 μm lateral spacing, a total of 1 125 000 tips would result. This methodology, based on present achievements can therefore fabricate $225 \cdot 10^6$ tips/cm^2. We believe that with further optimization of the vertical etch process and using the most recent photolithography, this estimate can be far exceeded.

Tip depth is a function of layout tip sharpness, as well as DRIE parameters. Even with the high density recipe, tip depths in excess of 900 nm have been achieved with layout of 25 degree acute angle. Radii of tips following DRIE vary between 15 nm and 30 nm. While apparently sharp, such tips have turn-on voltages of well over 100 V rendering them inadequate for low-power FED applications. Images of tips formed with each of the four recipes are shown in Fig. 2. All three SEMs were taken at a magnification of 40 000.

For a given recipe, tip density and depth varies visibly down the device. This affects the cathodeanode distance and consequently the turn-on voltage of individual tips. The variation is up to the order of 100 nm, and its overall effect is still being investigated. We believe, however, that when devices are operated in the high voltage regime, all tips contribute to the total current nearly equally.

Depending on the mask layout, two types of geometry can result from the etch. In one case, as in Fig. 2, the anode is separated from the cathode by layout and does not affect the tip formation. The electrode distance in that case is defined photolithographically. A triode is designed by adding two additional electrodes separated from the anode and cathode in layout as shown in Fig. 1(c). In the second case where there is a slight (<0.5 μm) overlap in the mask, the etch results with the form shown in Fig. 3, where cathode and anode electrodes are not separated, but connected via silicon nanowires, or more fully overlapping. Oxidation and subsequent oxide removal, as detailed in Section III-B, results in self-aligned cathodes and anodes where both sides are lined with sharp tips at a distance which is a function of the oxidation process.

B. Oxidation Sharpening

To increase the electric field at the cathode surface, the tips are sharpened by thermal oxidation [14], i.e. by repeatedly growing and removing (wet etching) a thermal oxide at temperatures not exceeding 1000 °C. Since tip radii after DRIE are already <30 nm, wet oxidation of $\sim$700 Å is sufficient to achieve atomically sharp tips. Indeed, the tip radius is sharp enough to not be distinguishable by the SEM, namely below 5 nm. Due to the stress-dependent nature of oxidation, tip depth is relatively unaffected.

Additionally, since oxidation consumes silicon, the oxidation sharpening cycle can be exploited to separate the aforementioned self-aligned tip geometries. This is similar to the methodology in [9]. The nanowires in Fig. 3 become symmetrically sharpened tips on the cathode and anode in Fig. 4. Not only does this result in electrode distances closer than those possible through lithographic definition and etch aspect ratio alone, but sharpened tips on both ends of the gap effectively double the electric field. In terms of (3), this doubles parameter β resulting in a fourfold increase in current.

Devices fabricated with the above methodology were characterized in a vacuum probing station with triax cables connected directly to the probes to minimize instrument noise. Vacuum measurements were taken at pressures in the millitorr range. An HP4145 Semiconductor Parameter Analyzer was used to generate the test voltages and measure device currents. Data from these automated measurements were collected through a GPIB connection to a desktop computer. Prior to taking any measurements, all pairs of probes are landed on the same silicon structure to characterize the contact current–voltage (I–V) relation. Only when this contact current was very high relative to the device current, indicating functional ohmic contact, are measurements reported. Measurements of electrodes separated by larger

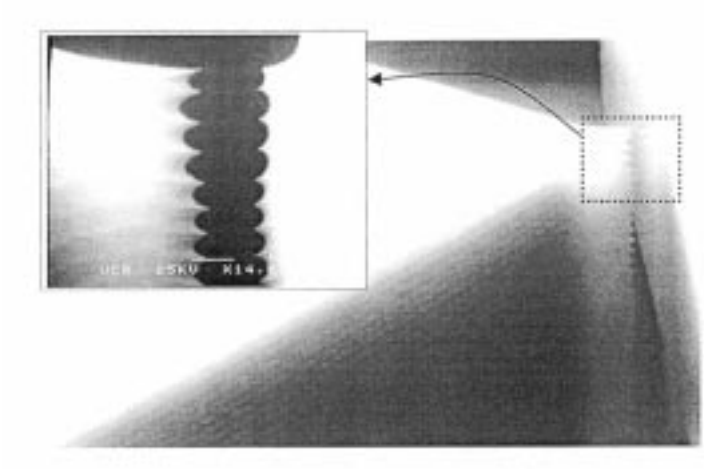

Fig. 4. SEM images of an LFED after DRIE etching and oxidation sharpening, showing multiple tips along the vertical edge. The main image at 2500 ×.

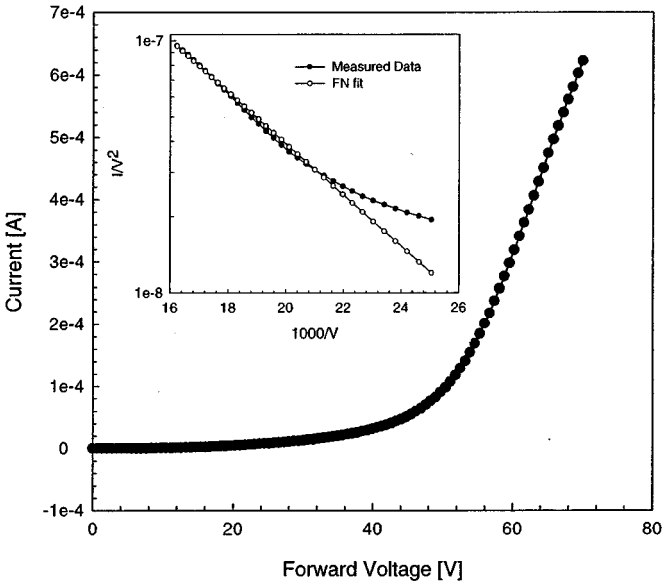

Fig. 5. Measured *I–V* characteristics of a typical SOI diode. Cathode-anode separation of 2.2 μm was measured on a SEM.

distances were carried out to ensure that no leakage paths existed among electrodes. In addition, many devices were tested before and after oxidation sharpening. The latter case did not result in measurable current and was further evidence that no leakage paths existed. Results of a typical sharpened SOI diode from a 22 μm SOI wafer are shown in Fig. 5. The diode shows hundreds of microamps of current at relatively low voltages. To our knowledge, this is the highest achieved current from a single lateral silicon tip. The data was fit to (1) extracting $a = 4.76 \cdot 10^{-6}$ and $b = 247$. Preliminary triode results in Fig. 6 show the emission current being tuned with varying gate voltages. Current was observed to undesirably flow between all pairs of electrodes in this device.

C. Submicron Electrode Self-Alignment with Sacrificial Sidewalls

Another approach was taken utilizing micromachining technology to preserve sharpness while maintaining a constant

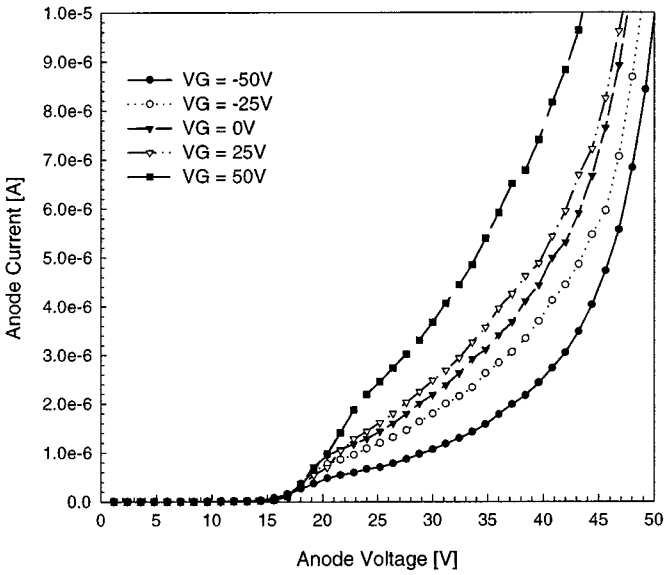

Fig. 6. Measured current–voltage characteristics of an SOI triode. Cathode-to-anode current is modulated by gate voltages in an SOI triode.

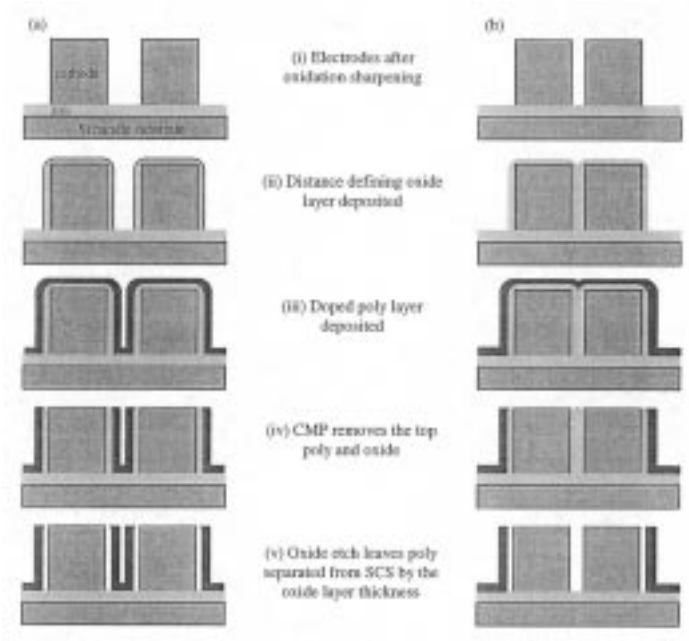

Fig. 7. Sacrificial sidewall process flow. In design (a), the electrodes are separated enough for poly to be deposited between them. In (b), the oxide prevents the poly from depositing between the electrodes. The oxide thickness precisely and controllably specifies the poly-SCS distance.

inter-electrode distance through the vertical length of the device. Moreover, this new approach illustrated in Fig. 7, offers arbitrary cathode-anode spacing. After DRIE and the oxidation sharpening cycle of the SOI wafer, an additional low-temperature oxide layer is deposited to define the inter-electrode spacing without removal of the thermal oxide. This is followed by an n-type doped polysilicon deposition that covers the top, the sidewalls and trenches surrounding the devices. Subsequent chemical mechanical polishing removes the polysilicon from the top of the devices to expose the underlying single crystal silicon (SCS) blocks. Over-polishing through the polysilicon,

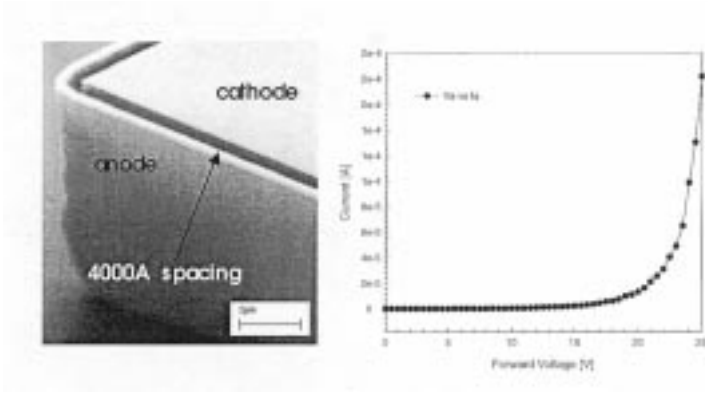

Fig. 8. Diode with 4000 Å spacing between SCS cathode and poly anode (a) footing is apparent at the base of the structure, and (b) a similar device with 8000 Å spacing has a turn-on voltage of 22 V. This structure corresponds to Fig. 7(a).

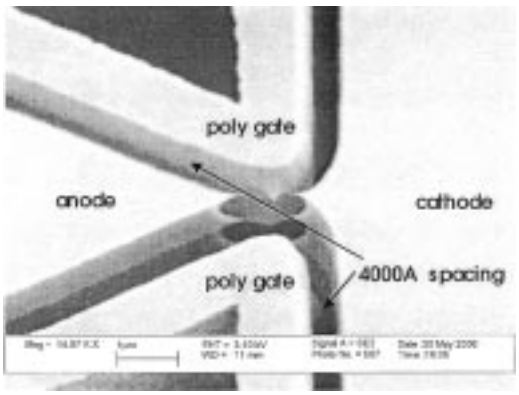

Fig. 9. An SCS diode with subsequent polysilicon processing can operate as either a triode or an electron source using the polysilicon walls as gates. This structure corresponds to Fig. 7(b).

oxide and the first micron of SCS removes the upper tips of the device which are often inconsistent. A timed HF removal of the sidewall oxide between the sharpened SCS tips and the polysilicon walls completes the fabrication. Typical resulting devices of this process are shown in Figs. 8 and 9.

This single-mask three-dimensional (3-D) fabrication methodology allows for arbitrary cathode-anode spacing with the polysilicon walls acting as the anode and SCS block as the cathode. Maintaining cathode tip sharpness while reducing the inter-electrode distance results in decreased turn-on voltages. One measured device [Fig. 8(b)] with 8000 Å distance resulted in a turn-on voltage of $\sim$22 V. Furthermore, the cathode-anode distance is now constant over the height of the device at exactly the oxide spacing that should result in all tips having a similar turn-on voltage.

Appropriately choosing the geometry of a self-separating SCS diode, as illustrated in Fig. 7(b), yields a triode in this process with the polysilicon walls acting as the gate (Fig. 9). Application of potential to the polysilicon modulates the cathode-anode current. Furthermore, a sufficiently high potential can be used to extract electrons from the cathode in an electron source configuration. With the cathode grounded, different extraction potentials are controlled by the gate voltage as illustrated in Fig. 10. The gate current for this device is below the nanoampere measuring threshold of the test equipment.

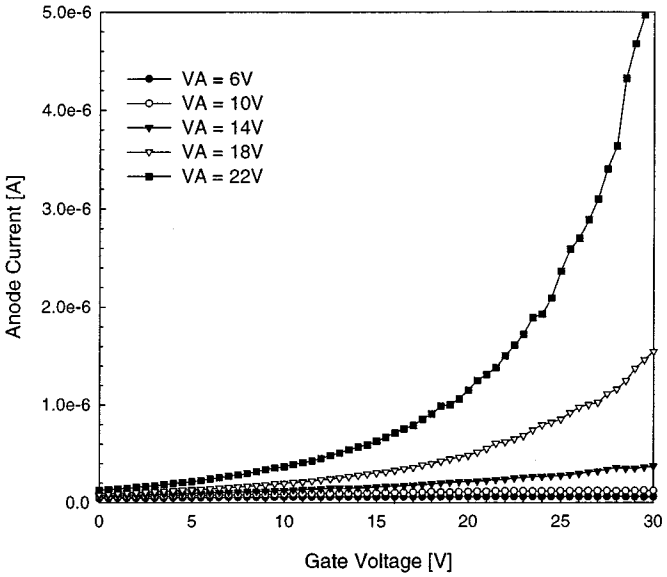

Fig. 10. Triode of Fig. 9 operating in electron source mode—increased gate potential extracts more current from the cathode to the anode.

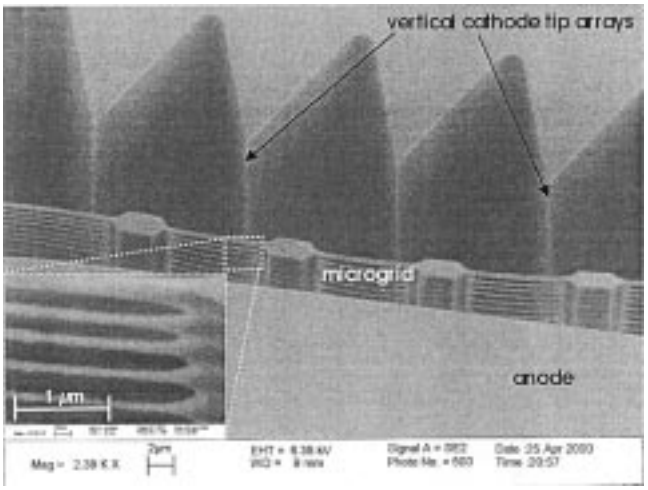

Fig. 11. Multi-tip cathode and anode pictured with a microgrid in between to modulate emission current. The zoomed-in image in bottom left corner shows that the diameter of silicon wires is <100 nm.

D. Fabrication of Microgrids

Another attempt at controlling emission current, as in classical vacuum tubes, is with silicon microgrids fabricated in the same process. SCS grids are designed in layout as very thin and modulated photoresist patterns, such that the vertical scalloping effect is sufficient to periodically etch through the structure and create airgaps. The horizontal width modulation in layout results in the microgrid structure shown in Fig. 11. This same phenomenon can be observed in Fig. 3. Attempts to date to test triodes based on such microgrid structures suffered from a common problem—electrostatic actuation of the microgrids. Namely, the microgrids are frequently fully released from wafer below and move and/or oscillate toward the cathode when applying test voltages. We are currently improving on the designs and fabrication to achieve functional devices of this nature.

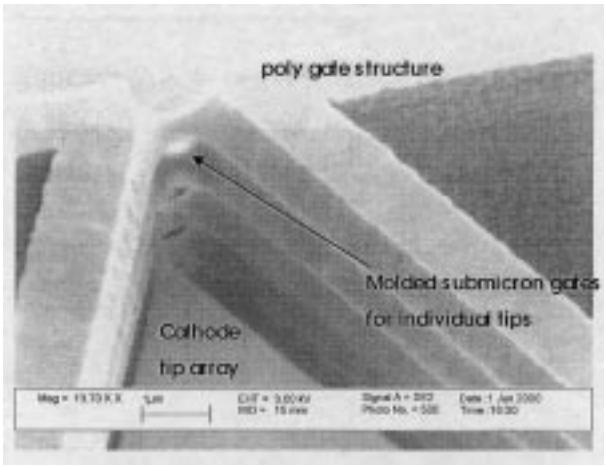

Fig. 12. Single-mask sacrificial sidewall technology allows for the fabrication of molded grid structures. The holes of the polysilicon grid align with and surround the tips of the cathode. For this SEM, poly gate structure was over-released in HF and partially extracted (raised) from between the cathode and anode to observe the small apertures.

The sacrificial sidewall technology enables the fabrication of a polysilicon grid structure that is both closer to the cathode tips and better aligned that the photolithographically-defined grids. This methodology is best understood with the DRIE result in Fig. 3 as the starting point. After a subsequent oxidation, the narrow silicon nanowires result in slightly separated atomically sharp silicon tips. At the same time, the oxide remains and isolates the structure from any subsequent depositions. When polysilicon is conformally deposited on such a structure, it fills the remaining openings between the oxide-covered nanowires, as well as covering sidewalls and tops of the structure. The result is difficult to image on a SEM, so for the example of Fig. 12, we extracted the poly gate from between the cathode and anode for inspection. The emission tips point directly toward the anode through holes in the molded grid. This type of device has not yet been characterized.

E. Two-Mask Three-Dimensional LFEDs

The addition of a second mask to the sacrificial sidewall process allows for the selective etching removal of polysilicon from areas directly before sharpened SCS tips. Namely, a diode structure as shown in Fig. 8(a) can be turned into a field emission array by selectively etching the polysilicon into an oxidation-aligned extraction gate. The oxide-defined spacing between the polysilicon cover and the SCS isolates the two layers and determines extraction voltages and efficiency as shown in the example of Fig. 13. This technology is in its very initial stages with no electrical characterization performed to date, but we hope it would ameliorate the effectiveness of the polysilicon in extracting electrons from the SCS cathode and result in ultra-dense FEAs.

IV. Microelectromechanical FEDs (MEMFEDs)

MacDonald *et al.* [16] have demonstrated the integration of cold cathodes with MEMS actuators. In their work, and that of Kenney *et al.* [15], numerous advantages of sensors based on tunneling are discussed. Due to the lateral structure of our proposed devices and high achievable currents, these FEDs lend themselves to numerous related applications. They are easily integrated with electrostatic actuators and fabricated in the same DRIE/oxidation process on SOI wafers. While the work is in initial stages, the result will be a variety of tunable diodes, triodes, and other vacuum devices. The example in Fig. 14 is a diode with ~ 600 atomically sharp tips with an electrostatically adjustable cathode-anode distance. Preliminary results in Fig. 15 show an increase of diode current in this device with the application of actuation voltage to the comb-drive structure which brings the cathode to a submicron distance from the anode. One goal of this research is a fully tunable RF-capable triode in which either placement of both gate electrodes or of all electrodes is adjustable electrically, and gap distances are varied electrostatically either with comb-drives or gap-closing actuators.

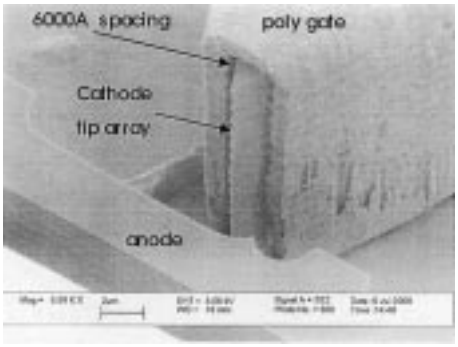

Fig. 13. Electron gun device fabricated with a two-mask process. SCS vertical cathode tip array is shown extending beyond a 3-D polysilicon covering acting as a lateral extraction gate. The oxidation-controlled spacing of 6000 Å is visible between the two layers following oxide removal.

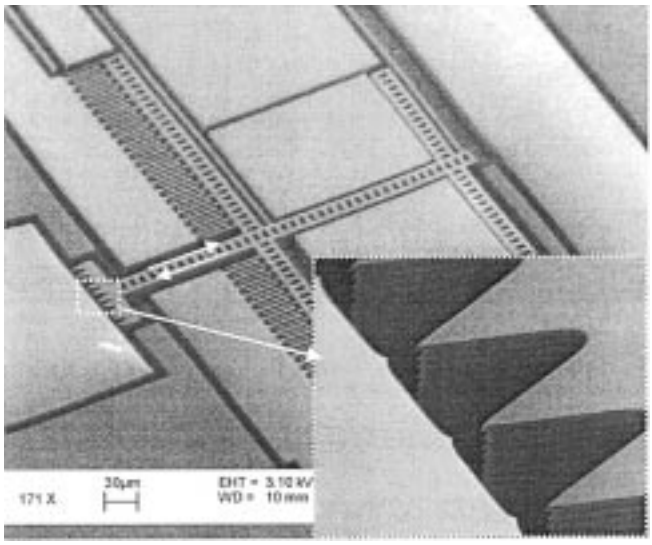

Fig. 14. Microelectromechanical field emission device (MEMFED) with multiple columns of submicron spaced tips. The cathode–anode separation of ~ 3 μm. can be adjusted with the comb-drive down to < 0.5 μm.

V. Batch Transfer of Devices

Fabrication of vacuum microelectronics is typically incompatible with other processes, e.g. CMOS, due to high-temperature oxidation sharpening. For most applications that may

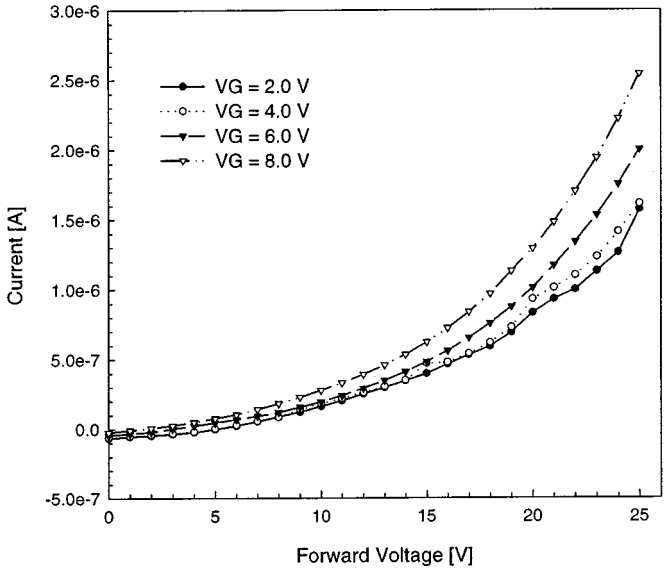

Fig. 15. Measured *I–V* characteristics of an electrostatically tunable field emission diode (MEMFED).

utilize the proposed MEMFED methodology, it would be advantageous to have the capability of integration with CMOS drive/sense circuits via batch transfer of the former from separate wafers. We utilized the methodology of Maharbiz *et al.* [12] on a variety of devices such as diodes, triodes, and electron sources. The devices were fabricated in the following four-mask process: starting with a 100 mm silicon wafer (*donor* wafer), 1.8 μm of low-stress nitride is deposited and patterned as the structural material over 2 μm of sacrificial oxide. This structural pattern was used to etch the sacrificial oxide as well to expose the wafer surface outside of device areas. Next, 4 μm of doped polysilicon was deposited. This polysilicon material was subsequently patterned and etched (DRIE) to form diodes and triodes over the structural nitride islands. After cycles of oxidation sharpening, as described in Section III-B, the thermal oxide on top surfaces was removed in a blanket etch. At this point the device fabrication is complete and bumps are added for release and bonding. A 150 Å/600 Å Cr/Au layer is evaporated as a seed layer; 6 to 8 μm gold bumps are electroplated in a resist mold.

The donor wafers are then diced. After resist-stripping, the structures on donor wafers are then released in concentrated HF for $\sim$4 min. The released structures remain on the individual chips due to the small gold bump *staples* [12], which were plated over the structures and surrounding silicon as shown in Fig. 14(a). At that point, the devices are batch-transferred using a flip-chip bonder after careful alignment of *donor* and *target* chips, as illustrated in Fig. 14(b). The target quartz wafer for the demonstration was plated with gold and patterned with pads in areas to where FEDs would be transferred. Although the process is designed for wafer-level transfers, at this time only chip-level transfers were considered and implemented. The target and donor substrates are aligned and pressure is applied to form a gold–gold compression bond; the donor substrate is then removed, leaving the switches in place over the pads. We verified that the devices continue to operate, as shown on a measured transferred diode in Fig. 16. This emission curve is similar to those found on pre-transfer polysilicon diodes (see Fig. 17. Diodes fabricated in polysilicon are significantly less consistent in emission characteristics and tip shape than those fabricated in SCS suggesting that batch transfer methods should be explored for the latter material.

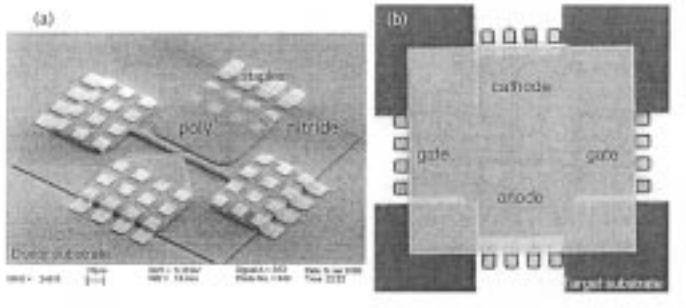

Fig. 16. Polysilicon triode fabricated for batch transfer to other substrates: (a) on donor substrate, released with gold staples holding it in place, and (b) after transfer to quartz target substrate, upside down; electrodes still visible through the nitride.

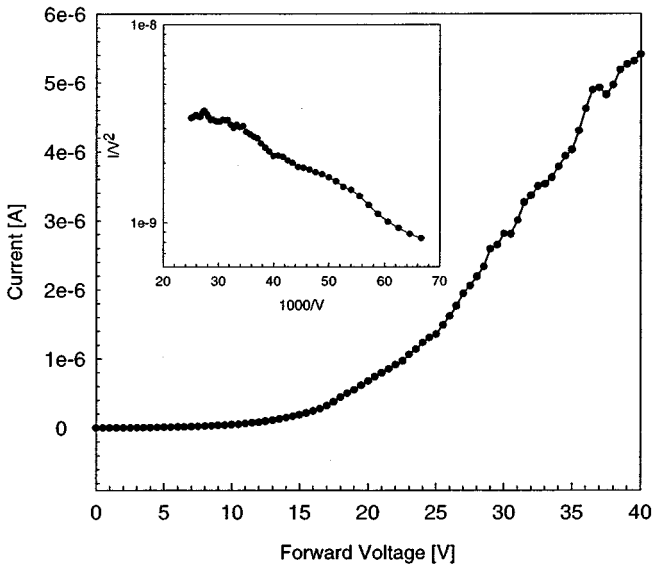

Fig. 17. *I–V* performance characteristics of a transferred polysilicon diode.

VI. Conclusions

The use of the scalloping formed in DRIE for sharp emission tips has been reported, resulting in achievable tip density of over $150 \cdot 10^6$ tips/cm^2, and current of over 150 A/cm^2. By utilizing sacrificial sidewall spacing, electrodes were placed at 4000 Å. We further utilized MEMS actuators to laterally adjust electrode distances. To improve the integration capability of the FEDs, we demonstrated batch bump-transfer integration of working FEDs onto a quartz target substrate.

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