# CMOS "smart pixel" for free-space optical communication

Brian S. Leibowitz, Bernhard E. Boser, Kristofer S. J. Pister

Berkeley Sensor and Actuator Center
497 Cory Hall
University of California, Berkeley
Berkeley, CA 94720-1774

## ABSTRACT

Fully integrated imaging receivers present a method of low power free-space optical communication with advantages over radio frequency and single element optical communication for a variety of network scenarios. This paper discusses the theoretical performance of such receivers and the design of a single "smart pixel" for use in a 2.5 Mbps integrated CMOS imaging receiver. The receiver has a simulated input referred noise power of –51 dBm (optical) and a dynamic range greater than 30 dB (optical) when operating at 2.5 Mbps. Power consumption is less than 50 μW and the pixel fits on a 150 μm pitch in a standard 0.35 μm digital CMOS process, readily allowing fabrication of inexpensive imaging arrays as large as 64 × 64 pixels. The receiver presented covers all aspects of reception from optical detection through A/D conversion (thresholding). An asynchronous digital serial receiver could decode the resulting data stream from this receiver. A low overhead architecture for communicating decoded data packets from any pixel in the imaging array to the edge of the chip is briefly described.

A prototype of this receiver has been fabricated and demonstrated to receive a –32.6 dBm optical signal at 875 kbps with a bit error rate of $74 \times 10^{-6}$. Although this receiver demonstrates the feasibility of a smart pixel imaging receiver consuming less power than comparable RF receivers, the fundamental limits based on thermal noise suggest an opportunity to improve the minimum detectable signal by one order of magnitude over the current implementation.

Keywords: smart pixel, imaging, receiver, free-space, optical, wireless, communication, low power

## 1. INTRODUCTION

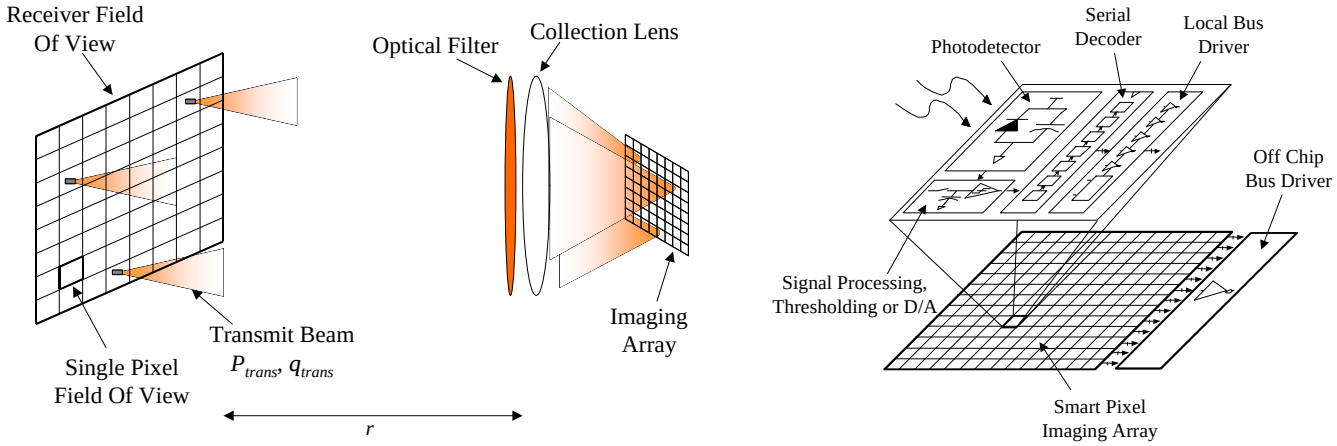
Portable computing and communication devices and wireless distributed sensor networks such as "smart dust" are just two applications driving the need for novel low power communication links[1]. Demand for longer battery life or reliance on micro-power energy sources such as solar cells severely limits the available transmission power in these scenarios. In most cases it is equally important to minimize power consumption in the receiver.

If line of sight is available, optical communication has many advantages over radio frequency communication when designing these small, low power devices. The most important advantage for low power communication is the ability to generate low divergence optical beams from small transmitters. Even millimeter scale optical transmitters can achieve diffraction-limited beam divergence better than 1 milliradian, leading to effective "antenna gains" in excess of one million compared to isotropic radiators. These high antenna gains, which cannot be realized at this scale for radio frequencies, allow optical transmissions with energy levels on the order of 1 fJ/bit to 1 nJ/bit to be received over distances of several meters to several kilometers, respectively. Optical communication also permits direct base band signaling, avoiding the added complexity of modulation and demodulation as well as the power consumption of carrier and intermediate frequency circuits.

The superior diffraction limit is advantageous at the receiver as well. Receiver optics built on the millimeter scale can achieve narrow acceptance angles similar to corresponding transmitter beam divergences. This dramatically reduces noise from ambient light and rejects interference from neighboring transmitters. Thus, an array of single channel optical receivers each with a different acceptance orientation can form a multi-channel optical receiver capable of isolating simultaneous transmissions based solely on their physical origin. Receivers implementing this technique known as space-division-multiple-access (SDMA) are referred to as imaging receivers, or angle-diversity receivers. A simple example of such an imaging receiver presented in this conference consists of a video camera with real time video signal processing to detect optical transmissions[2]. In this system each pixel functions as a single channel optical receiver that monitors a different portion in the overall field of view of the video camera.

---

Correspondence: B. S. Leibowitz; Email bsl@eecs.berkeley.edu; Telephone: 510-642-4571; Supported by the Fannie and John Hertz foundation. Other author information: B. E. Boser; Email: boser@eecs.berkeley.edu. K. S. J. Pister; Email: pister@eecs.berkeley.edu.




(a) (b)

**Figure 1: (a) The imaging receiver concept. (b) Basic components of a "smart pixel" in an integrated imaging receiver.**

Free-space imaging receivers achieving bit rates of one hundred megabits per second per pixel have been demonstrated by dedicating high speed electronic receivers to each photodetector in a custom photodetector array[3]. These high performance arrays typically consume several Watts of power and are relatively expensive.

This paper discusses a hybrid of these two architectures in which a single chip contains a photodetector array similar to those found in CMOS cameras, but with a complete electronic receiver integrated into every pixel in the array. A single pixel for such an array including a photodetector and analog signal reception has been implemented to demonstrate the feasibility of such an architecture. Only recently has CMOS transistor scaling allowed so much functionality to be integrated into a single pixel, or "smart pixel". This integration provides an elegant way to achieve high per pixel bit rates compared to the video frame processing solution. At the same time, readily available CMOS batch fabrication allows for very inexpensive production of such a receiver.

Such smart pixel imaging arrays offer performance benefits for a wealth of current applications. For example, imaging receivers consuming only a few milliwatts of total power could form the basis of ad hoc room-wide wireless networks with Mbps links. In such a network SDMA allows many simultaneous transmissions without channel sharing, achieving aggregate bandwidths of several Gbps with relatively simple protocols. In contrast, current IrDA implementations consuming slightly less power only offer short-range point-to-point communication[4]. Radio frequency LANs offer the distinct advantage of communication through several rooms from an individual transceiver, but require much more signal processing to achieve multiple access and overcome multi-path fading. Longer haul optical links have already found commercial use for building-to-building network links due to their rapid deployment, low cost, and avoidance of RF regulations.

Imaging receivers are also an enabling technology for novel applications where radio frequency links are simply impractical. For example, smart dust networks consisting of hundred or thousands of cubic millimeter sensors distributed throughout a room or over a large outdoor environment could all transmit data to a single imaging receiver simultaneously. Thus, imaging receivers allow large amounts of collective data to be rapidly extracted from such networks with minimal communication complexity.

Section 2 of this paper discusses the fundamental optical performance imaging receivers, which forms the basis of the design process and allows us to calculate performance limits in any of these scenarios. In Section 3 a practical smart pixel receiver architecture for use in a fully integrated CMOS imaging receiver is proposed. Section 4 shows a particular circuit implementation of the critical analog portion of this architecture along with experimental data. The results of these discussions and experiments are summarized in Section 5.

## 2. IMAGING RECEIVERS

### 2.1 Signal Reception

Fig. 1a demonstrates the concept of an imaging receiver. The receiver collects light from some field of view that contains one or more transmitters. The transmitters are on-off modulated (OOM) point sources that are oriented toward the receiver. If we

approximate the transmission beams as having uniform power density within some half angle $q_{trans}$ then peak power collected by the receiver is

$$P_{rec} = \frac{2P_{trans}}{p\left(rq_{trans}\right)^2} A_{lens} \cos(q_a) \tag{2.1}$$

where $P_{trans}$ is the average optical transmission power, $r$ is the link range, $A_{lens}$ is the area of the collection lens and $q_a$ is the angle of the transmitter in the field of view relative to the optical axis of the receiver. In many cases the receiver field of view is small enough that $\cos(q_a)$ can be neglected in Eq. 2.1. Ideally, all of this collected power is imaged onto a single photodetector in the imaging array. In this case the received peak signal current is

$$i_{sig} = P_{rec} \cdot T \cdot R \tag{2.2}$$

where $T$ is the overall transparency of the optics and the transmission channel and $R$ is the responsivity of the photodetector at the transmission wavelength.

In practice, the signal power may be split among neighboring pixels in the imaging array. In such cases maximum ratio combining provides an optimal way to combine the resulting signals[3]. However, in practice the optical power may be focused onto a spot much smaller than the dimensions of individual photodetectors, minimizing the likelihood of the signal power being divided among neighboring pixels. This is the case for the smart pixel receiver design discussed below. In such cases the likelihood of the signal power striking a photodetector is equal to the fill factor, the ratio of the photodetector area to the total pixel area. One way to alleviate this problem is to use a micro-lens array to focus the collected optical power onto the photodetectors[5]. Otherwise, the reduction in signal power or the probability of not detecting a signal as a result of low fill factor must be taken into account in the system design. In some applications, such as collecting data from distributed sensor networks, it is acceptable to lose a fraction of the incoming transmissions.

**2.2 Optical Noise**

The fundamental limiting source of noise in an imaging receiver is due to ambient light reflected from the field of view, which may be bright sunlight in the worst case. To calculate the received ambient power, the background scene in the field of view is modeled as a diffuse Lambertian reflector. Therefore the received ambient power does not depend on the angle of the background surface with respect to the receiver, so we can assume a normal background surface to simplify the calculations. Thus, the effective ambient optical power incident on the field of view of one pixel is simply

$$P_{BG} = Ir_{amb} \cdot \left( r \cdot \frac{q_c}{N} \right)^2 \cdot \Delta l \tag{2.3}$$

Where $Ir_{amb}$ is the ambient spectral irradiance in W/m$^2$·nm at the communication wavelength, $q_c$ is the full field of view of the receiver, and $\Delta\lambda$ is the optical bandwidth of the receiver filter in nm. This generates a background illumination current in each pixel given by

$$I_{BG} = \frac{P_{BG} \cdot R_{BG}}{pr^2} A_{lens} \cdot T \cdot R \tag{2.4}$$

where $R_{BG}$ is the reflectivity of the background. Note that the collected background power depends on the receiver field of view and array resolution, but not on the link range. This induced DC current leads to white shot noise with spectral density

$$\overline{di_{shot}^2} = 2q_e I_{BG} / \Delta f \tag{2.5}$$

The optical SNR of the link is

$$SNR_O = \frac{i_{sig}^2}{\overline{di_{shot}^2} \cdot NBW} \tag{2.6}$$

where $NBW$ is the noise bandwidth of the receiver, which optimally is approximately equal to the bit rate for a non-return-to zero (NRZ) receiver.

### 2.3 Link Design

Eqs. 2.1 through 2.6 guide the initial design of the imaging receiver. Many of the parameters are determined by the target application. For example, the transmit beam divergence and receiver aperture are limited by the dimensions of the transmitter and receiver, respectively. Table 1 shows several scenarios that can achieve sufficient $SNR_O$ for reliable communication. The first row demonstrates the ability of low power millimeter scale transmitters to communicate over moderately long outdoor links. The second row shows that the same low power transmitter with somewhat better beam divergence can communicate over long hauls if a large receiver aperture exists, enabling satellite uplink. Communication between spacecraft, such as in satellite networks, can be implemented very efficiently with imaging receivers. The last two rows in Table 1 demonstrate typical room-wide LAN configurations.

| Bit Rate | Link Range | $q_{trans}$ | Ambient Illumination | Receiver Aperture | Full Receiver Field of View | Pixel Array | $i_{sig}$ | $SNR_O$ |
|---|---|---|---|---|---|---|---|---|
| 5 Mbps | 3 km | 1 mrad | Bright Sun | 15 mm | 45 º | 16 × 16 | 9.4 nA | 34 dB |
| 1 Mbps | 500 km | .15 mrad | Bright Sun | 20 cm | 5 º | 16 × 16 | 2.7 nA | 24 dB |
| 5 Mbps | 10 m | 20 º | Office | 10 mm | 90 º | 8 × 8 | 3.1 nA | 23 dB |
| 100 Mbps | 10 m | 5 º | Office | 10 mm | 90 º | 8 × 8 | 49 nA | 24 dB |

**Table 1. Examples of viable free-space optical communication links according to Eqs. 2.1 through 2.6. In all cases $P_{trans}$ = 5 mW, Äë = 10 nm, ë = 830 nm, $R$ = 0.3 A/W, $R_{BG}$ = 0.3 W/W, $T$ = 0.5 W/W.**

The results of Eqs. 2.1 through 2.6 determine the electrical constraints for the receiver. For example, the receiver must be sensitive enough to detect $i_{sig}$, but must also be able to handle the DC offset $I_{BG}$. This second constraint may force the designer to increase the array resolution beyond what is required to achieve sufficient $SNR_O$. In such cases the optical noise becomes negligible and the overall noise performance is determined solely by the electronic noise in the receiver. Array resolutions as large as 64 × 64 may be desirable for some applications. However, increasing the array resolution limits the available area and power for each pixel and probably reduces the fill factor. The design of an imaging receiver typically involves a few iterations between the optical link calculations and practical implementation considerations such as these.

## 3. SMART PIXEL IMAGING RECEIVER ARCHITECTURE

Fig. 1b shows the basic components of a smart pixel for an integrated imaging receiver. The signal generated by a photodetector is amplified and filtered in the analog domain. A threshold operation or A/D conversion converts the signal into a digital serial data stream. If a simple threshold is used then a standard serial data decoder can receive the incoming data packets. These packets must then be communicated to the edge of the array for use by the host platform.

Many coupled engineering tradeoffs are involved in the design of such a smart pixel, making a general treatment difficult. However, the need for array resolutions potentially as high as 64 × 64 pixels leads to a basic requirement that minimal circuit area should be used to allow for a reasonable fill factor within a reasonable die area. In addition, power consumption per pixel must be kept very low either to preserve battery life or to avoid the thermal dissipation limit of the die package. These constraints may require a pixel pitch as small as 200 μm and power consumption in the range 25-100 μW per pixel. Another common requirement is to have a wide dynamic range since the received signal strength varies greatly over the link range. In order to manufacture inexpensive imaging receivers, integrate dense digital electronics at every pixel in the array, and possibly fabricate imaging receivers along with other digital blocks on a singe die it is assumed that a modern digital CMOS process will be used.

The most critical and challenging portion of the design is the analog signal path, which will be the main focus of this section. A simple digital communication scheme to send received data packets to the edge of the array is also proposed.

### 3.1 Analog architecture

Fig. 2 shows the proposed signal processing blocks for the smart pixel receiver. The photodetector is a reverse biased p-n junction diode, which is often well-substrate junction for maximum responsivity. Photons absorbed in or near the depletion region of the diode generate electron hole pairs that drift across the junction due to the electric field leading to a reverse bias current flow. Thus the photodiode is modeled as its junction capacitance in parallel with the signal current $i_{sig}$+$I_{BG}$ and the reverse bias leakage current of the diode, which is usually negligible.

A front-end charge amplifier then converts the photocurrent into a voltage signal and is the main source of electronic noise. Due to the relatively low bit-rates under consideration and the absence of high-density capacitors other than MOS gates in digital processes, it is not practical to AC couple the front-end amplifier. Therefore the DC ambient photocurrent will

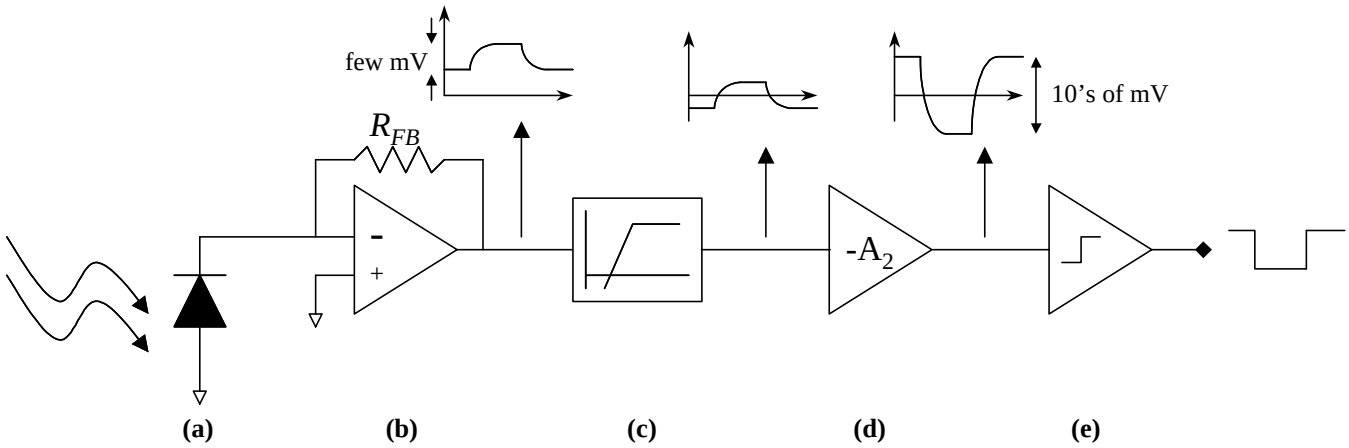



**Figure 2: Proposed analog architecture for an on/off modulated (OOM) optical receiver. (a) Photodiode detector. (b) Front-end photocurrent amplifier, shown as a trans-impedance amplifier for example. (c) High pass filter to remove ambient signal power. (d) Post amplifier. (e) Comparator for signal thresholding. Shown for reference are typical signals after each block.**

be amplified and must not lead to saturation. The use of narrow band optical filters and the division of ambient power throughout the pixel array according to Eq. 2.3 typically alleviate this problem.

A high pass filter then removes the DC component of the signal. In contrast to AC coupling, the corner frequency of the high pass filter can readily be implemented with high-density MOS gate capacitors, as shown in Section 4.2. The signal is then further amplified so that it can be accurately compared to a threshold voltage. An asynchronous serial decoder could receive the output data stream.

### 3.2 Front-end amplifier topology

A front-end impedance amplifier is needed to amplify the photocurrent detected by the photodiode. As discussed above, it is important to minimize the complexity of the amplifier to conserve area. Since this amplifier is DC coupled to the photodiode, it must also have a reasonable dynamic range to avoid saturation due to ambient illumination and to accommodate considerable variation in signal power as the link range varies.

Three common amplifier topologies shown in Fig. 3 can be used to perform this function. The following comparison of these amplifiers is based on Heatley's analysis[6]. The high-impedance receiver has a characteristic $RC_{diode}$ time constant that is much longer than one bit period, which requires the use of an equalization filter to produce a correct output signal. It has been shown that this topology offers the best noise performance of the three, primarily due to the low noise contribution of the large sense resistor. However, this large sense resistor also causes it to have the lowest dynamic range of the three. In addition, the need for a matched equalization filter makes it more complex than the others. Conversely, the low-impedance receiver has an $RC_{diode}$ time constant that is much shorter than one bit period. This alleviates the need for the equalization filter. Although the small sense resistance leads to the highest dynamic range of the three amplifiers, it also causes it to have

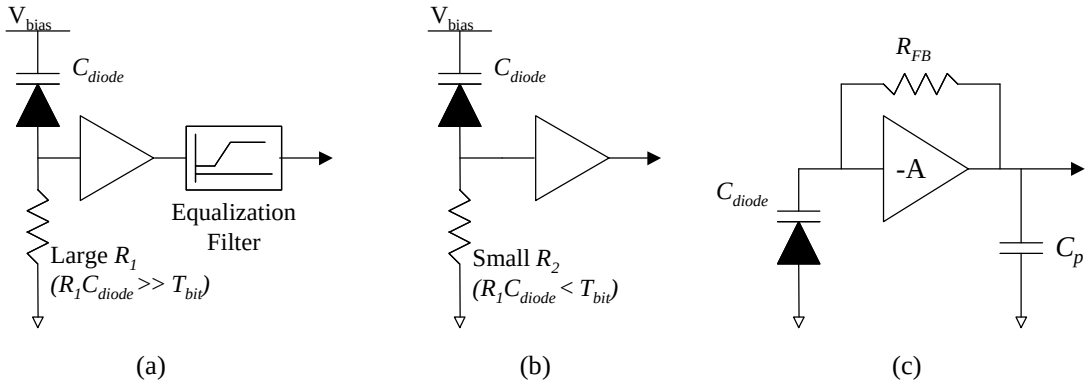



**Figure 3: Basic impedance amplifier topologies. (a) High-impedance amplifier with bandwidth much less than the bit rate (b) Low-impedance amplifier where bandwidth is commensurate with the bit rate (c) Transimpedance amplifier.**

the worst noise performance.

The transimpedance amplifier offers a compromise between these two extremes, offering decent dynamic range and noise performance while avoiding the complexity of the high-impedance design. The negative feedback loop offers a simple mechanism to bias the photodiode as well as the core voltage amplifier, further reducing complexity. Further, $R_{FB}C_{diode}$ may be much longer than one bit period without the need for equalizing filters. This allows the use of relatively large feedback resistors to achieve high sensitivity and low noise. These benefits make the transimpedance amplifier the most attractive choice for a smart pixel receiver.

The transimpedance of this amplifier is approximately equal to $R_{FB}$ under the assumption $A >> 1$. Since the diode capacitance is relatively large the input node sets the dominant closed-loop pole of the transimpedance amplifier. The effective impedance at this node is set by $R_{FB,}$ which is Miller divided by the voltage amplifier. The closed loop bandwidth is therefore

$$f_{p1} = \frac{1}{2p}\frac{A+1}{t} \tag{3.1}$$

where $t \equiv R_{FB}C_{diode}$. About three $t$ are required per bit period to allow for settling; hence the receiver is designed with $f_{p1}$ at approximately half the bit rate. Note that by increasing the gain $A$ it is possible to use a larger feedback resistor to achieve higher transimpedance and lower thermal noise density for a fixed bandwidth. If a single stage voltage amplifier is used, the only other significant pole is from the output node at frequency

$$f_{p2} = \frac{1}{2p}\frac{G_M}{A \cdot C_p} \tag{3.2}$$

where $G_M$ is the transconductance of the amplifier and $C_p$ is the load capacitance.

It can be shown that the open loop pole at frequency $f_{p1}/(A+1)$ leads to unity loop gain and 90° phase shift at $f_{p1}$. Setting $f_{p2} \geq f_{p1}$ would contribute at most an additional 45° phase shift at this frequency, leaving a 45° phase margin for stability. All other high frequency poles should contribute minimal phase shift at $f_{p1}$ for this claim to be valid. This stability requirement can be expressed as

$$C_p \leq C_{diode}\frac{R_{FB}}{r_o \cdot A} \tag{3.3}$$

There are two main noise contributions in the transimpedance amplifier. First, the feedback resistor generates thermal noise that is best modeled as a parallel noise current here. This thermal noise current adds directly to the input. Second, the amplifier contributes thermal noise that is dominated by its input transistor. To analyze the noise performance of this amplifier, it is most useful to compare the input current power with the output noise voltage power divided by $R_{FB}^2$. The output noise spectrum is given by

$$\frac{\overline{dv_o^2}}{R_{FB}^2} = \frac{4kT}{R_{FB}}\left(\frac{1}{1+\frac{f}{f_{p1}}}\right)^2 \cdot \Delta f + \frac{8}{3}\frac{kT}{g_m R_{FB}^2}\left(\frac{1+\frac{f \cdot A}{f_{p1}}}{1+\frac{f}{f_{p1}}}\right)^2 \cdot \left(\frac{1}{1+\frac{f}{f_{p2}}}\right)^2 \cdot \Delta f \tag{3.4}$$

where $g_m$ is approximately equal to the transconductance of the input transistor, or $G_M$ in the case of a single stage amplifier. Flicker noise is typically negligible since low frequency signals will later be filtered out. The first term in Eq. 3.4 is the thermal noise current of the feedback resistor, which is filtered by the approximate amplifier frequency response. The noise contribution from the input transistor can be understood as follows. For frequencies below $f_{p1}/A$ the feedback path has unity gain, so the output noise density is equal to the equivalent input noise voltage of the input transistor. As frequency increases from $f_{p1}$/A to $f_{p1}$ the output noise power density rises by a factor $A^2$ due to the decreasing feedback factor. Above $f_{p2}$ the output noise voltage density falls with the high-frequency roll-off of the voltage amplifier. Fig. 4 shows the asymptotes of these noise contributions.

In a single stage amplifier $g_m R_{FB} > A$, so the input transistor noise is negligible compared to thermal noise from $R_{FB}$ at low frequencies. However, between $f_{p1}$ and $f_{p2}$ the normalized input transistor noise density shown in Fig. 4 may be more or less than unity. Since this noise density covers a wide frequency range, the input transistor may dominate noise performance. However, most of this noise is out of the signal band and can be filtered. Further, the amplifier may be designed for $f_{p2} = 2f_{p1}$ (60° phase margin) in order to achieve maximally flat magnitude response and optimal settling time[7]. In this case it can be

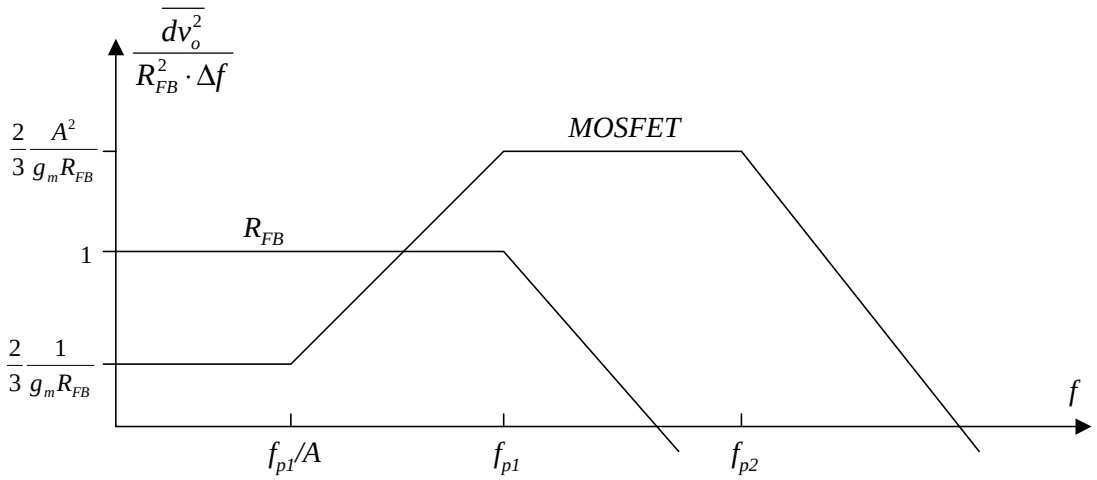



**Figure 4: Transimpedance amplifier noise spectrum contributions normalized to $4kT/R_{FB}$.**

shown that the peak noise density contributed by the input transistor is approximately an order of magnitude less than the top asymptote shown in Fig. 4.

### 3.3 Filtering and further amplification

For minimum strength input signals, the output signal from the transimpedance amplifier is often too small to be accurately compared against a threshold. It is necessary to further amplify the signal, but the DC offset induced by the ambient photocurrent must not be amplified to prevent saturation. Therefore a high pass filter should be implemented before further amplification takes place. The corner frequency of this filter must be set low enough that it doesn't block a significant amount of signal power, but should be as high as possible to avoid the need for large filter capacitors. For this reason it is desirable to use Manchester encoding instead of NRZ encoding to reduce low frequency signal content.

Minimum strength signals must be amplified to levels greater than input error of the comparator, which is typically set by the threshold variation between two transistors. This consideration sets the minimum gain for this stage. However, the dynamic range of the receiver is almost always larger than the ratio of the supply voltage to threshold variations. Therefore maximum strength input signals cannot be amplified linearly in this stage and the amplifier must be able to compress large signals without degradation in its transient response. However, signal strength will vary relatively slowly, so it is not necessary to rapidly recover from large signal transients to accurately amplify small signals.

### 3.4 Serial Decoding and Off-Chip communication

Once the signal is compared to a threshold, a standard serial decoder can receive the resulting digital serial data steam. Due to limited area available for each pixel, the serial receiver will have a packet size in the range 8-16 bits. Using such a short packet length has other advantages as well. For example, atmospheric turbulence modulates the transmission channel with millisecond time constants. If packet lengths are only a few microseconds long, then turbulence mainly contributes quasi-static signal attenuation for each packet. Another advantage of short packets is tolerance of relatively high bit error rates while only using simple error detection algorithms such as parity checks.

Once a valid data packet is decoded it must be delivered out of the imaging array. Many pixels throughout the imager may be receiving data simultaneously, and the resulting data packets must eventually share a single bus. However, the tight constraints on chip area and power prohibit the implementation of complex chip-wide communication networks. Passing received packets out of the imaging array in a "bucket brigade" fashion can solve this problem. Such a scheme only requires local communication between neighboring pixels, which can be implemented with simple handshaking protocols. Although data arrives asynchronously at each pixel, it is possible to use synchronous communication between pixels to simplify the logic design. Statistical analysis must be done to insure that resource contention will not lead to backlogs under conceivable conditions. One simple way to avoid this possibility is to simply note that in some applications individual data packets are not critical, and one data packet can be discarded every time two packets compete for one "bucket".

## 4. ANALOG CIRCUIT IMPLEMENTATION

The architecture for a smart pixel receiver described above from photodetection through signal thresholding has been fabricated in a 0.35 μm digital CMOS process. The receiver has been designed for the target application in given in the first line of Table 1, except that 2.5 Mbps Manchester encoding will be used instead of 5 Mbps NRZ coding as discussed in Section 3.3. This implementation demonstrates the feasibility of the proposed smart pixel architecture within the area and power constraints of a high-resolution imaging receiver.

### 4.1 Photodetector and transimpedance amplifier

A 50 × 50 ìm photodiode consisting of a parallel combination of p+/n-well and n-well/p-substrate junction diodes is chosen for this receiver. The diode structure is chosen for its high responsivity and the dimensions are chosen to be comparable with the estimated circuit area to achieve a reasonable fill factor. At a reverse bias of 1.7 V this diode structure has a measured responsivity of 0.27 A/W at 633 nm, corresponding to a quantum efficiency of 52%. The diode junction capacitance is approximately 2 pF.

The schematic for the transimpedance amplifier is shown in Fig. 5. The core voltage amplifier consists of three identical stages each with a gain of 3. This has two key advantages over a single stage amplifier. First, each amplifier stage can achieve a relatively wide frequency response at low bias current due to its low voltage gain. Second, the small-signal amplifier gain is set to first order by the geometric ratio of two devices. This allows the absolute amplifier gain to be accurately designed, which is important since this gain determines the closed-loop bandwidth according to Eq. 3.1. A key disadvantage of this design compared to a single stage amplifier is the introduction of two additional poles, which must be kept well above the signal bandwidth for stability.

For a total amplifier gain of 27 and a closed loop bandwidth of 4.5 MHz, Eq. 3.1 specifies the feedback resistor to be 500 kΩ. This value is too large to implement with on chip resistors under the tight area constraints for a smart pixel. A PMOS transistor biased in the linear region is used instead. This transistor is biased with $V_{GS}$-$V_{TH}$ large compared to threshold variations to generate a reliable small-signal resistance. The large signal performance of the feedback PMOS device leads to gain compression, extending the dynamic range of the amplifier[8]. The gate voltage of the feedback PMOS is modulated to enhance this gain compression, further extending the dynamic range. The simulated and measured large signal transimpedance characteristics are shown in Fig. 6.

The load capacitor on the first amplifier stage is used to generate a maximally flat magnitude (MFM) frequency response; i.e., the two poles closest to the origin are at ±45°. This leads to optimal small-signal settling. This capacitor is implemented as a MOS gate capacitor to achieve maximum density. The two poles from the last two stages of the voltage amplifier are set high enough to contribute little phase lag at the closed-loop unity gain frequency to insure stability.

Integration of Eq. 3.4 using the $g_m$ of the input transistor predicts an equivalent input rms noise current of 1 nA for this amplifier. Simulation predicts an equivalent input noise current of approximately 2 nA. This discrepancy is partly due to the noise factor associated with the input stage due to load noise, which has been neglected in Eq. 3.4. This is equivalent to an optical input referred noise power of 8 nW, or –51 dBm. For the minimum signal current of 9.4 nA from Table 1 the signal-to-noise ratio is 13.4 dB, which is sufficient to achieve a BER of almost $10^{-6}$ in an OOM receiver[9]. This corresponds to an optical input power of approximately 40 nW, or –44 dBm.

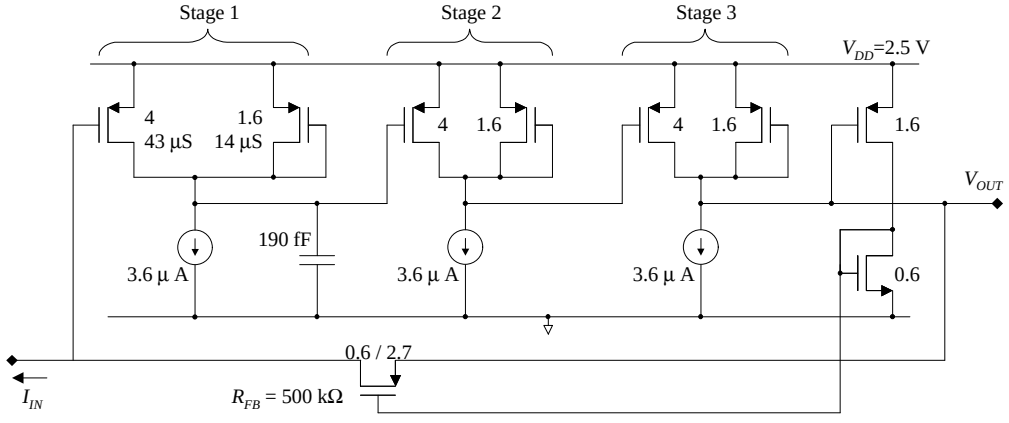
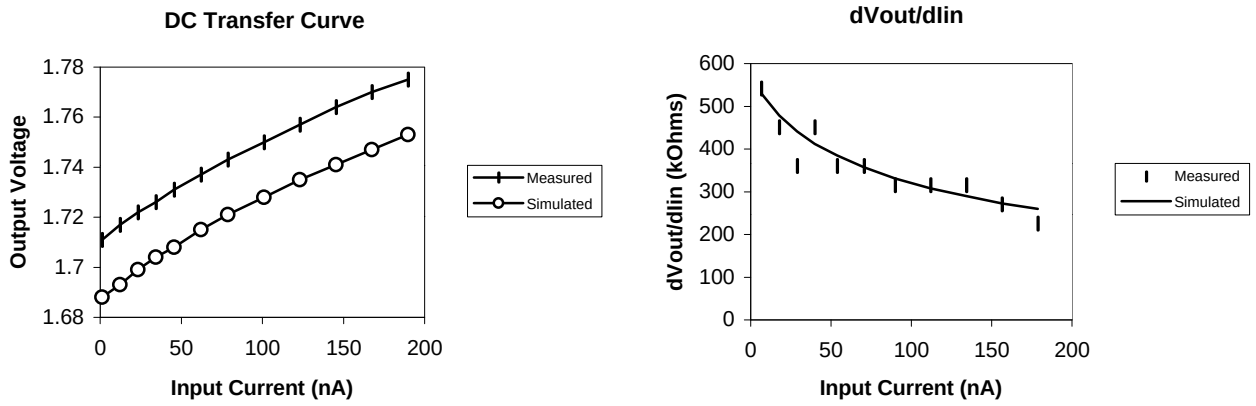



**Figure 5: Schematic of implemented transimpedance amplifier. Transistor widths are labeled in microns. All transistor lengths are 0.35 mm unless labeled otherwise.**




(a) (b)

**Figure 6: Simulated and measured (a) DC transfer characteristic and (b) incremental transimpedance for the transimpedance amplifier shown in Fig. 5. Note that positive input current refers to sinking current out of the amplifier input in these graphs.**

This transimpedance amplifier can accept a maximum input current of 5.3 μA. This limit is set by the peak output current of the final amplifier stage, which must provide all of the current flowing through $R_{FB}$. For larger input currents, the output voltage folds back as the input signal directly drives the output through $R_{FB}$. Thus the amplifier has a dynamic range of 5.3 μA/2 nA, or 68 dB. Since the signal current is directly proportional to the incident optical signal power, the dynamic range of the optical input is 34 dB.

### 4.2 High-pass filter and amplification

The high-pass filter and post amplification are combined in the high-pass amplifier shown in Fig. 7. Again, a chain of low gain amplifier stages is used to achieve wide bandwidth with minimal bias current. The –3 dB frequency for the high-pass corner is approximately equal to twice the pole frequency associated with each of the three capacitors, since there are three overlapping poles. The –3 dB frequency is 190 kHz for this circuit.

A replica bias circuit is used to generate a reference voltage to compare the amplifier output against during thresholding. Threshold voltage mismatch between neighboring transistors is the dominant source of error in generating this reference voltage. The following comparator will have a similar amount of input offset error as well. Thus, the gain is set high enough to amplify minimum strength output signals above typical threshold voltage variations to insure accurate comparison. When receiving strong signals the diode connected load devices effectively clamp the outputs and allow quick recovery from saturation.

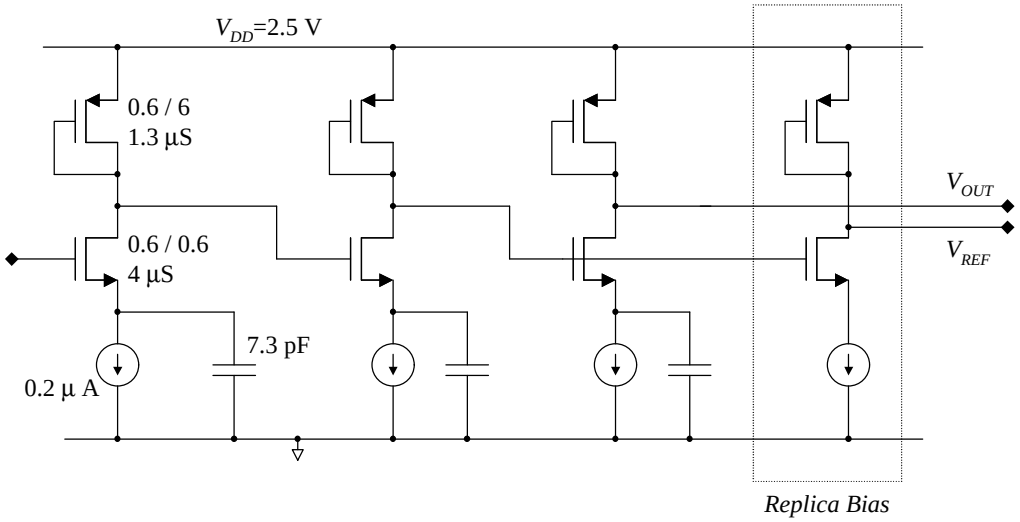



**Figure 7: Schematic of implemented high-pass amplifier and threshold reference generation. All four stages are identical except for the lack of a capacitor in the replica bias circuit.**

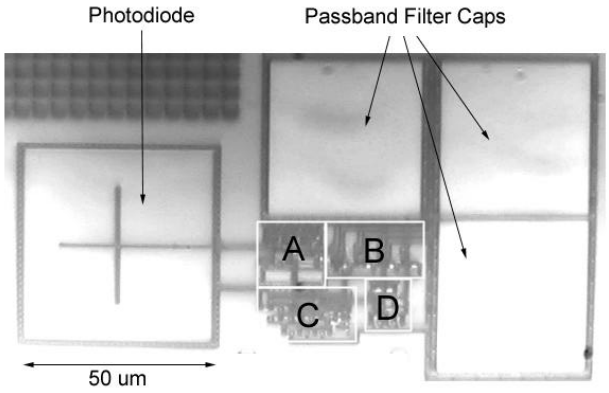



**Figure 8: Die photograph of the implemented receiver. The lettered regions are A - transimpedance amplifier, B – high-pass amplifier, C – bias circuits, and D – comparator. Not present in this photo is the top-level metal light shield, which covers the entire layout except for the photodiode.**

Since linearity is not important in this amplifier, the relatively large filter capacitors are implemented as MOS gate capacitors to achieve maximum density. The area of each capacitor is approximately 1600 $\mu m^2$.

### 4.3 Comparison

Comparison is performed with a conventional differential pair configured as a single stage operational transconductance amplifier. Since the bit rate is quite low relative to the intrinsic device performance, it is not necessary to use a high-speed comparator topology for the thresholding operation.

The transimpedance amplifier, pass-band amplifier, and comparator consume 29.3 μW, 2.1 μW, and 9.5 μW respectively for a total power consumption of 40.9 μW from a 2.5 V power supply. Bias generation consumes approximately 40 μW as well. However, this power would be averaged among many pixels in an imaging array. Power consumption for a 2.5 Mbps digital serial decoder is roughly estimated to be 1-5 μW at 2.5V if all minimum size devices are used. Thus, total power consumption should be less than 50 μW per pixel for a complete imaging receiver. A die photograph of the implemented receiver is shown in Fig. 8.

### 4.4 Performance

Preliminary tests have been performed on the complete analog signal path based on the architecture proposed in Fig 2. and fabricated as shown in the preceding sections.

When no optical signal is present the receiver output is observed to oscillate intermittently at a frequency of 1-2 MHz with intervals of several microseconds. The cause of this oscillation is still under investigation and several possibilities are being considered. Although receiver performance is severely degraded by this instability, it does correctly receive sufficiently strong optical signals, albeit at reduced bit rates. An 875 kbps psuedo-random Manchester data stream with 550 $nW_{p-p}$ optical power and 500 nW DC offset at 810 nm was received with a bit error rate of $74 \times 10^{-6}$ averaged over one minute. Fig. 9

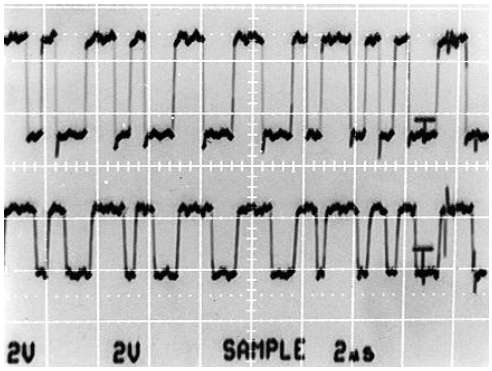



**Figure 9: Psuedo-random Manchester test sequence (top) and received serial data stream (bottom).**

shows a synthesized psuedo-random test sequence and the corresponding received serial data stream.

This received signal power is approximately one order of magnitude higher than the minimum receivable signal power calculated in Section 4.1 and specified by the application in the first line of Table 1. Since the received signal power decreases as the square of the link range, reducing the link range specification from 3 km to a little less than 1 km would compensate for this deficit in detectable signal strength. Further, since this performance deficiency is not attributed to fundamental noise constraints, it is expected that a more reliable circuit implementation could come closer to meeting the original performance specification.

## 5. RESULTS AND DISCUSSION

When line of sight is available, optical communication using collimated transmission beams and integrated imaging receivers offers many advantages over RF that make it useful for inexpensive low-power links ranging from a few meters to many kilometers. The combination of small optical diffraction limits even for millimeter scale devices and use of SDMA to handle multiple access with no special protocol allows for energy efficient, low complexity, high aggregate bandwidth communication networks. Section 2 showed that free-space optical transmission energy can be on the order of 1 fJ to 1 nJ per bit for useful scenarios including room wide LANs and distributed wireless sensors networks with possible aggregate bandwidths of several Gbps. Previous work has demonstrated such free-space optical communication links with a low bit rate, high resolution imaging array consisting of an off-the-shelf camera and real time video processing as well as at high bit rates with a low-resolution imaging array and external signal processing[2,3].

Fully integrated smart pixel arrays provide an inexpensive, low power solution to achieve high bit rates while maintaining moderately high array resolution in an imaging receiver. Such receivers can provide low cost, relatively high performance communication links for low power devices. The primary challenge of such receivers is implementing a complete asynchronous serial receiver to detect very weak input signals within the tight area and power constraints necessary to fabricate large arrays.

This work has discussed the theoretical optical performance of imaging receivers as well as the design of a small, low power smart pixel for use in such an receiver. The pixel architecture is kept as simple as possible to meet these tight area and power constraints of the imaging array. A prototype smart pixel based on this architecture has been fabricated, demonstrating that integrated imaging receivers consisting of large smart pixel arrays can be readily fabricated in a modern digital CMOS process. This single pixel implementation has been demonstrated to receive a -32.6 dBm optical signal at 875 kbps, or approximately 300 fJ/bit while consuming 60 pJ/bit from a 2.5 V power supply. However, fundamental limits based on thermal noise calculations suggest that an improved implementation can receive a 2.5 Mbps Manchester data stream with a received energy of approximately 20 fJ/bit, or 80,000 photons/bit at 830 nm, with a power consumption of 20 pJ/bit. A $16 \times 16$ imaging receiver made from these smart pixels would consume approximately 13 mW of power, allow an aggregate bandwidth in excess of 25 Mbps, and would fit on a $3 \times 3$ mm die in a 0.35 μm CMOS process.

## 6. REFERENCES


1. J. M. Kahn, R. H. Katz and K. S. J. Pister, "Mobile Networking for Smart Dust," *ACM/IEEE Intl. Conf. on Mobile Computing and Networking (MobiCom 99)*, Seattle, WA, August 17-19, 1999
2. M. Last, S. Patel, B. Fisher, C. Ezekwe, S. Hollar, B. Leibowitz and K. S. J. Pister, "Video Semaphore Decoding for Free-Space Optical Communication," *Proceedings of the SPIE - The International Society for Optical Engineering*, vol.4303 (Electronic Imaging '01), San Jose, CA, 21-26 January 2001.
3. J. M. Kahn, R.You, P. Djahani, A. G. Weisbin, Beh Kian Teik and A. Tang, "Imaging diversity receivers for high-speed infrared wireless communication," *IEEE Communications Magazine*, vol. 36, no. 12, p. 88-94, Dec. 1998.
4. IrDA Data Sheets: http://www.vishay.com/pdf/tfd_4.pdf, http://ftp.agilent.com/pub/semiconductor/ir/hsdl3201.pdf
5. H. Sankur, E. Motamedi, R. Hall, W. J. Gunning, and M. Khoshnevisan, "Fabrication of refractive microlens arrays," *Proceedings of the SPIE - The International Society for Optical Engineering*, vol.2383, (Micro-Optics/Micromechanics and Laser Scanning and Shaping, San Jose, CA, USA, 7-9 Feb. 1995.)
6. D. J. T. Heatley, "Optical Receivers," *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing (2nd Edition)*, J. Franca and Y. Tsividis, eds., Prentice Hall, Englewood Cliffs, NJ, 1994.
7. D. A. van Blerkom, Chi Fan, M. Blume and S. C. Esener, "Transimpedance receiver design optimization for smart pixel arrays," *Journal of Lightwave Technology*, vol. 16, no. 1, p. 119-26, Jan. 1998.
8. M. Ingels, G. Van Der Plas, J. Crols and M. Steyaert, "A CMOS 18 THz Omega 248 Mb/s transimpedance amplifier and 155 Mb/s LED-driver for low cost optical fiber links," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, Dec. 1994.
9. S. Benedetto, E. Biglieri, V. Castellani, *Digital Transmission Theory*, Prentice Hall, Englewood Cliffs, NJ, 1987