Static analysis of gates
I/O H L voltages
Static power
Switching speed
Universal gates

Dynamic power

Flip flops

MUX, Decoders
Resistors
SRAM
DRAM

Assume R_{off} is infinite \Rightarrow static power = 0
Is there any power dissipated? Yes

\begin{align*}
Q &= CV_{DD} \\
E_i &= QV_{DD} = CV_{DD}^2
\end{align*}

\begin{align*}
E_{bat} &= CV_{DD}^2 \\
E_{cap} &= \frac{1}{2}CV_{DD}^2 \\
\text{R}_{on} &= \text{load in } R_{on} \\
\text{f}_{0-01} &= 16 \text{ Hz}
\end{align*}

\begin{align*}
P_{average} &= \frac{E_{bat}}{T_{charge}} \\
E_{x: 10 \text{ FETs, } C_g = 1.5 \text{ F}} \\
V_{DD} &= 1 \text{ V}
\end{align*}
Story bits

Do how to set?

Last time

Simple

\[ A \rightarrow D \rightarrow Y \]
\[ \text{EN} \rightarrow \text{Q} \]
\[ \text{EN} = 0 \rightarrow \text{EN} = 1 \]

- \[ A \rightarrow D \rightarrow Y \]
- \[ Y \text{ floats} \]

Close, and sometimes good enough, but we want something that only looks at the input right on the clock edge, at \( n \text{CLK} \).

\[ \text{CLK} \]

\[ \text{D}_1 \rightarrow \text{Q}_1 \]
\[ \text{D}_2 \rightarrow \text{Q}_2 \]
\[ \text{EN}_1 \]
\[ \text{EN}_2 \]

When \( \text{CLK} \) goes high, \( \text{D}_1 \) holds the last value that was on \( \text{D}_1 \).

\( \text{Q}_2 \) loads whatever is on \( \text{Q}_1 \), and \( \text{Q}_2 \) would change if \( \text{Q}_1 \) changed, but while \( \text{CLK} \) is high. \( \text{Q}_1 \) won't change.
Edge triggered D flip flop

![Diagram of an edge triggered D flip flop]

Often drawn as

\[
\begin{align*}
\text{CLK} & \quad \text{D} \\
\text{Q} & \quad \text{Q}
\end{align*}
\]

2 input mux

\[
\begin{align*}
A & \quad B \\
0 & \quad 1
\end{align*}
\]

\[Y = \overline{A}S + BS\]

16 input mux

\[
\begin{align*}
A & \quad B & \quad C \\
0 & \quad 0 & \quad 0 \\
0 & \quad 0 & \quad 1 \\
0 & \quad 1 & \quad 0 \\
0 & \quad 1 & \quad 1 \\
1 & \quad 0 & \quad 0 \\
1 & \quad 0 & \quad 1 \\
1 & \quad 1 & \quad 0 \\
1 & \quad 1 & \quad 1
\end{align*}
\]

\[Y = \overline{S}L + \overline{L}S\]

Register file

32 registers, 8 bits each, 2 outputs

\[
\begin{align*}
\text{LDQ} \\
\text{LD1} \\
\text{LD31}
\end{align*}
\]

![Diagram of a register file]
1-of-2 decoder

<table>
<thead>
<tr>
<th>A</th>
<th>Y₀</th>
<th>Y₁</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
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<td>0</td>
<td>0</td>
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D.S. Sc

WE

<table>
<thead>
<tr>
<th>LD1</th>
<th>LD0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
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Rog 32xN

ALU - Arithmetic & logic unit

ALU-SEL

many different functions, one output (controlled by ALU-SEL)