3D-Solenoid MEMS RF Inductor Design in Standard CMOS Technology

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Abstract

A new 3-D solenoid-inductor structure that is compatible with standard CMOS technology is proposed. Simulation shows excellent area efficiency of more than 80% saving over conventional planar spiral inductor. If combined with post-micromaching, a peak quality factor greater than 10 at 30GHz can be realized.

Introduction

The rising demand for low-cost radio frequency integrated circuits (RF-IC's) has generated tremendous interest in on-chip passive components. Currently, there are several integrated resistor and capacitor options and most of these are easy to implement. Considerable effort has also gone into the design and modeling of inductor implementation, like the use of bond wires and planar spiral geometries. Although bond wires permit a high quality factor to be achieved, their inductance values are constrained and can be rather sensitive to production fluctuations. So a layout-based approach is preferred [1].

The most popular on-chip inductor structure now is spiral inductors. Spiral inductors are widely used in RF IC's design due to their nice process compatibility with standard CMOS technology [1]. Though it benefits the fabrication compatibility, this planar implementation suffers a lot from the poor quality factor (Q) and inefficient chip area usage. The later problem becomes more severe with recent fast shrinking of active devices and competitive reduction of fabrication cost. For example, the typical size of a present day communication chip is about 3mmx3mm, with 4-8 300μmx300μm inductors for voltage-controlled oscillator (VCO), power amplifier, LC filter, and impedance matching network. As there is no active device laid out under the inductors to avoid noise coupling, such an inefficient usage of as much as 10% of the total chip area is unacceptable for future scaling down technology.

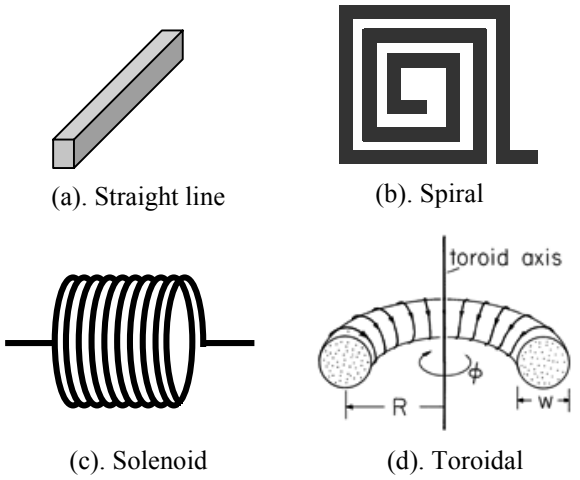
There are several previous publications to improve the area cost and Q factor, using either standard CMOS plus post micromachining [3] or customized MEMS technology to fabricate 3D structures [4][5]. In [3], the Si substrate has been etched out after the planar inductors fabricated to enhance the Q factor; still, it cost a large Si area. In [4][5], a 3D solenoid MEMS inductor is laid out on top of the normal Si to minimize the substrate capacitive coupling and inductor area; however, both are customized MEMS process and thus, the fabrication complexity and cost are significantly increased. In this work, we propose a new 3D spiral inductor structure that combines the advantages of the above work while their drawbacks are minimized.

In the following part, our presentation is organized as this: first, the theoretical studies are carried to physically under the design space for spiral inductors; second, based on those analysis, the new 3D inductor is proposed and the possible process steps are described; third, we run the electromagnetic and equivalent circuit simulation to evaluate this idea, as a comparison with conventional planar structures; finally, we conclude our work and discuss possible improvements.

Theoretical Analysis of Inductor Structure

Inductance originates from the interaction between electrical and magnetic field. Fig. 1 shows Table 1 lists the theoretical inductance value comparison between straight line, planar spiral, solenoid, and toroidal structures [7].

The self-inductance of a straight line is larger than any loop shapes, because all the mutual coupling between points of the wire are positive. However, it is not of



(a). Straight line (b). Spiral

(c). Solenoid (d). Toroidal

Fig 1. Different types of inductor design

practical interest because the line cannot be isolated from the environment, which depending on the return path, will greatly decrease the inductance values. Practically in order to well control the inductance value, some loop structures, like planar spiral, 3D solenoid and toroidal are preferred because the magnetic field is well confined.

The loop inductors typically have similar inductance values, all proportional to (l/(w+t))^3/2. Planar spiral inductor has been used in PCB and on-chip applications since it has good process compatibility. The disadvantage of the spiral inductor is large ground capacitance thus the resonant frequency is very hard to increase. Solenoid structures generally have more than twice inductance as the toroidal structure because of stronger mutual coupling. But when induced electromagnetic interference is a problem, toroidal inductors may be preferred to solenoids because of very small external magnetic field [8].

For on-chip applications, the design choice lies in the process compatibility, resonant frequency, and Q values. Solenoid structures have a significant advantage because it has lower ground capacitance, and is much more area efficient.

CMOS Compatible Solenoid Inductor Design

Based on the above theoretical analysis, a new solenoid structure is proposed as shown in Fig. 2a. It utilizes the existing multiple-level interconnect in the standard CMOS technology. Therefore, the nice process compatibility of planar inductor is maintained. The process details are listed below:

(1) The pad and top planar metal is fabricated using the last metal layer;
(2) To separate the bottom planar lines from the top line, which conducts opposite direction of current, as far as possible, the bottom lines are formed with two layer of intermediate interconnects, linked by the vias between them to realize the similar sheet resistance as that of the thicker top metal. The via linkage maintains equal voltage of these two layer of interconnects, but not conduct any current under the high frequency [9]. As shown in Fig. 2b, this treatment equivalently merges two layers into a thicker layer to reduce the resistance.
(3) The vertical lines are formed by via contacts and metal segments. As copper interconnect technology is widely used, the via uses the same copper material as normal interconnect and behaves similarly to the metal line.

Post-micromachining: After the inductor is fabricated, there is an optional post-micromachining step to remove the substrate to eliminate the substrate loss under high frequency, and thus boost the Q factor and resonance frequency. The detailed process step can include an RIE, followed by isotropic etching, as demonstrated in [3].

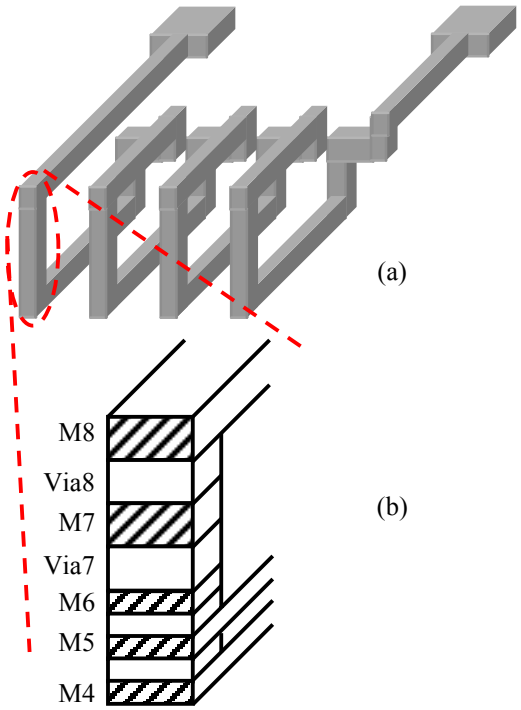


Fig 2. Solenoid inductor in standard CMOS process
(a) schematic of the inductor
(b) details of the cross-section layer. (not to scale)

As the plane where the current flows is perpendicular to the substrate, minimal capacitance coupling and maximum area efficiency are expected. The novel aspects of the new structure is summarized as follows:

- It has a similar solenoid structure as those in [4][5] to realize area efficiency;
- The 3D solenoid is built up by utilizing the multiple level interconnect structure in the standard CMOS technology;

Experimental Evaluations

To verify the advantage of this idea over conventional planar spiral inductor, we choose a typical present-day 0.18μm eight level copper technology, as shown in Fig. 3., and evaluate the performances of the new structure and the sample planar one. The 3D integrated solenoid inductor as that in Fig. 2 is designed between metal 8 and metal 5/4. The distance between them, i.e., the length of the vertical lines, are thus 6μm. Although a wider line is preferred in

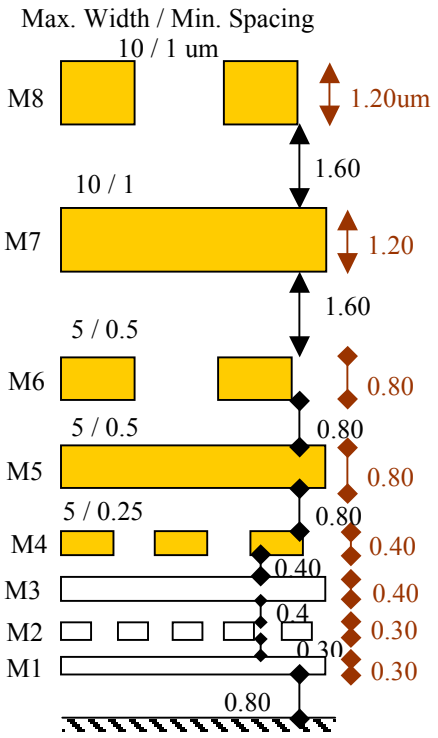


Fig 3. The metal layer structure of a standard 0.18um CMOS SOI technology. Eight level of metal (Cu). The design rule is marked on each layer.

conventional structures to reduce DC resistance, too wide line in this structure may lead to waste of magnetic field coupling. For this consideration, the width of the lines is fixed as 6μm in order to be comparable to the vertical length. Minimum spacing (=1μm) is used to increase the coupling with neighboring lines that conduct the same direction of current and thus positively contributes to the inductance. To be a fair comparison, the planar spiral inductor has the same width and space between turns. It is designed in such a way that its DC resistance is the same as that of the solenoid inductor, or in other words, they have the same total metal length. Therefore, their performances can be evaluated by the frequency characteristics of Q factor and area efficiency, which is defined by the area of minimum rectangle on the chip to include the inductor.

First, structure optimizations are performed on both structures. As we fix the resistance of them, the basic optimization variable is the number of turns (N) to maximize inductance. Raphael^{TM}, which is an EM simulator using Partial-Electrical-Element-Circuit (PEEC) theory and has excellent simulation accuracy for on-chip interconnect parasitics, is used for this optimization. Fig. 4 shows the inductance as a function of the number of turns. For planar inductor, its inductance will saturate as the current loop is getting smaller. For solenoid inductor, the best case happens when the crosssection is symmetrical [8]; however, as the number of turns is getting large, such an inductance gain becomes smaller as the distance between loops are larger. We pick up the turning point from Fig. 4 as the optimized results for solenoid to save the computational time. The results are summarized in Table xxx and will be carried for later performance comparisons.

As Table xxx shows, the 3D solenoid significantly saves the area cost. With the fixed resistance assumption, it only use 20% of the area occupied by conventional design. Thus, it is more compact and more economic for chip design. The 3D solenoid inductor has a worse inductance as a result of the smaller diameter of the current loop. This is the limitation from the current CMOS technology. For future technology generations, as the number of metal levels and the distance from top metal to the substrate will increase dramatically, we expect this limitation will decrease. Even for current technology, the Q factor may not be degraded as the capacitance is also reduced in such a structure, as shown in the next section.

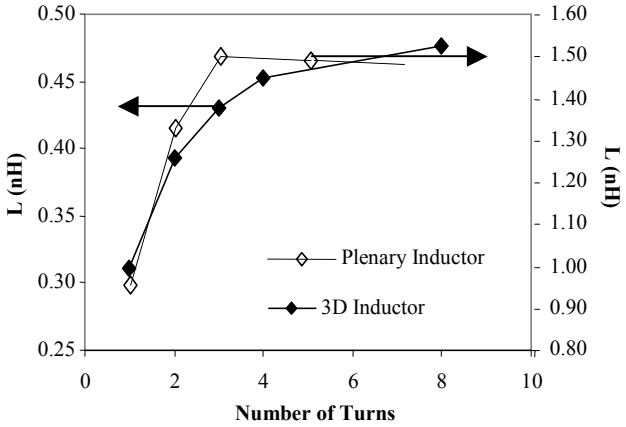


Fig 4. Inductance as a function of the number of turns. (R=3.117Ω)

Table 2. Optimization Results

	Planar Inductor	Solenoid Inductor
Rdc (Ω)	3.117	3.117
Ldc (nH)	1.5	0.452
N	3	4
w (μm)	6	6
s (μm)	1	1
Length (μm)	122	118
Area (μm^2)	14884	3186

The most critical metric to evaluate the spiral inductor is its quality factor, as defined by –Im(Y11)/Re(Y11). For simulation efficiency, an industrial common used methodology is use to extracted the Q factor: first, a single-Π equivalent model is set up to link the electrical performance to the geometrical specifications (Fig. 5) [9]; second, the substrate capacitance and resistance, along with metal-to-substrate capacitance and metal-to-metal coupling capacitance, are calculated out with analytical model in [6][9]; finally, AC resistance and inductance is extracted around the peak frequency of Q, which is estimated from the self-resonant-frequency, and used in the single-Π circuit model for SPICE simulations. The simulated Q for both planar inductor and solenoid inductor, with and without the post-micromaching to remove the substrate, are presented in Fig. 6. As the solenoid inductor has smaller inductance and capacitance, it can operate at higher frequency than the planar one: in our example, even when substrate exists, the frequency of peak Q is around 30GHz, which leaves a sufficient margin for RF frequency tuning. For the absolute Q values, the solenoid inductor has the peak values of 9.64 (@31.6GHz) and 13.0 (@41.7GHz) with and without substrate, respectively. The corresponding values in planar inductor case are 13.56 (@9.37GHz) and 21.00 (@14.8GHz), which are only slightly better than the solenoid one, and drops to zero before the solenoid reaches peak. In this sense, we are convinced that the new solenoid inductor is a better candidate for future design, besides its full compatibility with CMOS technology and great area efficiency.

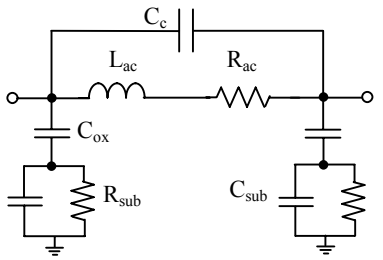


Fig 5. Single-Π circuit representation of on-chip inductor.

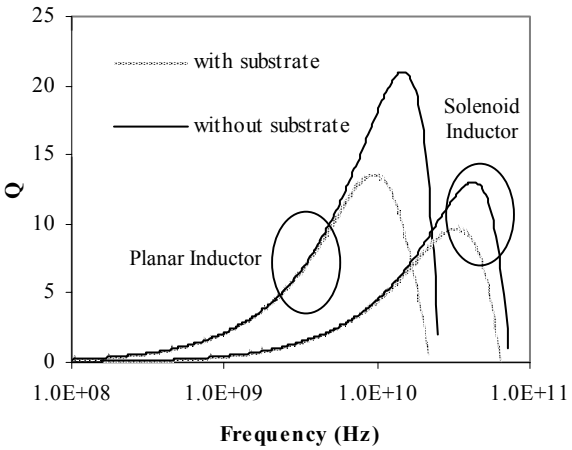


Fig 6. Q factor comparisons.

Conclusion and Discussion

In this paper we demonstrated an area-efficient, high resonance frequency 3-D on-chip inductor structure. This structure is compatible with standard CMOS technology thus is promising to be used in system integration. Because of smaller footprint and less ground capacitance, higher Q and self-resonant frequency can be realized. Also because of its 3-D geometry, the interference between inductors can be greatly reduced if placed orthogonal. The performance of this inductor is verified with Raphael simulations. Further performance improvement is possible with post-micromachining process and design optimization.

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