Multilevel Beam SOI-MEMS Fabrication and Applications

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***Abstract*—A microfabrication technology has been developed and demonstrated, which enhances the capabilities and applications of high aspect ratio silicon-on-insulator microelectromechanical systems (SOI-MEMS) by enabling additional independent degrees of freedom of operation: both upward and downward vertical pistoning motion as well as bi-directional rotation. This is accomplished by applying multiple-mask high aspect ratio etches from both the front- and back-side of the SOI device layer, forming beams at different levels. The processes utilize four masks, two for front-side and two for back-side etching. As a result, single-crystal silicon beams with four different cross-sections are fabricated, and can be combined to form many additional beam cross-sections. This provides a wide variety of possible mechanical designs that can be optimized for optical and other applications. By this methodology, unique high aspect ratio micromirror devices were demonstrated with fully isolated and accurately self-aligned vertical combdrives in the SOI device layer, with initial combfinger overlap. Examples of fabricated devices are shown with performance summaries. [886]**

***Index Terms*—Deep reactive ion etch (DRIE), inductively coupled plasma (ICP) etch, microfabrication, micromirrors, optical MEMS, self-alignment, SOI-MEMS, vertical combdrives.**

I. Introduction

THE recent focus of the MEMS world on optical applications of micromachined devices has pushed the field out of surface micromachining technology [1]–[7]. This is mainly due to the need for optically very flat and smooth structures, as well as due to the desire for large deflections and large actuation forces available using high aspect-ratio micromachining. Silicon on insulator (SOI)-based MEMS have become increasingly interesting recently as a platform for a variety of optical applications [8]–[16]. By moving to silicon-on-insulator (SOI) technology, the flatness issue is mostly ameliorated (e.g., [8]–[10]). The biggest remaining obstacle in SOI-MEMS is the inherent lack of out-of-plane motion. For a variety of optical applications in telecommunications, as well as in biomedicine, new degrees of freedom of out-of-plane motion, in addition to traditional SOI-MEMS in-plane x-y displacement, are necessary. Traditionally, SOI-MEMS actuators have provided only in-wafer-plane motion. In some cases that may be adequate for less demanding optical applications [12]. At the same time, for optical applications such as scanning micromirrors, a variety of methodologies are investigated to provide the needed additional degrees-of-freedom (DoF). Particularly of interest is providing 1DoF (or single-axis) and 2DoF (two-axis) rotation of micromirrors. There is also demand for micromirrors with independently controlled rotation and pistoning motion [7].

Of interest was to enable fabrication of vertically displaced structures to provide conversion of in-plane actuation to out-of-plane actuation and rotation, or to enable fabrication of vertical combdrives and directly convert electrostatic force to rotation. Vertically staggered SOI combdrives perform well for single-sided rotation applications [8], [9], [16] and demonstrate advantages of SOI-MEMS with respect to surface-micromachined examples of vertical comb drives [5]–[7]. However, in these previous SOI-MEMS processes, no isolation is available between combdrive fingers in either upper or lower combdrives, limiting devices to one-sided rotation. Rotation of devices is accompanied by undesired downward and lateral actuation due to the electrostatic force which is undesirable for phased-array applications. Also, the support beams are full thickness SOI device layer beams which are stiff for torsion-rotation and especially inadequate for pistoning actuation. Lastly, in previous implementations of vertical combdrives in SOI-MEMS the upper and lower comb-finger sets are separated by the thickness of insulating (buried) oxide ($\sim$ 1–2 μm), as they are etched in the device- and handle-layers of an SOI wafer, respectively. This often requires large biasing (pretilting) of devices before the comb-fingers are adequately engaged. Preengagement of vertical comb-fingers is highly desirable for well-behaved performance at lower actuation voltages [6]. Preengagement was previously demonstrated in a silicon optical scanner fabricated by eutectic bonding assembly [17]. The latter process suffers from difficult alignment between comb-fingers and utilizes metals and alloys that can reduce repeatability and reliability of device operation.

The fabrication process presented in this work is a 4-mask SOI-MEMS process that alleviates the above limitations. Namely: 1) all combfingers are fabricated in the device layer allowing isolated independently powered vertical combdrive sets. This enables independent up- or down-pistoning and bidirectional rotation; 2) comb-fingers are timed etched such that there is several microns of preengagement (overlap) allowing constant force operation from 0 V; 3) support beams can be of any desired thickness for lower voltage operation, and optimized rotation versus vertical pistoning compliance; 4) masks for etching of comb-fingers are self-aligned by a single mask; 5) structures are made in monolithic single-crystal silicon for repeatable and reliable operation. The process requires selective, high aspect ratio multilevel etching [18] of SOI wafers, using deep reactive ion etching (DRIE) [19], [20]. The timed, multilevel etch from front and back of device layer results in the various types of beams.

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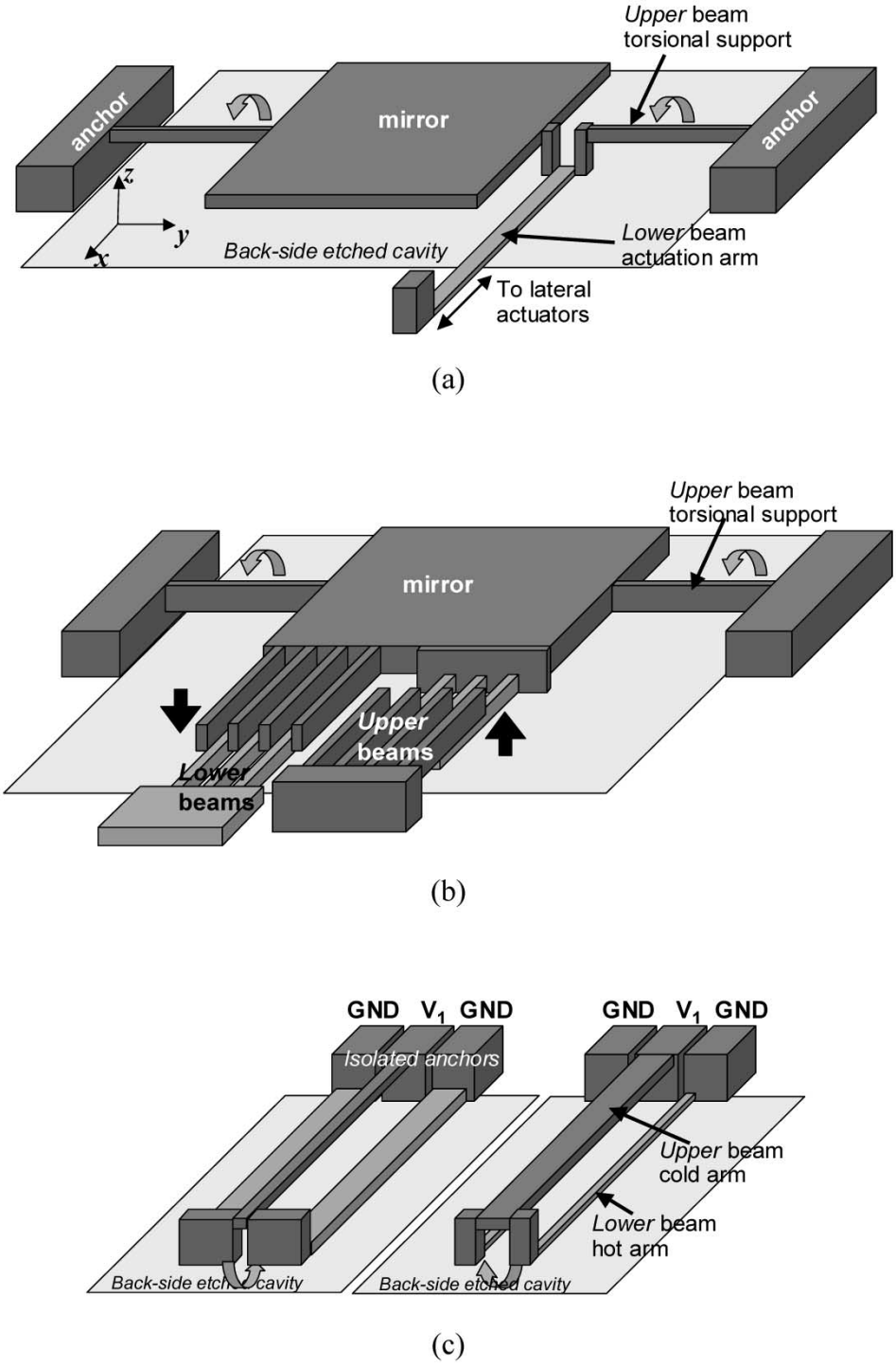

Fig. 1. Schematic of the applications of the multilevel beams concept implemented in SOI device layer: (a) vertically displaced beams are used to convert lateral motion to rotation [10] (b) vertically displaced beams in the device layer directly produce vertical actuation and rotation from electrostatic combdrive force, and (c) vertical actuation concept by thermal expansion differentials.

Section II describes in more detail the benefits of such a process and how it can be applied to enable high-performance devices. The details of fabrication steps for two distinct process flows are given in Section III with examples and discussion of resulting structures. Section IV describes three optical device examples fabricated in this technology and briefly discusses their performance.

II. Multilevel Beams in SOI Device Layer

The microfabrication methodology described here was developed to provide conversion from traditional SOI-MEMS lateral (in-plane) motion into vertical motion or rotation. Namely, in traditional SOI-MEMS devices, a DRIE step is used to etch the SOI device layer terminating on the insulating

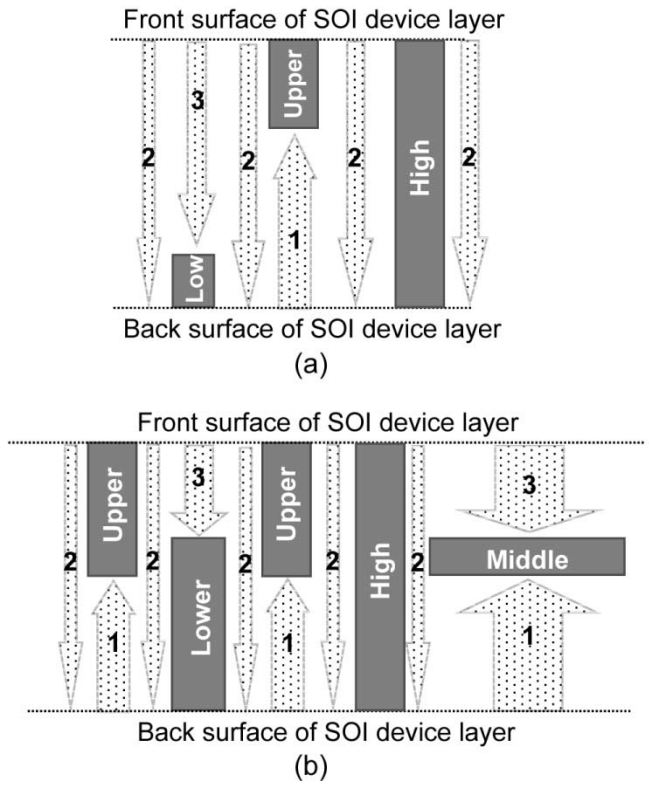

Fig. 2. Schematic of the multilevel beams concept implemented in silicon-on-insulator (SOI) device layer: (a) 3 masks can give 3 types of beams if *lower* and *upper* beam are of thickness $< 1/2$ *high* beam and (b) when *lower* and *upper* beam are thicker and overlap, a fourth beam is also given by the 3 masks, *middle* beam.

oxide layer. Due to the high-aspect ratio achievable by DRIE, many types of high-performance actuators have been developed and demonstrated with in-plane motion. Actuation from electrostatic comb drives (e.g., [10], [12]), gap-closing actuators (e.g., [21]) or thermal actuators have been demonstrated. More complex designs were developed to provide large in-plane displacements and 2-D in-plane displacements [21]. Hence, given such a well-developed infrastructure of lateral actuators, and with the new demands for advances of optical microsystems, it was of interest to provide capability for conversion of in-plane actuation to vertical actuation and/or rotation. That would enable a variety of high-performance microoptical elements.

Achieving that goal requires that the SOI-MEMS include structures that are vertically displaced from each other. If such vertically displaced single-crystal silicon (SCS) beams were available, there would be two possibilities for achieving vertical actuation and/or rotation: a) conversion of motion from adjacent lateral actuators to torque rotation by utilization of their vertically displaced sheer centers, as first proposed in [10], or b) direct vertical actuation, i.e., electrostatically, or thermally. These are illustrated in Fig. 1.

In the example of Fig. 1(a), a micromirror and its torsional support beams that allow micromirror rotation are vertically displaced above the actuation arm. Therefore if the actuation arm is laterally (in-plane) pushed or pulled by any adjacent lateral actuator, torque is applied on the support beams, which rotates

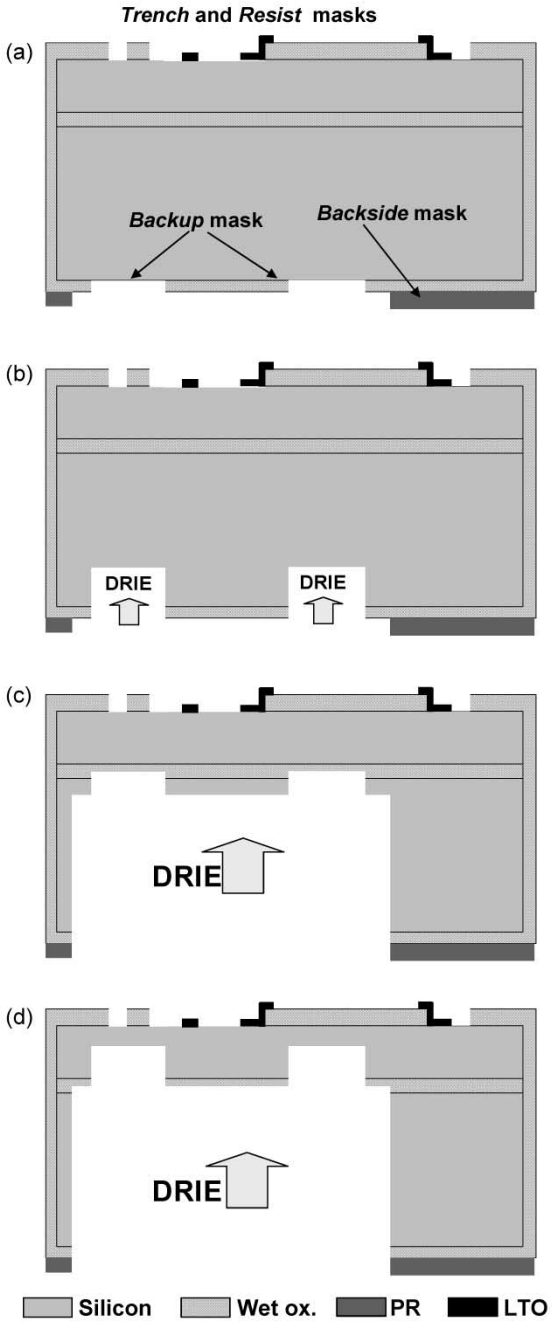

Fig. 3. After all four masks are applied to the wafer, etching of silicon with DRIE begins from the backside of the wafer. (a) wafer is ready for DRIE with two oxide masks on the front-side, an oxide *backup* mask on the backside, and the thick PR mask on the backside of the wafer (b) first backside etch is timed to $\sim 80\ \mu\mathrm{m}$ (c) after oxide etch, further backside DRIE reaches insulating oxide first in areas of *backup* mask – then oxide RIE thinks the insulating oxide, and (d) after completing backside silicon DRIE, oxide is thinned more exposing Si. Then final backside timed DRIE etches up to desired depth for *upper* beams.

the mirror structure, a concept introduced in [10]. Because the beams are micromachined at different vertical levels, they are termed *Lower* and *Upper* beams [see Fig. 1(a)]. For best performance, such a structure is connected to actuators that utilize the full thickness of the SOI device layer for best high-aspect-ratio performance, while the micromirror structure itself is made of thinner layers as shown in the illustration.

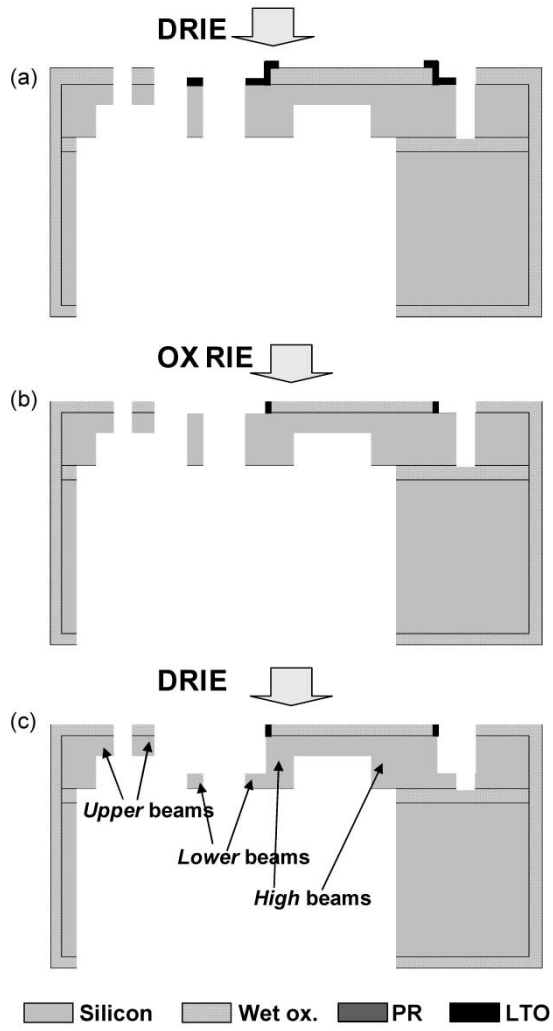

Fig. 4. After all backside etching is complete, front-side side DRIE steps begin: (a) first DRIE etches through the device layer and (b) timed plasma oxide etch removes one mask while *trench* mask remains (c) further DRIE creates the *lower* beams by stopping at desired time.

In Fig. 1(b) on the other hand, *Lower* and *Upper* silicon beams are placed closely and interleaved to create vertical combdrive structure, which converts electrostatic force directly to rotation, as previously demonstrated in [8]. However, unlike in previous work, the concept in Fig. 1(b) implies monolithic fabrication out of a single slab of single-crystal silicon (SCS) with several advantages: comb-fingers are pre-engaged giving significantly better performance at lower voltages [6], combdrives can be oriented to actuate *Up* or *Down* as illustrated in Fig. 1(b), no bonding processes affect the actual device which itself is fully monolithically fabricated, and easier access to all the electrodes in a given device from the top side, also readily integrated with silicon integrated circuits. Finally, unlike in previous processes, the comb-finger etch-masks are self-aligned to the same mask, as will be explained in detail in Section III-B2.

The examples in Fig. 1(c) show the use of vertically displaced beams to create vertical thermal actuators, by passing current between the center anchor/pad (electrode V_1) through the beams and back to the outer anchors/pads (*GND* electrode). In the left schematic of Fig. 1(c), the *Upper* beam is the hot actuator arm, expanding more than the cool *Lower* beams and thereby causing down motion. The setup in the right schematic of Fig. 1(c) has opposite action.

To achieve the above structures as illustrated conceptually in Fig. 1, we need the capability of etching a monolithic slab of SCS to different depths from the front- and back-side. This concept is illustrated in Fig. 2. In Fig. 2(a), a piece of SCS is first etched from the back-side with etch labeled "1", which is stopped before it reaches through the layer, leaving the *Upper* beam. That etch step needs to be masked from the back-side to only affect those areas aimed for *Upper* beam as shown. Then, from the front side etch "2" is done which etches the full thickness of the layer isolating the beams. Finally the third etch, "3" is done which is timed to produce *Lower* beam. It should be noted here that etch "2" and "3" therefore require separate masks from the front-side of the SCS, but those cannot be sequentially applied due to the high aspect ratio etch creating too much surface topography. Therefore, they are both applied before any etches, and removed one at a time during the process, in a methodology of multi-level etching [18]. The difference in Fig. 2(b) is the actual depth of etch "1" and "3" which in this case is such that the *Lower* and *Upper* beams overlap thickness. Therefore in places where both those masks are applied, a fourth type of beam is produced which we label *Middle* beam [see Fig. 2(b)].

III. Fabrication Process

Two distinct versions of the process have been developed and demonstrated. Both versions have certain advantages and draw-backs, and both have successfully demonstrated working microoptical elements, so they will be described in detail in this section. In all cases the aim is the same, as conceptually described above in Section II, and that is to micromachine a monolithic layer of single crystal silicon (SCS) from top- and bottom-side, such that SCS beams or structures remain fabricated at desired x-y locations in the layer, as well as at desired vertical positions z in the layer (see Fig. 1). The first version of the process has the advantage that it can be applied on any SOI wafer, i.e., it does not require actual SOI wafer preparation which includes a silicon fusion bonding step (although with no need for alignment.) The second version of the process includes necessary SOI wafer preparation by bonding which may be a drawback, but there are many advantages – the most important of which is that it provides very accurate beam alignment for high performance vertical combdrive fabrication.

A. Multilevel-Beam SOI-MEMS: Front- and Back-Side Multilevel DRIE for Three-Level Beam SOI-MEMS

The process requires four photolithography masks – three for the desired three-level beams (as conceptually described in Section II,) and one for the bulk backside etch. The latter, *Backside* mask provides dry release for devices in the SOI device layer, as well as space for rotation and vertical displacement of structures. Also, in this process it has an additional role. It is used to provide access to the backside of the SOI device layer during the fabrication process itself, so that the *Backup* mask can be applied from beneath the device layer giving as a result the *Upper* beam of Figs. 1 and 2.

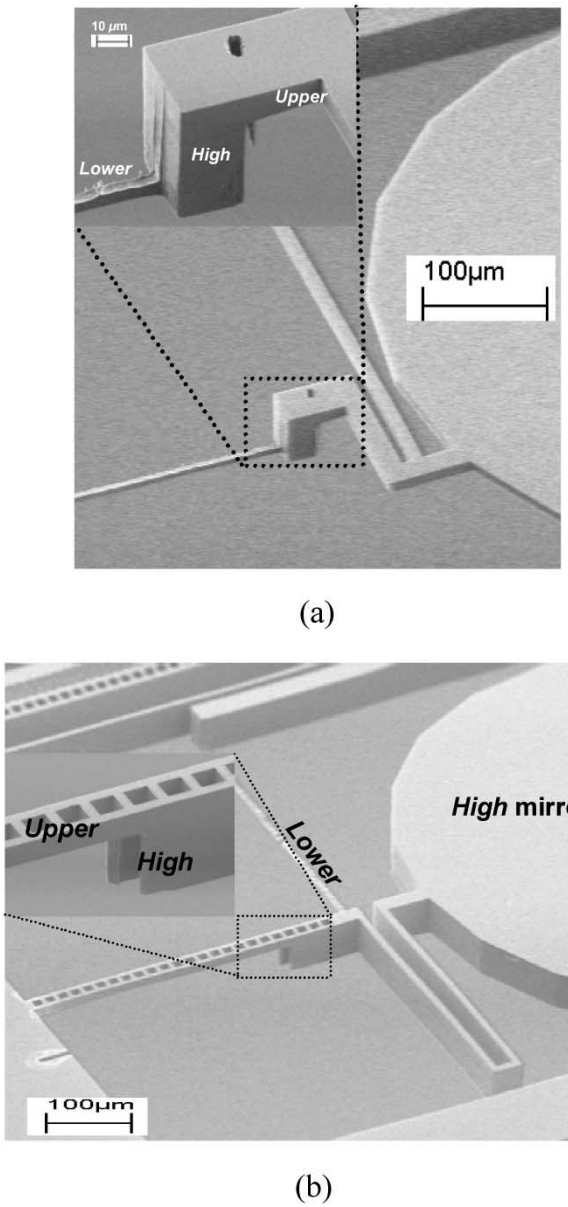

Fig. 5. SEM images of scanning micromirrors [11] fabricated as described in Section III-A: (a) beams at three different levels are fabricated, *lower*, *upper*, and *high*. The micromirror in this case is in the *upper* layer giving higher frequency of operation than full thickness of SOI device layer and (b) another micromirror which achieved 20° of optical deflection when combdrive pulls the *lower* beam achieving torque and rotating the structure around the perforated *upper* support beam.

1) SOI Wafer Preparation: The fabrication process begins with bonded and double-side polished 100 mm diameter SOI wafers with desired device layer thickness (in this work 50 μm), with a 2-μm insulating oxide layer, and with a 300-μm–thick silicon handle wafer. Each SOI wafer is either purchased or fabricated from two n-type doped prime-quality silicon wafers as follows. One wafer, intended for the SOI handle is purchased double-side-polished with accurate thickness of 300 ± 1 μm. The second wafer which is to become the device layer in the SOI wafer is n-type prime wafer, standard thickness 525 ± 25 μm, and single-side polished. A wet thermal oxide of 1 μm is grown on both wafers. Both wafers are then cleaned for 600 s in the *piranha* bath (2 l of H_2SO_4 + and 100 ml of H_2O_2) heated at 120°C, followed by de-ionized water rinsing and spin-drying. Immediately after spin-drying, the wafers' polished sides are put in contact, causing fusion pre-bonding of oxide surfaces. This is followed by an anneal with N_2 flow of 1 h at 1100 °C which makes the bond permanent creating a "sandwich" of wafers with 2 μm of thermal oxide in between.

Such wafers are then sent for grinding and polishing back from the thicker, device wafer's side, down to the total SOI wafer thickness of 353 μm (for 50 μm device-layer thickness.) When that is done, the remaining thermal oxide is stripped from wafer surfaces and the result is a double-side polished SOI wafer.

2) Preparation of Masks: The wafer first undergoes a 1.5 μm wet thermal oxidation. First mask (*Trench*) for deep front-side trenches is then etched into the oxide on the front side of the wafer, stopping on silicon. Then, 0.75 μm of low-temperature oxide (LTO) is deposited on the wafer to prepare the second front-side mask. Second mask (*Resist*) for protection of shallow front-side etches is etched into the LTO, again stopping on silicon in some areas, and stopping on the thermal oxide in other areas. Both masks are now transferred onto oxide layers on the wafer for later etching, and the front side of the wafer is thus ready for DRIE. This can be seen on the top surface schematic in Fig. 3(a). The thickness of these two oxide layers is chosen to be sufficiently thick during the DRIE steps which have roughly 1:100 selectivity of oxide etching to silicon etching.

Because the process utilizes both front-side and back-side multilevel etching, it can be done in either order: by applying DRIE to the front-side first, and then to the back-side, or vice versa. Best results are obtained by etching the backside of the wafer first, because that allows for the insulating oxide layer to be fully removed from any areas that will have suspended structures before those are actually released, preventing issues with the high compressive stress in that layer. Since back-side is to be etched first, the front side of the wafer is coated with hard-baked photoresist for protection, while back-side work is done.

On the backside of the wafer, two masks are also employed. First mask defines so called *Backup* areas, i.e., areas where device single crystal silicon (SCS) will be thinned from beneath achieving a thin, *Upper* beam of Fig. 1. This mask is etched into the thermal oxide on the backside, also depicted in schematic in Fig. 3(a). Then, fourth mask (*Backside*) is applied with thick resist, usually ~ 8 μm thick G-line resist which will provide a good mask for the long back-side DRIE, as well as oxide RIE steps. At this point the wafer is fully prepared for the many etch steps, and has all of the process masks transferred onto it, as shown in the example of Fig. 3(a), such that no further photolithography would be necessary later in the process.

3) Backside DRIE: It should be noted here that before every DRIE step, we perform a ~ 15 s plasma oxide etch at lower power than for usual oxide etching which is aimed at removing any native oxide from the silicon surface. This step also removes approximately 10–20 nm of any mask oxide which is negligible.

Backside etch process consists of multiple etches, as illustrated in Fig. 3(b)–(d). First etch is timed, to a depth of about 80 μm [see Fig. 3(b)]. Then plasma oxide etch removes the *Backup* oxide mask, such that only areas with the *Backside* mask remain protected. Second DRIE is done until the deeper trench (areas already etched to 80 μm by *Backup* mask) reaches

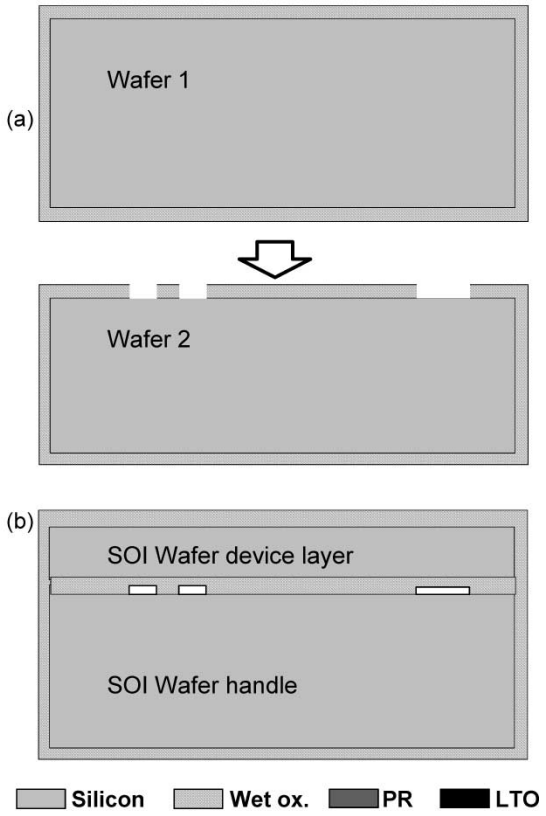

Fig. 6. Beginning steps of the fabrication process: (a) after first mask of the process (*backup*) is applied to the wet thermal oxide of wafer2, it is silicon-fusion bonded to wafer1 with no alignment needed, and (b) after grinding and polishing the bonded wafer to desired SOI device layer thickness, an SOI wafer results with buried *backup* mask.

the insulating oxide. At the point when those areas exposed by *Backup* mask have reached the oxide on the entire wafer, the rest of backside area has about 60 μm of silicon remaining as seen in Fig. 3(c). Now the *Backup* mask, originally applied to the backside of the wafer, can be transferred onto the insulating oxide to be used to undercut the SOI device layer for *Upper* beams. The insulating oxide is thinned from 2.0 μm to 0.8 μm in those areas by oxide RIE [also shown in Fig. 3(c)]. Then the remaining backside DRIE is done until all backside trenches reach the oxide, and clear the corners on the entire wafer which can require significant DRIE overetch. The wafer now goes back for oxide RIE which is timed such that the thinner oxide (initially ~ 0.8 μm) is fully etched up to the SOI device layer silicon, while other areas have about 1.0 μm remaining. Effectively, the mask, *Backup* has been transferred from the backside surface onto the insulating oxide. The final backside step shown in Fig. 3(d) is to perform the actual *Backup* DRIE into the device layer. This etch is timed to leave a desired thickness of *Upper* beams which can vary from run to run depending on designs, etc. In most cases, we etched about 35 μm of device layer silicon such that the *Upper* beam thickness would be ~ 15 μm. Last, the insulating oxide is fully removed by oxide RIE etch from the back-side.

4) Front-Side DRIE: Wafers are cleaned of any photoresist or other polymer residues and prepared for front-side DRIE by bonding their backside to a plain silicon wafer for easier handling, as well as to protect the DRIE etcher. This is done using photoresist to stick the wafers together until the completion of the process. Front-side DRIE steps are illustrated in Fig. 4, without showing the handling wafer beneath the fabricated wafer.

First DRIE step etches through the device layer [see Fig. 4(a)]. Then, oxide plasma etch on the front side thins down oxide everywhere such that the *Resist* mask is fully removed, and only *Trench* mask remains with ~ 0.7 μm thickness of wet thermal oxide [see Fig. 4(b)]. At this point, the *High* and *Upper* beams are complete. The second and final DRIE is done until the *Lower* beams are lowered to desired height, e.g., 8 μm. The final result is shown in the schematic in Fig. 4(c).

Because our designed layout positions backside etches under *all* moving structures, those structures are inherently dry-released in the process due to the earlier backside etch and insulating oxide removal. Therefore, the wafer at this point contains fully functional MEMS ready for testing. This alleviates many issues with wet releasing of structures. Mechanical and electrical tests can be performed immediately after the DRIE step. In many cases, after initial testing, DRIE was continued to further lower the *Lower* beam, since the masks had not yet been removed.

Finally, wafers are cleaned from any residual polymers by 300 W oxygen plasma and remaining oxide masks are removed in a 2-min-etch using hydrofluoric acid. This recovers smooth-polished and flat Si mirror surface as shown in Fig. 4.

5) Results: The above fabrication process was developed and utilized to fabricate laterally actuated micromirror devices [10]. To achieve the best performance, those devices require thin *Upper* and *Lower* beams, such that the micromirror torsional supports as well as the actuation arms are highly compliant. Because the beams are thin, their sheer centers are vertically separated by $\sim$ 35–40 μm, which provides a significant torque distance for the lateral actuation concept [10]. Examples of those resulting structures are shown in Fig. 5. Fig. 5(a) shows an example of a micromirror device in which the *Lower* beam is employed as the torsional support giving maximum compliance for rotation. At the same time the entire micromirror as well as the actuation arms are fabricated in the *Upper* layer. This gives the actuating arm the needed compliance as well as vertical separation from the support beam, and lowers the micromirror's mass significantly. The micromirror in Fig. 5(a) is 12.5 μm thick, and 600 μm in diameter. The thinning from the original 50 μm thickness results in approximately two-fold increase in the resonant frequency for the micromirror, while the device still maintains flatness with radius-of-curvature $(\mathrm{RoC}) > 4$ m [11]. The micromirror device in Fig. 5(b) uses the multi-level beam in reverse manner – namely, the *Upper* beam is utilized as the torsional support while the *Lower* beam is the actuating arm. This micromirror demonstrated $> 20^\circ$ of static, and $> 90^\circ$ of dynamic optical beam deflection [11].

Since our process methodology employs timed DRIE to define thicknesses of beams critical to mechanical design, we monitored the thickness variations when possible. We have found that the thickness of a certain *Upper* beam design varied across the wafer by approximately ± 1.8 μm. This is a direct, and predicted result due to $\sim$ 5% variation in etch rate over the 100 mm wafer for our DRIE recipes. The result for *Lower* beams was similar, with variation of approximately ± 2.0 μm.

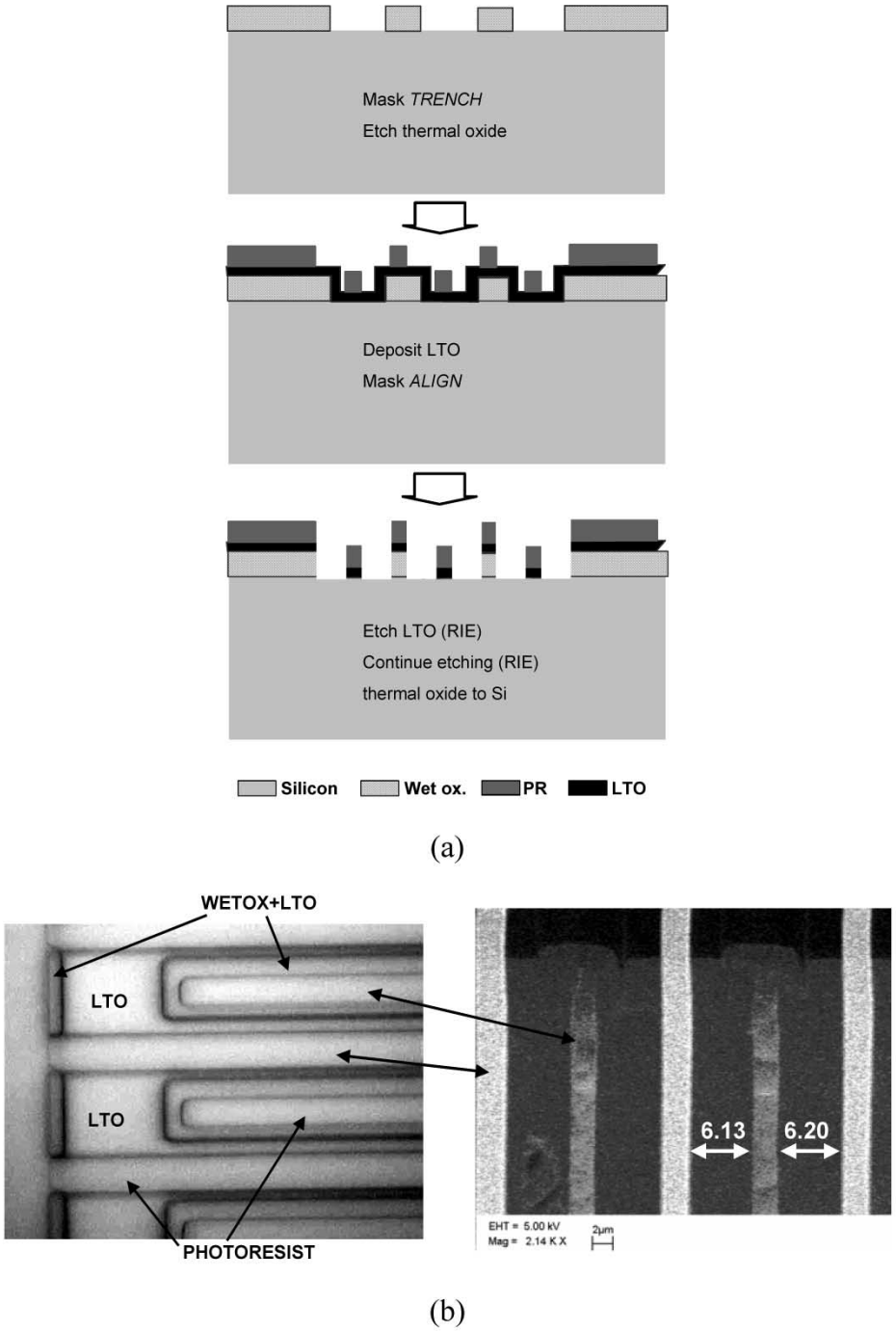

Fig. 7. Mask self-alignment methodology: (a) since top side multilevel etching requires oxide masks of two different thicknesses [10], those masks are self-aligned by growing the first mask by 2 μm, and then cutting it back with the second mask such that *upper* and *lower* fingers are both in the same (second mask). (b) microscope image on the left shows some misalignment between the *trench* mask and the *align* mask. This misalignment however disappears after the align mask is used to etch both the LTO and the thermal oxide, thus after DRIE resulting in self-aligned combfingers as shown in the SEM on the right.

B. Advanced Multilevel-Beam SOI-MEMS: Four-Level Beams and Self-Aligned Vertical Combdrive Actuators

The process in Section III-A is adequate for many applications. However, because it utilizes front-to-back alignment to produce the beams and due to any imperfections in the backside etch, it is generally not possible to align those structures with enough accuracy for implementation of high-performance vertical combdrives. To accomplish such accurate alignment and to allow the *Upper* beams to be of any feature size as available by stepper aligner available in this work, the process in Section III-A was improved to pre-embed the *Backup* mask into the insulation oxide while making the SOI wafer by bonding.

1) SOI Wafer Preparation: The preparation of the SOI wafer in this section is similar to that in the previous version of the process in Section III-A1. The significant difference which provides the many advantages to this version of the process is that the oxide on the handle wafer's side intended for bonding is patterned before the bonding as illustrated in Fig. 6. Namely, after thermal oxide of 1 μm was grown on both wafers, the

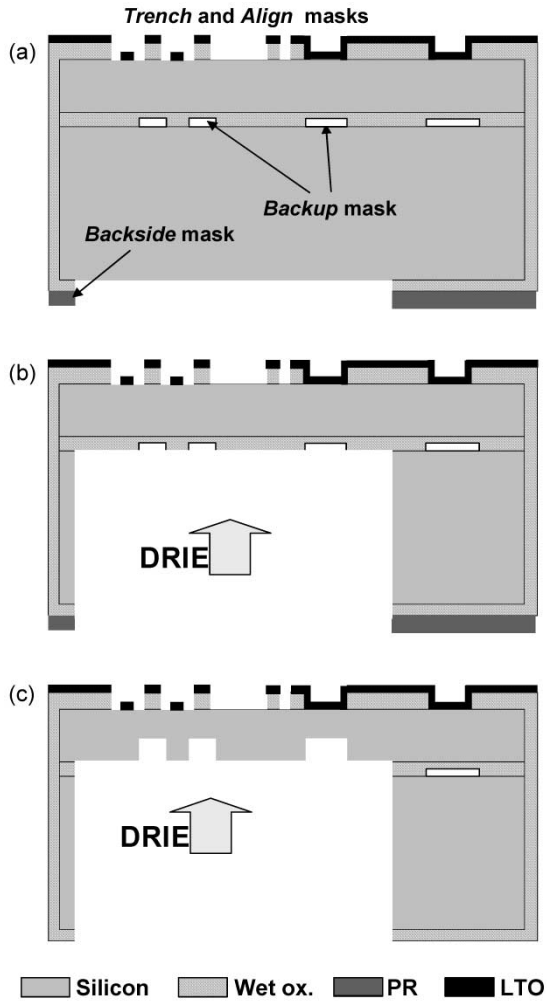

Fig. 8. After all 4 masks are applied to the wafer, etching of silicon with DRIE begins from the backside of the wafer. (a) Wafer is ready for DRIE with two oxide masks on the front-side, a thick PR mask on the backside of the wafer, and a buried oxide mask in the insulating oxide layer. (b) First backside etch removes handle wafer Si up to the insulating oxide which is followed by timed oxide etch to expose device silicon where *backup* mask was applied. (c) DRIE of device layer up to desired depth to achieve *upper* beams from the front-side.

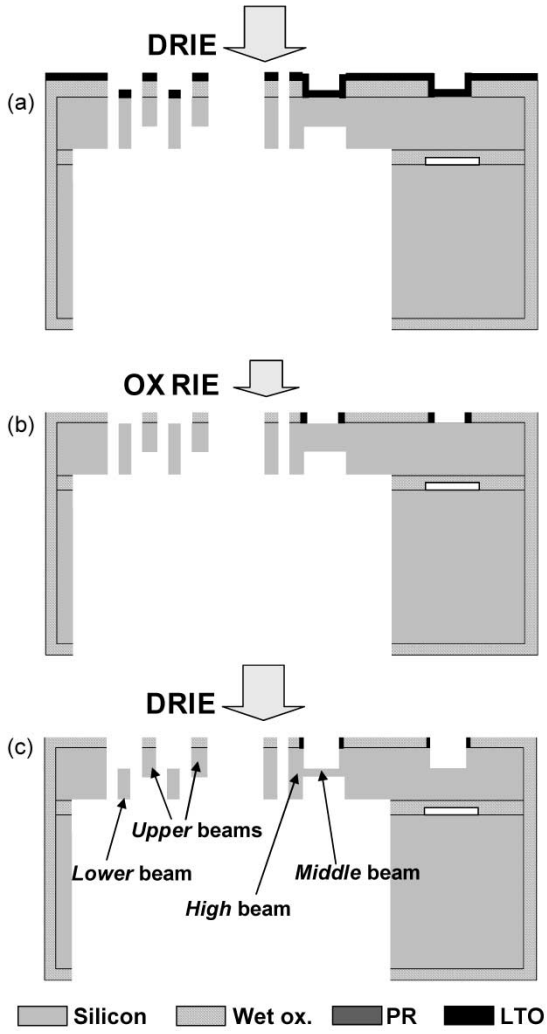

Fig. 9. After backside etches are completed, etching continues on front-side of the wafer. (a) first front-side DRIE etches deep trenches through the full thickness of device layer; (b) oxide RIE step thins oxide masks effectively exposing Si for shallow trenches; (c) second DRIE of device layer is timed to provide desired thickness of *lower* beams.

wafer intended for SOI handle (*Wafer2* in Fig. 6) is patterned with mask *Backup* and the oxide is etched down to silicon. After removing the mask and thorough cleaning of both wafers as described previously in Section III-A1, wafers are prebonded, annealed, and sent for grinding and polishing to desired device layer thickness. Finally, any surface oxides are removed in HF after the wafers are returned and wafers are re-cleaned.

2) Mask Preparation and Self-Alignment Methodology: The two front-side masks are prepared utilizing oxides of two thicknesses, as in Section III-A2. However, the mask preparation in this section is modified from Section III-A2 to provide self-alignment of both front-side masks for high-performance vertical combdrives. In addition, due to the fact that the *Backup* mask is already buried within the SOI wafer, the mask preparation process is different in that both of the front-side masks need to be aligned to that buried layer.

The SOI wafer, prepared as described in Section III-B1 above, has 0.75 μm of thermal oxide grown on it. It is coated with photoresist and exposed in the wafer stepper with a blanket mask (no mask, clear reticle) in only two chip-locations, those used for stepper alignment (wafer edges), as done in previous work [8], [9]. This photoresist exposure and a subsequent front-side DRIE step down to the insulating oxide is used to recover the alignment mark features that were included in the *Backup* mask and were buried by the bonding process. All subsequent masks can now be aligned to those features which are again visible from the surface.

Front-side mask preparation with the following self-alignment methodology (depicted in Fig. 7) is then performed. The *Trench* mask patterns the thermal oxide on the top surface [see Fig. 7(a)]. But, to provide margin for subsequent self-alignment by the *Align* mask, the features of the *Trench* mask were previously enlarged from the designed features for the beams and other structures. Namely, the CAD layouts of *High* beam, *Upper* beams, and *Middle* beams are flattened, merged and grown by 2 μm on all sides to form the *Trench* mask. The thermal oxide is etched with this mask down to Si substrate, as in Fig. 7(a). It should be noted that this step does not require critical alignment

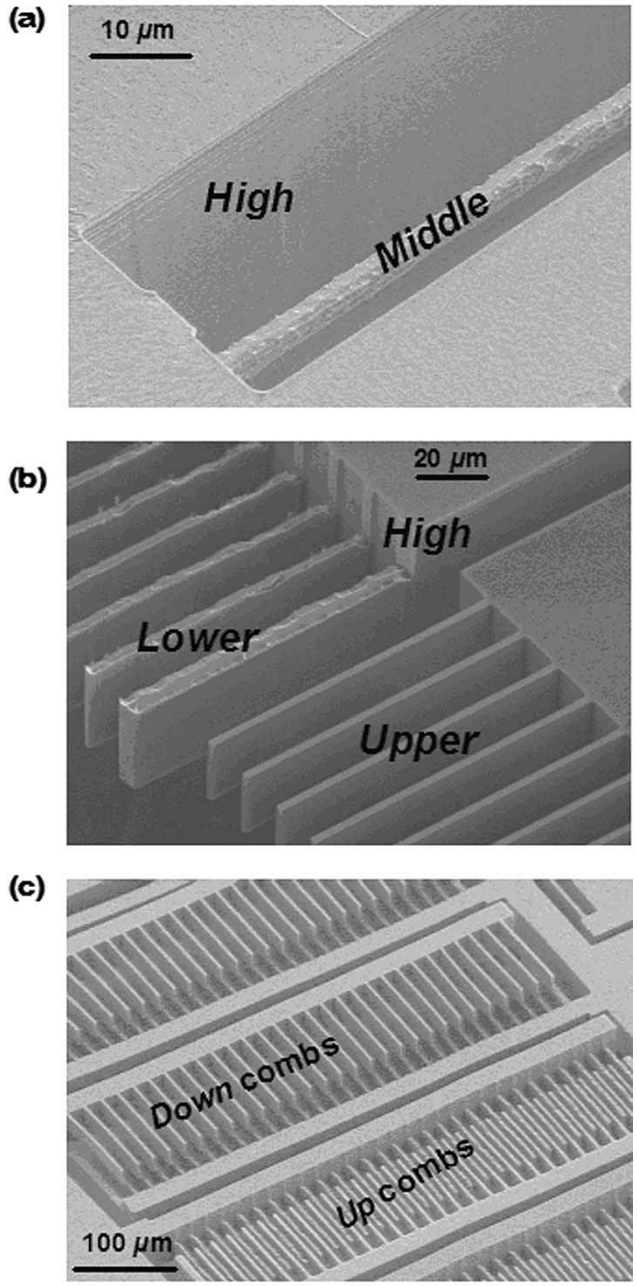

Fig. 10. SEM of resulting structures after complete fabrication described in Section III-B: (a) *middle* beam, fabricated by timed back- and front-side DRIE, and *high* beam structures around it; (b) test structure for *lower* beam comb-fingers and *upper* beam comb-fingers with comb-fingers separated; (c) actual fabricated combdrives with self-aligned *upper* and *lower* beam comb-fingers. Two independent sets are shown here, attached to the same support beam for choice of downward or upward actuation.

since the buried *Backup* layer includes a $\sim 2.0\ \mu\mathrm{m}$ margin for alignment since it is grown $2.0\ \mu\mathrm{m}$ larger than the desired final *Upper* beams.

Then, $0.75\ \mu\mathrm{m}$ of un-doped low-temperature oxide (LTO) is deposited on the wafer to prepare the second oxide front-side mask. Second mask, *Align* is applied as shown in Fig. 7(a). This mask contains the designs for *Lower* beams, as well as the designs for all other beams but this time with correct dimensions from the original layout. This step will therefore determine the final position of all structures and beams which will thereby be self-aligned to each other. As shown in Fig. 7(a), the mask is used to etch the LTO, and thermal oxide wherever exposed. Both masks are now transferred onto oxide layers on the wafer for later etching, and the front side of the wafer is thus ready for DRIE. Fig. 7(b) shows the actual microphotograph of the masks during these steps, with apparent misalignment between the *Trench* and *Align* masks of $\sim 1\ \mu\mathrm{m}$ which is subsequently removed by etching back the *Trench* mask. The resulting comb-fingers have been fabricated with near perfect alignment.

On the backside of the wafer, a single mask is employed and aligned to the front-side features. This, fourth *Backside* mask is applied with thick resist as before in Section III-A2. Because the backside of the wafer also has $1.5\ \mu\mathrm{m}$ of oxide from front-side preparation, the oxide is etched to Si substrate, and the wafer is prepared for DRIE steps as shown in Fig. 8(a).

3) Backside DRIE: Backside etch process consists of multiple etches, as illustrated in Fig. 8. First DRIE is done until the etched trench reaches the insulating oxide. This exposes the insulating oxide and the buried *Backup* mask [see Fig. 8(b)]. The insulating oxide is then thinned (by timed oxide etch) $\sim 1.2\ \mu\mathrm{m}$ which exposes the device silicon layer in areas of buried *Backup* mask [also shown in Fig. 2(c)]. The final backside DRIE step shown is to perform the actual *Backup* DRIE into the device layer. This etch is timed to leave a desired thickness of *Upper* beams which can vary from run to run depending on designs, etc. In most cases we etched about $20\ \mu\mathrm{m}$ of device layer silicon such that the remaining *Upper* beam thickness would be $\sim 30\ \mu\mathrm{m}$. Last, the insulating oxide is fully removed by oxide RIE etch from the back-side [see Fig. 8(c)].

4) Front-Side DRIE: The front-side DRIE steps are almost identical to those in Section III-A.IV. The steps are shown in Fig. 9 to better understand the formation of vertical combdrives. First DRIE etches through the device layer as shown in Fig. 9(a). Then, oxide plasma etch of $\sim 0.8\ \mu\mathrm{m}$ on the front side thins down oxide everywhere removing the thinner oxide mask [see Fig. 9(b)]. The second and final DRIE is done until the devices are done, i.e., until the *Lower* beams are lowered to desired height of $30\ \mu\mathrm{m}$. The final result is shown in the schematic in Fig. 9(c). Finally, wafers are cleaned from any residual polymers by 300 W O_2 plasma and remaining oxide masks are removed in a 120 s etch using concentrated hydrofluoric acid (49% wt. in H_2O).

5) Results: Examples of fabricated structures and beams are shown in SEM micrographs of Fig. 10. Due to the $20\ \mu\mathrm{m}$ etch of the device layer from the backside and the $20\ \mu\mathrm{m}$ etch of the layer from the front-side, the resulting *Middle* beams have average thickness of $\sim 10\ \mu\mathrm{m}$. Such a beam is shown in Fig. 10(a). Also, due to the $\sim\ 5\%$ etch rate variation across the wafer, the thicknesses of resulting *Middle* beams vary from $8\ \mu\mathrm{m}$ to $12\ \mu\mathrm{m}$. It is visible in the SEM that the surface of the beam is not smooth like the device layer surface because it is defined by timed DRIE. The smoothness can be improved with further etch recipe development. Another issue with such thin beams was the apparent overheating during the final etch steps which resulted in cases of pure isotropic etching and destruction of the beams. It is expected that etching such thermally isolated beams raises the temperature to the point where the deposition cycle of

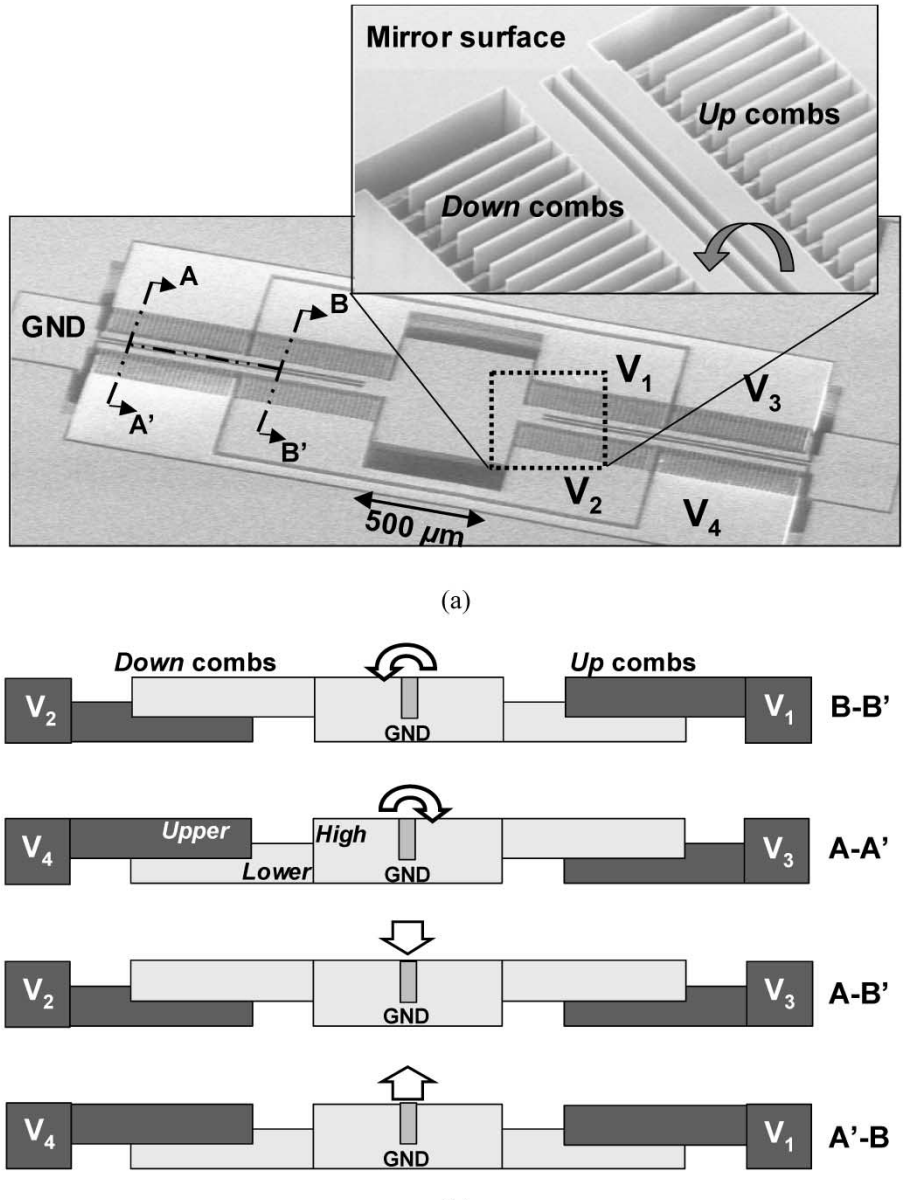

Fig. 11. Application example: fabricated and characterized micromirror with 4 isolated vertical combdrive sets for up and down piston motion as well as independent bi-directional rotation [22]: (a) SEM micrograph of the device and (b) schematic of four possible cross-sections of the device giving four types of actuation.

DRIE cannot adequately coat the structure, such that the etch cycle isotropically etches. This is being further investigated but is not the case in structures that are better thermally 'grounded' to the bulk substrate, and thereby to the He cooled chuck.

Fig. 10(b) shows resulting *Upper* and *Lower* beams, which when interleaved as in Fig. 10(c) result in densely packed preengaged vertical combdrives. The SEM in Fig. 10(c) was taken after the electron beam was first used to charge one of the combdrive sets to result in full upward actuation. Therefore, the upward actuating combdrive is fully engaged (in position of maximum capacitance) while the combfingers of the downward actuating combdrive set is fully disengaged. Thus the main goal of fully isolated upward and downward actuating self-aligned combdrive sets was achieved.

IV. Application Examples

Three application examples will be mentioned in this section to better illustrate the usefulness of the new fabrication methodology. In the first example [22] monolithic high aspect ratio silicon micromirror device was demonstrated using the proposed fabrication methodology. As seen in Fig. 11, the device is suspended by torsional support beams and is structured to enable bidirectional single-axis rotation, as well as independent up- and down-pistoning actuation. Namely, due to the capability of employing isolated combdrive sets for upward or downward actuation, the device was designed to have four possible cross sections for four modes of actuation as depicted in Fig. 11(b). By electrically activating the proper pair of electrodes, the four actuation modes have been independently demonstrated [22].

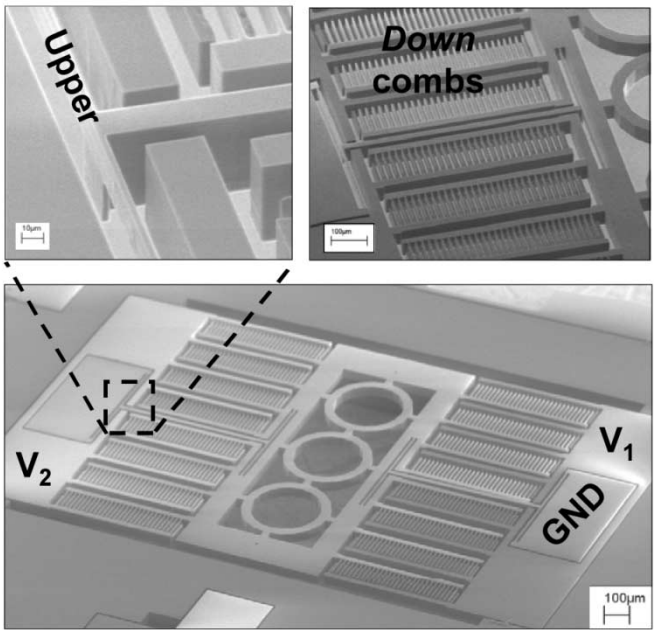

Fig. 12. Application example: fabricated and characterized vertical actuator device for miniature 3-D scanner applications with isolated vertical combdrive sets for low-voltage piston motion [23].

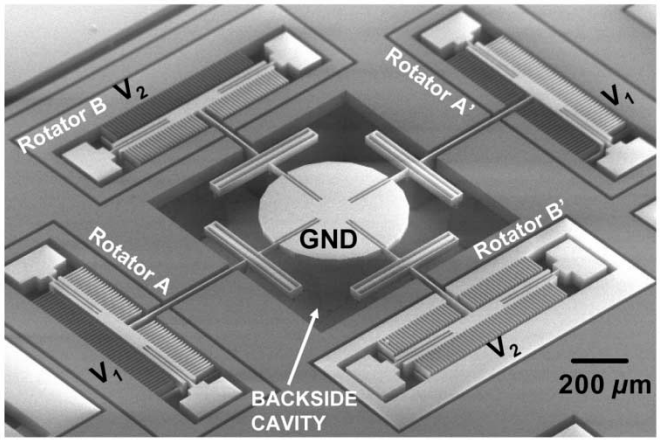

Fig. 13. Application example: SEM micrograph of a fabricated gimbal-less two-axis scanner showing the complete device with four rotating actuators, 2 degree-of-freedom linkages connecting to the center, and a 600 μm diameter micromirror, thinned from the backside [24].

Such a device with a 30 μm thick *Upper* support beam measured static optical beam deflection from -20° to 19° and bi-directional pistoning motion from -7.5 μm to 8.25 μm. In pistoning mode, the device exhibits resonance at 2619 Hz while in rotation mode at 1491 Hz. Another similar device which utilizes the highly compliant *Middle* beam (10 μm thick support beam) measured static optical beam deflection from -14° to 16° and downward pistoning motion to -12.5 μm, all at < 70 Vdc.

The second application example is a vertical actuator device for microlens actuation in three-dimensional (3-D) imaging applications [23] with emphasis on pure pistoning actuation and low-voltage operation. In the SEM micrographs of the device shown in Fig. 12, it can be seen that the device structure utilizes the self-aligned and preengaged *Upper* and *Lower* beams to form a large vertical combdrive. The suspension utilizes the *Upper* beam for compliant torsional operation which gives the low voltage of operation but also maintains good stability through the full range of actuation. Due to the availability of upward and downward pistoning, two types of devices were demonstrated. Single-directional devices (downward pistoning only) demonstrate maximum static downward displacement of 8 μm at 10 V_{dc}. Bi-directional devices demonstrate vertical actuation from -6.5 μm to $+9$ μm at max 12 V_{dc} and a vertical displacement of up to 55 μm peak-to-peak is achieved at the resonance near 400 Hz. At the full piston displacement of ~ 8 μm, the structure tilts very slightly by $< 0.034^\circ$, and compensation of that tilt using an isolated comb bank was demonstrated [23].

The final application example is a two axis, monolithic and gimbal-less micromirror scanner [24], for fast and large-angle static optical beam deflection in two axes. The main advantage of the scanners is their high frequency of operation for both axes. Namely, the actuators allow static two-axis rotation of a micromirror without the need for gimbals, or specialized isolation technologies. As seen in Fig. 13, the device is actuated by four orthogonally-arranged vertical combdrive rotators etched in the device layer of an SOI wafer, which are coupled by mechanical linkages and mechanical rotation transformers. The transformers allow larger static rotations of the micromirror from the combdrive-stroke limited rotation of the actuators, with a magnification of 1.7 $\times$ angle. In more recent devices, angle magnification of 4 $\times$ has been demonstrated. A device with a mirror diameter of 600 μm exhibits lowest resonant frequencies of 4.9 kHz and 6.52 kHz for x-axis and y-axis, respectively. The static optical deflection of the x-axis up to 9.6° and of the y-axis up to 7.2°, are achieved for < 275 Vdc. Another type of device, designed for lower-voltage operation exhibits static optical deflection about the x-axis to 10.8° and about the y-axis to 11.7°, for < 85 Vdc. In the same device, lowest resonant frequencies were 1.69 kHz for the x-axis and 2.43 kHz for the y-axis.

V. Conclusion

The combination of back- and front-side multilevel etches with new alignment strategy allows for a new genre of high aspect ratio MEMS with additional degrees of freedom such as rotation and vertical actuation. One obvious application area as demonstrated is in MEMS micromirrors, micromirror arrays, phased-arrays, and other optical devices, as demonstrated by application examples to date. Another area where we are currently exploring this methodology is RF MEMS, specifically in high performance tunable capacitor devices.

Overall, the main technical limitation to what this type of process can achieve is the aspect ratio of the DRIE tool. In other words, beam dimensions, gaps, power densities, device sizes, speeds, are essentially all derived from the approximate 20:1 aspect ratio of our current DRIE process. This has been proven to us through several generations of devices we have successfully fabricated.

However, another limitation of the process remains, which can affect device performance and what is also important, affects the uniformity among the fabricated devices. It is the dependence of the timed-etched beams on the uniformity and

precision of the timed DRIE steps, as was discussed in Sections III-A5 and III-B5. This is a drawback of the methodology, but how significant its effect is depends on the application of the technology. We have found, e.g., that while it can have a significant effect on the laterally actuated mirrors of Fig. 5, it has a very minor or no effect on the vertical comb-drive devices, if they are designed properly. The uniformity should be improved in the processing by further process development and possibly improvements in DRIE technology, but the actual effect of the uniformity on any given device remains to the device designer to determine and minimize where possible.

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