A 22nm SoC Platform Technology Featuring 3-D Tri-Gate and High-k/Metal Gate, Optimized for Ultra Low Power, High Performance and High Density SoC Applications

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Abstract

A leading edge 22nm 3-D tri-gate transistor technology has been optimized for low power SoC products for the first time. Low standby power and high voltage transistors exploiting the superior short channel control, < 65mV/dec subthreshold slope and <40mV DIBL, of the Tri-Gate architecture have been fabricated concurrently with high speed logic transistors in a single SoC chip to achieve industry leading drive currents at record low leakage levels. NMOS/PMOS Idsat=0.41/0.37mA/um at 30pA/um Ioff, 0.75V, were used to build a low standby power 380Mb SRAM capable of operating at 2.6GHz with 10pA/cell standby leakages. This technology offers mix-and-match flexibility of transistor types, high-density interconnect stacks, and RF/mixed-signal features for leadership in mobile, handheld, wireless and embedded SoC products.

Introduction

As CMOS technology scales down to 22nm, traditional planar transistor architectures [1-3] have reached a fundamental limit for the required short channel control necessary to continue scaling at the rate dictated by Moore's Law. Recently, novel 3-D Tri-Gate transistors have been proven to be capable of high volume manufacturing for high performance CPU products [4]. This paper reports, for the first time, a leading edge 22nm SoC process technology featuring 3-D Tri-Gate transistors which employs high speed logic transistors, low standby power transistors and high-voltage tolerant transistors simultaneously in a single SoC chip to support a wide range of products, including premium smart phones, tablets, netbooks, embedded systems, wireless communications, and ASIC products.

Transistor Architecture and Process Flow

This Tri-Gate-based 3-D SoC technology employs a dual-gate oxide flow to support three main transistor families, including high-speed logic (HP/SP), low-power logic (LP/ULP) and high-voltage I/O (TG) transistors, to simultaneously reduce the leakage floor to ~10 pA/um and to extend the supportable voltage ceiling to > 5V. HP/SP and LP/ULP transistors share the same low gate leakage high-k/metal-gate dielectric stack, while the TG transistors employ a hybrid SiO_2/high-k high voltage tolerant gate stack as shown in Figs. 1-2. Each transistor family supports individual electro-static tuning mechanisms to achieve the necessary device and reliability targets, and is fabricated with an overall process sequence similar to the 32nm planar SoC technology, with the exception of the addition of fin-related diffusion fabrication [3].

Table I. 22nm modular SoC transistor options and device characteristics

Transistor Type	High Speed Logic		Low Power Logic		High Voltage	
Options	High Performance (HP)	Standard Perf./ Power (SP)	Low Power (LP)	Ultra Low Power (ULP)	1.8 V	3.3 V
Vdd (Volt)	0.75 / 1	0.75 / 1	0.75 / 1	0.75/1.2	1.5/1.8/3.3	3.3 / >5
Gate Pitch (nm)	90	90	90	108	min. 180	min. 450
Lgate (nm)	30	34	34	40	min. 80	min. 280
N/PMOS Idsat/Ioff (mA/um)	1.08/ 0.91 @ 0.75 V, 100 nA/um	0.71 / 0.59 @ 0.75 V, 1 nA/um	0.41 / 0.37 @ 0.75 V 30 pA/um	0.35 / 0.33 @ 0.75 V 15 pA/um	0.92 / 0.8 @ 1.8 V 10 pA/um	1.0 / 0.85 @ 3.3 V 10 pA/um

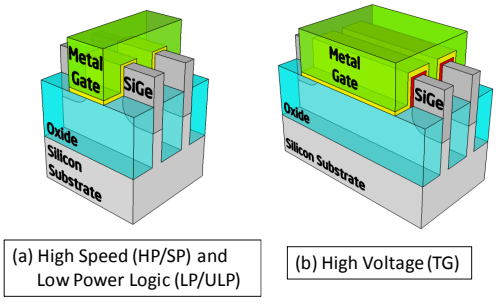

Fig. 1. 22 nm SoC Tri-Gate transistor families, including high speed logic (HP/SP), low power logic (LP/ULP) and high voltage (TG)

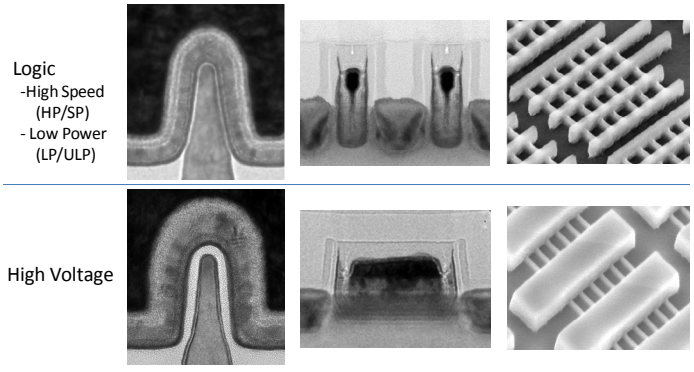

Fig. 2. Fin cut TEM, gate cut TEM, and tilted SEM of logic thin gate (top) and high-voltage thick-gate (bottom) transistors

The device characteristics of these transistors are summarized in Table I. 193nm immersion lithography is widely used at design rule sensitive process steps. Self-aligned contacts (SAC) are developed for aggressive transistor pitch scaling. High Ge-embedded epitaxial SiGe technology is used for PMOS, raised S/D technology is used in NMOS, and fifth-generation strained silicon technology is used to provide compressive and tensile stress on P-ch and N-ch devices.

Logic Transistor–High Performance (HP)/Standard (SP)

The high speed logic transistor family includes two device types – HP (High Performance) and SP (Standard Performance/Power). This family of devices is constructed on a 90nm pitch with a 30nm and 34nm gate length, and achieves subthreshold leakages ranging from 100nA/um to 1nA/um for HP and SP transistors, respectively. Both device types can be simultaneously employed with the low power logic and high voltage transistor families in a single SoC chip. The device characteristics of the high speed logic family are similar to previously reported state-of-the-art 22nm Tri-Gate technology for high performance microprocessors already in HVM production, and exhibit ~70mV/dec. subthreshold slopes and low DIBL (~50mV/V) on both NMOS and PMOS transistors [4].

Low Power Logic Transistor – LP and ULP

Low leakage (< 50pA/um) logic transistors are crucial for low standby power and always-on-always-connected circuitries in battery-powered SoC products. Traditional planar transistors require high channel doping and V_T to control subthreshold leakages; such processes are not scalable and result in severe mobility and drive current degradation, and high junction leakages. The Tri-Gate architecture alleviates these challenges with superb short channel control at minimal channel doping levels, reducing subthreshold currents and resulting in significant mobility and drive current gains over an equivalent planar architecture. Further junction leakage reduction is realized through the use of a fully depleted fin and optimized source/drain and junction engineering to minimize parasitic leakages. Figures 3 and 4 show that LP NMOS/PMOS drive currents can achieve 0.41/0.37mA/um at 30pA and 0.75V, respectively. This represents a 50% performance increase when compared to the previously reported 32nm SOC planar process, and achieves the highest reported performance to date at the given operating conditions. The ULP transistors use the same junction engineering optimizations as the LP devices, but increase the gate pitch from 90nm to 108nm and the gate length from 34nm to 40nm. The longer channel of the ULP transistor enables a lower total leakage floor and supports higher operating voltages. Figures 5 and 6 show that an outstanding subthreshold slope of < 65mV/dec. and 30-40 mV/V DIBL are achieved. A 100 mV V_T reduction has been realized in the 22nm low power transistors vs. 32nm planar devices across a wide range of transistor gate lengths as shown in Fig. 7. The junction profile has been optimized to mitigate the GIDL effect, which is the dominating source of junction leakages as shown in Fig. 8.

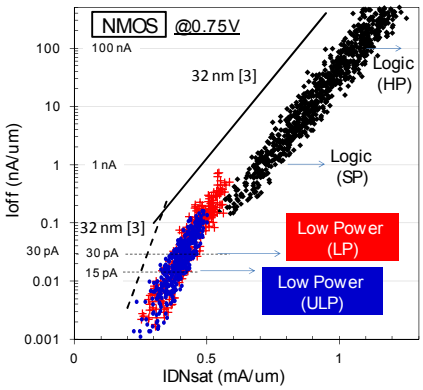

Fig. 3. NMOS Ion vs. Ioff at 0.75V showing improvements of 21%, 42% and 64% at 100nA/um (HP), 1nA/um (SP) and 30pA/um (LP), respectively

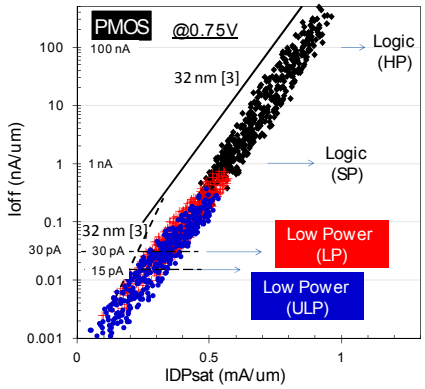

Fig. 4. PMOS Ion vs. Ioff at 0.75V showing improvements of 26%, 44% and 68% at 100nA/um (HP), 1 nA/um (SP) and 30pA/um (LP), respectively

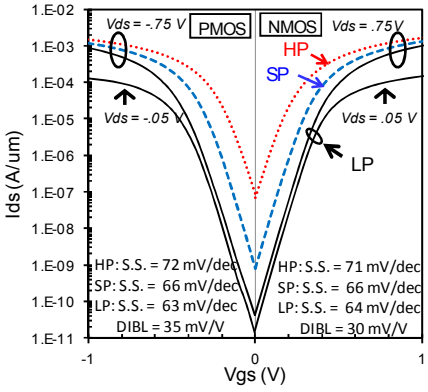

Fig. 5. Id-vs.-Vg characteristics showing steep subthreshold and low DIBL, especially for LP transistors (< 65mV/dec S.S. and < 40mV DIBL)

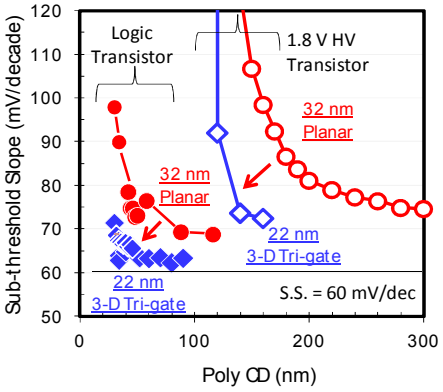

Fig. 6. Subthreshold slope comparison of 32nm planar vs. 22nm Tri-Gate for logic and 1.8V HV transistors

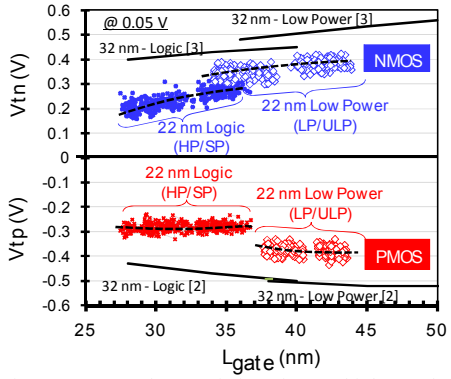

Fig. 7. Vt-vs.-L characteristics of 22nm high speed logic (HP/SP) and low power logic (LP/ULP)

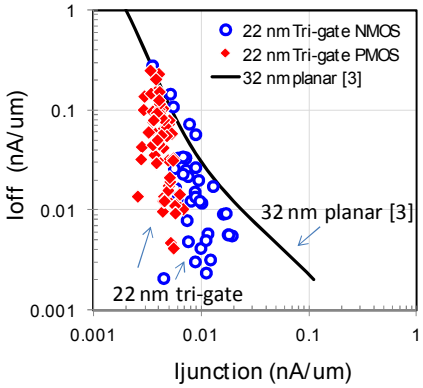

Fig. 8. Ioff vs. GIDL/Ijunction trade-off and optimization for 22nm Tri-Gate process compared to the 32nm planar

High Voltage I/O Transistors

High voltage transistors are required in an SoC process technology to support legacy high voltage I/Os, analog circuits, voltage regulation and communication designs. This technology offers native 1.8V or 3.3V transistors constructed using a composite high-k/oxide gate dielectric. The short channel control benefits of the Tri-Gate architecture also pertain to these high-voltage transistors, resulting in >50% drive current improvements and great I/O scaling over the 32nm planar counterparts (Figs. 9/10). NMOS/PMOS I/O transistor drive currents are 0.92/0.8 mA/um at 1.8 V and 10 pA/um Ioff (Table 1) - the highest reported performance for an SoC technology. The primary integration challenges for high voltage transistors are the many inward and outward edges and corners existing in the non-planar technology, but extensive integration optimizations have resolved these issues to achieve the good TDDB, hot carrier, and BTI reliability results shown in Figs. 11-13.

Interconnects

This technology offers the flexibility of mixing-and-matching eight to eleven layers of low-k (LK) and ultra low-k (ULK) carbon-doped oxide (CDO) ILD stacks, as shown in Fig. 14, for different SoC product segments. M1 employs double patterning to enable tight pitch and complex layouts. All other metal layers are fabricated with cost effective single patterning lithography. The tightest pitch layers are patterned with the self-aligned via (SAV) process with a sacrificial hard mask [5]. A 6um thick top metal layer is used for on-die power distribution and spiral inductors (Fig. 15). Density focused products employ up to six layers of minimum pitch (80nm) metal layers, while RC driven products are optimized for more relaxed pitcher layers (Table 2 and Fig. 16).

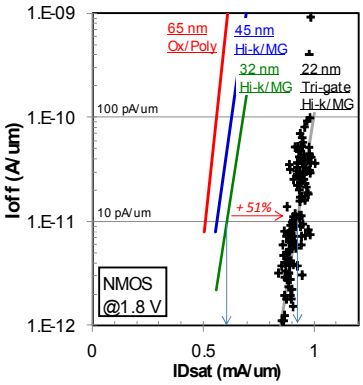

Fig. 9. NMOS high voltage transistor drive current trend showing 51% performance improvement over 32nm

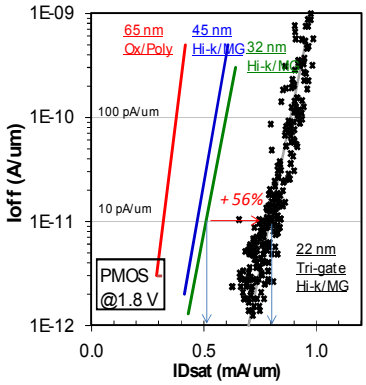

Fig. 10. PMOS high voltage transistor drive current trend showing 56% performance improvement over 32 nm

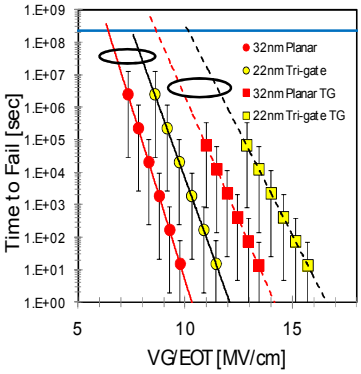

Fig. 11. PMOS logic and HV I/O gate dielectrics TDDB comparison – 32 nm vs. 22 nm

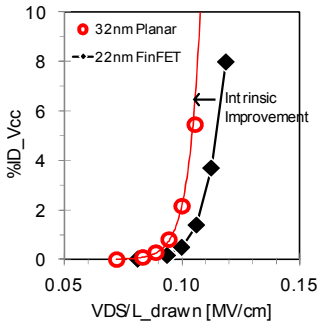

Fig. 12. NMOS HV I/O transistor hot carrier effect – 32 nm vs. 22 nm

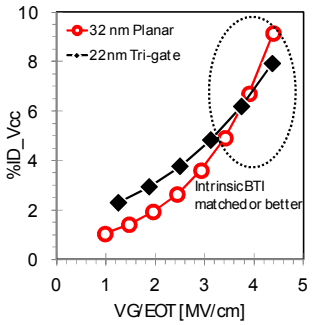

Fig. 13. PMOS HV I/O transistor NBTI comparison – 32 nm vs. 22 nm

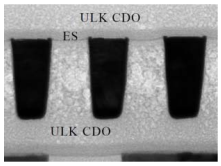

Fig. 14. Ultra low k (ULK) carbon-doped oxide (CDO) employed in the tight pitch interconnect layers of this technology

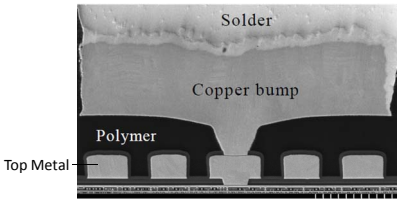

Fig. 15. Thick top metal, copper bump and solder joint developed for the 22 nm node process

Table 2. 22 nm interconnect pitches

Layer	Pitch (nm)	Process	Dielectric Materials	CPU	SoC
Fin	60	-	-	Fin	Fin
Contact	90	SAC	-	Contact	Contact
M1	90	SAV	ULK CDO	M1	M1
MT - 1X	80	SAV	ULK CDO	M2/M3	2-6 layers
MT – 1.4x	112	SAV	ULK CDO	M4	Semi-global
MT – 2x	160	SAV	ULK CDO	M5	Semi-global
MT – 3x	240	SAV	ULK CDO	M6	Global Routing
MT – 4x	320 360	Via First	LK CDO	M7/8	Global Routing
MT - TOP	14 um	Plate Up	Polymer	M9	Top Metal

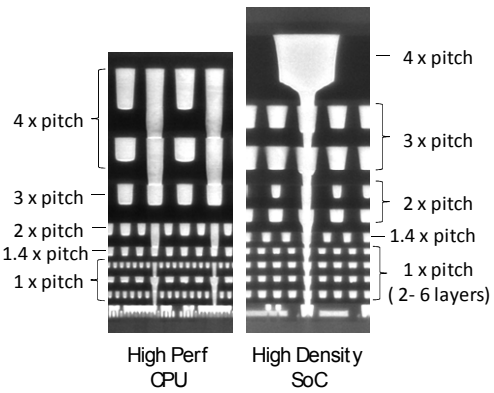

Fig.16. Interconnect architecture comparison of 22 nm CPU and SoC technologies

Analog/Mixed Signals and Passives

A full suite of analog and mixed signal features are offered in this technology to meet the divergent SoC product needs. Gm-Rout metrics are significantly improved due to improved channel control as shown in Fig. 17, and is critical for enabling analog features to maintain the pace of CMOS digital technology scaling. Precision resistors achieve < 15% variation for a large population of sites (Fig. 18). In addition to the standard device and metal finger capacitor offerings, a new MIMCAP architecture is supported in this technology to provide an additional high density capacitance source (Fig. 19). Spiral inductors are constructed on a thick metal (TM) layer to support inductive SoC circuitries (Fig. 20).

Low Voltage and Low Standby Power SRAM

A rich collection of single and dual-port SRAMs are offered in this technology, Fig. 21. Single-port SRAM options include high density/ low leakage (0.092um^2, HDC), low voltage (0.108um^2. LVC) and high performance (0.130um^2, HPC) bit cells [6]. Dual-port SRAM options include synchronous and asynchronous cell types. Exploiting the supreme short channel control of the Tri-Gate technology, a > 4 x improvement has achieved at 1 V standby benchmark conditions for HDC LP SRAM, as shown in Fig. 22. The SRAM operating frequencies have improved to 4.6, 3.5 and 2.6 GHz at 1V for HP, SP and LP processes as shown in Fig. 23. Low Vccmin and high SRAM yields have been achieved on 380 Mb SRAM, equivalent to the CPU technology.

References

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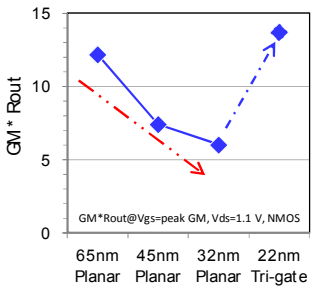

Fig. 17. Analog device characteristics g_m*Rout trend showing significant improvement from planar (65nm- 32nm) to Tri-Gate (22nm)

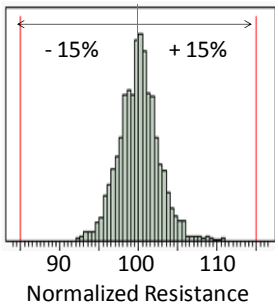

Fig. 18. A precision resistor is offered with well-controlled resistance distribution

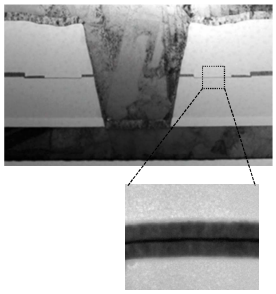

Fig. 19. MIMCAP developed for 22nm Tri-Gate process [4]

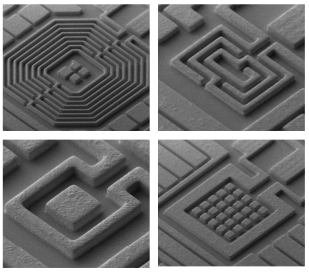

Fig. 20. A full collection of high quality factor spiral inductors are offered for mixed-signal and communication applications

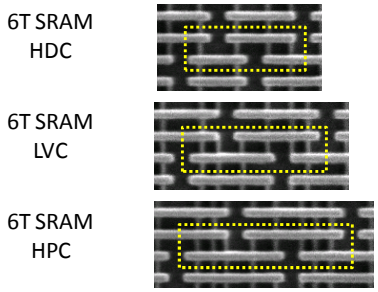

Fig. 21. Selected SRAM options provided in this SoC technology, including high density /low leakage (HDC), low voltage (LVC), high performance (HPC) and dual port

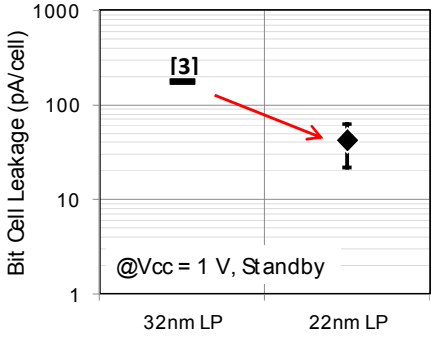

Fig. 22. HDC SRAM bit cell standby leakages comparison at 1 V showing 4-5x improvement ver 32 nm planar LP SRAM [3] via low standby power Tri-Gate process

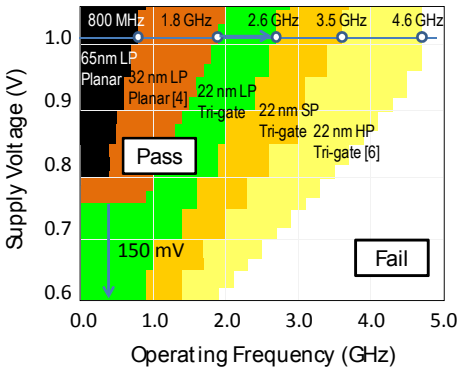

Fig. 23. SRAM operating frequency Schmoo plot of LVC cells showing 40% frequency (2.6GHz vs. 1.8GHz at 1V) or 150mV Vmin reduction over 32nm planar LP SRAM