EE147/247A Final 2021 NAME____________________

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1) [4] List four different silicon etchants:
   a. isotropic liquid etchant
      HNA
   b. anisotropic liquid etchant
      KOH
   c. gas phase etchant
      XeF_2
   d. a gas used in plasma etching
      SF_6

2) [4] List four different ways that you can get silicon dioxide on a wafer
   a. Two high temperature conformal ways
      Thermal w/ O_2 or H_2O, HTO
   b. On top of aluminum
      PSG, LTO, PECVD, ALD
   c. Lowest temperature
      PECVD ALD

3) [3] Write a formula that will let you calculate the angle between different <111> family directions in a cubic crystal. How many different angles are there (and how do you know?).

   $111, \bar{1}11, \bar{1}\bar{1}1, \bar{1}\bar{1}\bar{1}$ ex: $|111||\bar{1}\bar{1}\bar{1}| \cos\theta = -3 \Rightarrow \theta = 0°$

   3 angles

4) [2] Are the {111} sidewalls of a KOH-etched self-terminated etch pit at exactly 54.74 degrees from the surface? Why, or why not?

   No. 111 etch rate is non-zero

5) [2] If you are putting down a metal and want it to cover some existing steps on the wafer that are comparable to the thickness of metal you want to deposit, should you use sputtering or evaporation? Why? Sputter for better step coverage

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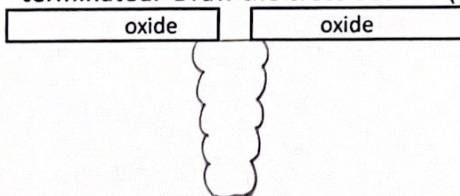
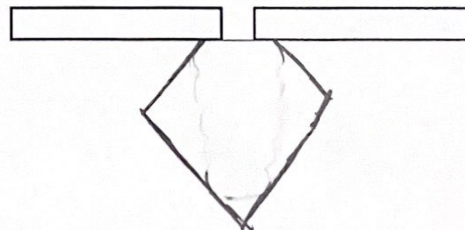
6) [2] If you are putting down a metal and patterning it using liftoff, should you use sputtering or evaporation? Why?

   Evaporation because you want poor step coverage

7) [4] A circular hole 1um in diameter is etched into a 1um thick oxide on a bare silicon wafer. This is then used as a mask for a 5 um DRIE etch with 1um etch per pulse. Carefully draw the cross-section (below left). After the DRIE etch, the wafer is dropped into a KOH etch and left there until the etch has self-terminated. Draw the cross-section (below right).





8) [7] You are developing a new structural material for MEMS and make arrays of cantilevers and clamped/clamped beams out of a 1um thick film.

   a. [2] You observe that the 100 um cantilevers have curled up by 1um. How much curling would you expect in 300um long cantilevers? 9μm

   b. [1] You change the process somewhat, and find that the cantilevers now curl down. Is your film more tensile on top than on bottom, or the other way around?

      tensile on bottom

   c. [2] You change the process again, and find that cantilevers are flat, but your clamped-clamped beams look funny under the microscope. For any beam less than 1 mm long, they all look the same uniform color. But at L=1mm or more, there are dark and light bands along the length of the cantilever. What is going on? compressive stress buckling

   d. [2] You do another run with the new low-gradient process parameters, but reduce the thickness of the film to 0.5um. At what length do you expect to see cantilevers that are showing weird dark and light bands along the length?

      $\sigma_{crit} \sim \frac{a^2}{L^2}$ $L \sim a$ $\frac{1}{2}$ of 1mm. 500μm

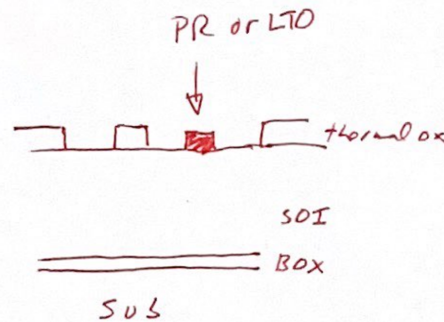
9) [8] In Milanovic's paper on multi-level SOI beams

   a. [2] How did he get a patterned SiO2 layer as the buried oxide in an SOI wafer?

      pattern oxide before wafer bond (1, 1)

   b. [6] How did he get beams that were both the full thickness of the device layer, and "low" beams that were only a fraction of the device layer thickness, but still attached to the buried oxide? Using just two frontside masks (ignore any backside processing) list the process steps and draw a cross-section (that will yield both beams) just before the first DRIE etch. Label all materials. 3 3

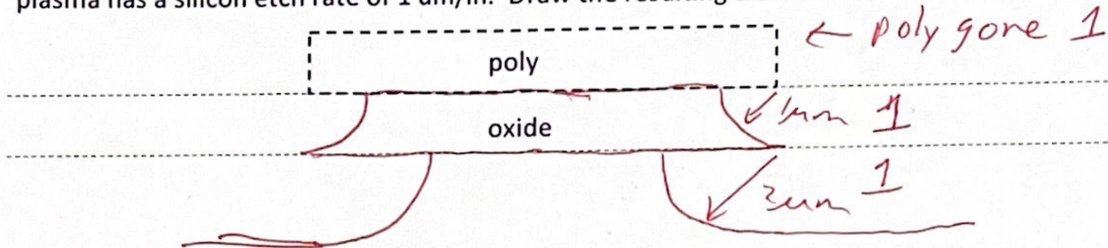
thermal oxide/TRENCH
LTO / RESIST
DRIE timed ½ or less
strip resist or etch LTO
DRIE remaining



10) [15] A 1 um thick thermal oxide is grown on a silicon wafer. 1um of LPCVD polysilicon is deposited on the wafer and patterned with RIE to form a 6um diameter circle. The etch rate of the oxide is 1um/min in 49% HF.

a. [1] How long would it take to release the circle in 49% HF? 3 min

b. [3] The wafer is etched in 49% HF for 1 minute, and then in an SF6 plasma for two minutes. The plasma has a silicon etch rate of 1 um/in. Draw the resulting cross-section

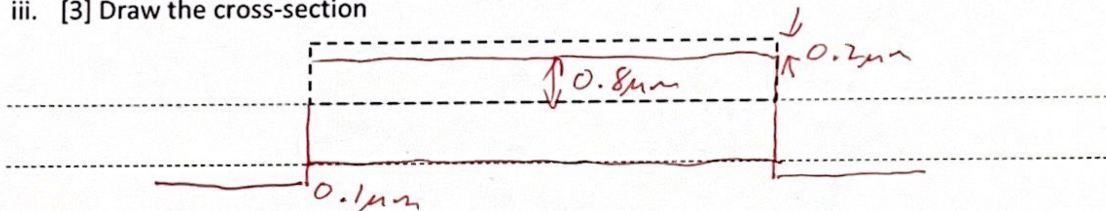


c. [6] A similar starting wafer (with the oxide and polysilicon circle) is etched in an unmasked oxide RIE for 5 minutes. The RIE etch rate is 0.4 um/min, and the selectivity to silicon is 10:1.

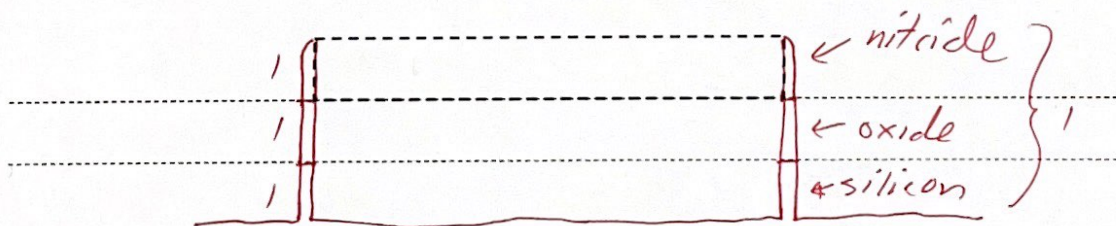
i. [1] How much exposed oxide will remain after this etch? none

ii. [2] How thick will the polysilicon be after this etch? $1 - 2(\frac{1}{10}) = 0.8$

iii. [3] Draw the cross-section



d. [4] A similar starting wafer (with the oxide and polysilicon circle) gets a 0.1um LPCVD nitride deposition, followed by an unmasked 0.1um nitride RIE. This is followed by an unmasked 1um silicon RIE, an unmasked 1um oxide RIE, and an unmasked 1um silicon RIE. Draw the resulting cross-section and label the materials.



e. [1] Why might someone want to do the previous process?

Finfets

sub-lithographic lines

12

11) [~~10~~] You have an accelerometer with ω_n=10^4 rad/s, K=100 N/m, and b=10^{-5} Ns/m at atmospheric pressure.

2 a. What is the quality factor? $\frac{K}{b\omega_n} = \frac{100}{10^{-1}} = 10^3$

2 b. Calculate the average thermal noise displacement of the spring.

$\frac{1}{2}K\bar{x}_n^2 = \frac{1}{2}k_BT$ $\bar{x}_n = \sqrt{\frac{4\times10^{-21}}{10^2}} = \sqrt{40}\,pm \approx 6\,pm$

2 c. What is the power spectral density of the thermal noise due to damping?

$\frac{\bar{P}_N}{\Delta f} = 4k_BT = 16\times10^{-21}\,\frac{W}{Hz}$

2 d. Calculate the average thermal noise force on the resonator, F_N, in a 1Hz bandwidth.

$\bar{F}_n = \sqrt{4k_BTb\Delta f} = \sqrt{(16\times10^{-21})(10^{-5})(1)} = 4\times10^{-13}\,N$

e. What is the average displacement due to thermal noise in a 1Hz bandwidth at atmospheric pressure:

2 i. near DC $\frac{4\times10^{-13}\,N}{10^2\,N/m} = 4\times10^{-15}\,m$

1 ii. at resonance

$Q\,\bar{x}_{DC} = 4\times10^{-12}\,m$

1 iii. at 10 times the resonant frequency

$\frac{x_{DC}}{10^2} = 4\times10^{-17}\,m$

12) [~~10~~] A piezoresistive acceleration sensor has a sensitivity of 1V per gravity. The piezoresistors have a combined effective impedance of 10 Ω. Assuming no other noise sources,

8

2 a. what is the voltage noise on the piezoresistors in a 1 Hz bandwidth at room temperature?

$0.4\frac{nV}{\sqrt{Hz}}\sqrt{1} = 0.4\,nV$

2 b. What is the voltage noise on the piezoresistors in a 100 Hz bandwidth at room temperature?

$4\,nV$

2 c. What is the noise-equivalent acceleration in a 100 Hz bandwidth at room temperature?

$\frac{4\,nV}{1\,V/g} = 4\,ng$

2 d. If the temperature increases by -60 C to roughly -40C, what is the fractional change in the absolute temperature, and what is the resulting fractional change in the noise-equivalent acceleration?

$\frac{\Delta T}{T} = -20\%$ $a_n \sim \sqrt{T}$ so 10% less

13) [10] We looked at several different CMOS-MEMS processes this semester. For three different processes (your choice which) identify the structural material(s), the sacrificial material(s), and the etchant(s) used to release the structures.

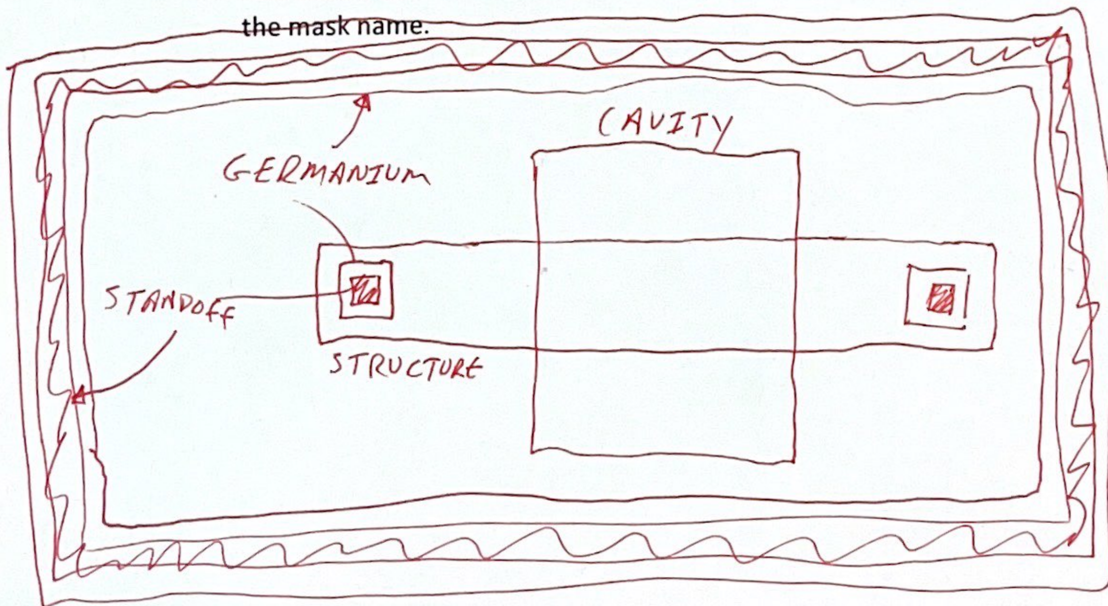
Structural material(s)	Sacrificial material(s)	Etchant(s)
all dielectrics, metals	silicon	KOH or isotropic plasma after RIE oxide
all dielectrics, metals	aluminum wiring silicon substrate	H_2O_2 XeF_2
aluminum	dielectrics/oxide	vapor HF

14) [10] In the Nasiri process,

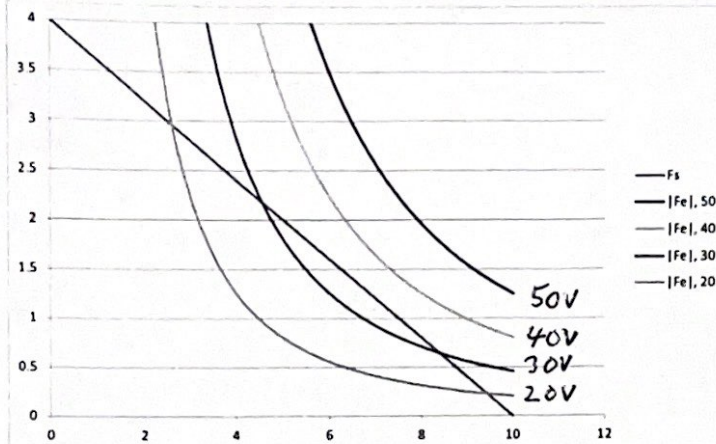
a. list the names of the masks used **on the MEMS wafer(s)** and explain the purpose of each mask. You can ignore the alignment mask, CMOS masks, and any optional masks for this whole problem.

2 CAVITY - "release" etch
1 STANDOFF - mechanical/electrical connection to CMOS
2 STRUCTURE/SOI - structures
1 GERMANIUM - eutectic bond

b. If we want a resistor (simple beam) suspended inside a gas-filled cavity with both ends electrically connected to the CMOS chip, draw the layout. Label every piece of geometry with the mask name.



15) [10] The figure below shows the spring force and the magnitude of the electrostatic force vs. deflection for a gap-closing relay actuator running at four different applied voltages. The horizontal axis is in microns, the vertical is in microNewtons. The initial gap is 10um, and there is a gap stop at 4 um.



a. [1] Estimate the pull-in voltage, with some confidence interval (e.g. 200V +/-3V)

32-38V

b. [1] Estimate the pull-out voltage, with some confidence interval

25-29V

c. [1] Estimate the deflection with 20 V applied.

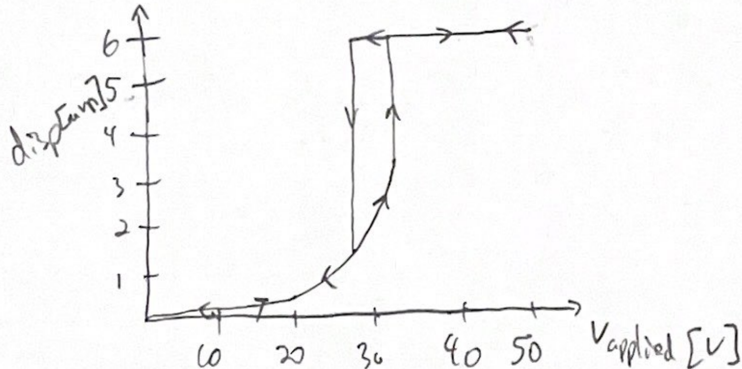
0.2um-0.8um

d. [3] Estimate the force (electrostatic minus spring force) on the relay contacts if 50V is applied. You should be able to do this very accurately if you think carefully.

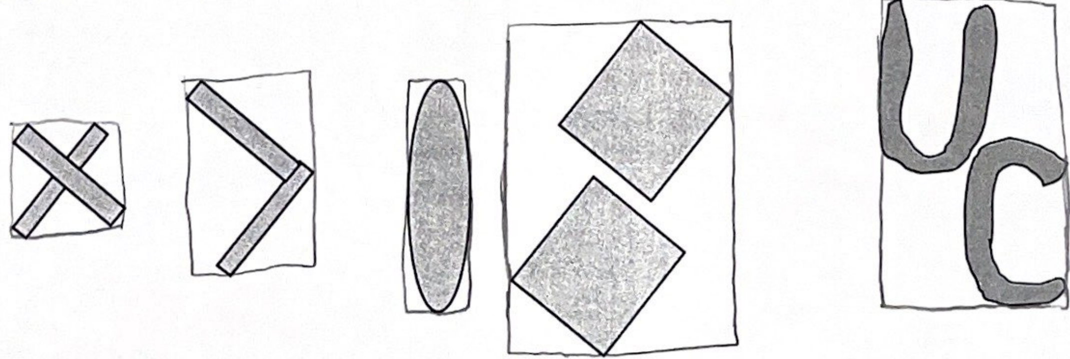
$F_s = 0.6\,\mu m \cdot 0.4\,\frac{N}{m} = 2.4\,\mu N$ $F_{el} = 2\,\mu N$ @ 50V when $g = 8\,\mu m$. 50V > V_{PI} so $g = 4\,\mu m \rightarrow F_{el} = 8\,\mu N$ $\frac{1}{g^2} \rightarrow 4 \times F$

$F_{net} = 5.6\,\mu N$

e. [4] **Carefully** sketch the displacement of the actuator as the voltage is increased from 0 to 50 V, and then decreased from 50 V to 0. Try to use specific points from the graph above. No sloppy sketches!



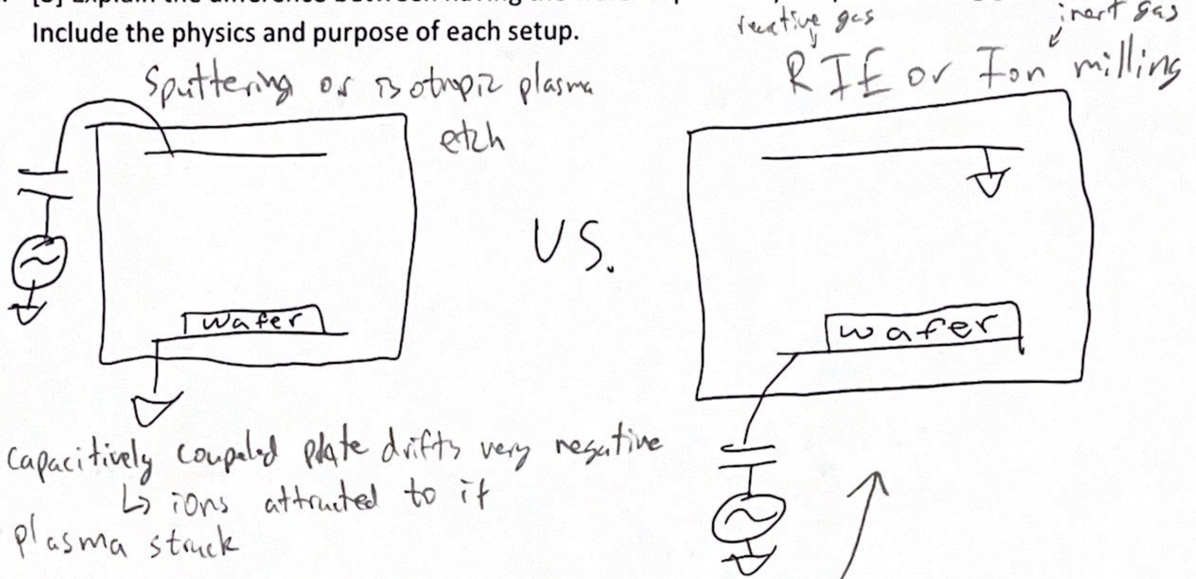
16) [5] A (100) wafer coated with silicon nitride has the following regions opened to the silicon surface. The wafer is dropped in a KOH etch and the etch runs until only 111 planes are exposed. What is the outline of the etched regions under the silicon nitride (i.e. where is the region where the nitride will not be supported by silicon)? Assume that this page is oriented with the wafer flat.



Dillon's page!

17) [10] Processing

a. [3] Explain the difference between having the wafer capacitively coupled vs being grounded. Include the physics and purpose of each setup.



• capacitively coupled plate drifts very negative
↳ ions attracted to it
• plasma struck

b. [1] What gas is used for ion milling?

Ar

c. [3] Explain the physics of RIE.

· Reactive gas is struck into a plasma
· Directed towards wafer w/ bias

d. [3] Explain the difference between DRIE and RIE.

· Teflon conformal dep to protect sidewalls · many isotropic etches · Reactive plasma · ions break up teflon on bottom surface

18) [7] Electrostatic

a. [1] There is 10uN of force when 10V is applied to two parallel plates. What is the force when -10V is applied?

10 uN

b. [3] What is the force between two gap-closing parallel plates?

$\frac{1}{2}\epsilon_0 V^2 \frac{A}{g^2}$

i. How does this force scale?

1

ii. How does the comb drive force scale?

1

c. [3] In an SOI process, where 2um is the smallest possible feature, and 100V is the maximum voltage.

i. What is the maximum electric field between 2 plates in this process?

$50 \frac{MV}{m}$

ii. Lightning strikes when the electric field between the earth and clouds exceeds 3MV/m. Will "lightning" strike between the parallel SOI plates? Explain why or why not.

No. Paschen's curve. As the gap decreases the electrons need more voltage to cause breakdown because not enough time between collisions