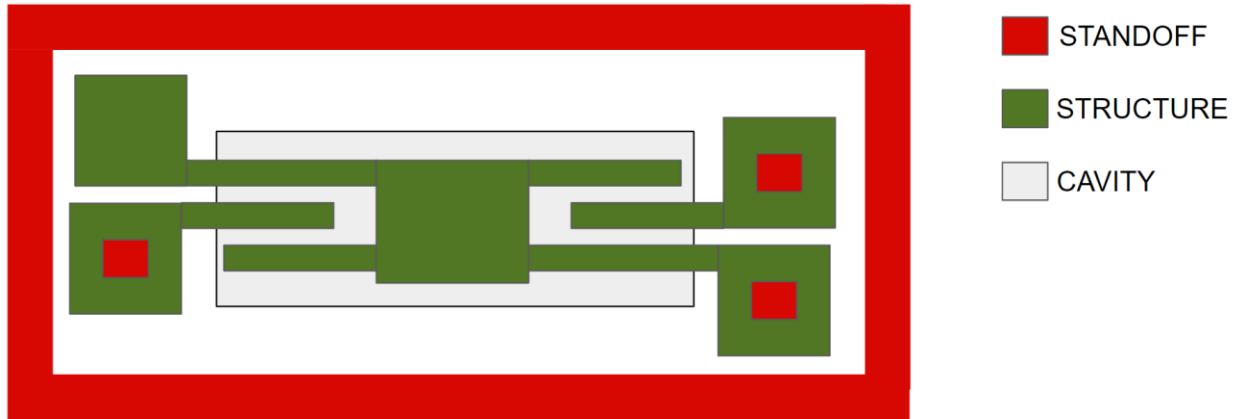


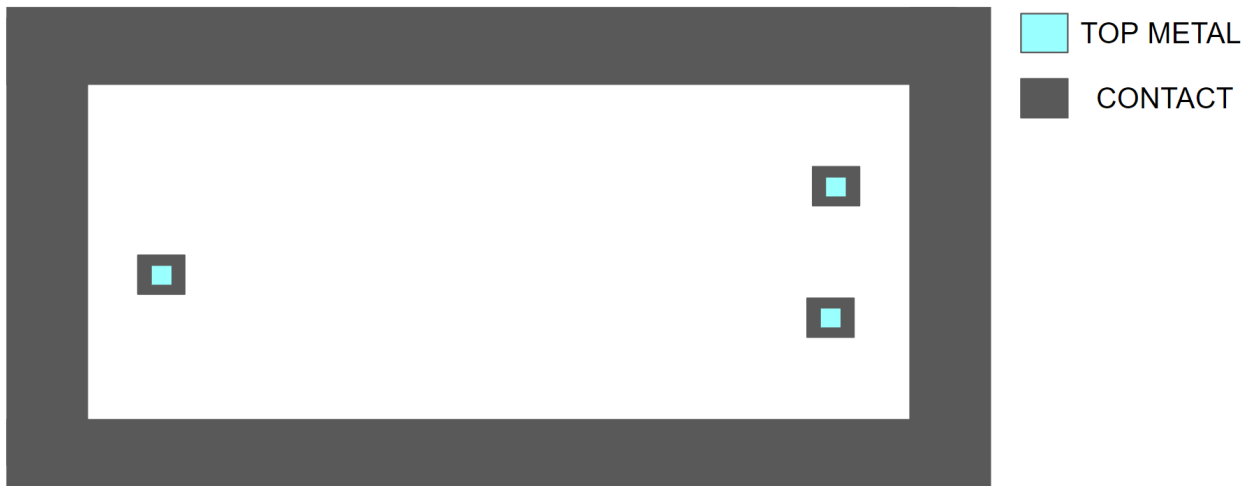
Hw7 Solutions

[53 points]

1. [5 points] Cube
 - a. [1 point] 0.543nm
 - b. [1 point] 1000:1
 - c. [1 point] 10^5 (log plot means every 1 is a power of 10). Phosphorous doping leads to a higher conductivity – resistivity is plotted. 10^{20} doped Si has a resistivity of 10^{-3} , while copper and aluminum have a resistivity of roughly 10^{-8} , 10^5 times lower. The difference between undoped and heavily doped Si is the same as the difference between heavily doped Si and metals like copper and aluminum.
 - d. [2 points] 1000C
 - i. After 10 minutes you've grown 0.02um of dry oxide and 0.1um of wet oxide
 - ii. After 1000 minutes you've grown 0.3um of dry oxide and 1um of wet oxide
2. [4 points] Argon
 - a. [1 point] Kinetic
 - b. [1 point] Anisotropic with vertical sidewalls
 - c. [1 point] No. Ion mill
 - d. [1 point] Capacitively isolated electrode. This electrode drops very negative due to the accumulation of electrons so the positive argon ions are attracted towards it.
3. [5 points] Boo Stanford, who wants to be a bird in a tree anyways
 - a. [1 point] No. The vertical profile comes from the isotropic SF6 etch being shaped by ions only removing teflon from the bottom surface, not the sidewalls.
 - b. [2 points] Chemical. Lots of isotropic etches cause the scallops.
 - c. [1 point] Very selective. The ions should just remove the Teflon, so the primary etching is chemical from SF6.
 - d. [1 point] The conformal deposition of Teflon, but only removing it from the plane parallel to the wafer: bottom of trench and top of wafer.
4. [16 points]



MEMS



CMOS

5. [3 points] Finfets
 - a. [2 points] 8nm width and 33nm height from slide dimensions and scaling from paper
 - b. [1 point] 0.543nm is Si unit cell so ~ 15 unit cells wide and 51 unit cells tall. TINY!
6. [6 points] DRIE
 - a. [1 point] From the text on slide 6: 65 cycles in 6 minutes and 4.5 $\mu\text{m}/\text{min}$ so 415nm/cycle
The slide and question didn't match, so give yourself a point for any answer here
 - b. [1 point] 76:1 selectivity means for every 76(μm , nm, m, etc.) Si is etched, PR is etched 1(μm , nm, m, etc.) so at least 10 μm of PR is needed to etch through 760 μm
 - c. [1 point] Roughly 15% increase in etch rate for a trench
 - d. [1 point] A quick Si isotropic etch like XeF₂ An isotropic etch works to get rid of the grass because though it may be tall, it's typically very thin so an isotropic etch will quickly remove it because it attacks all directions uniformly
 - e. [2 points] The sidewall for the 5 μm trench looks pretty close to 90%, although it isn't super straight. The angle gets larger (fatter etch pit) as the trench mask width gets wider. It looks like it's several degrees from vertical for the 200 μm etch.

7. [10 points] Nanolab

Thermal oxidation is done at a “high temperature”: easily 800°C but generally at or above 1000 °C

Parylene Deposition: 25 °C

LPCVD LTO: 425 °C

LPCVD PSG: 450 °C

LPCVD polysilicon: 580 °C-625 °C

LPCVD silicon nitride: done at 835 °C

Aluminum eutectic formation with Si: 450 °C

Photoresist Melting Point: Depends on the PR. Tons of types all with different properties. Generally want to keep it below 100 °C

Polysilicon <1400 °C

With this info you can see which depositions are allowed given each material that is already on the wafer. 1 pt each

	Aluminum	Photoresist	polysilicon
Thermal oxidation			
Parylene deposition			
LTO			
PSG			
POLY			
nitride			

8. [4 points] Oxidation

- a. [2 points] About 1000 minutes
- b. [2 points] As a general principle, the depth of pure silicon consumed in the oxidation process is 45% of the final oxide thickness. So the oxide thickness is ~222nm.