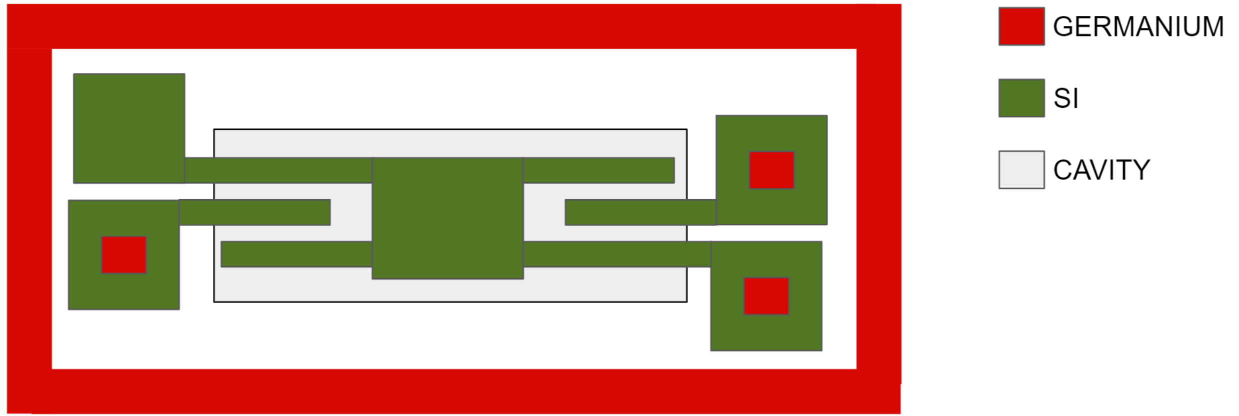
Hw7 Solutions

1. [5 points] Cube
   a. [1 point] 0.543nm
   b. [1 point] 1000:1
   c. [1 point] 10^5 (log plot means every 1 is a power of 10). Phosphorous doping leads to a higher conductivity – resistivity is plotted. 10^20 doped Si has a resistivity of 1 mΩcm, while copper and aluminum have a resistivity of a few $\mu\Omega$cm, several hundred times lower. Very very roughly this corresponds to the ratio of the number of dopant atoms in silicon vs. the number of atoms in a metal.
   d. [2 points] 1000C
      i. After 10 minutes you've grown 0.02um of dry oxide and 0.1um of wet oxide
      ii. After 1000 minutes you've grown 0.3um of dry oxide and 1um of wet oxide

      Clearly this is a nonlinear growth rate. Although it starts linear, pretty quickly diffusion becomes the dominant factor limiting growth rate.

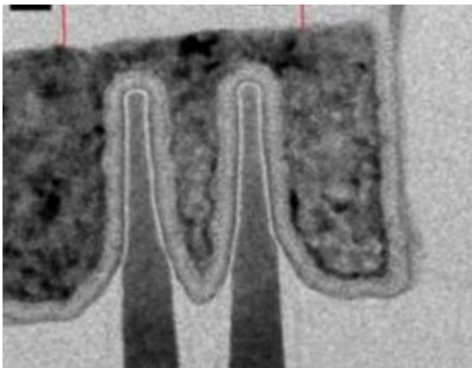
2. [4 points] Argon
   a. [1 point] Kinetic
   b. [1 point] Anisotropic with vertical sidewalls
   c. [1 point] No. Ion mill
   d. [1 point] Capacitively isolated electrode. This electrode drops very negative due to the accumulation of electrons so the positive argon ions are attracted towards it.
3. [5 points] Boo Stanford, who wants to be a bird in a tree anyways
   a. [1 point] No. The vertical profile comes from the isotropic SF6 etch being shaped by ions only removing teflon from the bottom surface, not the sidewalls.
   b. [2 points] Chemical. Lots of isotropic etches cause the scallops.
   c. [1 point] Very selective. The ions should just remove the Teflon, so the primary etching is chemical from SF6, which has great selectivity to aluminum, and pretty good selectivity to most other things. OK if you answered "somewhat selective".
   d. [1 point] The conformal deposition of Teflon (which is not removed from the sidewalls).
4. [15 points] The mask labeled GERMANIUM below should really be STANDOFF. There should be a metal contact mask on the CMOS chip.
   a. [4] Seal ring: STANDOFF, METAL, METAL contact [3], all the way around the outside [1].
   b. [4] Structure [1] and moving capacitor fingers [1] over CAVITY. Spring anchors [1] and fixed capacitor finger anchors [1] not over CAVITY (so that they are anchored)
   c. [5] Contacts: STANDOFF, METAL, METAL contact [3] connected to at least one spring [1] and one fixed capacitor finger [1].
      [2] points just for making an attempt.



MEMS

CMOS

5. [3 points] Finfets
   The table says that the pitch is 34 nm. The height is at least 1.5 times the pitch, but not 2x. So anything between 50 and 70 is fine. It looks like you can fit five fins across the pitch, so I'd guess about 7 nm width at the top. Anything between 5 and 10 is fine.



For example:

   a. [2 points] 8nm width and 33nm height from slide dimensions
   b. [1 point] 0.543nm is Si unit cell so ~15 unit cells wide and 51 unit cells tall. TINY!

6. [6 points] DRIE
   a. [1 point] From the text on slide 6: 65 cycles in 6 minutes and 4.5um/min so 415nm/cycle
      The slide and question didn't match, so give yourself a point for any answer here
   b. [1 point] 76:1 selectivity means for every 76(um, nm, m, etc.) Si is etched, PR is etched 1(um, nm, m, etc.) so at least 10um of PR is needed to etch through 760um
   c. [1 point] Roughly 15% increase in etch rate for a trench
   d. [1 point] A quick Si isotropic etch like XeF2 An isotropic etch works to get rid of the grass because though it may be tall, it's typically very thin so an isotropic etch will quickly remove it because it attacks all directions uniformly
   e. [2 points] The sidewall for the 5um trench looks pretty close to 90%, although it isn't super straight. The angle gets larger (fatter etch pit) as the trench mask width gets wider. It looks like it's several degrees from vertical for the 200 um etch.
7. [10 points] Nanolab

Thermal oxidation is done at a "high temperature": easily 800°C but generally at or above 1000 °C
Parylene Deposition: 25 °C
LPCVD LTO: 425 °C
LPCVD PSG: 450 °C
LPCVD polysilicon: 580 °C-625 °C
LPCVD silicon nitride: done at 835 °C

Aluminum eutectic formation with Si: 450 °C
Photoresist Melting Point: Depends on the PR. Tons of types all with different properties. Generally want to keep it below 100 °C
Polysilicon <1400 °C

With this info you can see which depositions are allowed given each material that is already on the wafer. 1 pt each

	Aluminum	Photoresist	polysilicon
Thermal oxidation			
Parylene deplosition			
LTO			
PSG			
POLY			
nitride			

8. [4 points] Oxidation
   a. [2 points] As a general principle, the depth of pure silicon consumed in the oxidation process is 45% of the final oxide thickness. So the oxide thickness is ~222nm.
   b. [2 points] About 1000 minutes