EE 147/247A Prof. Pister
Fall 2021

**Homework Assignment #7**

Due by online submission Monday 11/15/2021 (late Tuesday at 9am)

1) Check out the ever-popular fold-up crystal [1].
   a) What is the size of the silicon unit cell?
   b) What is the selectivity (ratio of etch rates) between <100> silicon and silicon dioxide in a KOH solution of 44 gm KOH in 100 ml water at 85C?
   c) How much does the resistivity of silicon change over the six orders of magnitude range of doping level shown, for boron doping, and for phosphorous doping? At the same level of doping (atoms/cc) is silicon more conductive when doped with boron, or phosphorous? How does the resistivity of heavily doped (10^20 atoms/cc) silicon compare to the resistivity of aluminum or copper?
   d) At 1000C, compare the oxide thickness of wet and dry oxidation
      i) After 10 minutes
      ii) After 1000 minutes
2) In an RF plasma etching system with only Argon as a feed gas,
   a) is the etching done primarily by chemical processes, or kinetic?
   b) Would you expect the etch to be isotropic, or anisotropic with vertical sidewalls?
   c) Would you expect the etch to have good selectivity between silicon and other materials?
   d) Would you expect that the wafer would be on the grounded electrode, or the capacitively isolated electrode?
3) In the Bosch Deep RIE process, your friend from Stanford says that the vertical etch profiles are due to really fast reactive ions digging straight into the silicon surface.
   a) Do you agree?
   b) Is the silicon etching primarily due to chemical etching, or kinetic? How can you tell from looking at the etched cross-section?
   c) Would you expect the silicon etch to be very selective to other materials, somewhat selective, or not selective?
   d) What prevents lateral etch due to reactive neutrals?
4) In the Invensense Nasiri process sketch the layout for the MEMS and the layout for the CMOS that you would need to build a simple vacuum-packaged capacitive accelerometer. The goal is just to show how the wiring is run between the structure and the CMOS chip. On the CMOS chip all that you need to show is the top metal and top metal contact mask. On the MEMS chip you need to show the cavity mask, the structure mask, and the standoff mask. Make sure that
   a) There is a sealing ring all around your structure
   b) Your structure is free to move in the spring/mass/capacitor part, but that it is appropriately mechanically anchored as well
   c) You make (at least) two independent electrical contacts to the capacitive accelerometer (to form at least one variable capacitor).
5) In the Intel 14 nm process presentation [2], slides 15-20 illustrate what the fin dimensions mean. In the IEDM paper on the Intel 10 nm process [3], use the fin pitch in Table 1, and the cross-section in Figure 7 and
   a) Estimate the finfet height, and the width of the fin where the gate overlaps it
   b) Calculate the height and width in silicon crystal unit cells
6) Check out the characterization of the Stanford DRIE machine [4]
   a) Estimate the etch depth per pulse in the cross-section figure on slide 6. Is that rate consistent with the depth per pulse that can be calculated from the data provided in the text on the left? And with the undercut?

b) With the recipe on slide 6, how thick would the photoresist need to be to etch all the way through a 760um thick wafer (about the thickness of a standard 300mm wafer)?
c) from the figures on slide 7, which rank the following by etch rate from fastest to slowest: trenches that are 7um and 12um wide, and holes that are 7, 10, and 12um wide. Very roughly, what's the percent difference in etch rate for a 7um hole vs. a 7um trench?
d) Look at slide 15 and cry a little imagining that this is your project/product. What process might get rid of the grass once it's grown?
e) Estimate the variation in sidewall angle vs. trench width in slide 16.
f) [Note, not a homework question] Take a look at slides 19, 20, and 21 – looks like I lied to Terry when I said that the deposition was conformal. Weird though – how does it protect the sidewalls? Something is wrong here…

7) Of the following process steps: thermal oxidation; parylene deposition (see nanolab manual); LPCVD LTO, PSG, polysilicon, silicon nitride; which can be used with a wafer that has
   a) aluminum on it; b. photoresist on it; c. polysilicon on it
8) You deposit silicon nitride by LPCVD on a silicon wafer, then deposit a 100nm thick polysilicon film on top of that. You put the wafer in a 900C dry oxidation furnace and convert all of the polysilicon into silicon dioxide.
   a) What will the oxide thickness be?
   b) Roughly how long will it take to grow that oxide?

[1] http://www-bsac.eecs.berkeley.edu/~pister/crystal.pdf
[2] https://people.eecs.berkeley.edu/~pister/147fa21/Resources/Intel14nm2014idf.pdf
[3] https://people.eecs.berkeley.edu/~pister/147fa21/Resources/Intel%2010nm%20IEDM2017.pdf
[4] http://robotics.eecs.berkeley.edu/~pister/147+247Afa14/Resources/BoschProc-STS.pdf