Wafer-Level Heterogeneous Integration for MOEMS, MEMS, and NEMS

Martin Lapisa, Göran Stemme, *Fellow, IEEE*, and Frank Niklaus, *Member, IEEE*

(Invited Paper)

***Abstract*—Wafer-level heterogeneous integration technologies for microoptoelectromechanical systems (MOEMS), microelectromechanical systems (MEMS), and nanoelectromechanical systems (NEMS) enable the combination of dissimilar classes of materials and components into single systems. Thus, high-performance materials and subsystems can be combined in ways that would otherwise not be possible, and thereby forming complex and highly integrated micro- or nanosystems. Examples include the integration of high-performance optical, electrical or mechanical materials such as monocrystalline silicon, graphene or III–V materials with integrated electronic circuits. In this paper the state-of-the-art of wafer-level heterogeneous integration technologies suitable for MOEMS, MEMS, and NEMS devices are reviewed. Various heterogeneous MOEMS, MEMS, and NEMS devices that have been described in literature are presented.**

***Index Terms*—Microelectromechanical system (MEMS), microoptoelectromechanical system (MOEMS), More-than-Moore, nanoelectromechanical system (NEMS), photonic integration, self-assembly, wafer-level heterogeneous integration.**

I. Introduction

MICROOPTOELECTROMECHANICAL systems (MOEMS), microelectromechanical systems (MEMS), and nanoelectromechanical systems (NEMS) typically are transducer systems with movable or suspended parts that sense or control optical, physical, or chemical quantities, such as, for example, electromagnetic radiation, inertia, or fluids. For the implementation of MOEMS, MEMS, or NEMS devices, it is desirable to use high-performance materials and subsystems in the device manufacturing. For example, the combination of high-performance photonic, mechanical, electrical, and nanomaterials such as monocrystalline silicon, germanium, III–V materials, piezoelectric materials, shape memory alloys (SMAs), carbon nanotubes (CNT) or nanowires enables high-performance devices and functionalities that would otherwise not be possible. Also, most transducers require electric interfacing to the outside world, which is typically done by electronic integrated circuits (ICs) that are combined with the transducers. The ICs may include signal conditioning functions such as analog-to-digital conversion, amplification, temperature compensation, storage, filtering, system test, logic, and communication functions.

In conventional bulk and surface micromachining technologies, MOEMS, MEMS, or NEMS devices are processed in bulk silicon substrates or are deposited and processed on top of silicon substrates [1]. However, many crystalline photonic materials and other high-performance MEMS and NEMS materials cannot be deposited directly on silicon substrates and thus cannot be integrated in this way. The conventional bulk and surface micromachining techniques have been adapted in various ways to integrate MEMS components with CMOS ICs on a single (monolithic) substrate [2]–[4]. These technologies are sometimes referred to as "monolithic integration." However, in these approaches the number of available materials and device designs typically are very limited, which can be particularly restrictive for optical MEMS devices.

One possibility to overcome the problem of material and process incompatibilities is the use of hybrid integration technologies in which the complete devices (e.g., MEMS and CMOS ICs) are manufactured on separate substrates with dedicated technologies. Thereafter, the substrates are diced into chips and the chips are hybridized. Hybridization means in this context that the individual chips are placed side-by-side or on top of each other in a package. Electrical connections between the individual chips can be established by forming wire bonds or by flip-chip bonding using bump bonds [5]. However, for these technologies the achievable integration densities, device miniaturization and number of electrical interconnects between the chips is limited. Thus, hybrid integration technologies typically have significant limitations for arrayed MOEMS devices such as micromirror arrays and infrared detector arrays and for emerging NEMS devices.

Heterogeneous integration technologies combine the advantages of monolithic and chip-level hybrid integration technologies and allow the manufacturing of complex micro- and nanosystems that are not possible to manufacture with conventional micromanufacturing techniques. For the purpose of this review, wafer-level heterogeneous integration refers to wafer-to-wafer and chip-to-wafer joining, processing and interconnecting materials and components that are prepared with different technologies including MEMS, MOEMS, photonics, electronic ICs, and emerging NEMS. Heterogeneous integration of ICs with

Manuscript received July 1, 2010; revised September 24, 2010; accepted October 25, 2010. Date of publication January 12, 2011; date of current version June 8, 2011. This work was supported in part by the European project ICU (Infrared Imaging Components for use in automotive safety applications) and in part by the European Union (EU) through its 7th Framework Program.

The authors are with the Microsystem Technology Laboratory, School of Electrical Engineering, KTH-Royal Institute of Technology, SE-100 44 Stockholm, Sweden (e-mail: frank.niklaus@ee.kth.se).

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Digital Object Identifier 10.1109/JSTQE.2010.2093570

TABLE I
OVERVIEW OF WAFER-LEVEL VIA-FIRST AND VIA-LAST HETEROGENEOUS INTEGRATION CONCEPTS FOR MOEMS, MEMS, AND NEMS

	Main Advantages	Main Disadvantages	Ref.
Via-First Approaches			
Integration of fully processed and packaged components (Fig. 3a).	Via-formation during bonding in one-step integration of pre-packaged components.	Limits in size reduction. Bond alignment required.	15, 54-56
Integration of partly processed and/or packaged components with subsequent wafer-level processing (Fig. 3b).	Via-formation during bonding in one-step integration and packaging process.	Limits in size reduction. Bond alignment required.	4, 10, 11, 57-64
Integration of pre-defined components or materials and subsequent etch of the sacrificial handle substrate (Fig. 3c).	Via-formation during bonding.	Limits in size reduction. Bond alignment required.	-
Integration of pre-defined components or materials and subsequent component release from the donor substrate (Fig. 3d).	Via-formation during bonding.	Limits in size reduction. Bond alignment required.	26-30, 33-39
Chip-to-wafer pick-and-place techniques (Fig. 3e).	Flexible and inexpensive for small volumes. Placement of known good chips on known good chips on the wafer.	Limits in size reduction. Bond alignment required. Serial processes.	55, 56, 131
Self-assembly techniques (Fig. 3e).	Highly parallel processes. Extremely small dimensions possible.	Non-deterministic.	53,70-73
Via-Last Approaches			
Integration of fully processed and packaged components (Fig. 14a).	Optimized component pre-packaging possible.	Bond alignment required. Post-bond processing.	130
Integration of materials(s), etching of sacrificial handle wafer and subsequent processing and definition of components (Fig. 14b).	Extremely small dimensions and vias possible.	Post-bond processing.	87-93, 96, 97, 99-101, 104-106, 111, 112, 122-128
Integration of materials(s), material release from donor wafer and subsequent processing of components (Fig. 14c).	Extremely small dimensions and vias possible. No bond alignment required.	Post-bond processing.	132-134
Full or partial processing of components, integration and subsequent etching of sacrificial handle wafer (Fig. 14d).	Very small dimensions and vias possible.	Bond alignment required. Post-bond processing.	94, 95, 110, 113
Full or partial processing of components, integration and subsequent component release from donor wafer (Fig. 14e).	Very small dimensions and vias possible.	Bond alignment required. Post-bond processing.	65-69
Chip-to-wafer pick-and-place techniques (Fig. 14f).	Placement of known good chips on known good chips on the wafer.	Bond alignment required. Post-bond processing.	131
Self-assembly techniques (Fig. 14f).	Very small dimensions and vias possible.	Non-deterministic. Post-bond processing.	71-73, 114, 115

MOEMS, MEMS, or NEMS has been reviewed briefly [6] and is mentioned as an important building block in the "More-Than-Moore" paradigm for future microsystems in the International Technology Roadmap for Semiconductors (ITRS) [7]. Wafer-level packaging technologies for MEMS have been reviewed thoroughly in recent publications [8], [9] and are not part of the present review.

This paper reviews the state-of-the-art of wafer-level heterogeneous integration technologies and platforms suitable for MOEMS, MEMS, and NEMS devices. Heterogeneous integration technologies can be placed in the two categories: 1) heterogeneous integration using via-first processes and 2) heterogeneous integration using via-last processes. In heterogeneous integration using via-first processes, the vias establishing electrical (or alternative optical) contacts between the components on the different substrates are defined during the bonding process. On the contrary, in heterogeneous integration using via-last processes the components are first bonded to each other and the vias establishing electrical (or alternative optical) contacts between the components on the different substrates are defined thereafter. The advantages, limitations and technological challenges of the via-first and the via-last approaches differ from each other to some extent and in the following sections the various wafer-level heterogeneous integration technologies are accordingly grouped in via-first and via-last technologies. Throughout this paper, the term "substrate" shall mean to be a wafer or a part of a wafer. Table I provides an overview of the via-first and via-last wafer-level heterogeneous integration concepts discussed in this paper.

II. HETEROGENEOUS INTEGRATION WITH VIA-FIRST PROCESSES

A. Basic Heterogeneous Integration Concepts Using Via-First Processes

In this section, basic conceptual approaches of heterogeneous integration using via-first processes that are suitable for MOEMS, MEMS, and NEMS devices are discussed. Not all of the presented approaches have yet been implemented for MOEMS, MEMS, or NEMS devices. Fig. 1 shows three concepts for defining electrical via contacts between the components on different substrates during bonding in via-first heterogeneous integration processes. Instead of electrical vias, optical vias can, in principle, be implemented in similar ways.

The process in Fig. 1(a) depicts a simple metal-bump-bonding approach. The bump bonding can be implemented by using, for example, solder bonding [4], [10]–[16], eutectic bonding [17]–[25] or direct metal thermocompression bonding [26]–[32]. Typical dimensions of such bump bonded metal vias are on the order of 100 μm $\times$ 100 μm. In wafer-level processes, it is challenging to obtain highly reliable processes for vias with dimensions of below 20 μm $\times$ 20 μm. The via-first approach shown in Fig. 1(a) has been used for heterogeneous integration of a number of MOEMS and MEMS devices [4], [10], [26]–[30].

The process depicted in Fig. 1(b) makes use of combined metal bump bonding and bonding with a nonconductive (dielectric) layer. All of the above mentioned metal bump-bonding processes can, in principle, be used for this approach. The

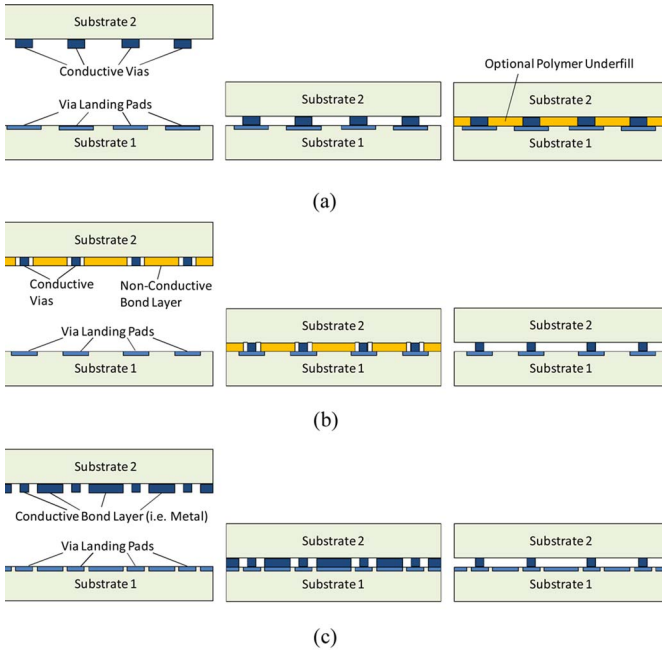


Fig. 1. Concepts for forming via contacts between the components on different substrates during bonding in via-first heterogeneous integration processes. (a) Metal bump bonding with optional polymer underfill. (b) Combined metal bump and dielectric layer bonding with optional etch of the dielectric layer. (c) Bonding with conductive layer (e.g., metal) with subsequent selective etch of parts of the bond layer.

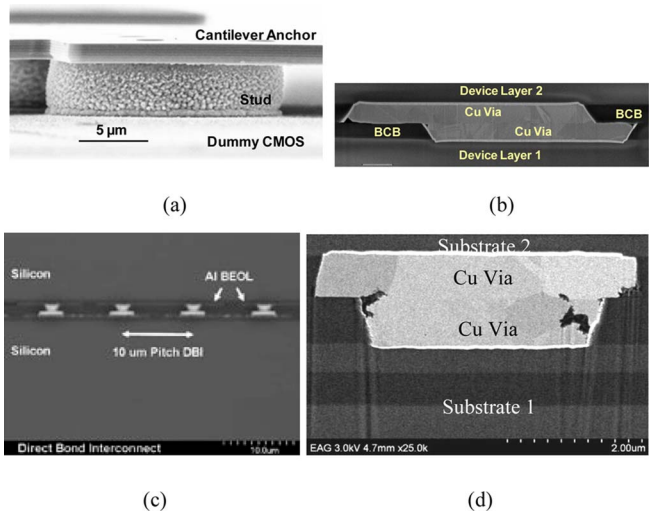


Fig. 2. Examples of combined via-first metal bump bonding with polymer dielectric layer bonding [(a) and (b)] [34, 41] and via-first metal bump bonding with SiO_2 dielectric layer bonding [(c) and (d)] [48] as illustrated in Fig. 1(b).

nonconductive bonding layer can be a polymer [33]–[45] or any layer with a flat surface that is suitable for bonding such as silicon or SiO_2 [46]–[48]. Test structures with via dimensions down to 5 μm $\times$ 5 μm have been demonstrated with these approaches. Fig. 2(a) shows an example of a via for MEMS structures that is fabricated with combined solder bump bonding and polyimide bonding [35], and Fig. 2(b) shows an example of a via for 3D-ICs that is fabricated with combined copper–copper direct bump bonding and BCB bonding [40]–[42]. Fig. 2(c) and (d) shows vias that are fabricated with combined copper–copper bump bonding and SiO_2 bonding [48]. The combination of solder bump bonding and polymer adhesive bonding has been demonstrated for heterogeneous integration of MEMS and ICs [33]–[38]. The combination of metal bump bonding and direct bonding has been proposed for heterogeneous integration of MOEMS devices [49], but no devices have been demonstrated yet.

Fig. 1(c) depicts a process in which metal bumps and metal support structures are created at the same time. The metal support structures provide additional mechanical support and larger bond areas and thus, enable the defined bonding of small metal vias. Thereafter, the support metal can be sacrificially removed. This concept has been proposed using eutectic bonding and subsequent selective electrochemical etching of the support metal [23]–[25], but no integrated MOEMS or MEMS devices have been reported yet.

All via-first processes outlined in Fig. 1 require accurate substrate-to-wafer alignment to match the corresponding prefabricated via bumps on the two surfaces. Very high demands on substrate-to-wafer alignment accuracies of below 3 μm for high-density vias significantly increase the process complexity, reduce yield and increase cost. Large research and development efforts are currently being undertaken for metal-to-metal bump bonding technologies with focus on stacking of ICs for 3D-ICs [50]. These research efforts also include the development of improved fabrication schemes for through-silicon-vias (TSVs) [50]–[53]. It can be expected that the results from the targeted research activities for 3D-ICs will also benefit the development of heterogeneous integration technologies for MOEMS, MEMS, and NEMS.

Fig. 3 shows five conceptual schemes of heterogeneous integration techniques using via-first processes that are suitable for MOEMS, MEMS, and NEMS devices. All via-first bump-bonding process discussed in Fig. 1 can, in principle, be used for the heterogeneous integration techniques in Fig. 3.

In the technique shown in Fig. 3(a), a completely processed and packaged MOEMS or MEMS component substrate containing metal bumps is bonded to a target wafer, typically a CMOS based IC wafer. This technique is simply an extension of conventional chip-to-chip bump bonding to substrate-to-wafer bump bonding [15], [54]–[56]. Due to the minimum size of the metal bumps and the thickness of a wafer with the packaged MOEMS or MEMS components, this technique allows only limited miniaturization and integration densities for the final devices. Chip-to-chip and chip-to-wafer pick-and-place techniques are often more cost-efficient than substrate-to-wafer bonding approaches because pick-and-place techniques allow the placement of known good chips on top of known good chips.

In the technique shown in Fig. 3(b), a partly processed MOEMS or MEMS substrate containing metal bumps is bonded to the target wafer. Thereafter, the components are further processed at the wafer-level to complete the MOEMS or MEMS devices using, e.g., etching and/or thinning processes. Although this technique allows only limited integration densities due to minimum dimensions of the metal bumps, it has been proposed

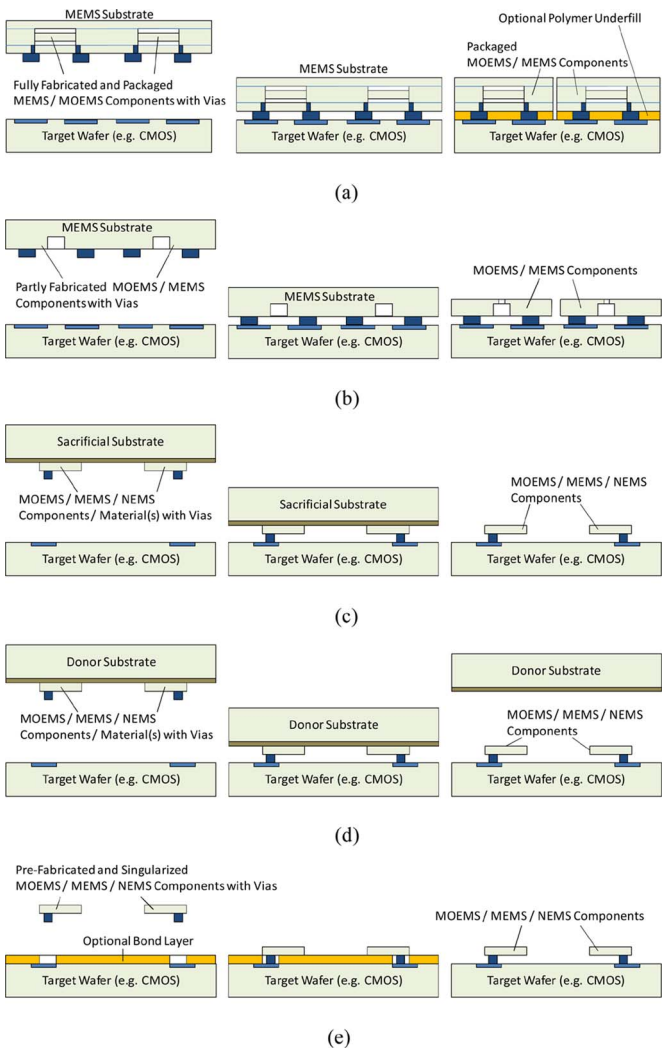


Fig. 3. Conceptual schemes of heterogeneous integration techniques using via-first processes. (a) Integration of fully processed MOEMS or MEMS components. (b) Integration of partly processed and/or packaged MOEMS or MEMS components with subsequent wafer-level processing. (c) Integration of predefined MOEMS, MEMS, NEMS components or materials and subsequent etch of the sacrificial handle substrate. (d) Integration of pre-defined MOEMS, MEMS, NEMS components or materials and subsequent component release from the donor substrate. (e) Chip-to-wafer pick-and-place and self-assembly techniques in which the pre-fabricated MOEMS, MEMS or NEMS components are placed and fixed on their final location on the target wafer.

for a number of MOEMS and MEMS devices [4], [10], [11], [17], [57]–[64] and has been successfully implemented for commercial MOEMS and MEMS devices [4], [10], [11], [17], [57], [58].

In the techniques shown in Fig. 3(c) and (d), the MOEMS, MEMS, or NEMS components with the metal bumps are fully or partly processed on a handle substrate. Thereafter, the handle substrate is bump bonded to the target wafer and the handle substrate is either sacrificially removed [see Fig. 3(c)] or the components are released from the handle (donor) substrate [see Fig. 3(d)]. Removal of the sacrificial substrate can, for example, be done by etching processes, by grinding processes, or by a combination of both [88]–[93], [96], [97], [99]–[101] [104]–[106], [111], [112], [122]–[128]. Component release from the donor substrate can be done in various ways, including bond-interface decomposition by exposure with light [33]–[39] or etchants [29], [30], by predetermined breaking points [26]–[28], [65], [66] or by deliberately weak bond interfaces [67]–[69]. The process shown in Fig. 3(d) has been implemented for heterogeneous integration of various MOEMS and MEMS devices [33]–[38].

In the technique shown in Fig. 3(e), the prefabricated and singularized MOEMS, MEMS, or NEMS components with metal bumps are assembled by chip-to-wafer pick-and-place processes [55], [56] or by self-assembly processes [53], [70]–[73]. Pick-and-place processes such as flip-chip-bonding are serial processes that are commonly used for electronic, photonic and MEMS components. However, components with very small dimensions cannot be economically handled in this way. Self-assembly processes are one way to overcome the problems of small component dimensions and serial assembly. Self-assembly processes have been used for heterogeneous integration of MOEMS, MEMS, NEMS, and photonic devices. Three recent review papers give an excellent overview of existing self-assembly approaches [71]–[73].

In Section II-B, examples of heterogeneous integration platforms using via-first processes that have been implemented for MOEMS, MEMS, or NEMS devices are discussed.

B. MOEMS, MEMS, and NEMS Devices Implemented With Via-First Heterogeneous Integration Platforms

1) Wafer-to-Wafer Heterogeneous Integration Platforms Using Via-First Processes: A number of wafer-to-wafer heterogeneous integration platforms using via-first processes for MOEMS, MEMS, and NEMS devices have been implemented for both research and commercial purposes. Early examples of via-first heterogeneous integration of MOEMS and MEMS include the integration of RF microrelays on RF substrates [26]–[28] and the integration of mirror arrays on silicon substrates [29], [30]. In both cases, the basic process depicted in Fig. 3(d) was used. For the RF relays, metal compression bump bonding [see Fig. 2(a)] in combination with predetermined breaking point release was used [26]–[28] and for the mirrors, metal compression bump bonding [see Fig. 2(a)] in combination with HF release etch was used [29], [30].

One of the first examples of via-first heterogeneous integration of MOEMS with functional CMOS ICs is the monocrystalline silicon mirror array shown in Fig. 4(a) and (b). The array consists of 32 $\times$ 32 mirrors with dimensions of each mirror pixel of 1 mm $\times$ 1 mm [4], [10], [11]. A variation of the via-first heterogeneous integration platform (Nasiri fabrication) shown in Fig. 5 has been used for the mirror integration [4], [10], [11], [17]. In this process, which is equivalent to the conceptual process scheme illustrated in Fig. 3(b), the mirrors, hinges, and via bumps are partly premanufactured in a silicon wafer stack before the wafer stack is bonded to the CMOS IC wafer. Thereafter, the bonded mirror wafer is thinned and further processed to form the mirror plates. Similar integration processes have also been proposed by other groups for various micromirror applications [59]–[64].

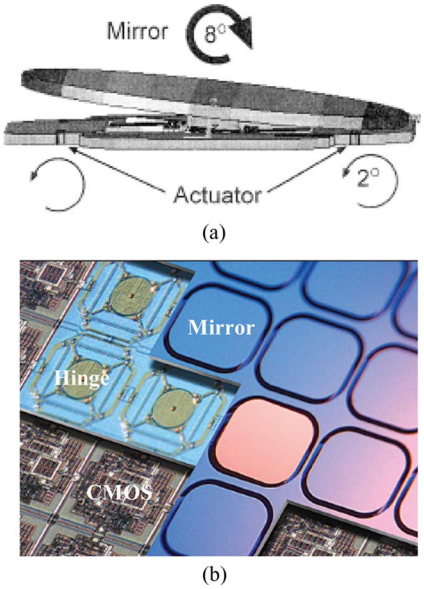


Fig. 4. Monocrystalline silicon mirror array integrated with CMOS ICs using a variation of the via-first heterogeneous integration platform (Nasiri fabrication) depicted in Fig. 5. Each mirror is 1 mm × 1 mm in size [4], [10], [11]. Reprinted with permission from NSTI.

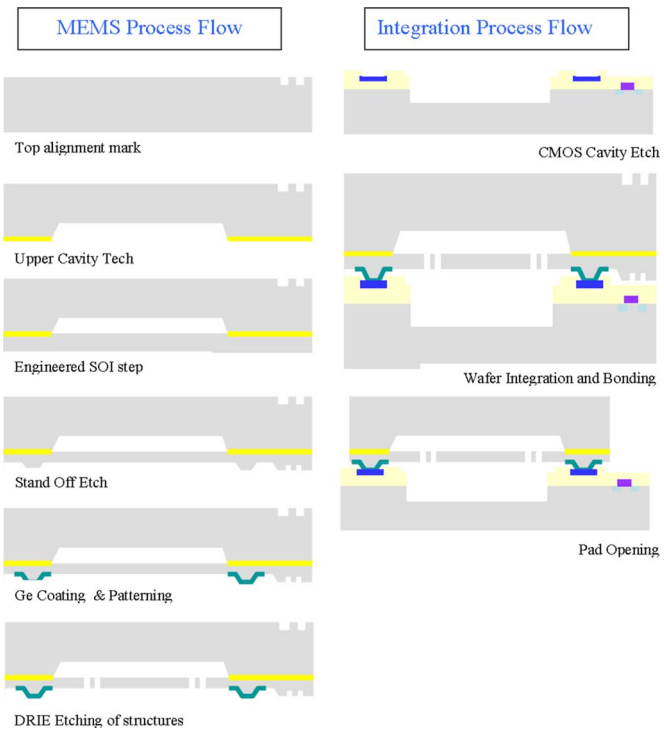


Fig. 5. Wafer-level via-first heterogeneous integration platform (Nasiri fabrication) from InvenSense that is used for high-volume manufacturing of commercially available gyroscopes [17]. Reprinted with permission from InvenSense.

The via-first heterogeneous integration platform shown in Fig. 5 is being used for manufacturing of gyroscopes [17], [57] and for manufacturing of combined three-axis accelerometers and three-axis gyroscopes that are integrated on a single chip [58]. These devices are sold at very high volumes for consumer products such as motion controls in gaming. As example

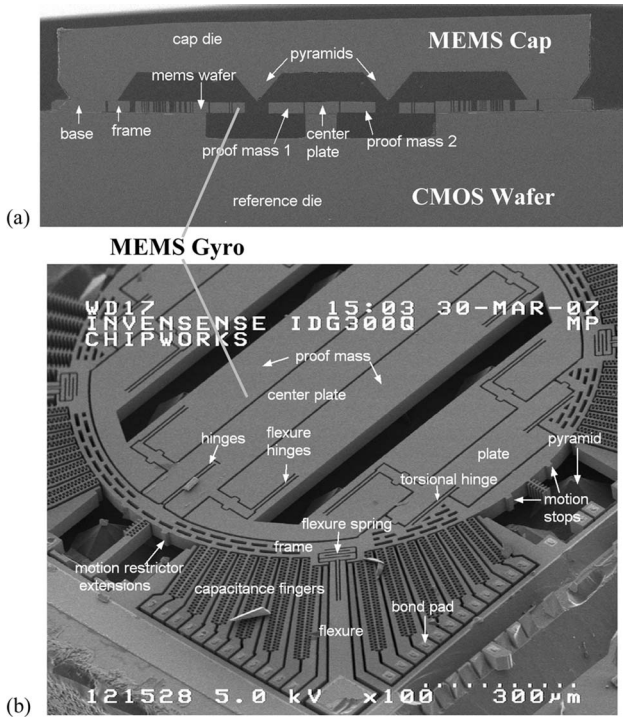


Fig. 6. Commercially available gyroscope integrated with CMOS ICs using the via-first heterogeneous integration platform (Nasiri fabrication) depicted in Fig. 5 [57]. Reprinted with permission from Chipworks.

of the gyroscope chip, the monocrystalline silicon capacitive gyroscope sensor and parts of the gyroscope package are prefabricated together and then bonded to the CMOS IC wafer that contains an etched cavity as indicated in Fig. 5. The bonding and sealing is done directly to the top CMOS Al metal layer using an Al/Ge eutectic bonding process [17]. Fig. 6(a) shows a cross-sectional image and Fig. 6(b) shows a top view of a commercial gyroscope that has been manufactured with this technique [57].

Another well-developed wafer-level via-first heterogeneous integration platform makes use of a donor wafer, as depicted in Fig. 3(d), with combined solder bump bonding and polyimide adhesive bonding as shown in Fig. 2(b). Fig. 7 shows a detailed process scheme of this integration platform, which has been used for integrating arrays of atomic force microscope (AFM) tips made of monocrystalline silicon on top of ICs [33], [34]. The AFM tips are first fabricated on a SOI wafer and then transferred to a glass wafer by polyimide bonding and sacrificial etching of the SOI substrate. Thereafter, metal via bumps and the patterned adhesive polyimide layer are formed on the backside of the AFM tips. Then, the glass wafer with the AFM tips is aligned and bonded to the electronic IC wafer using combined solder bump bonding and polyimide adhesive bonding. Finally the AFM tips are released from the glass wafer by laser debonding. The glass donor wafer is used to enable the laser debonding process and to facilitate accurate wafer-to-wafer alignment before bonding. Fig. 8 shows SEM images of the integrated AFM tips. The dimensions of the vias of the AFM tips are 15 μm in diameter, the AFM tip array has a pitch of 130 μm × 100 μm and the monocrystalline silicon AFM cantilevers are 300 nm thick.

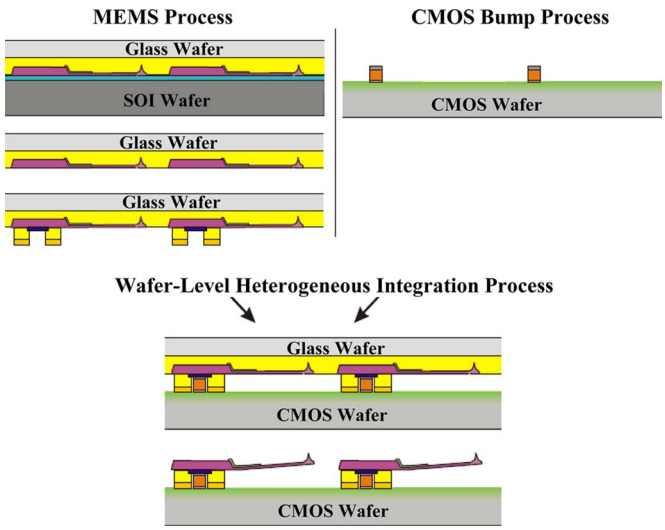


Fig. 7. Wafer-level via-first heterogeneous integration platform for arrays of AFM tips [34].

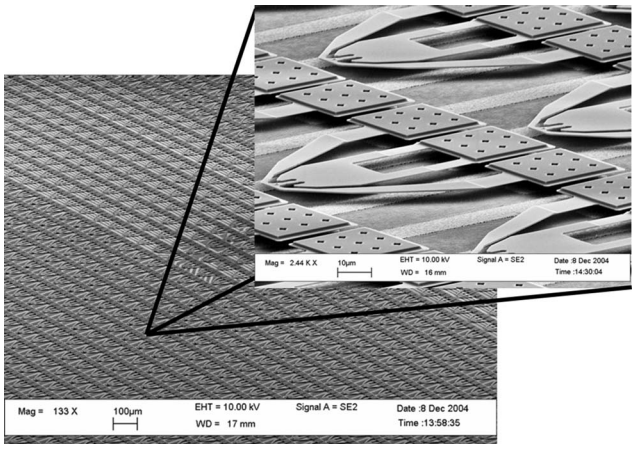


Fig. 8. Arrays of AFM tips integrated on electronic ICs using the via-first heterogeneous integration platform shown in Fig. 7 [34].

2) Wafer-to-Wafer Component Distribution and Chip-to-Wafer Heterogeneous Integration Platforms Using Via-First Processes: Conventional wafer-to-wafer heterogeneous integration platforms are an attractive and cost-efficient integration approach if the components manufactured on both wafers have high manufacturing yield and if they are comparable in size. These wafer-to-wafer integration platforms can also be cost-efficient if at least one of the two components to be integrated is very inexpensive as compared to the other. However, in many applications the manufacturing yield of one or both components to be integrated is low, the components are very different in size and/or both components are complex and expensive. Thus, when using conventional wafer-to-wafer integration approaches for these types of devices, the resulting yield is decreased dramatically since functional components may be combined with nonfunctional components. The resulting yield of the devices from the bonded wafer stack is then a product of the individual yields of the wafers. Also, severe cost penalties are imposed on the manufacturing of the smaller of the

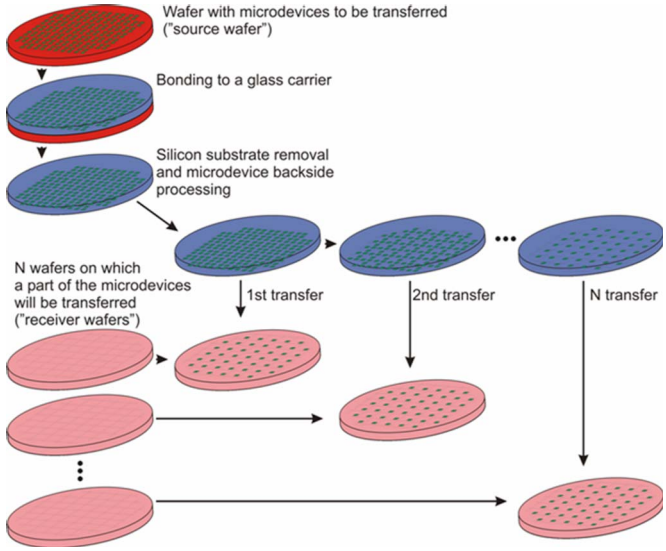


Fig. 9. Wafer-to-wafer selective component distribution (MD) from one donor wafer to several target wafers using a modified version of the process shown in Fig. 7 [35].

two components since its pitch on the wafer has to be adapted to the pitch of the larger component thus, reducing the number of components per wafer. In addition, materials such as expensive photonic III–V materials are only available in wafer sizes that are smaller than the standard silicon wafers sizes. This can make direct wafer-to-wafer integration of silicon and III–V materials extremely inefficient. Different modified heterogeneous integration schemes have been proposed to address the issues mentioned above. These technologies include wafer-to-wafer selective component distribution, also called microdevice distribution (MD) technology [35]–[38], conventional chip-to-wafer pick-and-place technologies [55], [56], and chip-to-wafer self-assembly techniques [70]–[73].

For wafer-to-wafer selective component distribution (MD), the via-first heterogeneous integration process shown in Fig. 7 has been adopted in a way that one MEMS donor wafer can populate up to 42 target wafers. In this approach, the pitch of the donor wafer is a multiple of the pitch of the target wafer and the donor wafer contains many more components than the target wafer. Instead of transferring all components from the donor wafer to the target wafer at the same time, only selected components are transferred from the donor wafer to the target wafer as illustrated by the process scheme shown in Fig. 9 [35]. After the transfer, the target wafer is fully populated with components. The component distribution relies on selective bump bonding in combination with adhesive polyimide bonding and subsequent selective component release by laser ablation. This method has been applied to different types of devices such as the integration of AFM tips [35], [36], the integration of SMA materials into microvalves [37] and the integration of PZT materials with RF MEMS switches [38]. Fig. 10(a) shows a transferred AFM tip [35] and Fig. 10(b) shows a PZT RF MEMS switch [38] manufactured with the selective component transfer method. Related approaches are transfer printing or stamping transfer methods [65]–[69] that, however, to our knowledge have not yet

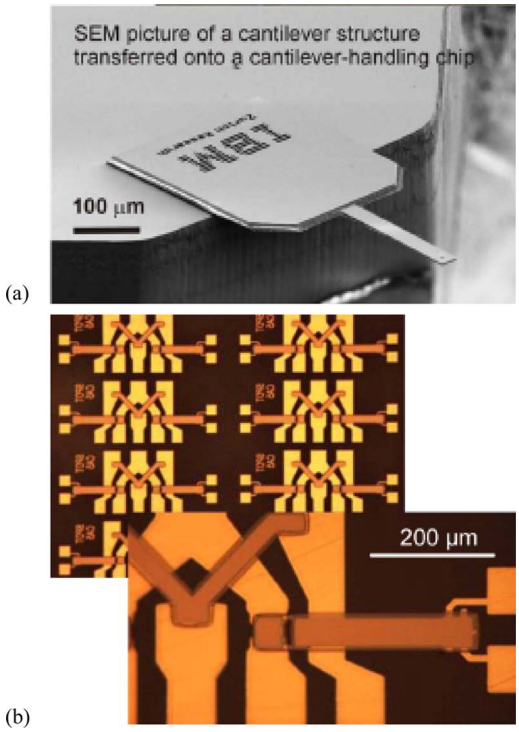


Fig. 10. (a) AFM tip [35] and (b) PZT RF MEMS switch [38] integrated with the wafer-to-wafer selective component distribution (MD) process shown in Fig. 9.

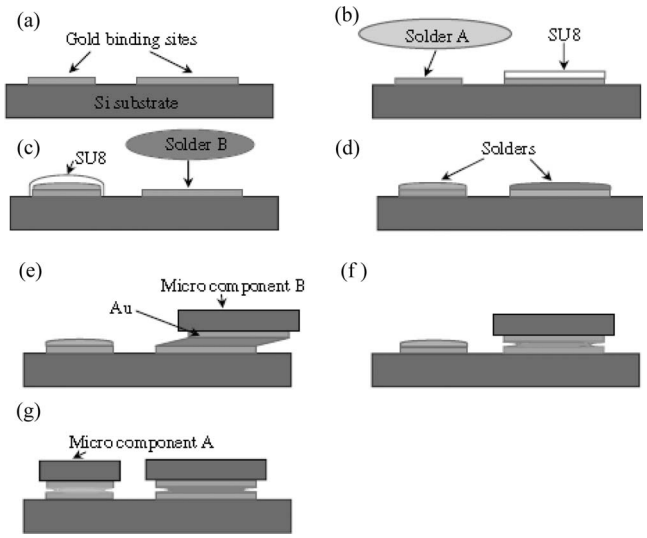


Fig. 11. Selective self-assembly in combination with solder bump bonds [70]. Reprinted with permission from IOP.

been implemented for MOEMS, MEMS, or NEMS devices in combination with via-first processes.

Finally, various self-assembly processes have been proposed for via-first heterogeneous integration of MOEMS, MEMS, and NEMS devices [70]–[73]. Self-assembly is an intriguing approach and a variety of physical effects can be used as driving mechanisms for the self-assembly process, including gravity, capillary forces, electromagnetic forces, etc. Fig. 11 shows an example of a selective self-assembly process in combination with solder bump bonds that is suitable for MEMS applications [70].

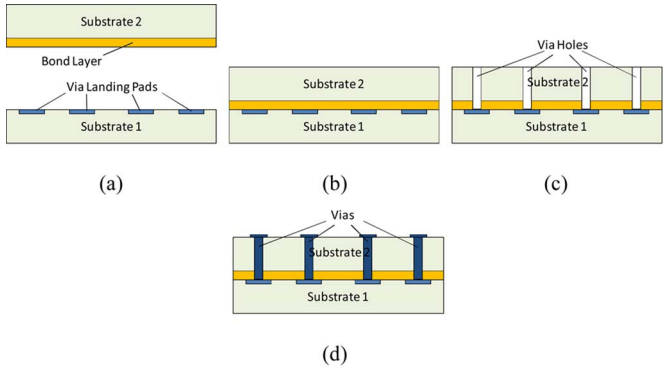


Fig. 12. Concept for forming via contacts between the components on different substrates after bonding in via-last heterogeneous integration processes.

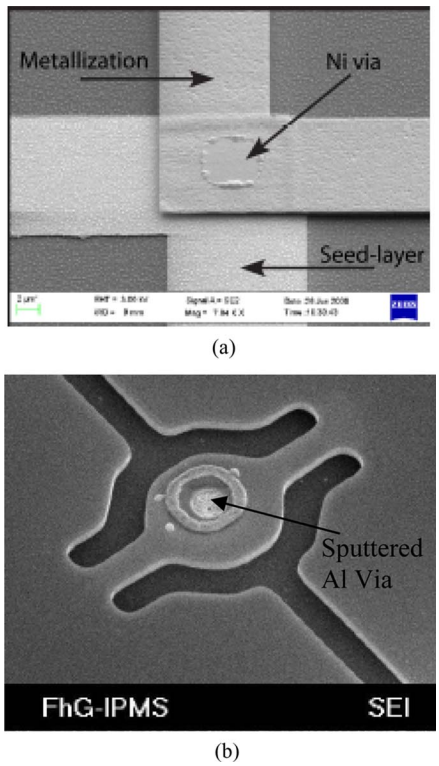


Fig. 13. (a) Examples of an electroless plated nickel via [98] and (b) 2-μm-diameter aluminum sputter deposited via [90] for very large scale via-last heterogeneous integration processes. Reprinted with permission from SPIE.

III. Heterogeneous Integration With Via-Last Processes

A. Basic Heterogeneous Integration Concepts Using Via-Last Processes

In this section, basic conceptual approaches of heterogeneous integration using via-last processes suitable for MOEMS, MEMS, and NEMS devices are discussed. Not all of the presented approaches have yet been implemented for MOEMS, MEMS, or NEMS devices. Fig. 12 shows a basic concept for

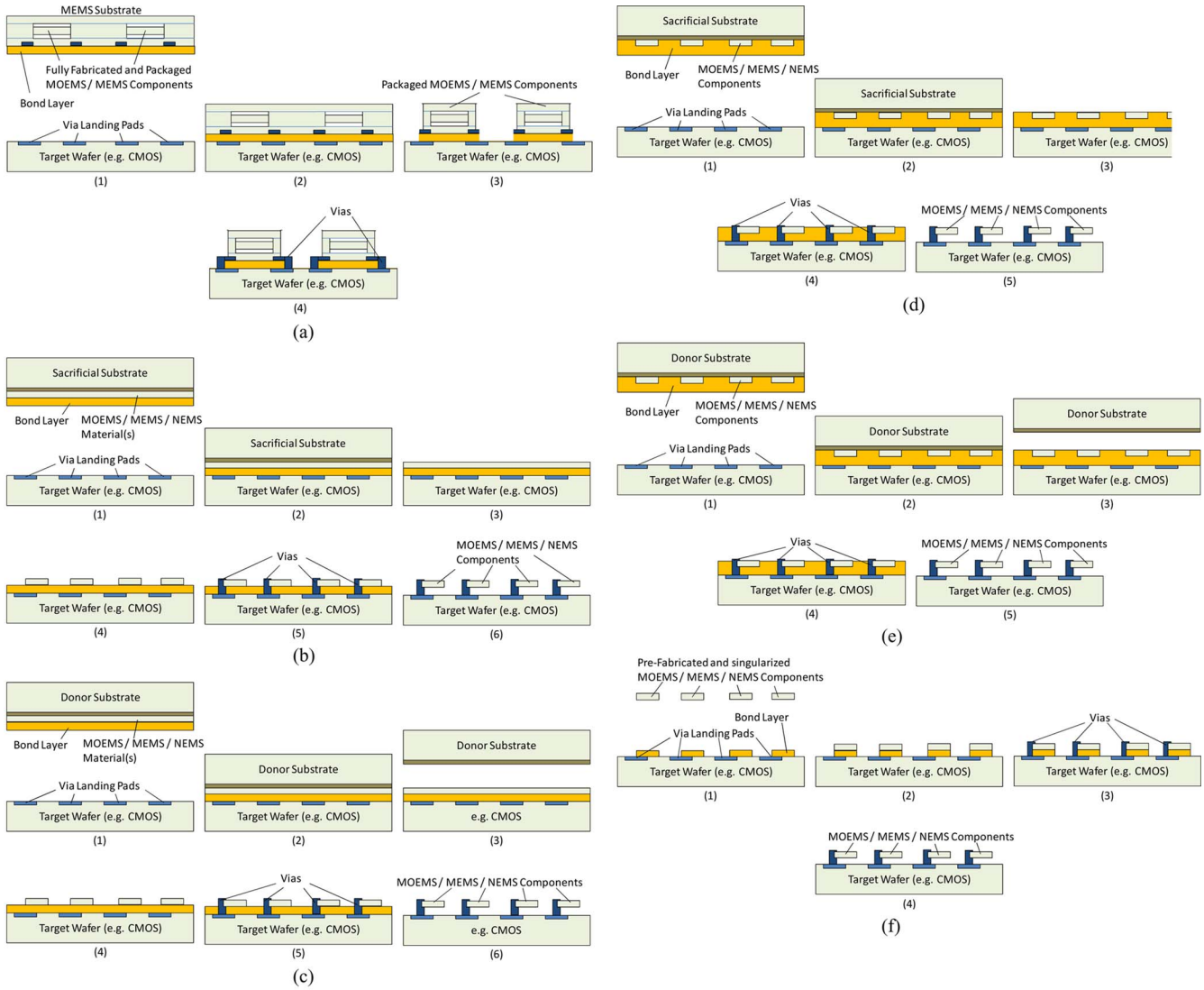


Fig. 14. Conceptual schemes of heterogeneous integration techniques using via-last processes. (a) Integration of fully processed and packaged MOEMS or MEMS components. (b) Integration of MOEMS, MEMS or NEMS materials(s), etching of sacrificial handle wafer and subsequent processing and definition of components. (c) Integration of MOEMS, MEMS or NEMS materials(s), material release from donor wafer and subsequent processing of components. (d) Full or partial processing of MOEMS, MEMS or NEMS components, integration and subsequent etching of sacrificial handle wafer. (e) Full or partial processing of MOEMS, MEMS or NEMS components, integration and subsequent component release from donor wafer. (f) Chip-to-wafer pick-and-place and self-assembly techniques in which the pre-fabricated MOEMS, MEMS or NEMS components are placed and fixed at their location on the target wafer by suitable means.

defining the electrical via contacts between the components on different substrates after bonding in via-last heterogeneous integration processes. Instead of electrical vias, optical vias can, in principle, be implemented in similar ways. In a first step, two substrates are bonded to each other with a defined intermediate bond layer as shown in Fig. 12(a) and (b). This can, in principle, be done with any suitable intermediate layer bonding technology using polymer [74]–[82] or inorganic intermediate layers [1], [83]–[87]. The intermediate bonding layer may also be patterned to provide localized bonding [74], [132]–[134]. The thickness control of the intermediate bond layer is critical as it defines the final gap distance between the target substrate and the MOEMS, MEMS, or NEMS components [88]–[90]. After bonding, via-holes are formed in substrate 2 by etching or any other suitable method to expose the via landing pads on substrate 1, as shown in Fig. 12(c). Thereafter, a metal is deposited inside the via-holes to establish an electrical contact between the via landing pads on substrate 1 and the components on substrate 2. The metal deposition may be done, for example, by sputter deposition [90]–[92], [94], [95], electroplating [96], [97] or electroless plating [93], [98], [99]. Various adhesive wafer bonding technologies in combination with via formation by sputter deposition [90]–[92], [94], [95], electroplating [96], [97] and electroless plating [93], [99] have been implemented for heterogeneous integration of MOEMS, MEMS, and NEMS devices. Bonding using planarized intermediate SiO_2 layers has also been implemented in combination with via formation by sputtering [100], [101]. The general advantage of via-last approaches is that they enable the implementation of extremely small vias with diameters of below 1 μm [102]. But also large vias with high aspect ratios can be implemented. Fig. 13 shows examples of vias with diameters of below 3 μm for MOEMS

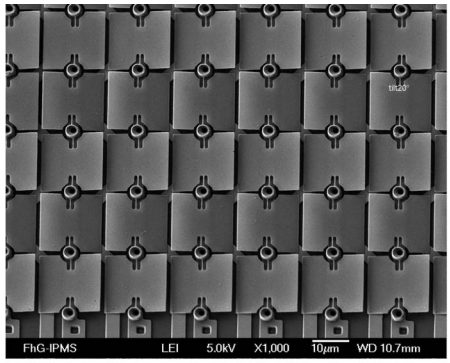
and MEMS devices that have been fabricated with electroless nickel plating [98] and with aluminum sputtering [90].

Fig. 14 shows six conceptual schemes of heterogeneous integration techniques using via-last processes that are suitable for MOEMS, MEMS, and NEMS devices.

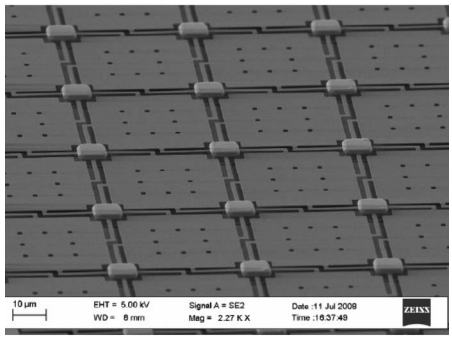
In the technique shown in Fig. 14(a), a completely processed and packaged MOEMS or MEMS component substrate is bonded to a target wafer, typically a CMOS IC wafer. Due the thickness of wafer containing packaged MOEMS or MEMS devices, this technique allows only limited integration densities and it has no obvious advantage as compared to pick-and-place chip-to-wafer bonding techniques or the comparable heterogeneous integration techniques using via-first processes shown in Fig. 3(a).

In the techniques shown in Fig. 14(b) and (c), a substrate containing the nonpatterned MOEMS, MEMS, or NEMS component material(s) is bonded to the target wafer. Thereafter, the handle substrate is either sacrificially removed [see Fig. 14(b)] or the material is released from the donor substrate [see Fig. 14(c)]. Removal of the sacrificial substrate can, for example, be done by etching processes, by grinding processes or by a combination of both. Component release from the donor substrate can, in principle, be done in various ways, including bond-interface decomposition by exposure with light [34]–[38] or etchants [103], by predetermined breaking points [65], [66] or by deliberately weak bond interfaces [67]–[69], [132]–[134]. After the MOEMS, MEMS, or NEMS component material is transferred, it can be further processed, patterned, and the vias between the components and the target wafer can be formed. Finally, the sacrificial bond layer is removed by a selective etch. Therefore, both ashing of polymers [88]–[97], [99] and vapor etching of SiO_2 [100], [101] has been used. The techniques shown in Fig. 14(b) and (c) have the advantage that no accurate substrate-to-wafer alignment during bonding is required. The via and the component positions on the target wafer are exclusively defined by the lithography and etching processes after bonding. Thus, critical device dimensions and overlay accuracies between NEMS components and structures on the target wafer can be achieved that are in the nm range, which is not easily possible with other techniques. This enables extremely accurate positioning of NEMS components on the target wafer. The processes shown in Fig. 14(b) and (c) have been proposed and implemented for heterogeneous integration of various MOEMS, MEMS, and NEMS devices [88]–[93], [96], [97], [99]–[101], [104]–[106], [109], [111], [112], [132]–[134].

In the techniques shown in Fig. 14(d) and (e), the MOEMS, MEMS, or NEMS components are partly fabricated on the handle substrate before the substrate is aligned and bonded to the target wafer. Thereafter, the process is essentially identical to the process shown in Fig. 14(b) and (c). The advantage of integrating partly prefabricating components, as compared to unpatterned material layers, is that more complex device designs can be implemented. However the penalty is that substrate-to-wafer alignment is required in the bonding process, which has limits in the achievable precision. Even with advanced alignment schemes repeatable alignment accuracies of below 1–2 μm are very challenging [79], [107], [108]. The process shown in Fig. 14(d) has been implemented for heterogeneous integration of MOEMS [94], [95], [113] and RF MEMS [110] devices.



(a)



(b)

Fig. 15. (a) Tilting monocrystalline silicon mirror array on CMOS driving electronics manufactured with a variation of the process shown in Fig. 14(b) [91], [92] and (b) piston-type monocrystalline silicon mirror array manufactured with the process shown in Fig. 16 [99].

In the technique shown in Fig. 14(f) prefabricated and singularized MOEMS, MEMS, or NEMS components are bonded to the target wafer by individual pick-and-place processes or by self-assembly processes. Thereafter, the vias are formed between the components and the via landing pads on the target wafer. Finally, the bond layer is sacrificially removed to form suspended MOEMS, MEMS, or NEMS devices. Self-assembly processes in combination with via last processes have been used for heterogeneous integration of various photonic and MEMS devices [114], [115]. Such processes are also reviewed and described in recent review papers [71]–[73].

In the following Section B, examples of heterogeneous integration platforms using via-last processes that have been implemented for MOEMS, MEMS, or NEMS devices are discussed.

B. MOEMS, MEMS, and NEMS Devices Implemented With Via-Last Heterogeneous Integration Platforms

1) Wafer-to-Wafer Heterogeneous Integration Platforms Using Via-Last Processes: A number of wafer-to-wafer heterogeneous integration platforms using via-last processes for MOEMS, MEMS, and NEMS devices have been implemented. Early demonstrations of via-first heterogeneous integration techniques for MOEMS and MEMS include infrared bolometer arrays [94], [95] and arrays of tilting micromirrors [88], [89]. For the infrared bolometer arrays the basic process shown in

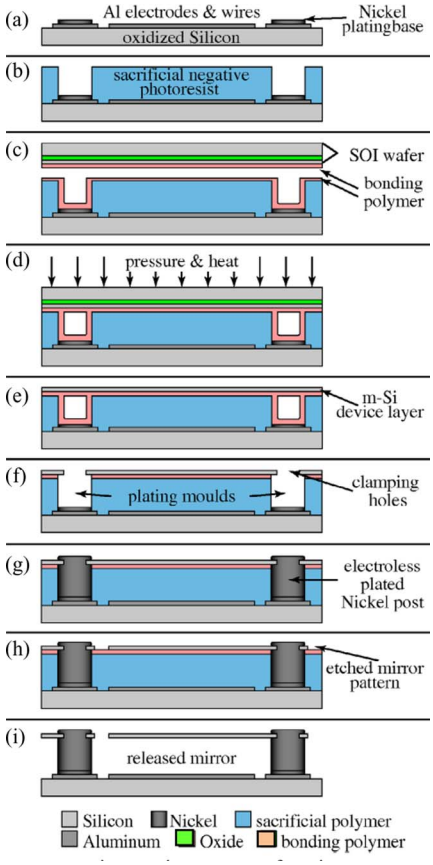


Fig. 16. Heterogeneous integration process for piston-type monocrystalline micromirror arrays shown in Fig. 15(b) [99].

Fig. 14(d) was used and for the micromirror arrays the basic process shown in Fig. 14(b) was used. In subsequent work, various demonstrator devices on fan-out wafers have been presented, including tilting and piston-type micromirror arrays made of monocrystalline silicon [90], [99], hidden-hinge micromirror arrays made of two stacked monocrystalline silicon layers [93], and uncooled infrared bolometer arrays made of high-performance sensor materials [97], [116]–[122]. The first MEMS device that includes fully functional CMOS ICs and that has been manufactured using very large scale heterogeneous system integration with the via-last approach is a 1-megapixel monocrystalline silicon micromirror array shown in Fig. 15(a) [91], [92]. In all cases, a polymer adhesive has been used as the bonding layer in combination with sputter-deposited aluminum vias [90]–[92], electroplated gold vias [97], or electroless plated nickel vias [93], [99]. Bonding with a polymer adhesive has the advantage that the MOEMS/MEMS/NEMS wafer and the CMOS IC wafer can be bonded with very high yield and without any surface pretreatment or surface planarization. Planarized SiO_2 layers have also been proposed a intermediate bonding layer for heterogeneous MOEM/MEMS integration [100], [101], [113]. All these approaches have been termed as Silicon-On-Integrated-Circuit (SOIC) technologies [81].

Fig. 15(b) shows a SEM image of a piston-type [99] monocrystalline silicon micromirror array and Fig. 16 depicts an example of a detailed process flow for the integration of

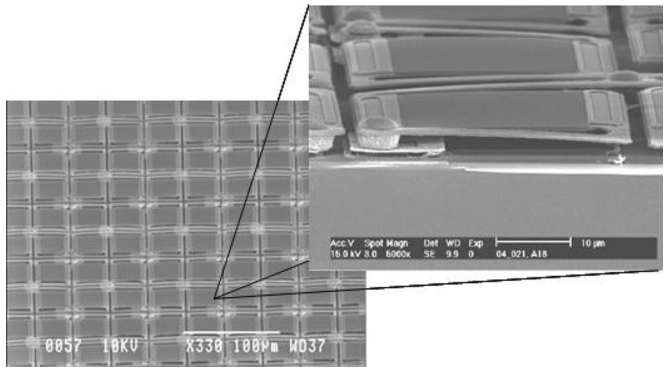


Fig. 17. Infrared bolometer array manufactured with the wafer-level via-last heterogeneous integration platform shown in Fig. 14(b) [96]. Reprinted with permission from SPIE.

the piston-type monocrystalline silicon micromirror array [99] shown in Fig. 15(b). The tilting monocrystalline silicon mirrors in Fig 15(a) are integrated on top of fully functional high-voltage CMOS driving electronics. The mirror array has a resolution of 1 megapixel and a pixel pitch of 16 μm $\times$ 16 μm. The silicon mirror membranes are 340-nm thick and have an extremely well-defined distance of 700 nm to the addressing electrodes on the underlying CMOS ICs. The mirror vias have a diameter of 2 μm and the torsional mirror hinges are 600 nm wide. The piston-type mirror array consists of 96$\times$96 mirrors with a pitch of 40 μm $\times$ 40 μm, 340-nm thick silicon mirror membranes and electroless-plated nickel vias. Fig 17 shows an image of an infrared bolometer array on a silicon fan-out wafer [96]. The infrared bolometer array consists of 320 $\times$ 240 pixels with a pixel pitch of 40 μm $\times$ 40 μm and 3 μm diameter electroplated gold vias.

Wafer-level via-last heterogeneous integration technologies have recently also been implemented for the integration of SMA sheets into MEMS actuators [105] and for various microwave frequency MEMS devices, including tunable RF metamaterials [106], RF phase shifters [109], PTZ microswitches [110] and RF filters and resonators [111], [112]. Fig. 18 shows an example of a RF metamaterial with electrostatically actuated silicon–gold membranes that are integrated on top of a substrate with an embedded reflective metal layer [106].

In addition, heterogeneous integration techniques have been proposed for the integration of graphene membranes into NEMS devices [132]–[134]. In these approaches, localized bonding with patterned intermediate bonding layers [74], 132]–[134] has been used to obtain suspended graphene membranes without the need for etching the intermediate bonding layer underneath the graphene membranes. These types of via-last heterogeneous integration technologies are extremely attractive and promising candidates for large-scale implementation of emerging graphene-based NEMS.

2) Wafer-to-Wafer Component Distribution and Chip-to-Wafer Heterogeneous Integration Platforms Using Via-Last Processes: To address the previously discussed shortcomings of wafer-to-wafer heterogeneous integration platforms with respect to cost and wafer-size incompatibilities for some

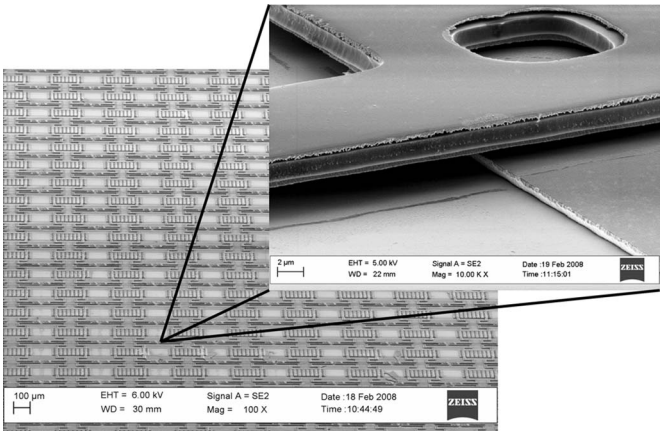


Fig. 18. Tunable metamaterial manufactured with wafer-level via-last heterogeneous integration platform shown in Fig. 14(b) [106].

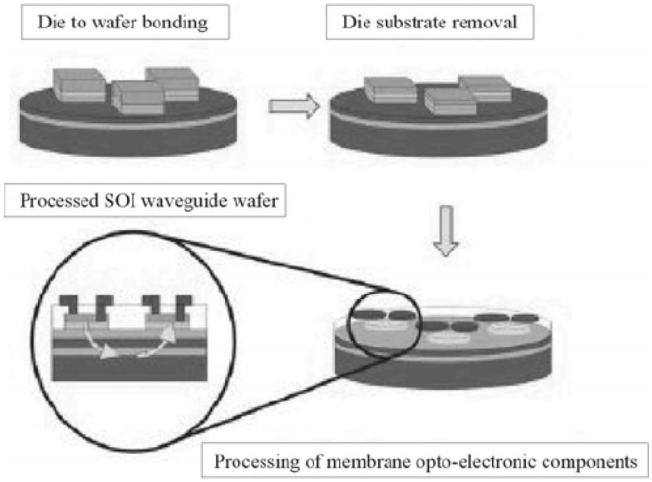


Fig. 19. Die-to-wafer placement of component materials and subsequent wafer-level bonding, processing, and interconnecting the integrated components [122].

applications, a number of modified approaches using via-last processes have been proposed.

An elegant solution for via-last heterogeneous integration of expensive III–V materials that are only available in small wafer sized onto standard-sized silicon wafers is shown in Fig. 19 [87], [122]–[128]. In this approach, nonpatterned dies (parts of a wafer) that contain the photonic layers of interest are placed on a polymer coated silicon target wafer in the areas were the components are needed. This can be done by inexpensive high-speed pick-and-place processes since only very low placement accuracies are required. After the dies are bonded, they are thinned, and subsequently patterned and etched using wafer-level processes to form the photonic devices. This solution also lessens problems caused by differences of thermal expansion between III–V and Si wafer materials during wafer bonding. The approach shown in Fig. 19 has so far only been implemented for the integration of photonic devices on top of silicon-based waveguide structures [87], [122]–[128], but it is, in principle, also an attractive approach for MOEMS, MEMS, and NEMS devices. An alternative approach that addresses the problem of integrating wafers of different sizes and/or wafers with different coefficients of thermal expansion in a cost-efficient way is the use of expandable handle substrates [129].

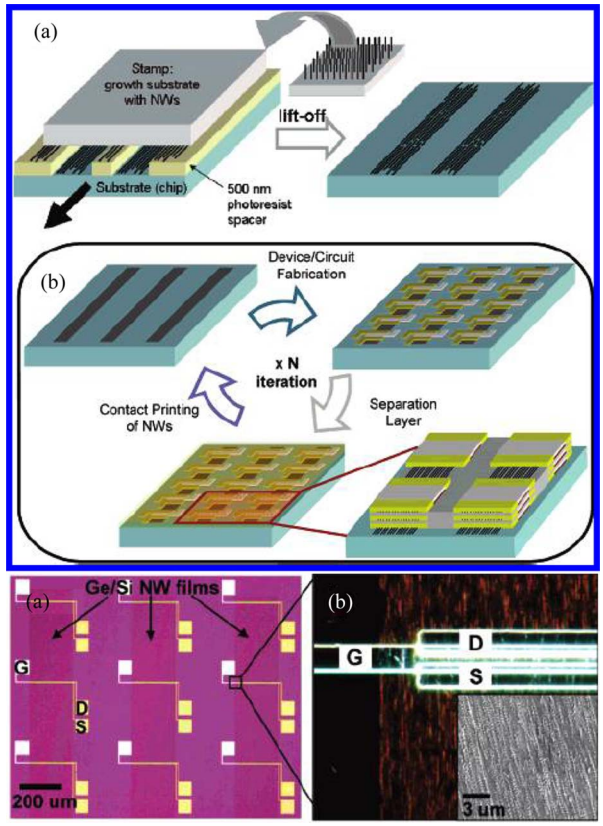


Fig. 20. Stamp-transfer of nanomaterials to predefined areas with polymer layers by mechanical release and subsequent contact metallization [65]. Reprinted with permission from ACS.

Other material-transfer approaches compatible with via-last processes include the integration of SMA metal wires on silicon wafers using wire frames [130] or wire bonders [131].

Furthermore, a number of transfer printing and stamping transfer methods using via-last processes have been proposed [65]–[69]. Fig. 20 shows a particular interesting process in which nanomaterials such as nanowires or carbon nanotubes (CNT) can be transferred with the help of a stamp to predefined areas covered by a polymer on a target wafer [65]. The polymer defines the areas were the nanomaterial is released from the stamp and transferred to the target wafer. Thereafter, the nanomaterials are electrically connected to the target wafer by Cr/Au metallization. The demonstrated devices are electronics but this approach is also applicable for integrating NEMS devices. Self-assembly processes have also been implemented for via-last heterogeneous integration of various MOEMS, MEMS, and NEMS devices [53], [71]–[73], [114], [115].

IV. Discussions

A large variety of heterogeneous integration technologies are available and they can conceptually be divided into via-first and via-last processes. Each of the proposed techniques has specific advantages and disadvantages. Via-first processes are currently

more mature and commercial devices based on some of these technologies are already in very high-volume production today [17], [57], [58]. The main advantages of via-first processes are that the MOEMS or MEMS components can be completely manufactured prior to bonding and integration and that the integration can essentially be done in a single-step bonding process. Disadvantages of via-first processes are that they all require aligned substrate-to-wafer bonding, which adds process complexity and has limitations in the achievable post-bond alignment accuracies. Also, the implementation of reliable via bonding processes for vias with dimensions of below 10 μm seems challenging. In contrast, via-last processes have not yet reached high-volume production status. However, they hold promise for MOEMS, MEMS, and NEMS with extremely small device dimensions in the nanometer range, very small via dimensions in the sub-micrometer range and placement accuracies of the components on the target wafer in the nanometer range. The distance between the device membrane and the substrate surface can be accurately defined in a large interval between below 100 nm and several tenths of micrometer by the thickness of the intermediate bond-layer. In addition, via-last integration schemes that rely on wafer bonding processes that have no precise substrate-to-wafer alignment requirements can be less complex and costly.

For some applications, wafer-to-wafer heterogeneous integration technologies may not be a cost-efficient solution. As discussed in the previous sections, this is, for example, the case in situations where the manufacturing yield of the components on one or on both of the wafers are low, where the components on the two wafers are very different in size and/or where the components on both wafers are complex and expensive. Also, some materials such as photonic III–V materials may not be available in standard silicon wafer sizes. These problems are being addressed by emerging heterogeneous integration platforms that are being developed, including wafer-to-wafer selective component distribution (MD) [35]–[38], chip-to-wafer pick-and-place integration [87], [122]–[128], expandable handle substrates [129], transfer stamping [65]–[69], and self-assembly processes [53], [71]–[73], [114], [115].

It is remarkable that heterogeneously integrated MEMS devices have recently emerged and succeeded in very competitive markets such as for very high-volume consumer applications [17], [57], [58]. Some of the contributing factors to this commercial success of heterogeneous integration technologies are their compatibility with fables MEMS business models, the ability to use standard CMOS ICs from various sources and the possibility to shrink the overall MEMS device dimensions, which enables the combination of multiple sensors on a highly integrated single chip. Most wafer-level heterogeneous integration technologies allow the placement of the electronic circuits and the MOEMS, MEMS, or NEMS components on top of each other on the same chip area. In the case of capacitive MEMS sensors, the MEMS sensing electrodes can be significantly reduced in size while maintaining the sensitivity because of the close proximity of the sensor electrodes and the capacitive read-out electronics reduces parasitic capacitances. Thus, the overall device dimensions, and consequently, their cost can be reduced. In addition, an infrastructure with several MEMS foundries has emerged in recent years that has made fables MEMS business models viable. Existing MEMS foundries include Dalsa Semiconductor, Micralyne, Silex Microsystems, Asia Pacific Microsystems (APM), IMT, Tronics Microsystems, and others [135], and many of the foundries offer wafer-level heterogeneous integration platforms to their customers.

V. Conclusion

Heterogeneous integration technologies allow the combination of different high-performance materials and subsystems to form advanced MOEMS, MEMS, and NEMS devices. Thus, heterogeneous integration technologies enable, for example, the integration of high-performance MOEMS, MEMS, and NEMS components on top of standard, foundry-based CMOS ICs or silicon-based photonic waveguide platforms. No compromise in the material selection has to be made and the same chip area can be used very efficiently both for the MOEMS, MEMS, or NEMS parts and for the electronic or photonic parts. These features will enable future complex, heterogeneous MOEM, MEMS and NEMS solutions with high integration densities and high performances.

Acknowledgment

The authors thank their colleagues at the Microsystem Technology Laboratory at KTH-Royal Institute of Technology, Stockholm, Sweden, for many fruitful discussions.

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Martin Lapisa received the "Diplomingenieur der Mikrosystemtechnik" (Diploma) degree from the Department of Microsystems Engineering (IMTEK), University of Freiburg i.Br., Freiburg, Germany, in 2006. He is currently working toward the Ph.D. degree in 3-D MEMS integration in the Microsystem Technology Laboratory, KTH-Royal Institute of Technology, Stockholm, Sweden.

Göran Stemme (F'06) received the M.Sc. degree in electrical engineering in 1981 and the Ph.D. degree in solid-state electronics in 1987, both from the Chalmers University of Technology, Gothenburg, Sweden.

In 1981, he joined the Department of Solid State Electronics, Chalmers University of Technology, where, in 1990, he became an Associate Professor (Docent) heading the silicon sensor research group. In 1991, he was appointed Professor at KTH-Royal Institute of Technology, Stockholm, Sweden, where he currently heads the Microsystem Technology Laboratory, School of Electrical Engineering. His current research interests include microsystem technology based on micromachining of silicon. He has authored or coauthored more than 260 research journal and conference papers. He has more than 22 patent proposals or granted patents.

Dr. Stemme is a member of the Royal Swedish Academy of Sciences (KVA).

Frank Niklaus (M'09) received the M.Sc. degree in mechanical engineering from the Technical University of Munich (TUM), Munich, Germany, in 1998, and the Ph.D. degree in MEMS from KTH-Royal Institute of Technology, Stockholm, Sweden, in 2002.

He was a Consultant for industry and a Visiting Scholar at the Rensselaer Polytechnic Institute, Troy, NY, where he was working with 3D-IC technologies. He is currently an Associate Professor in the Microsystem Technology Laboratory, KTH-Royal Institute of Technology, where he is the Leader of the Micro- and Nanosystem Integration Group.