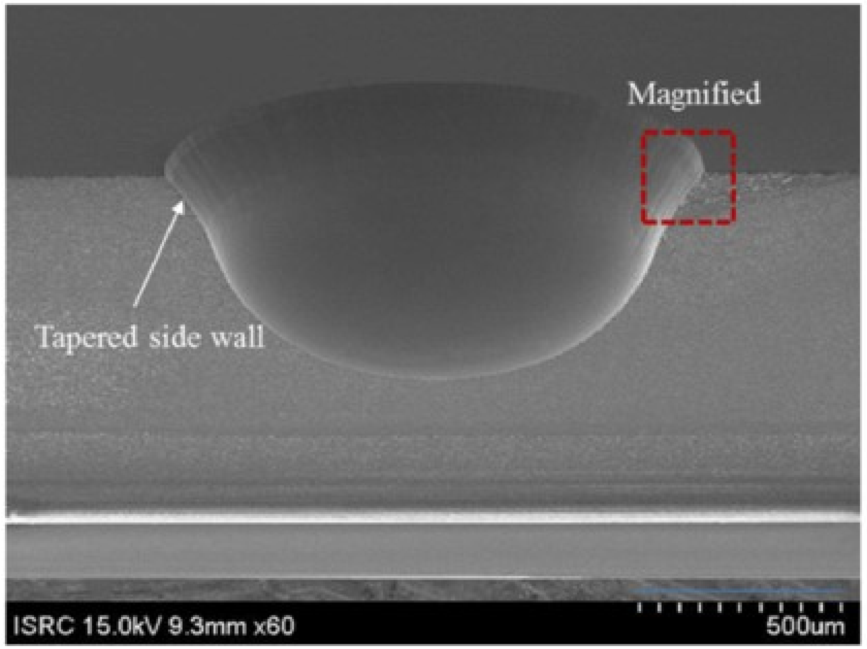
Deep Reactive Ion Etching

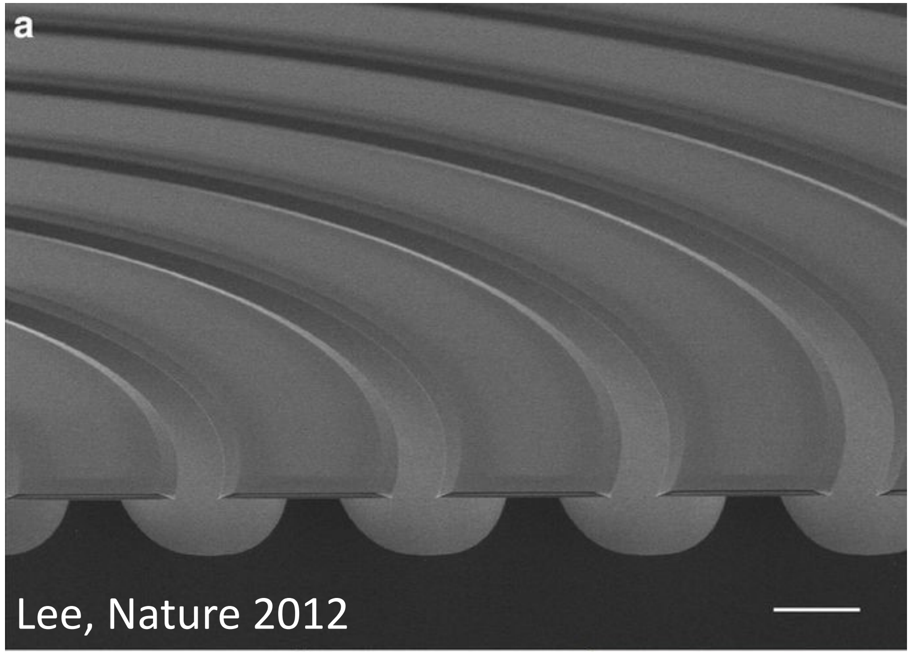
Joey Greenspun

Wet

Dry

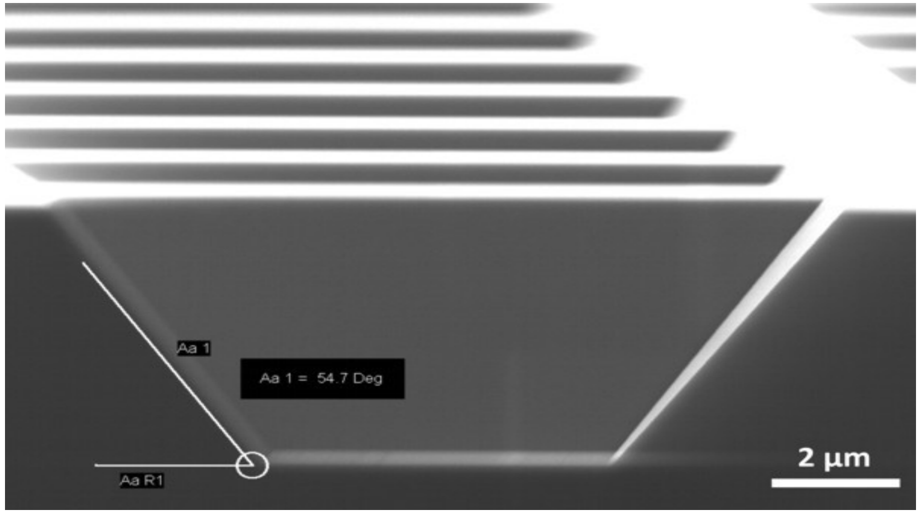
Isotropic

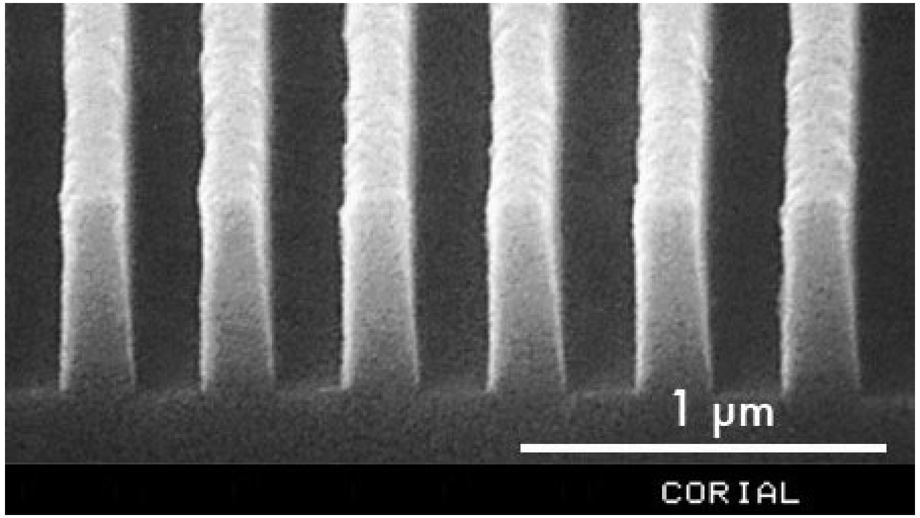




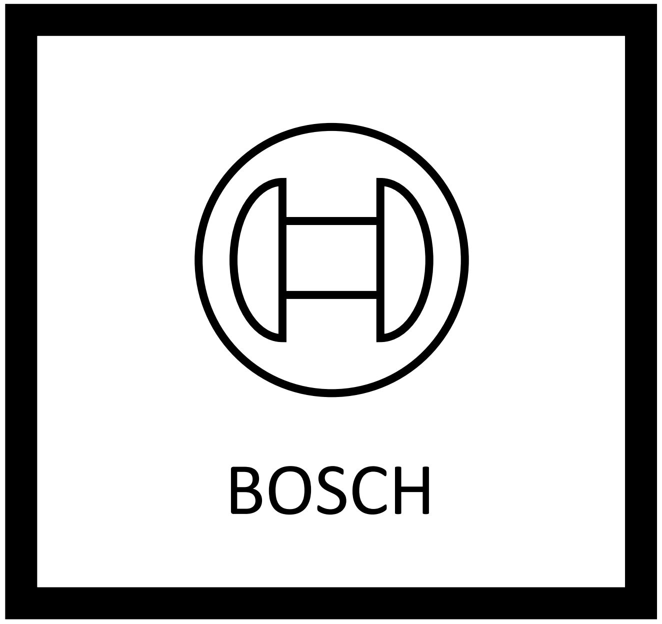
Lee, Nature 2012

Anisotropic

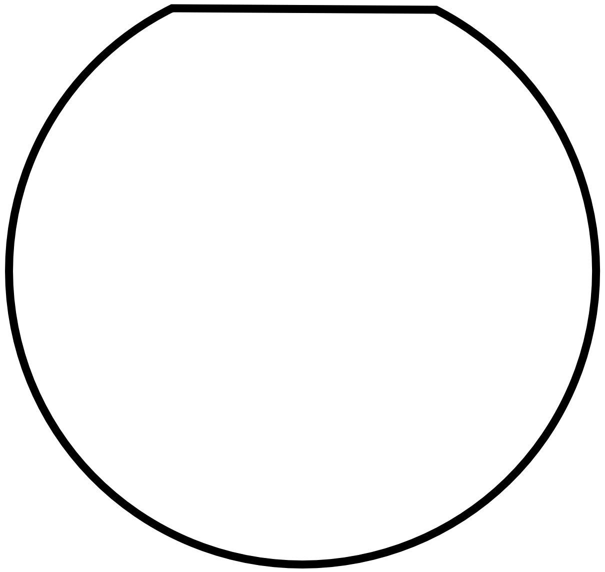




DRIE Goal: Etch deep, arbitrary features into silicon



Mask
(Black is Chrome)



Wafer

DRIE Goal: Etch deep, arbitrary features into silicon

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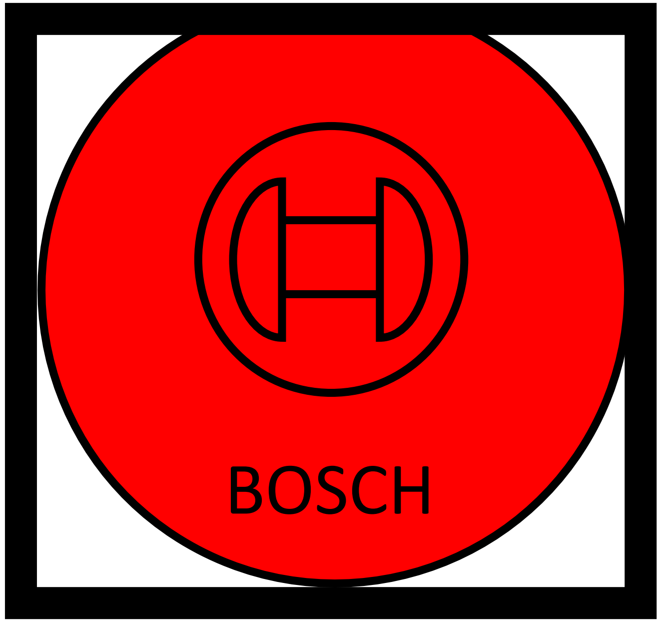
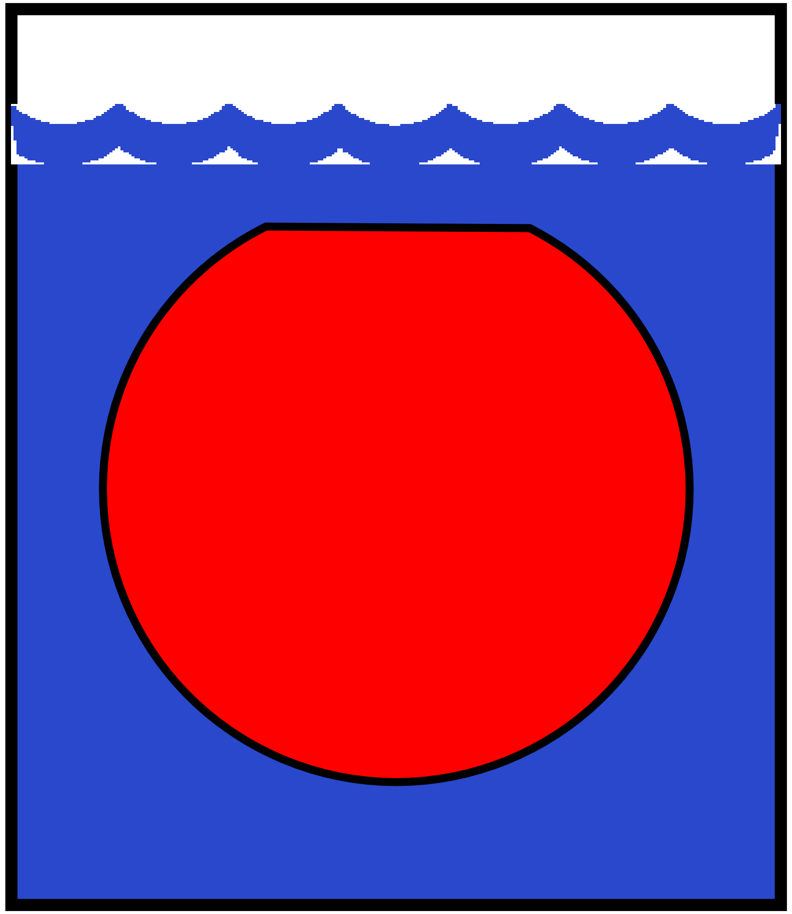


DRIE Goal: Etch deep, arbitrary features into silicon

BOSCH

DRIE Goal: Etch deep, arbitrary features into silicon



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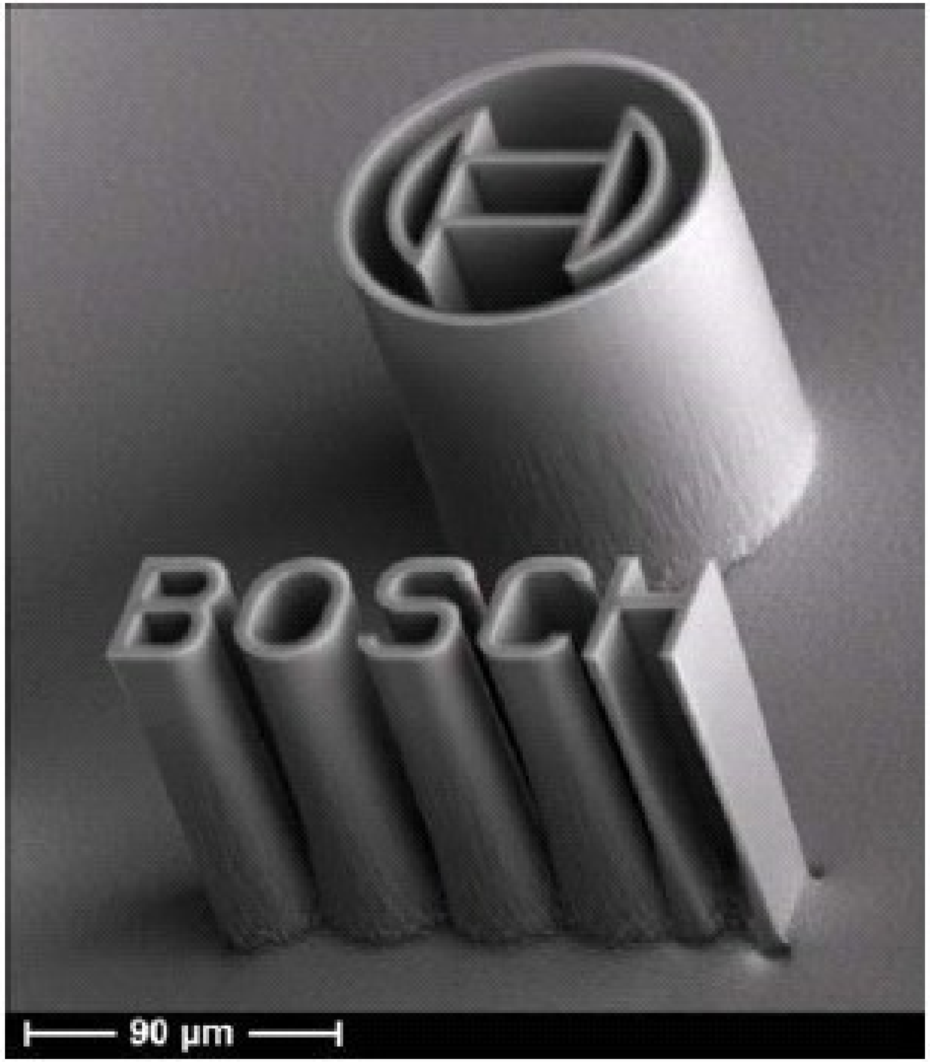
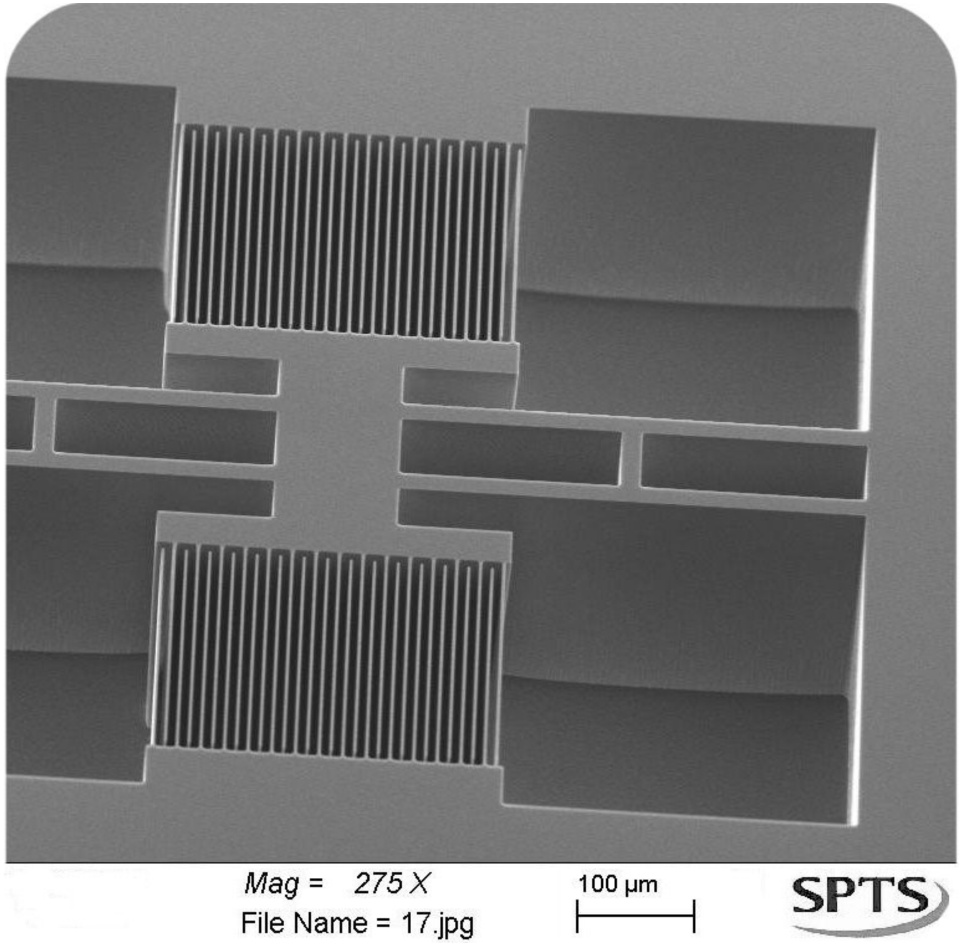
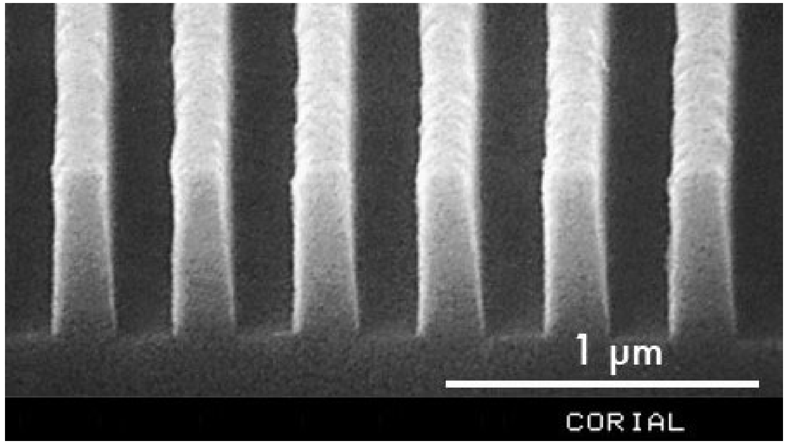


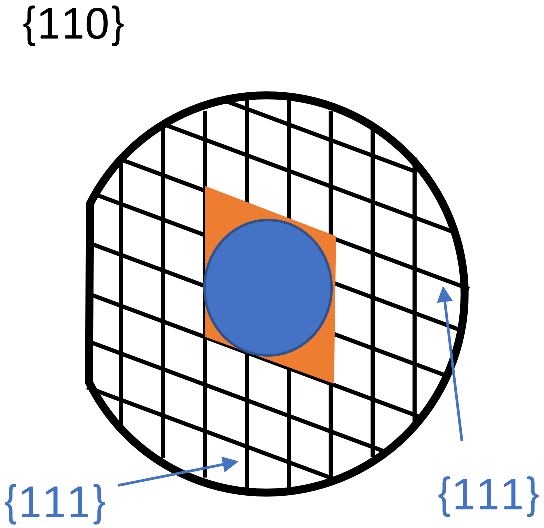


Goal: Etch deep, arbitrary features into silicon

Silicon Plasma Etch (RIE)



KOH with {110} wafers



Pro: Arbitrary features

Con: Limited aspect ration (~10:1)
Hard to etch deep (selectivity issues)

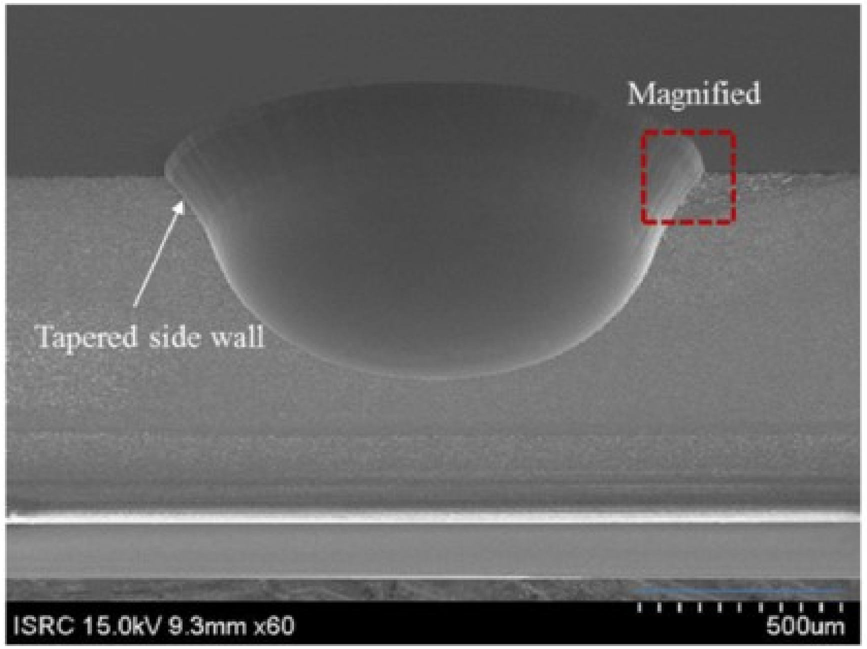
Pro: High aspect ratio > 600:1

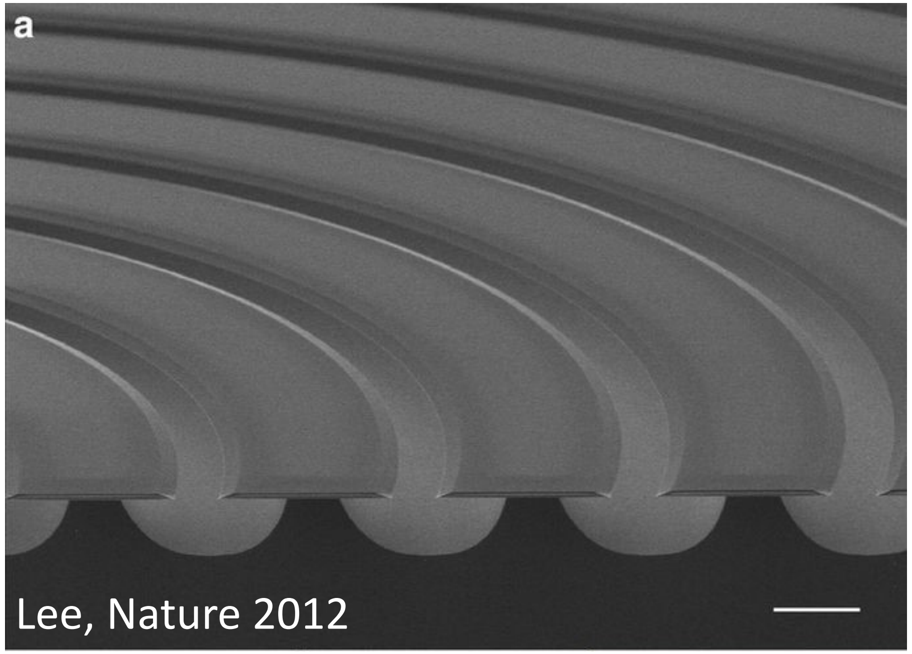
Con: Extremely limited features

Wet

Dry

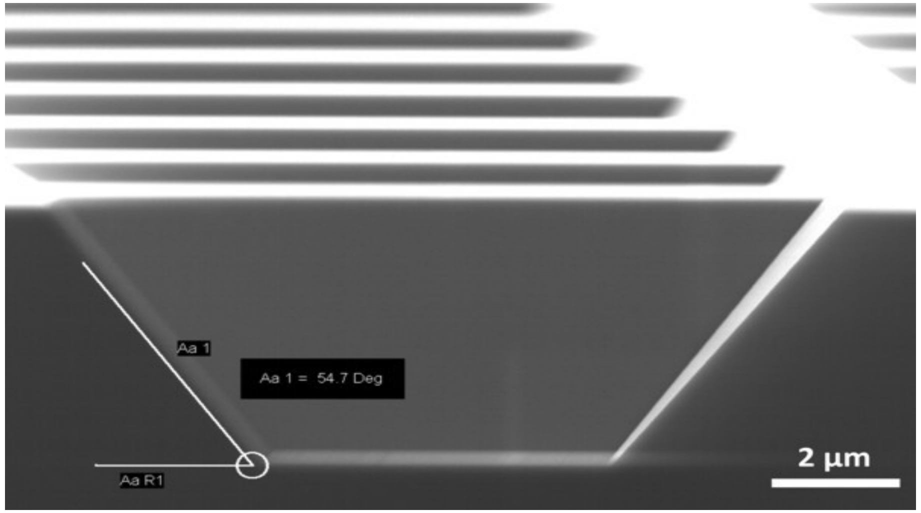
Isotropic

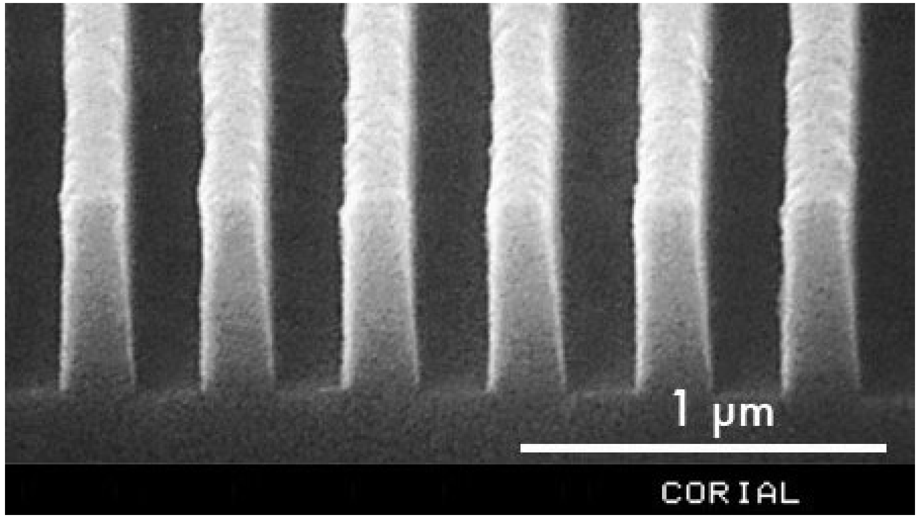




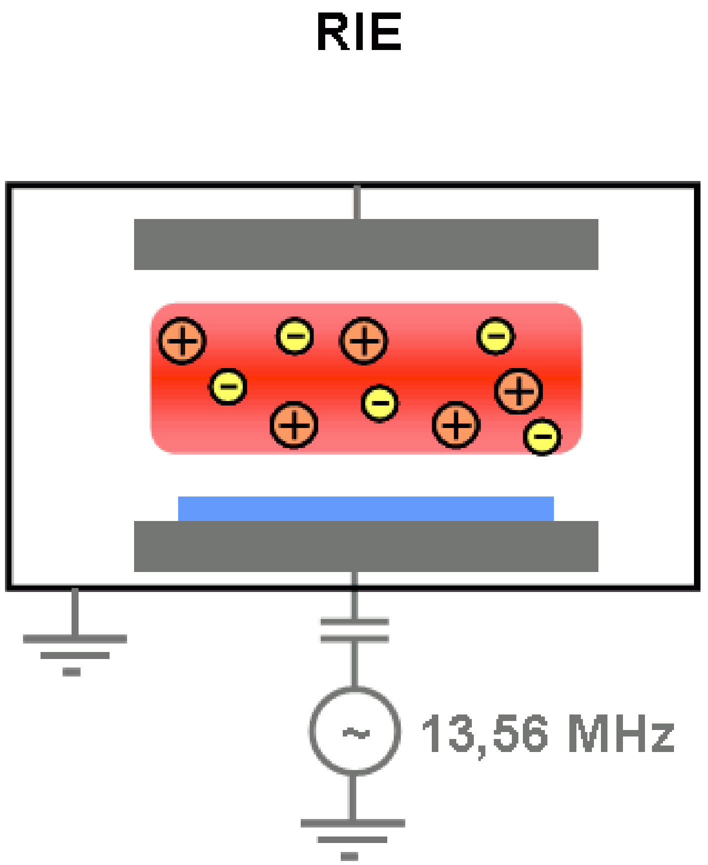
Lee, Nature 2012

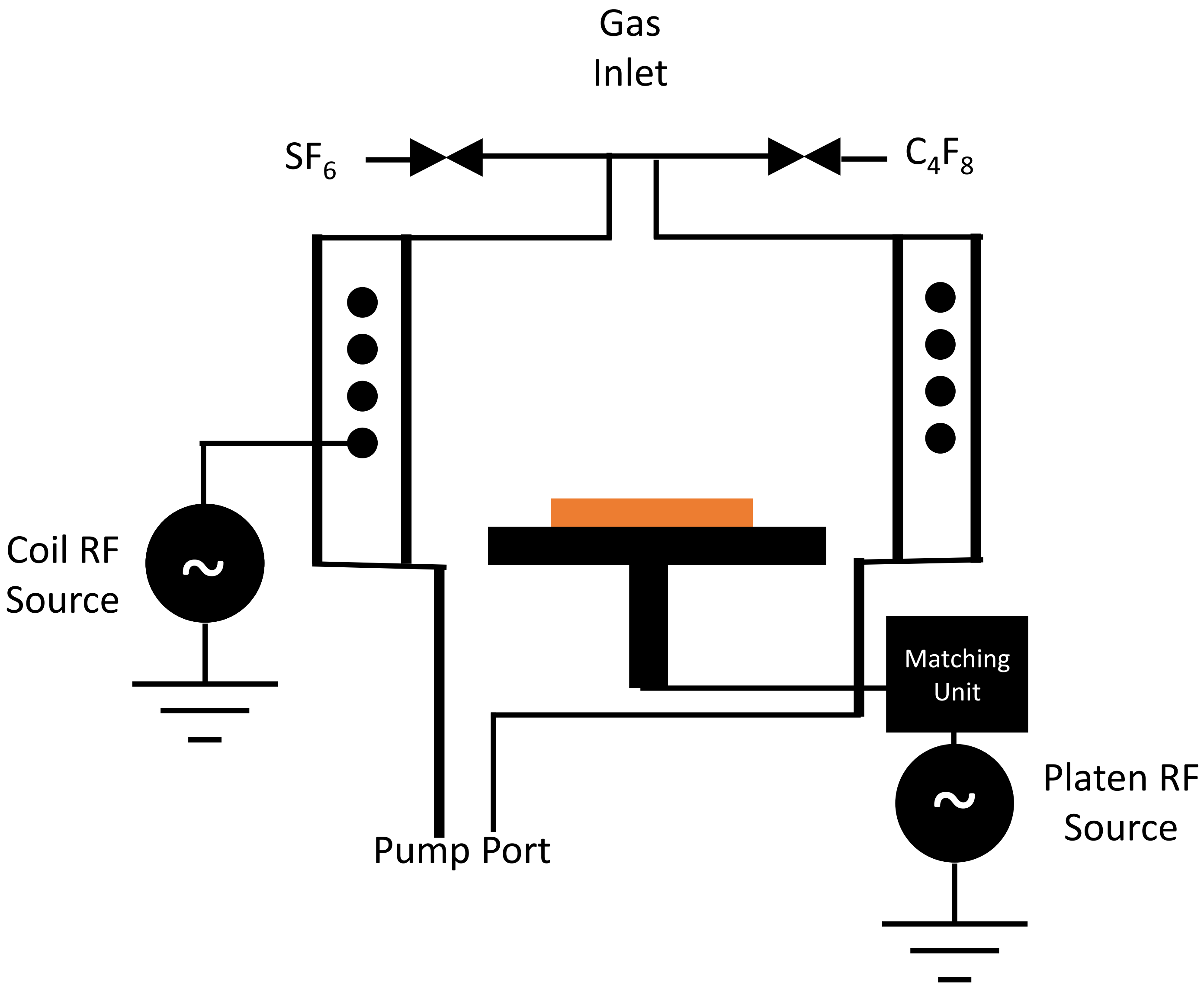
Anisotropic





Deep Reactive Ion Etching





Deep Reactive Ion Etching

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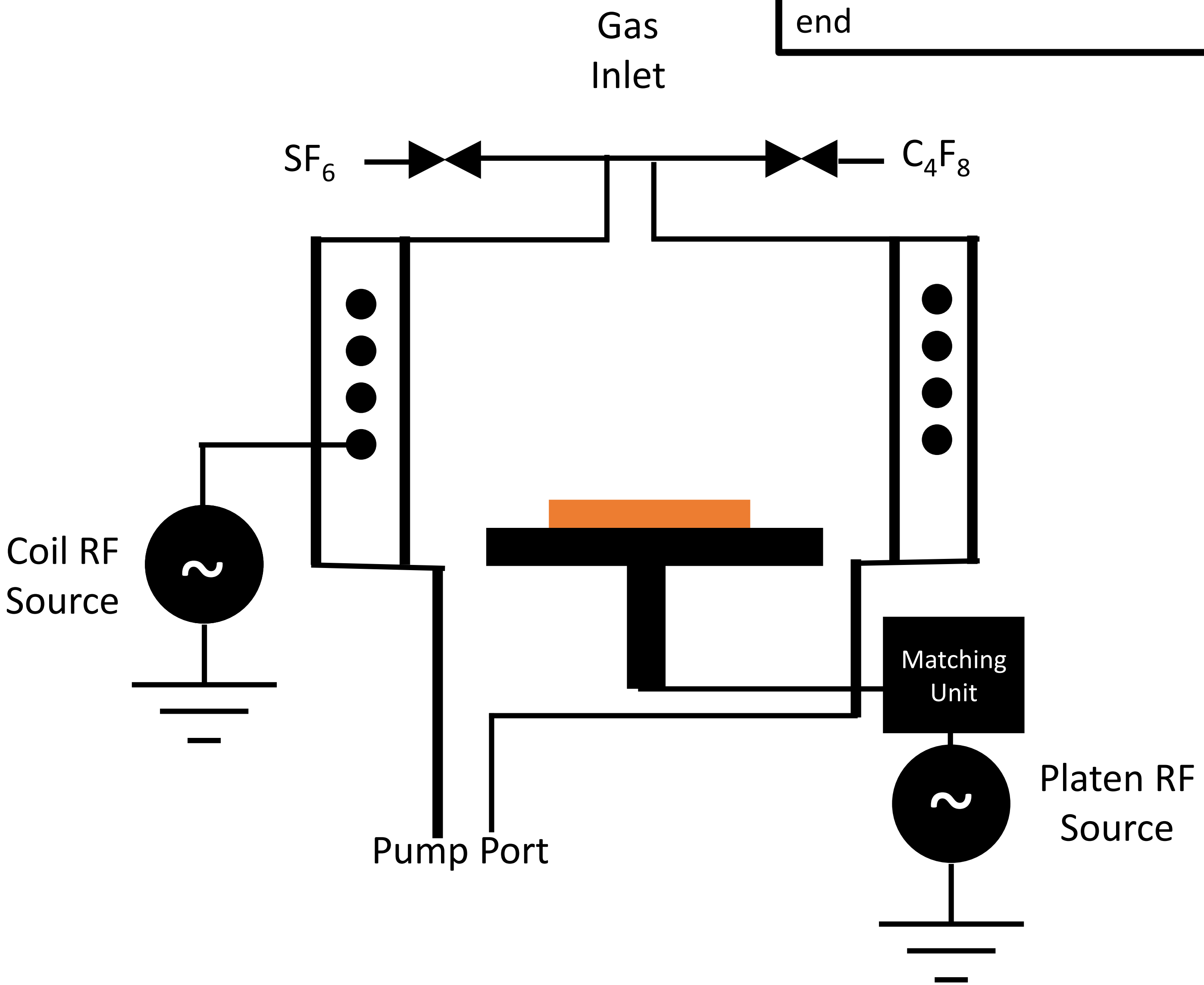

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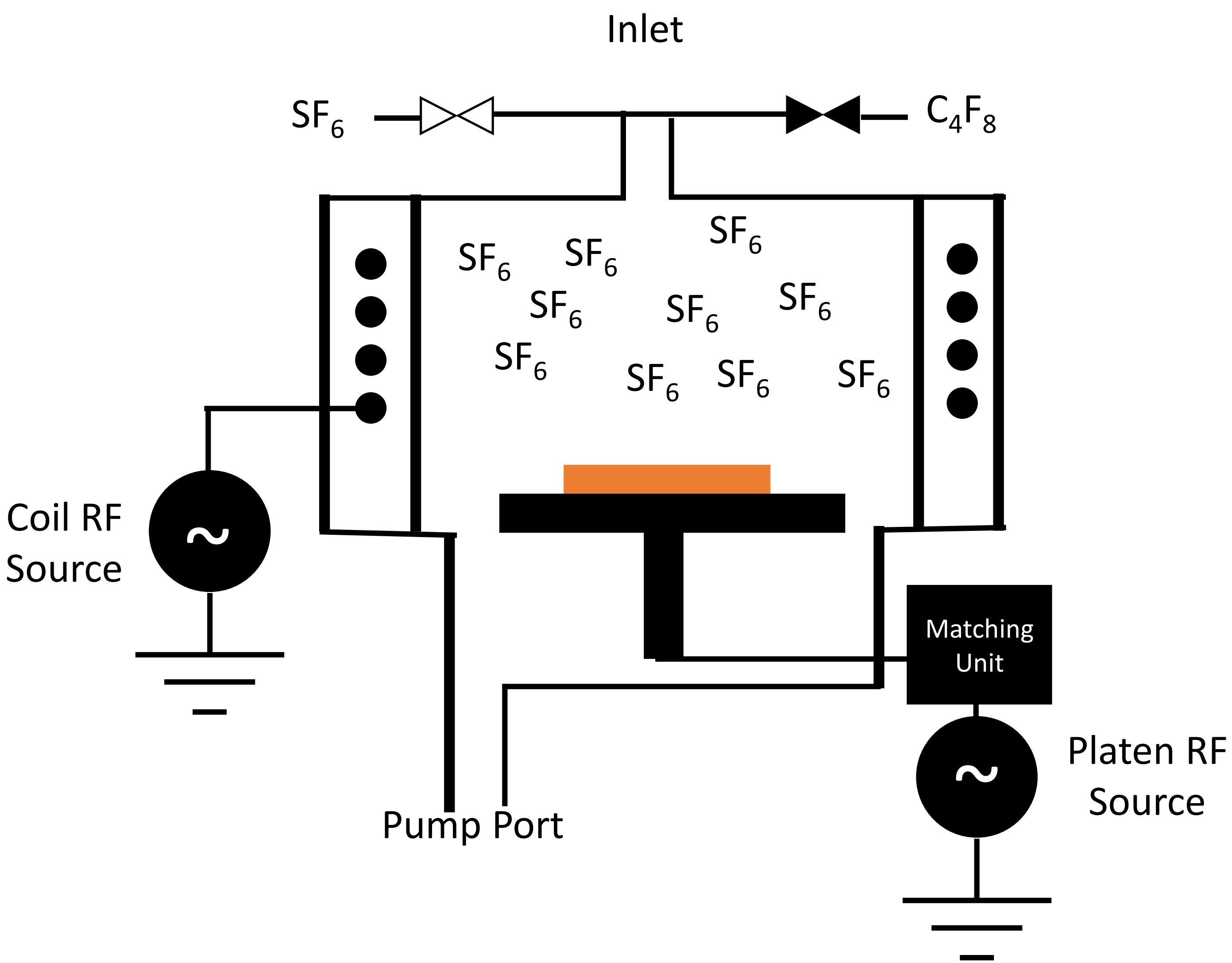

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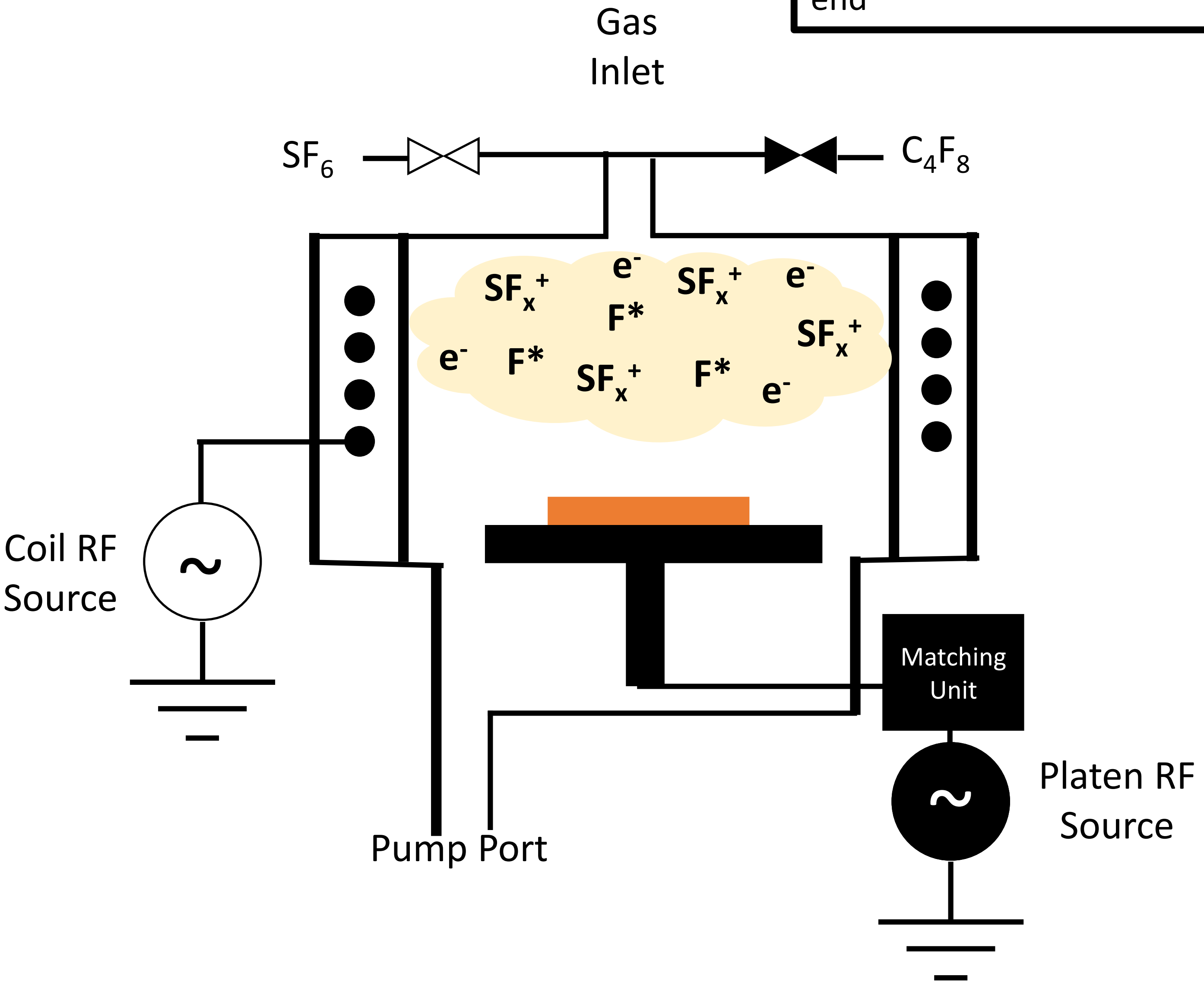

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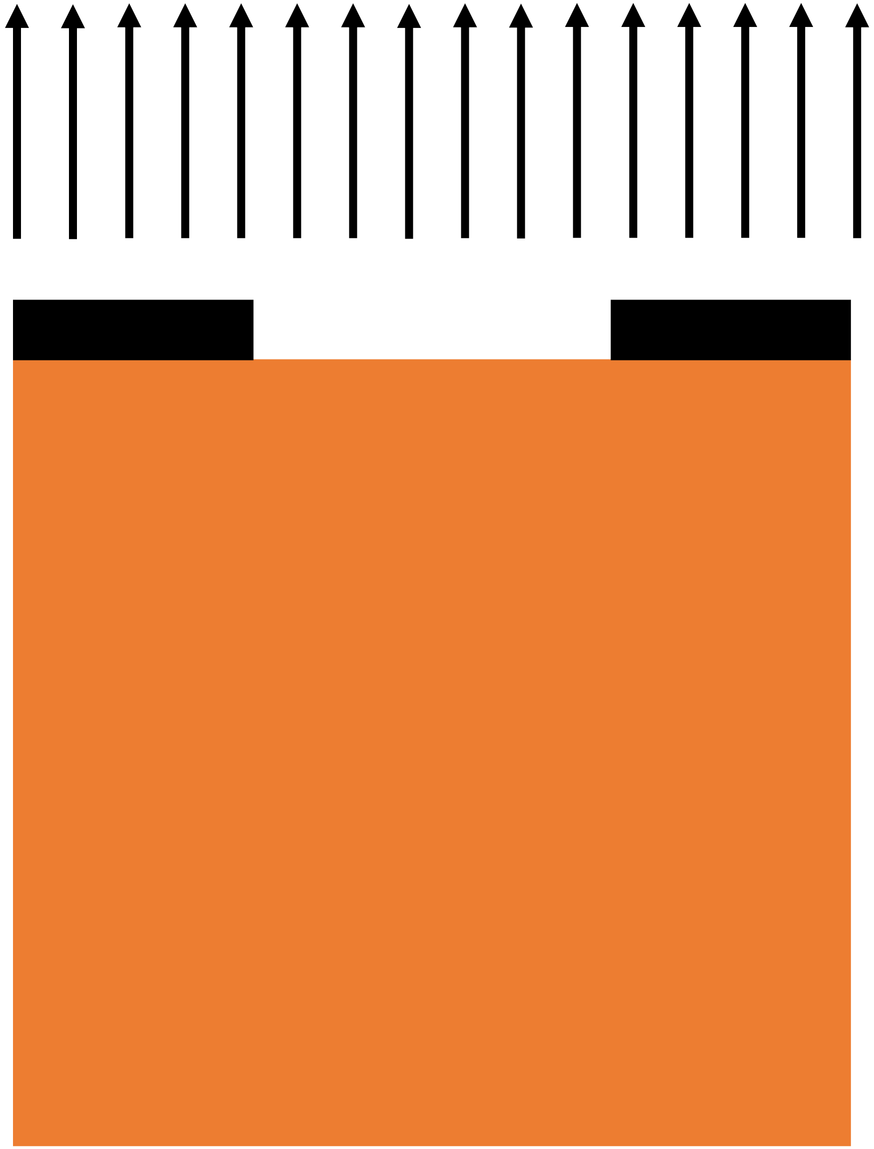

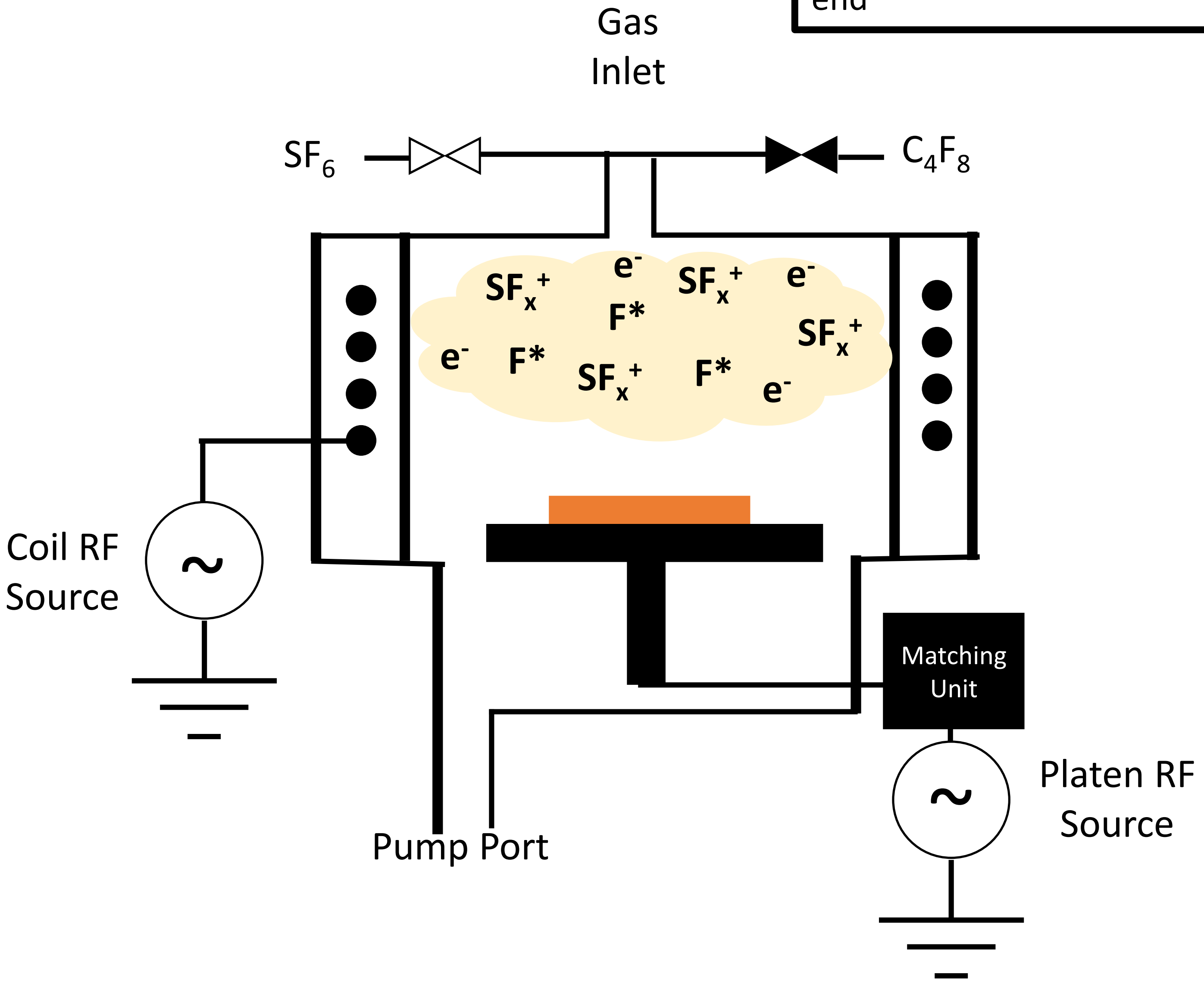

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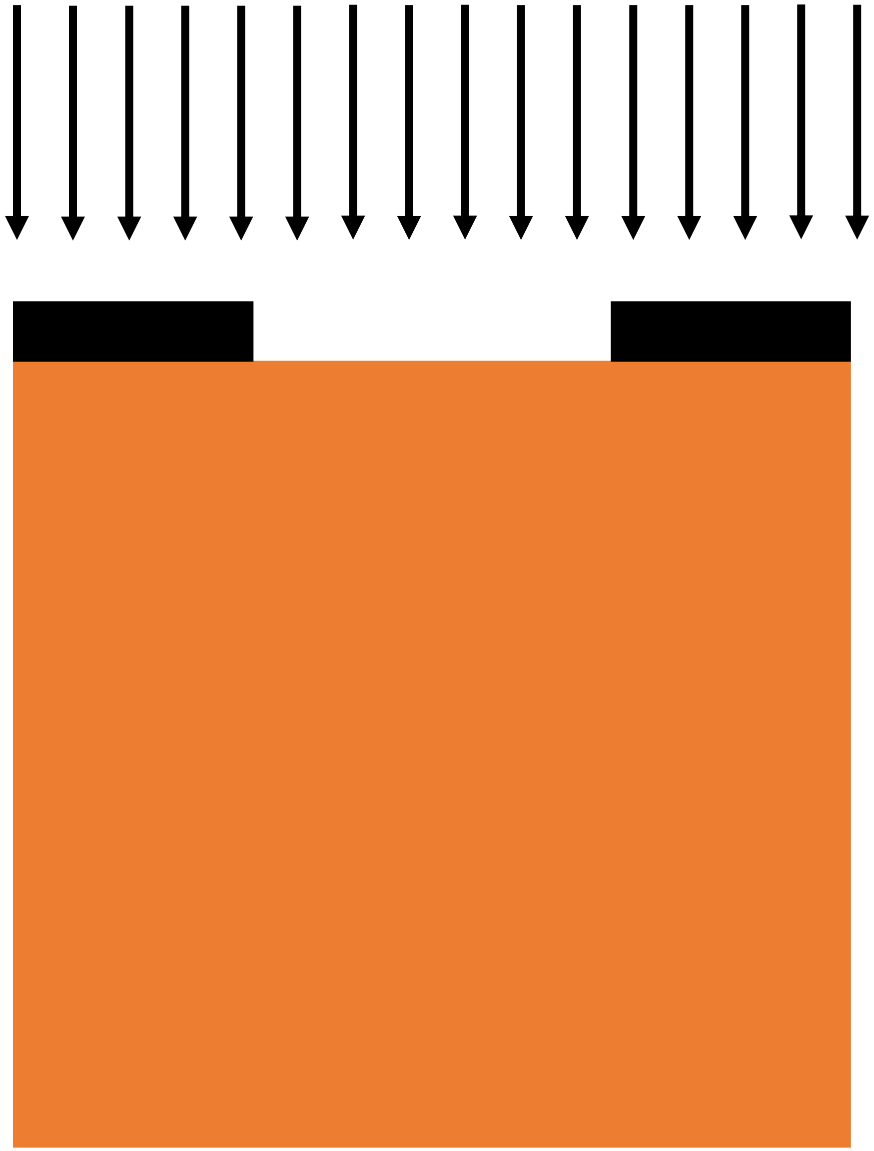

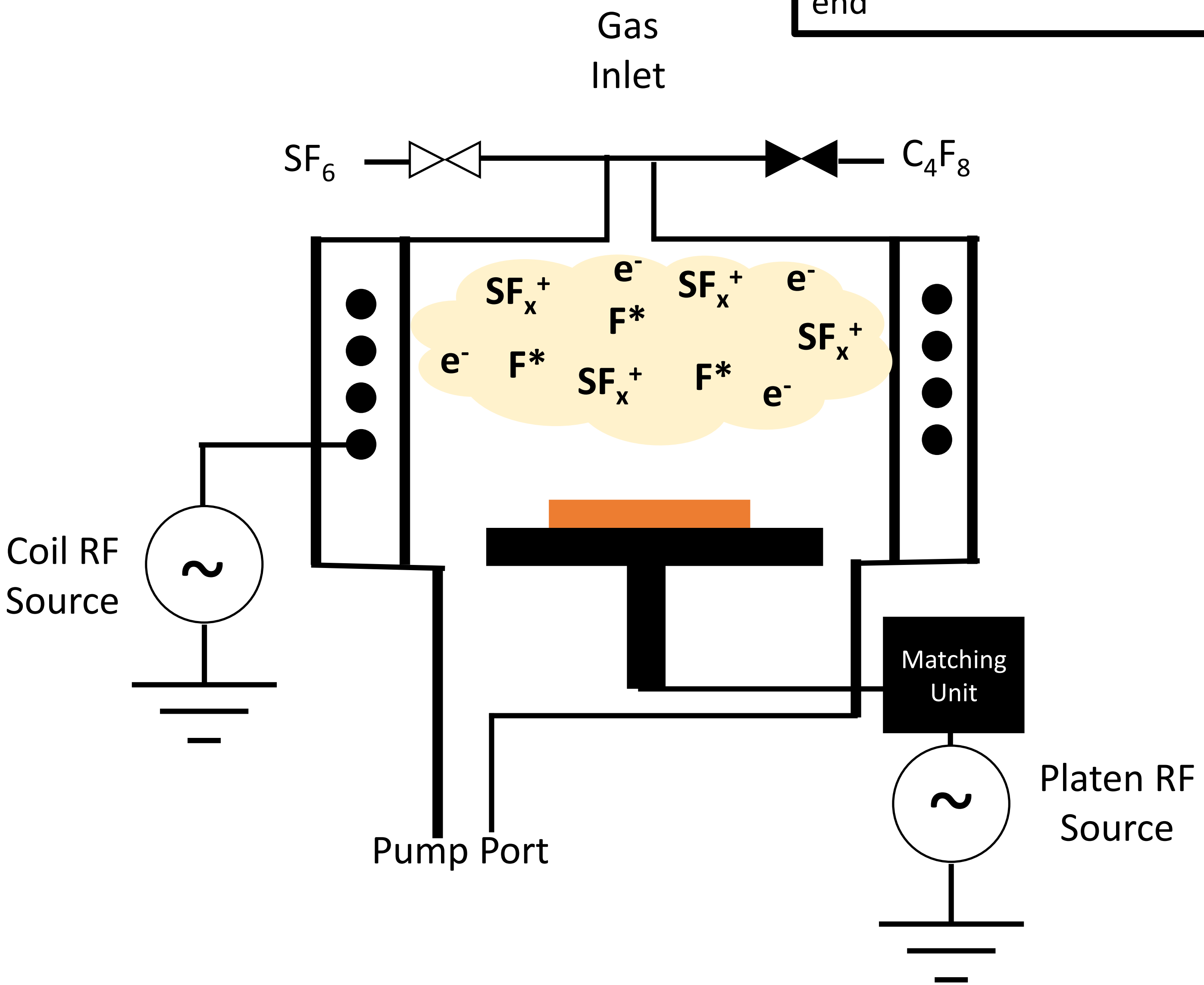

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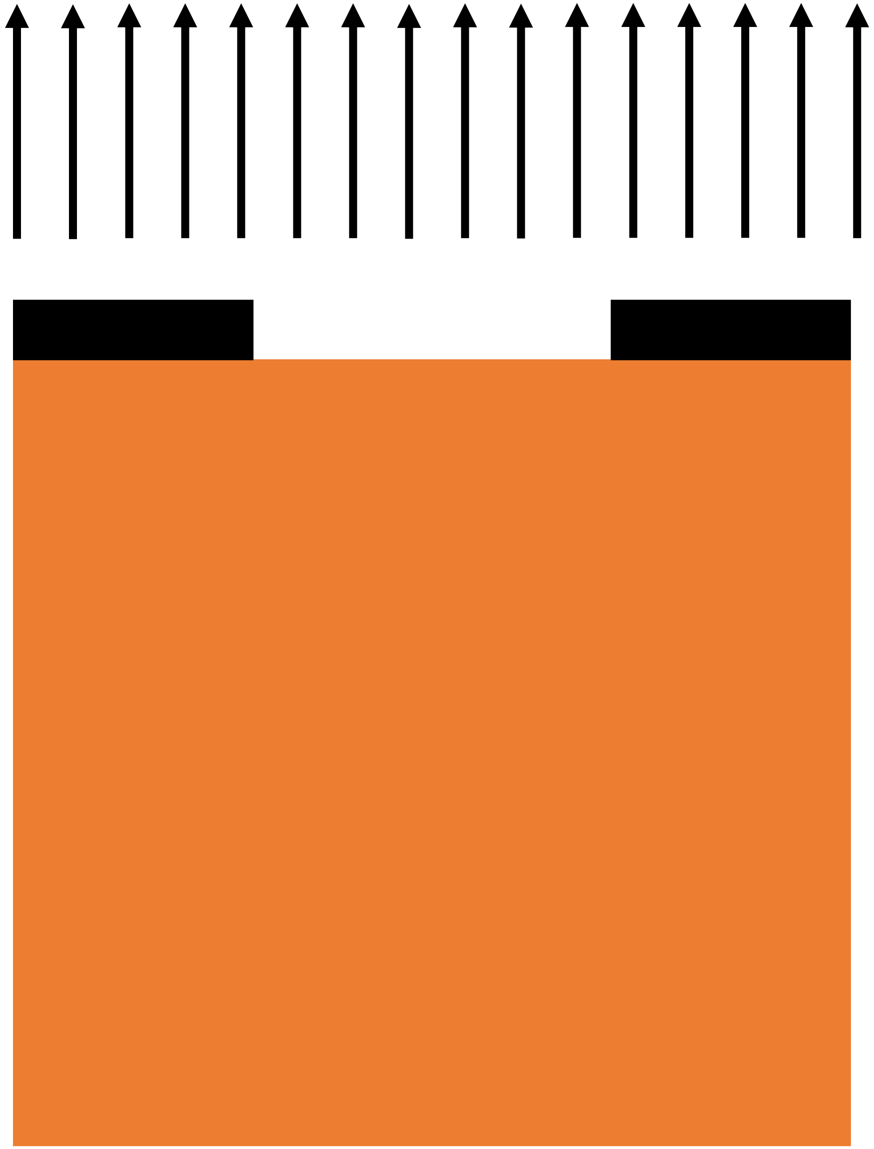

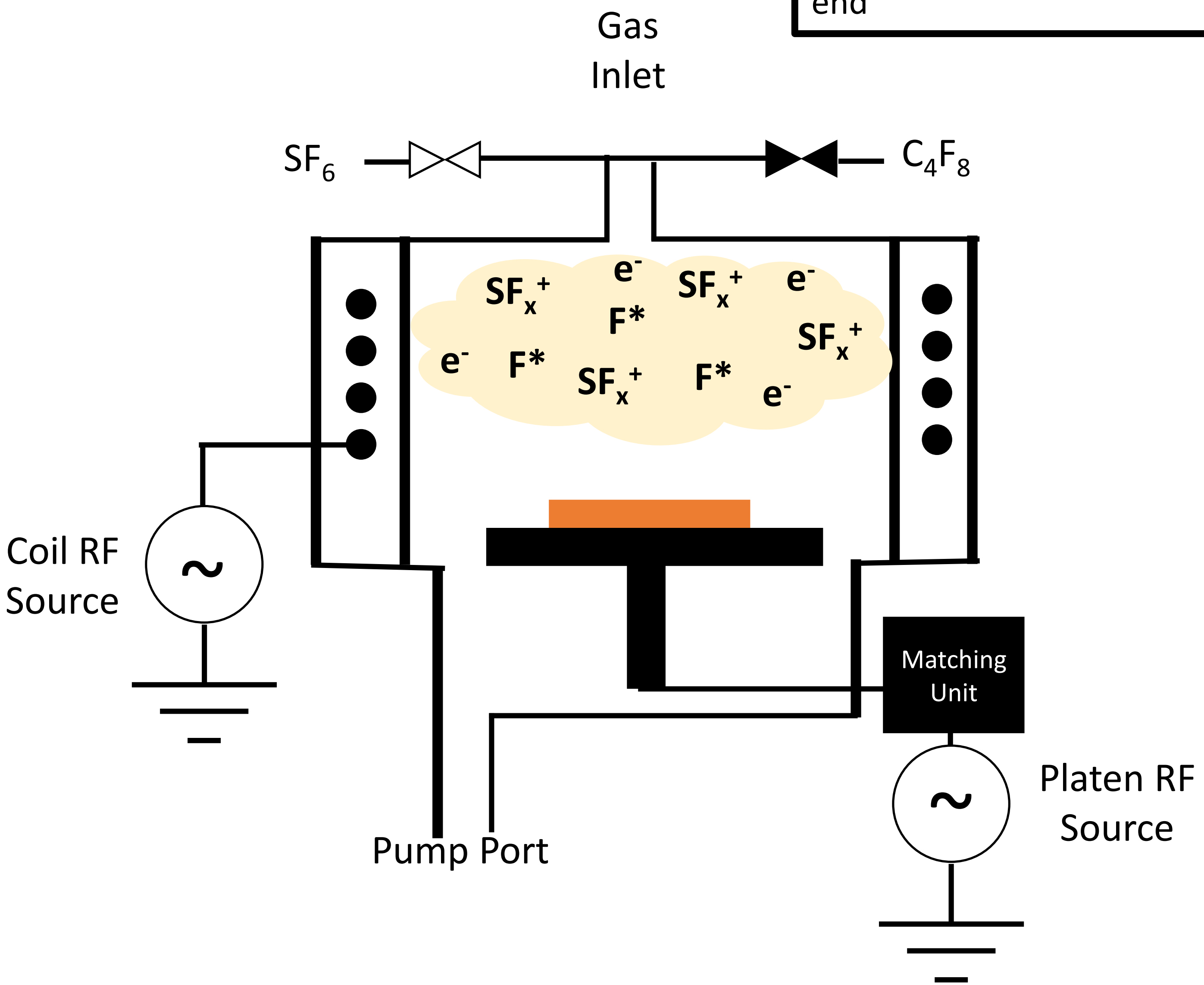

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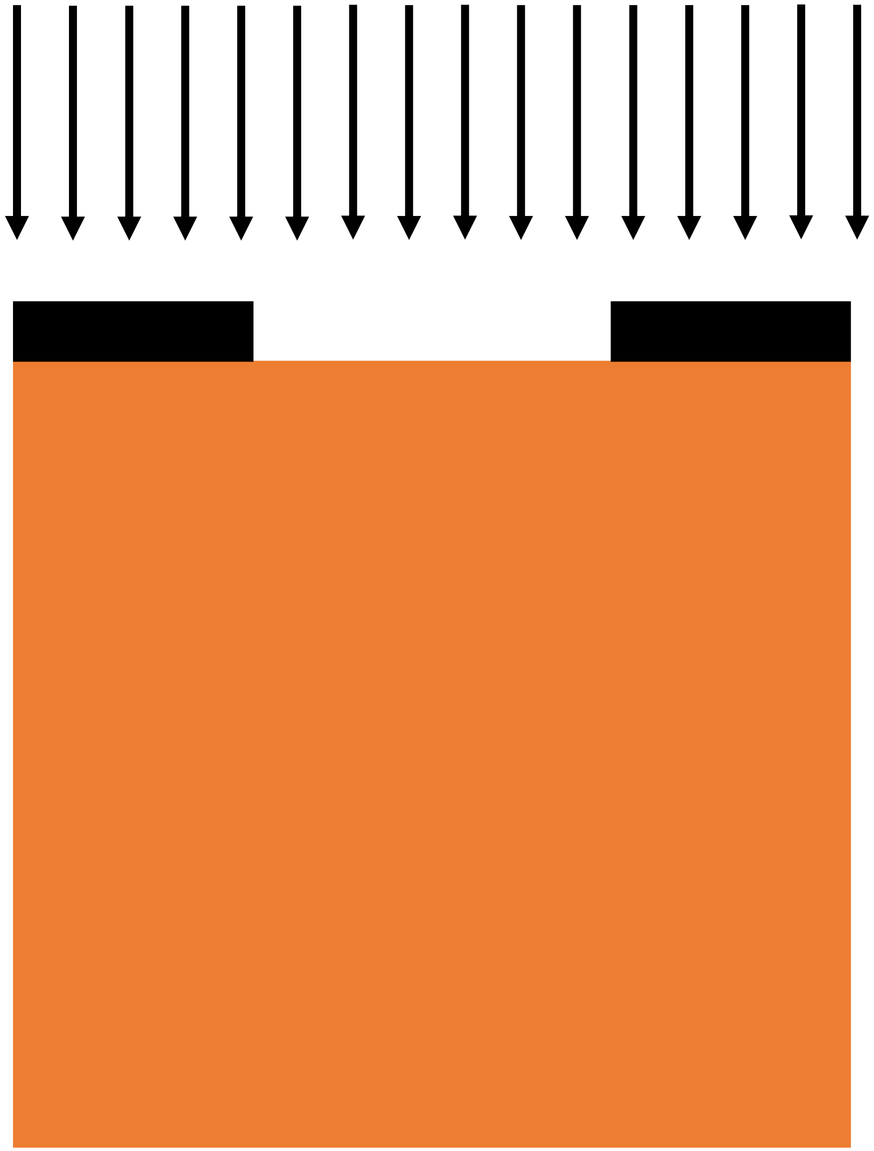

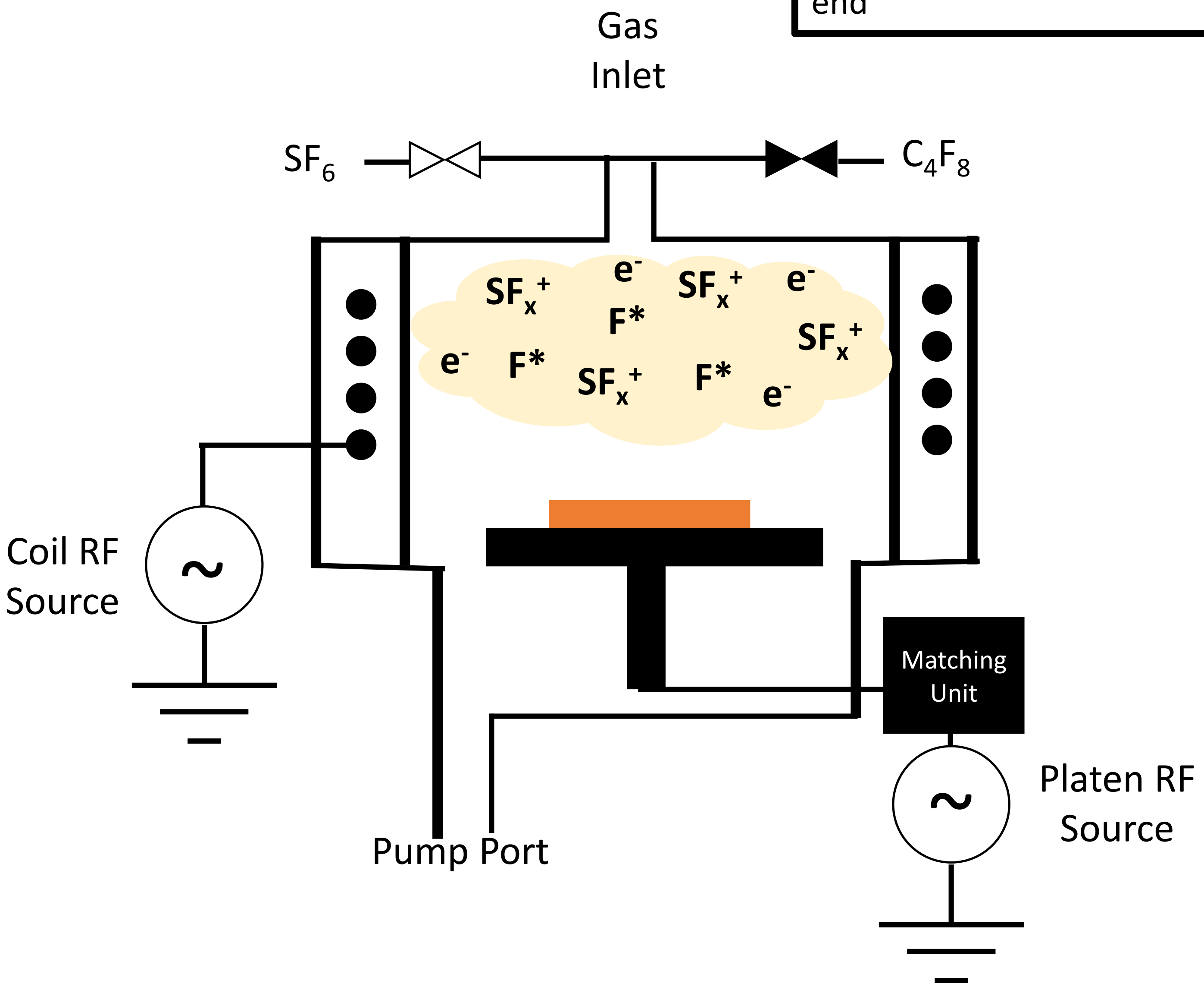

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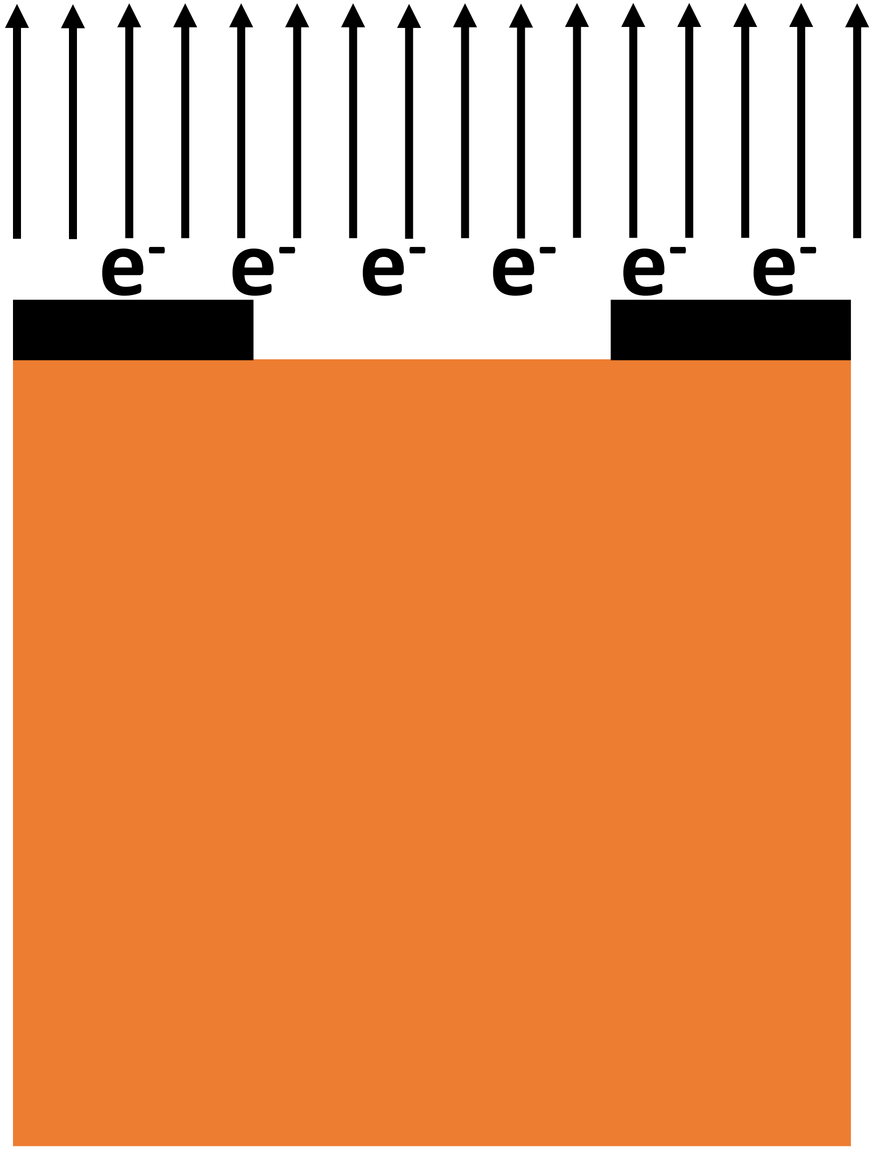

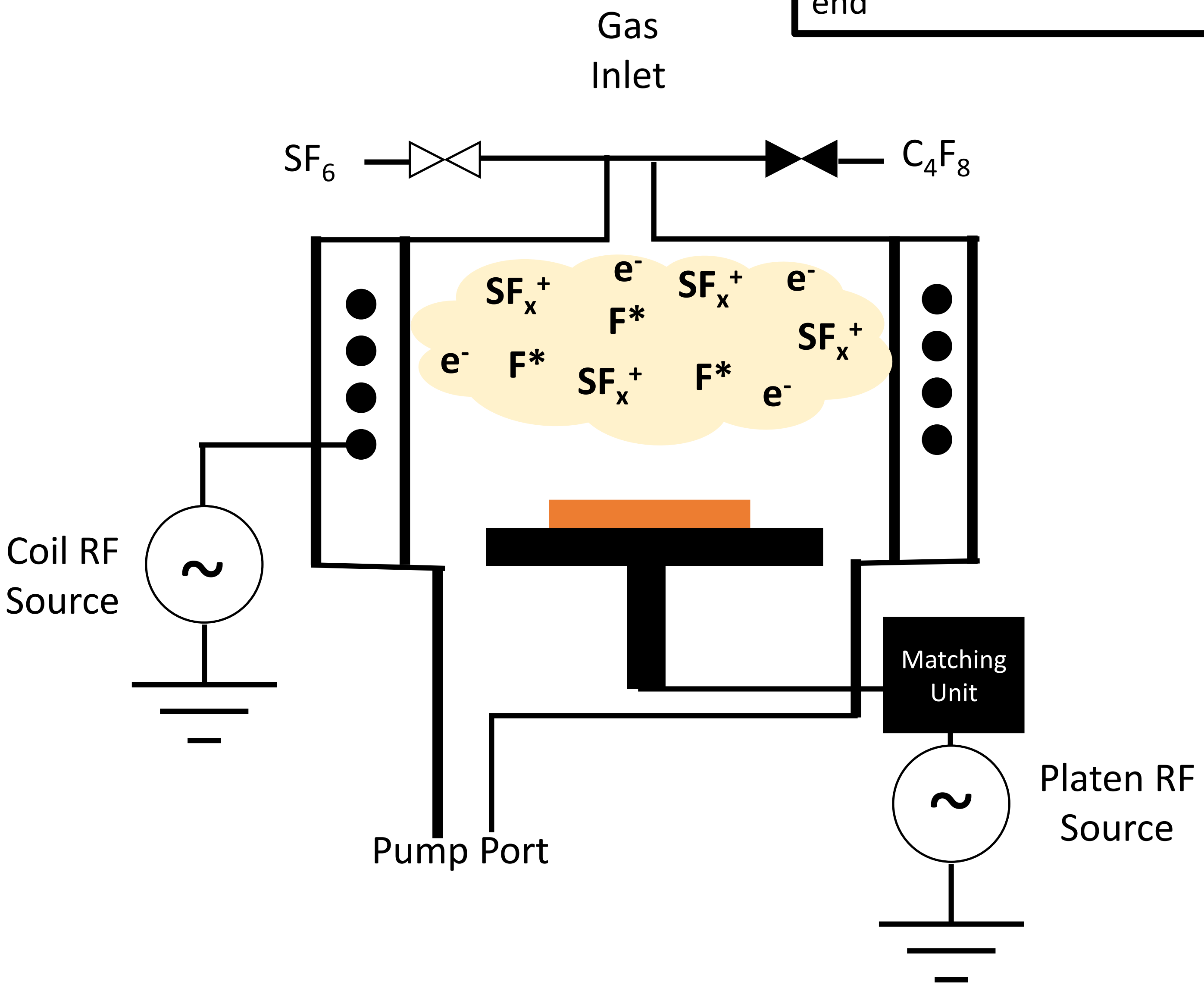

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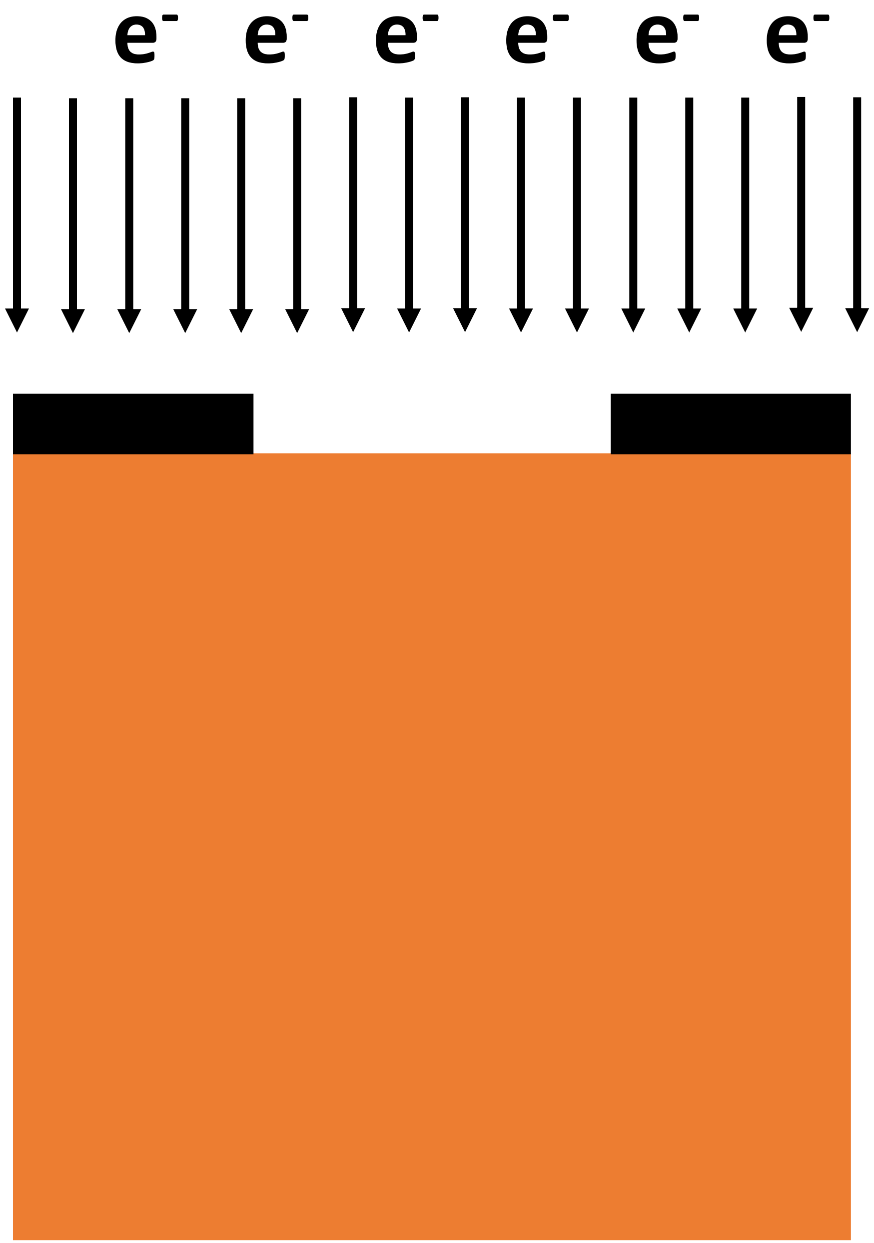

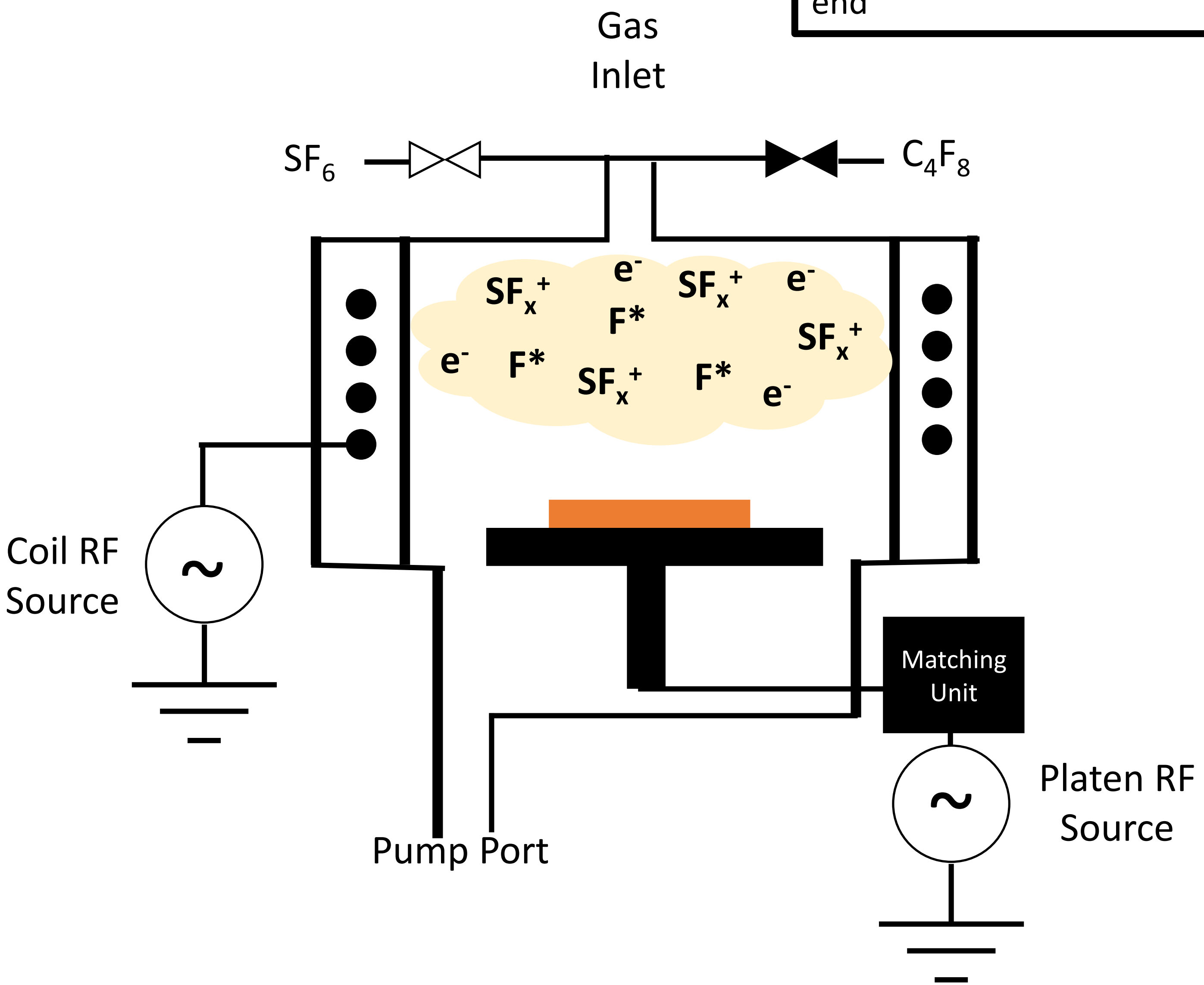

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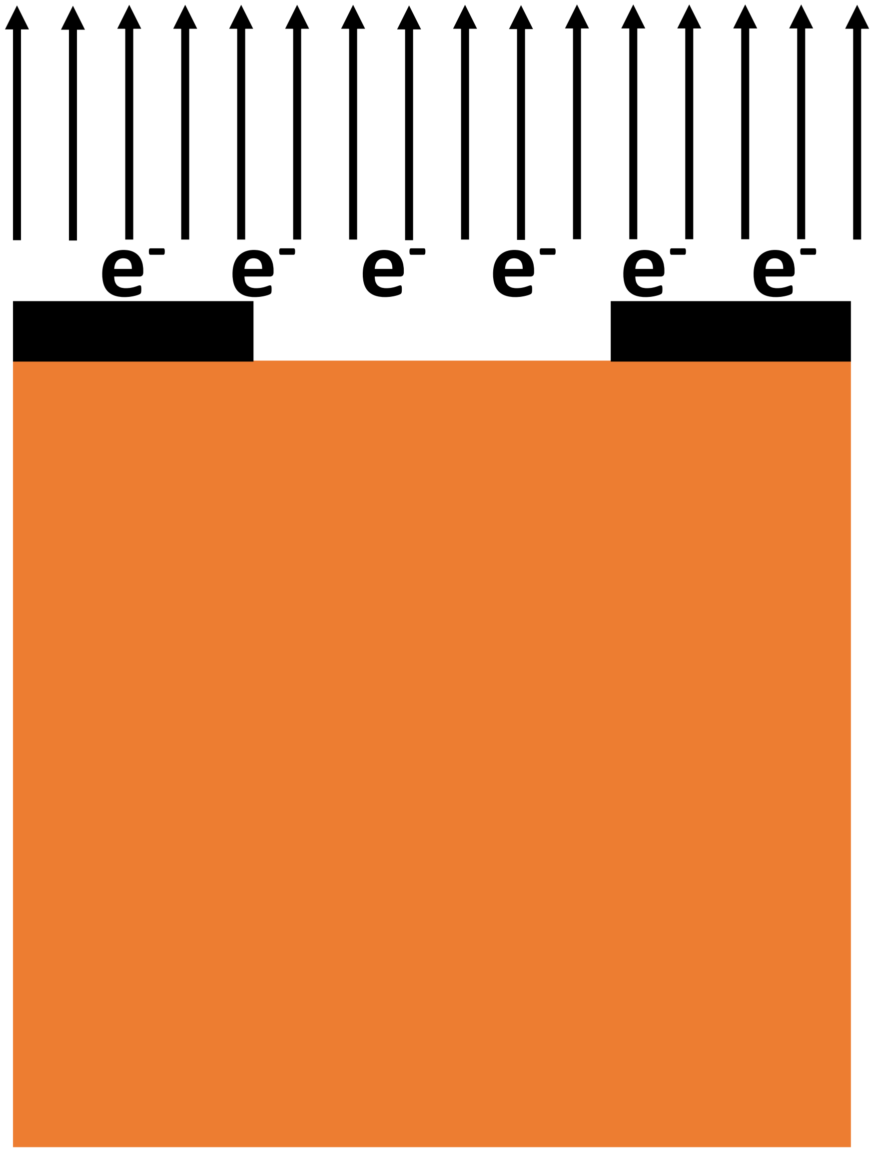

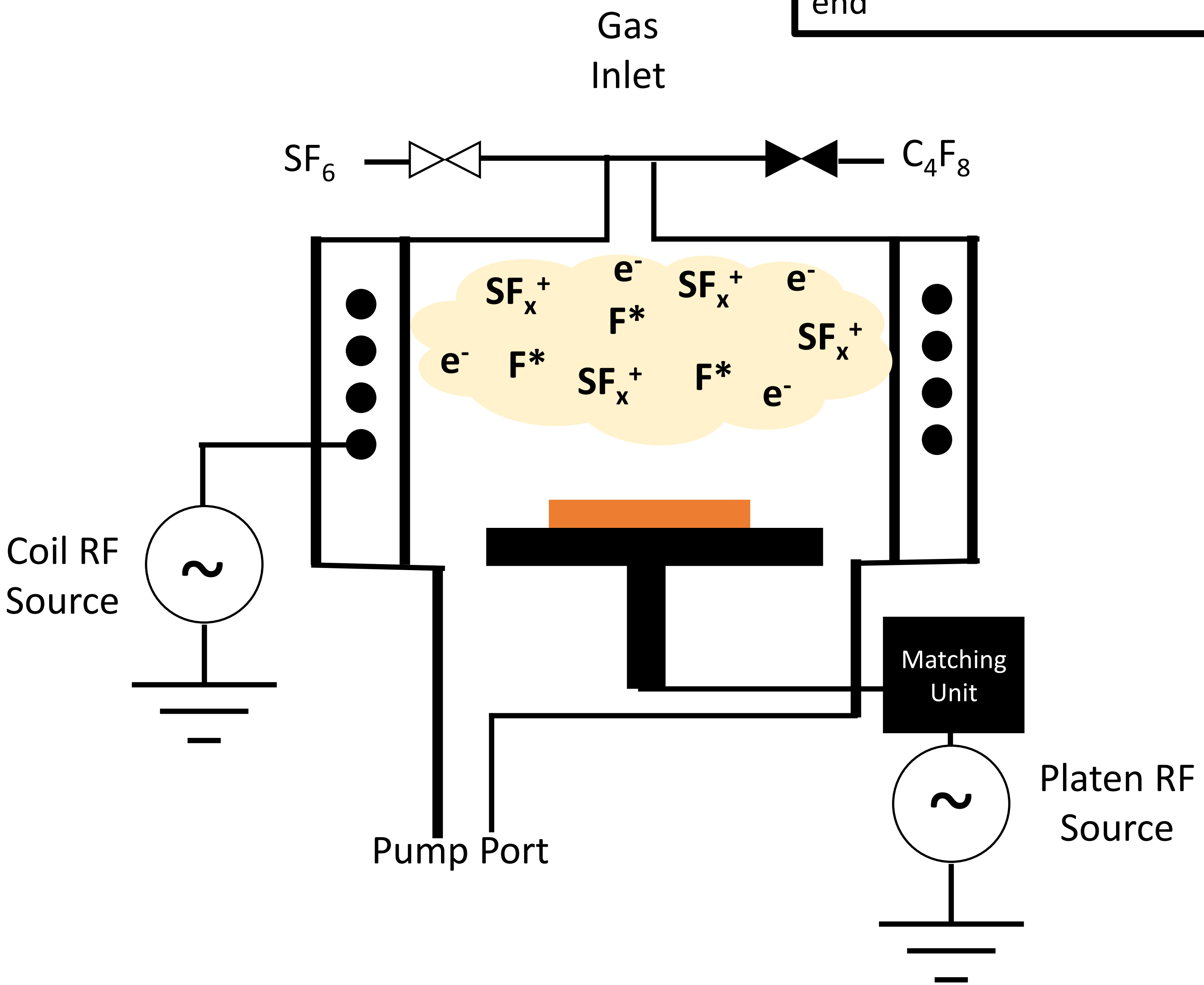

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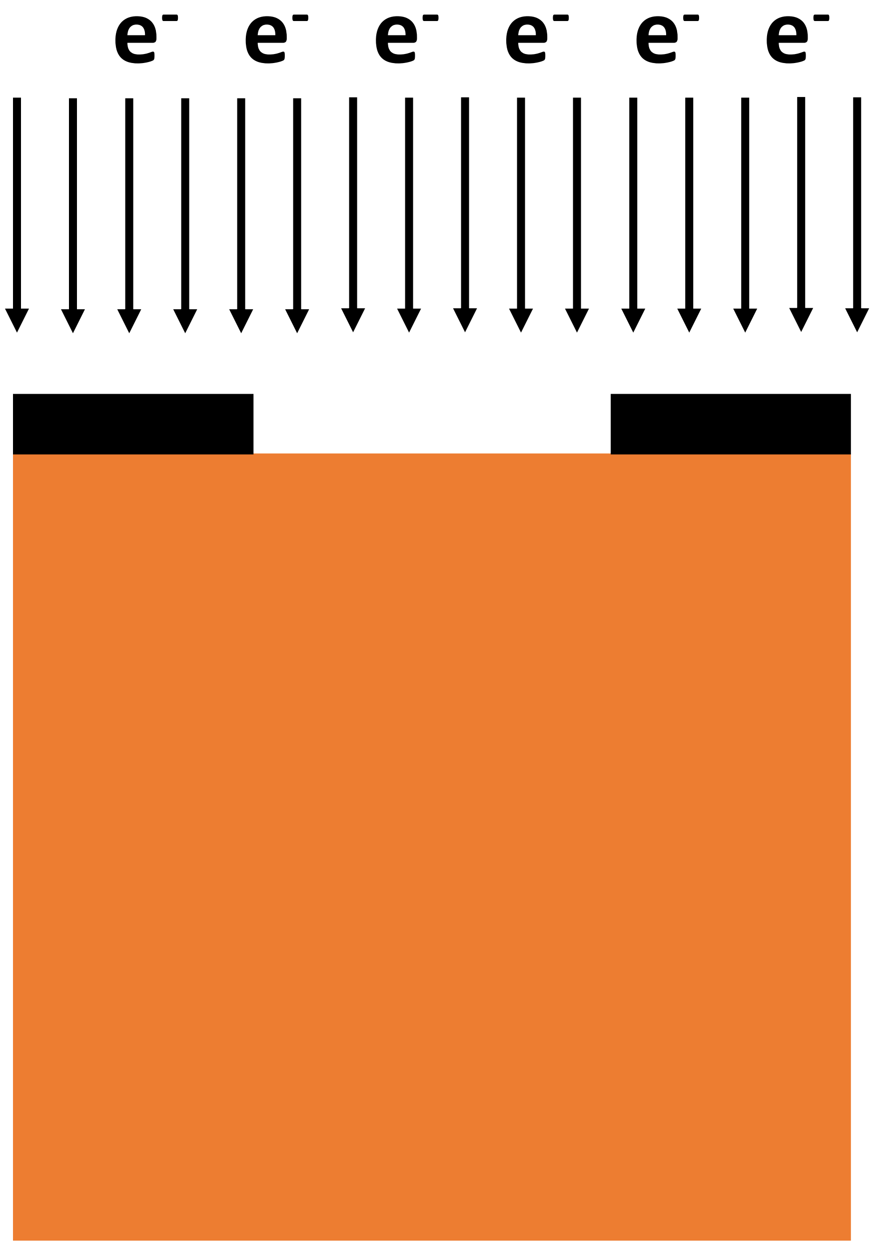

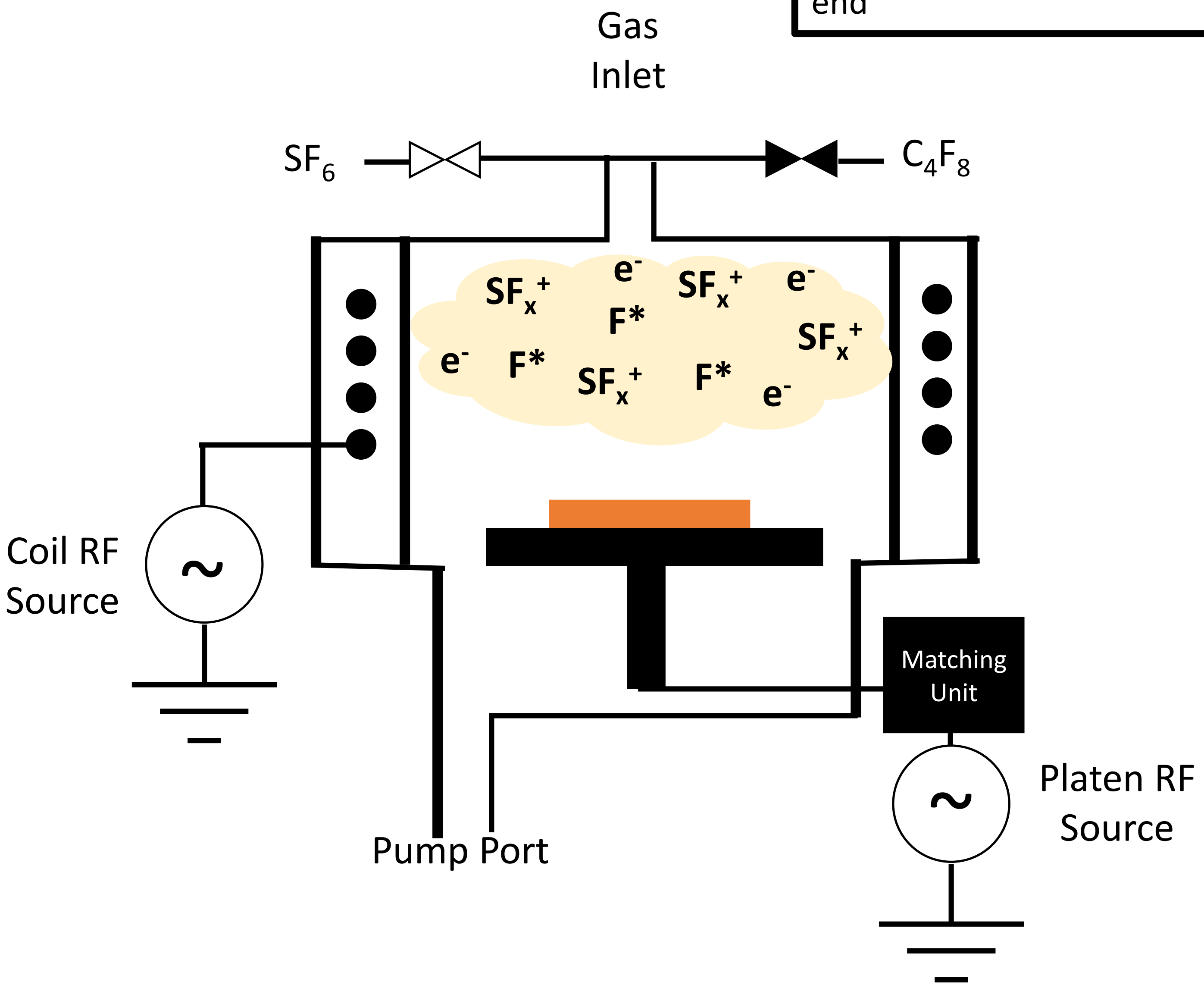

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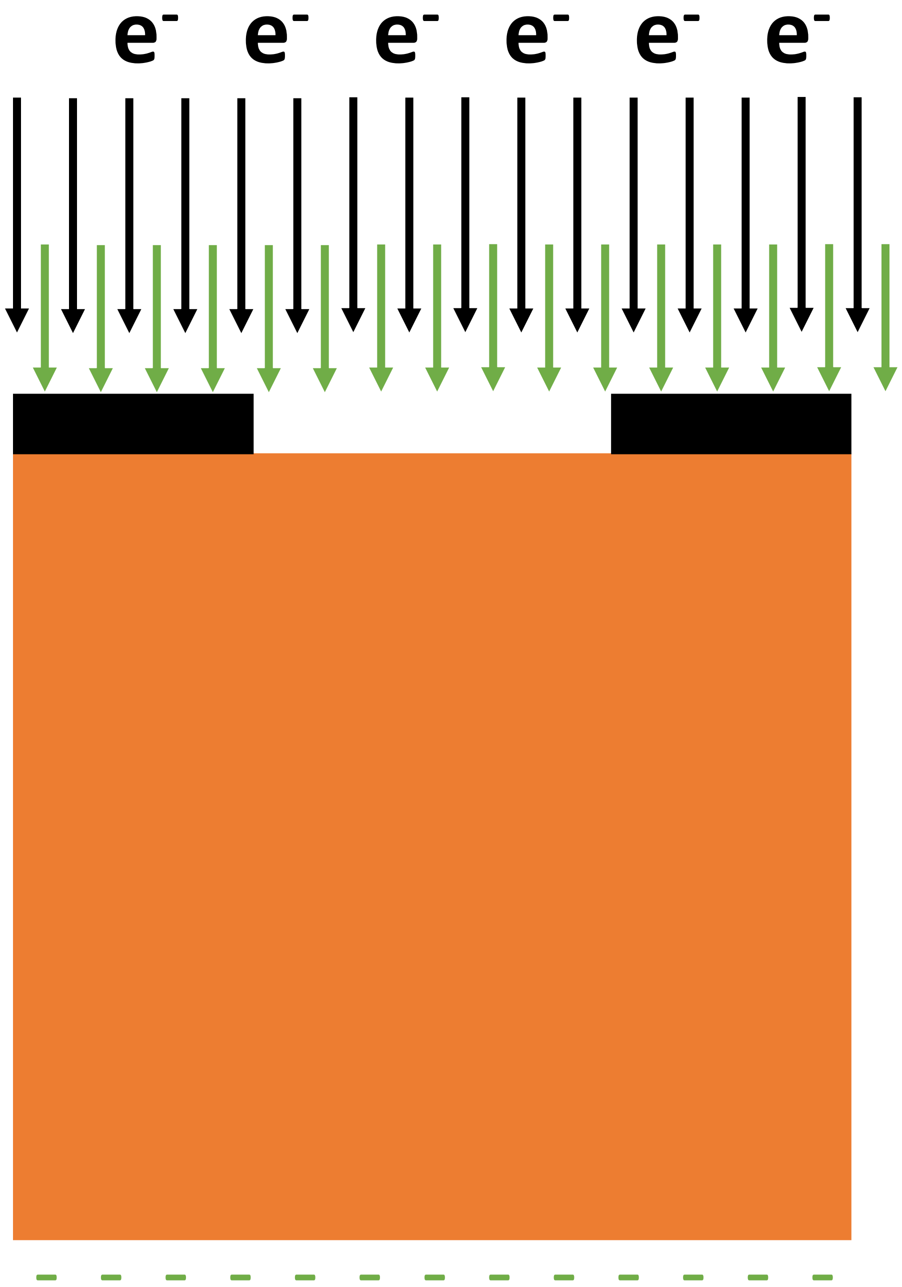

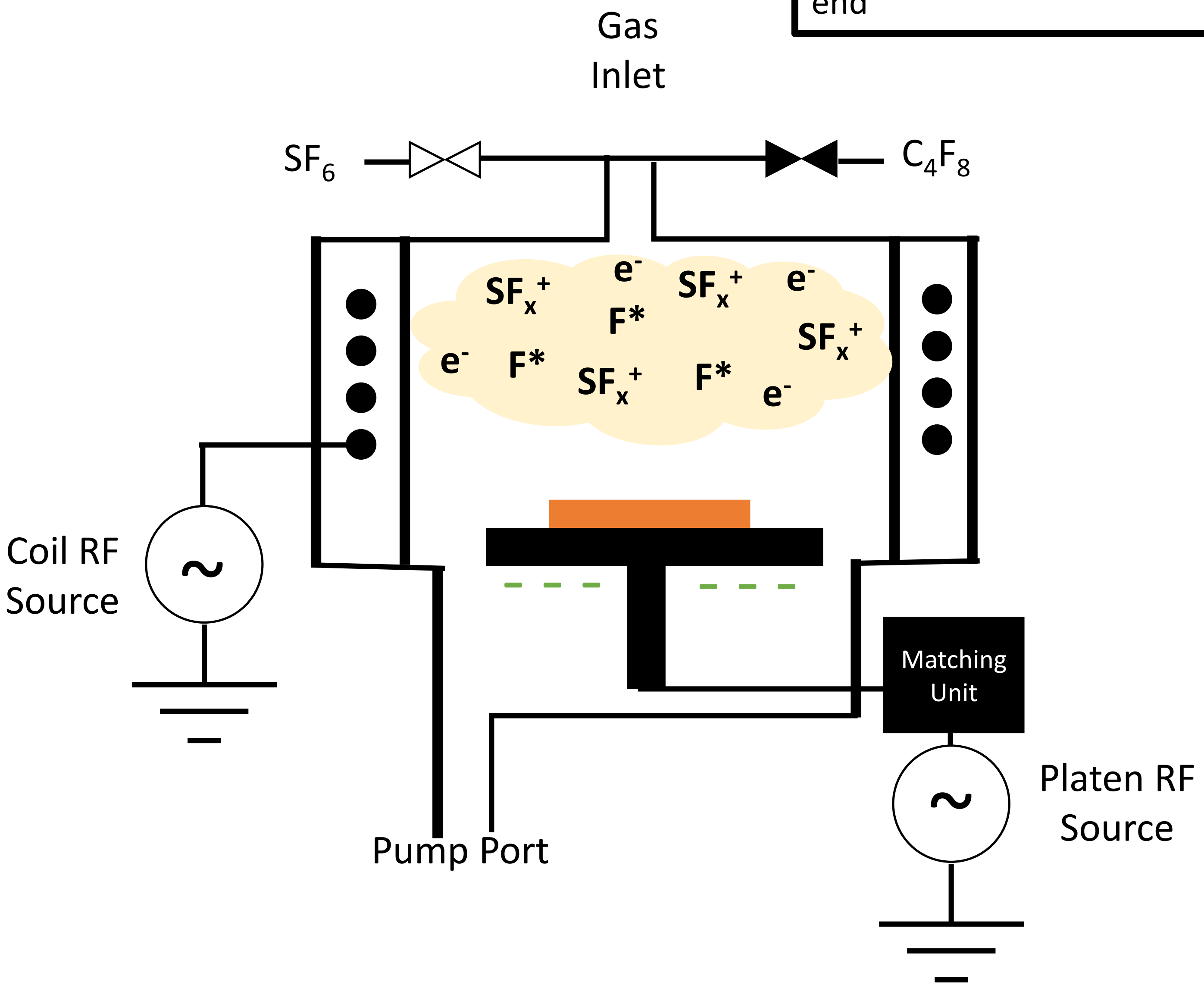

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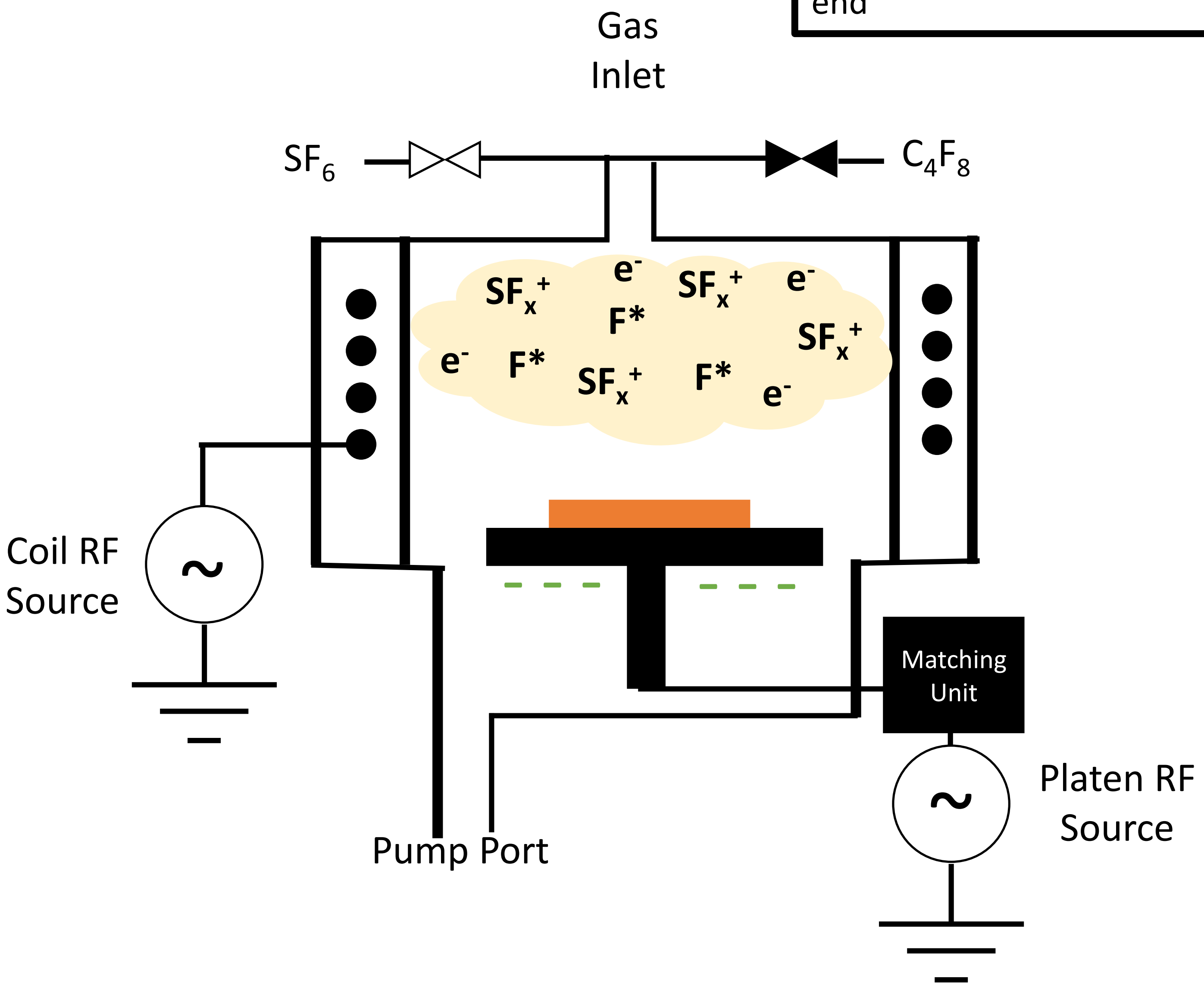

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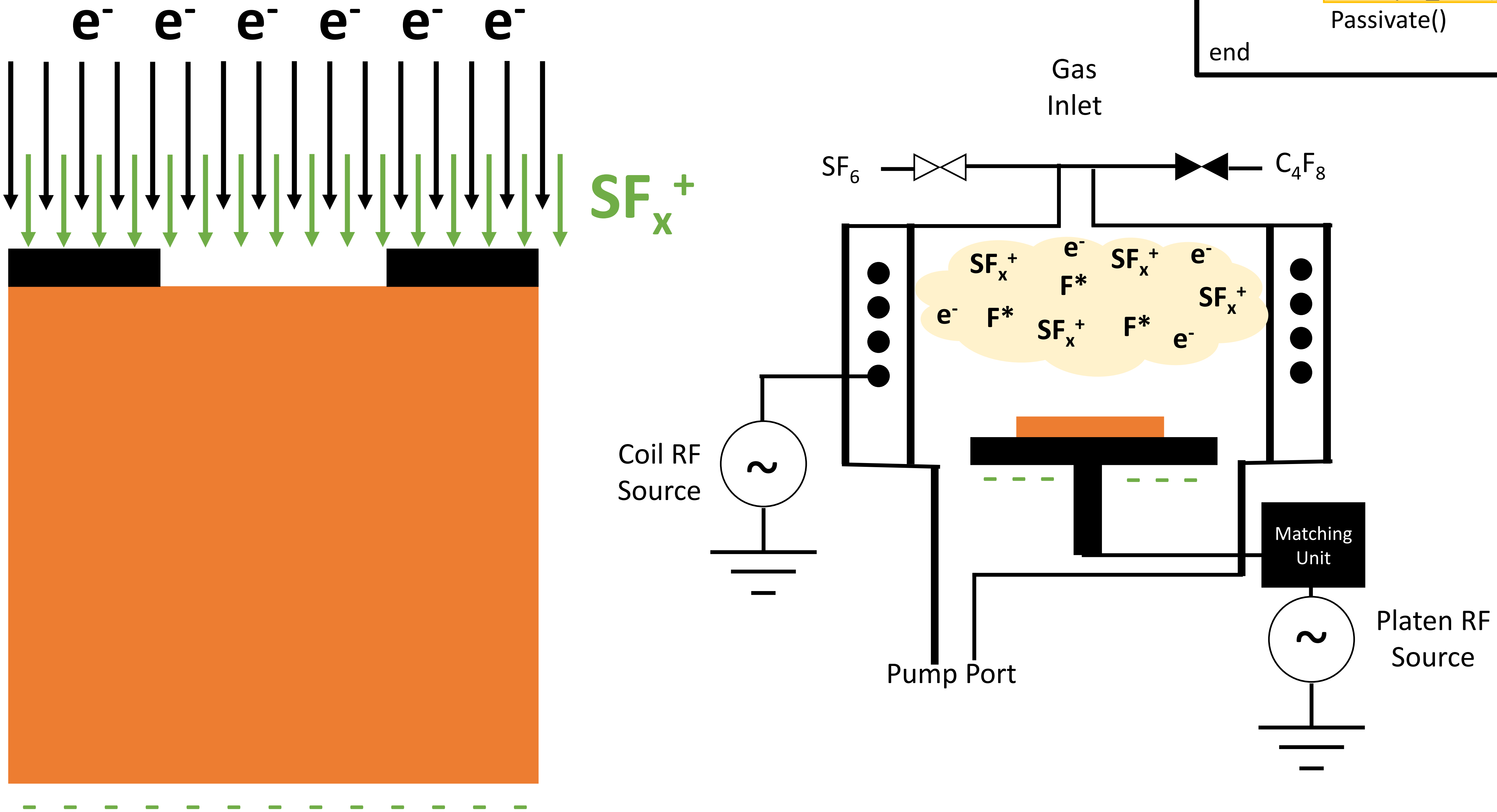

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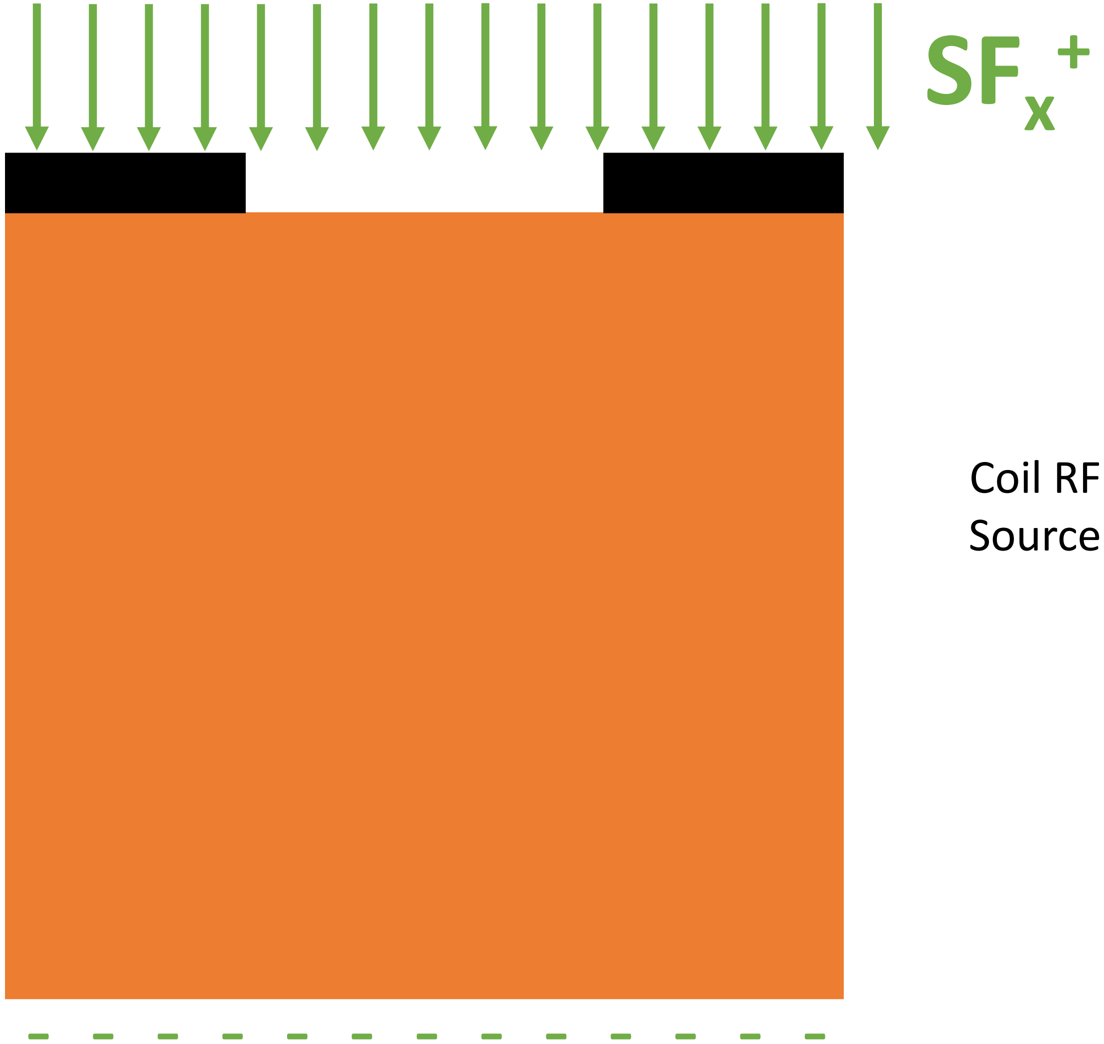

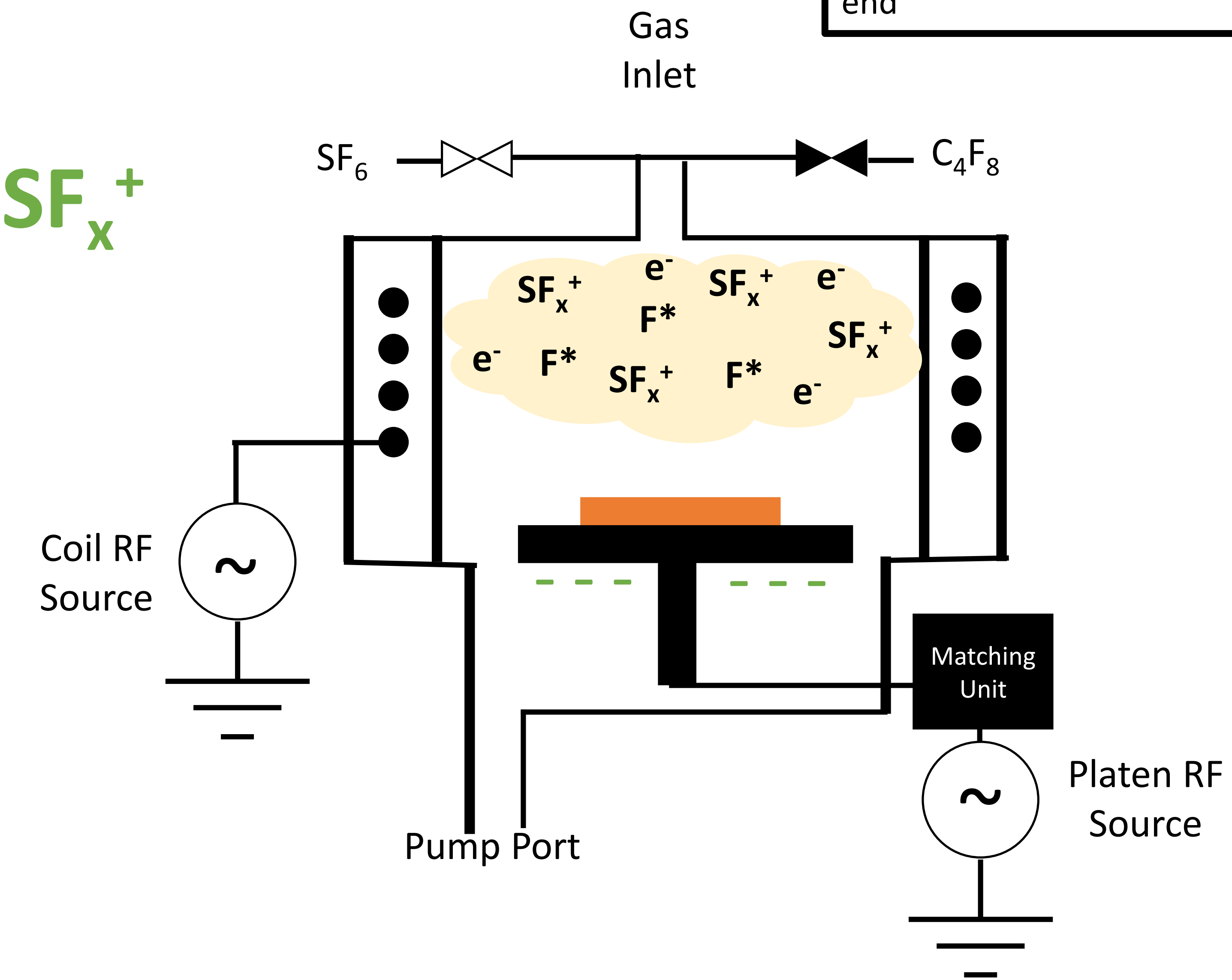

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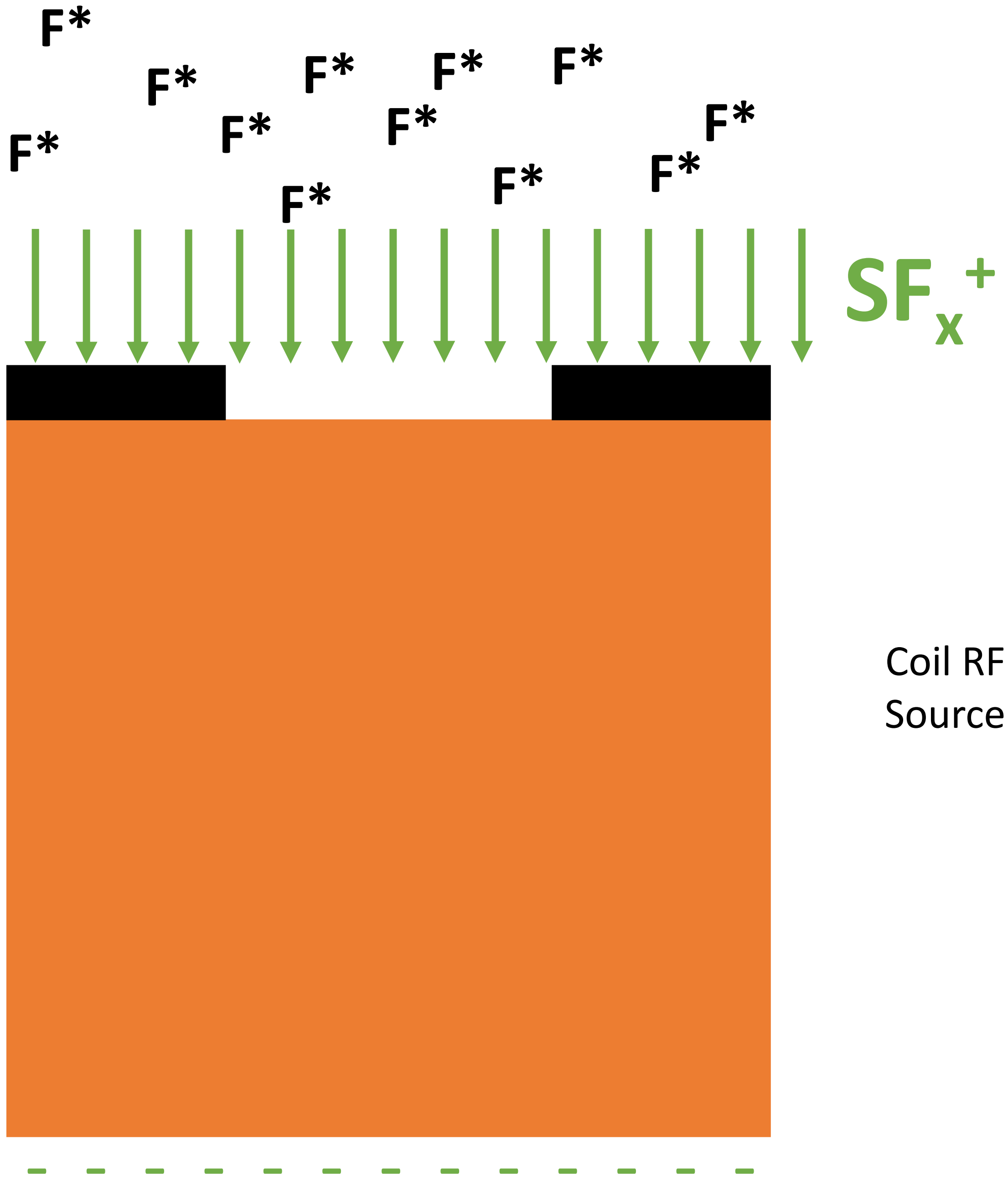

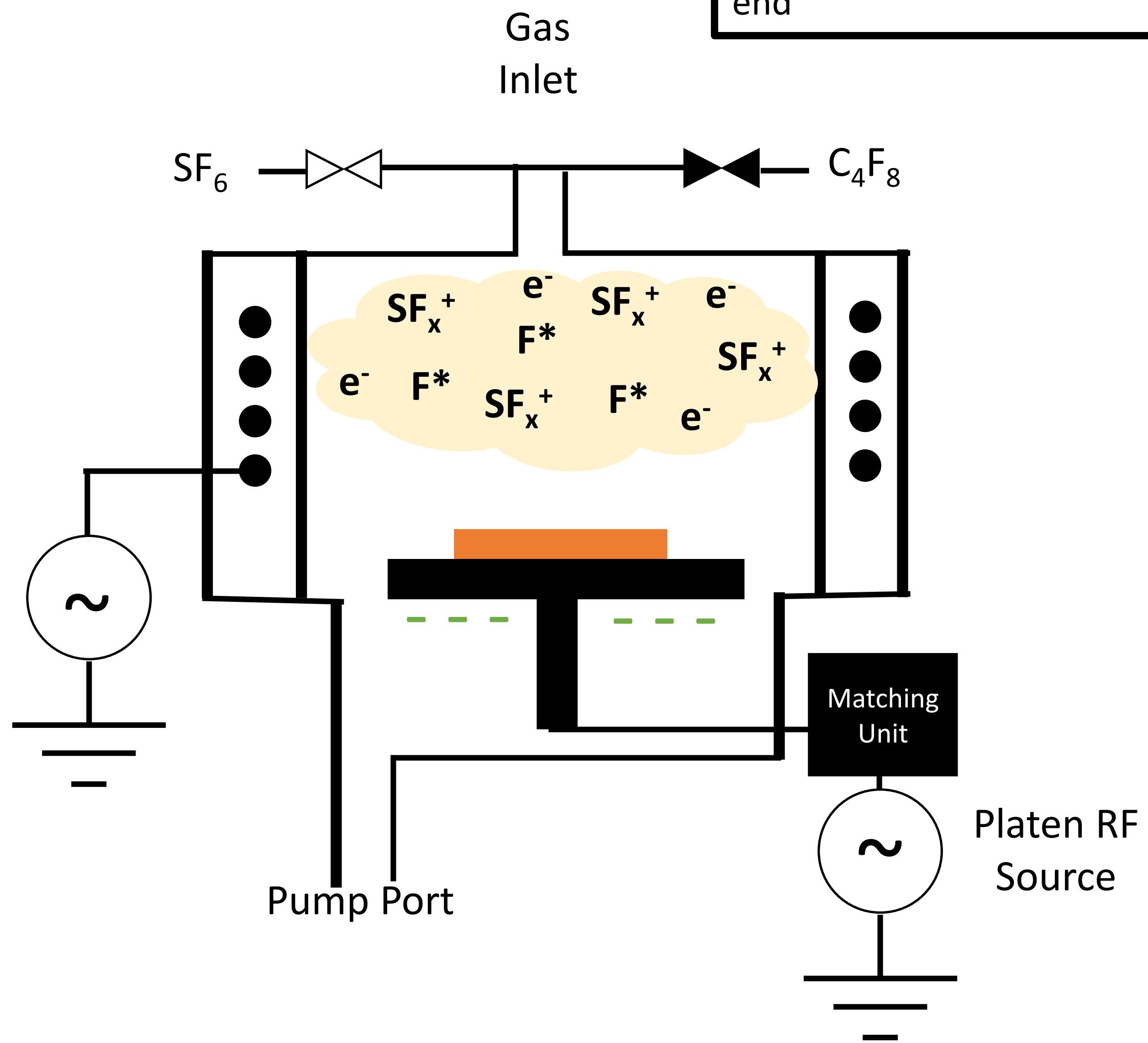

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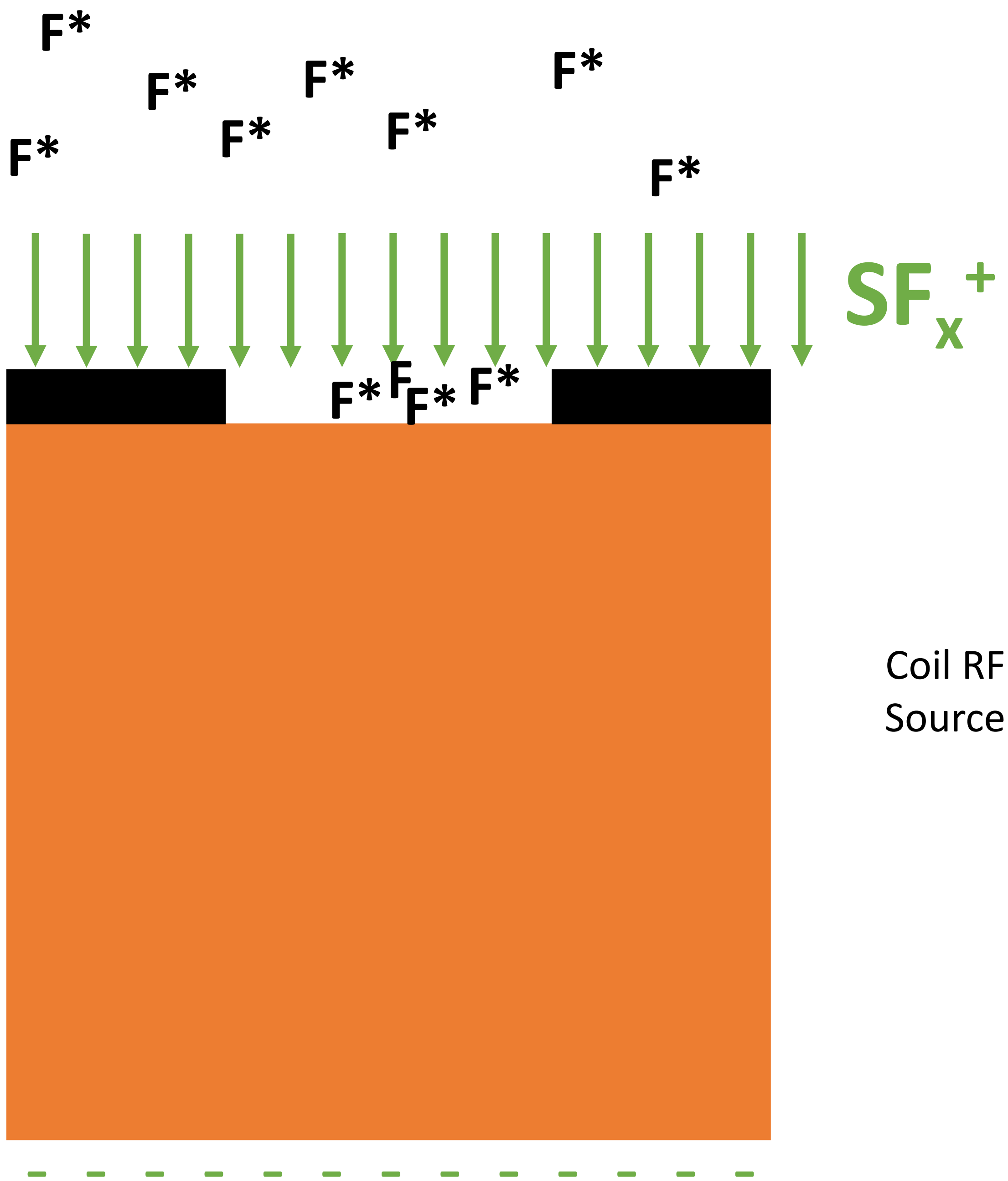

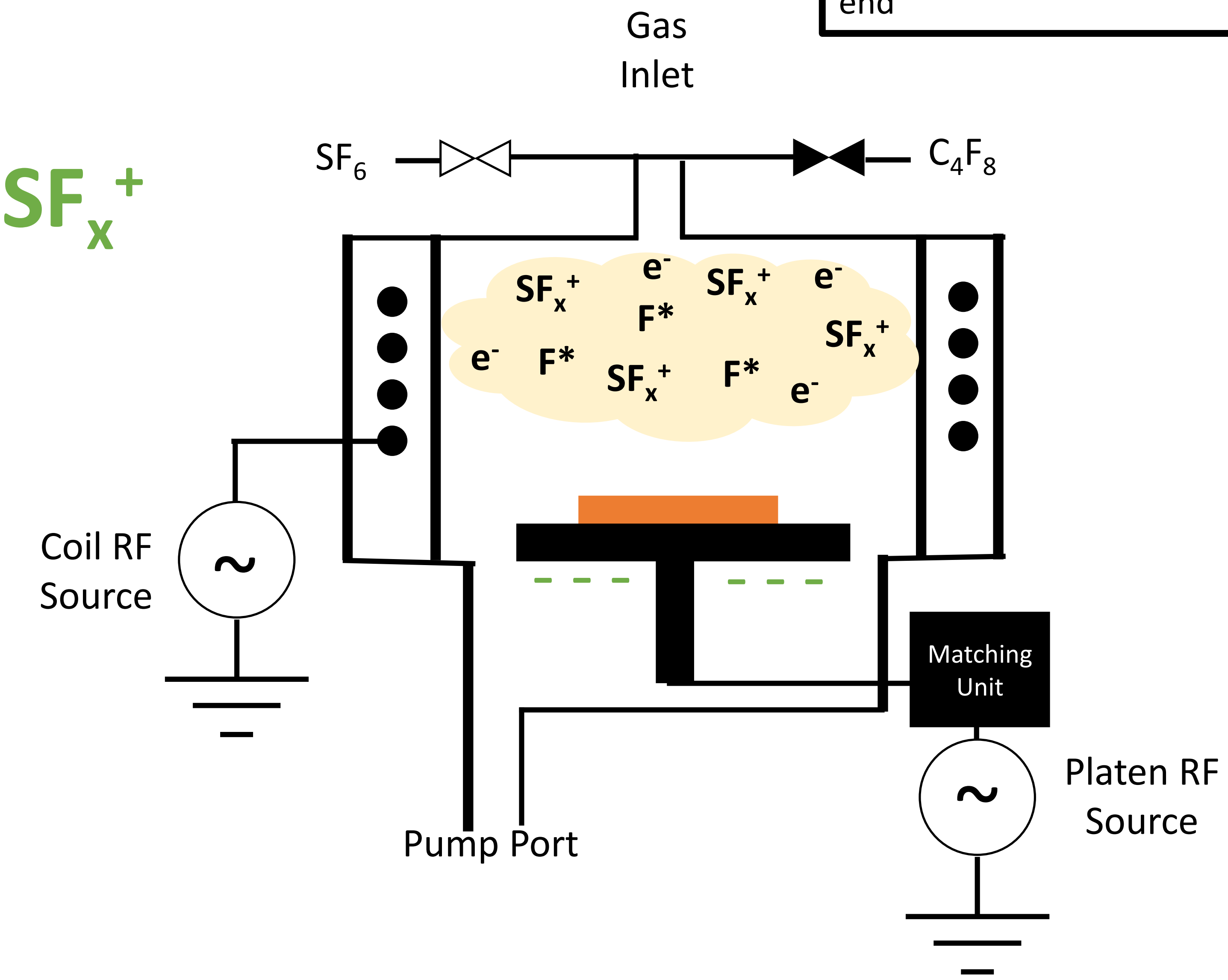

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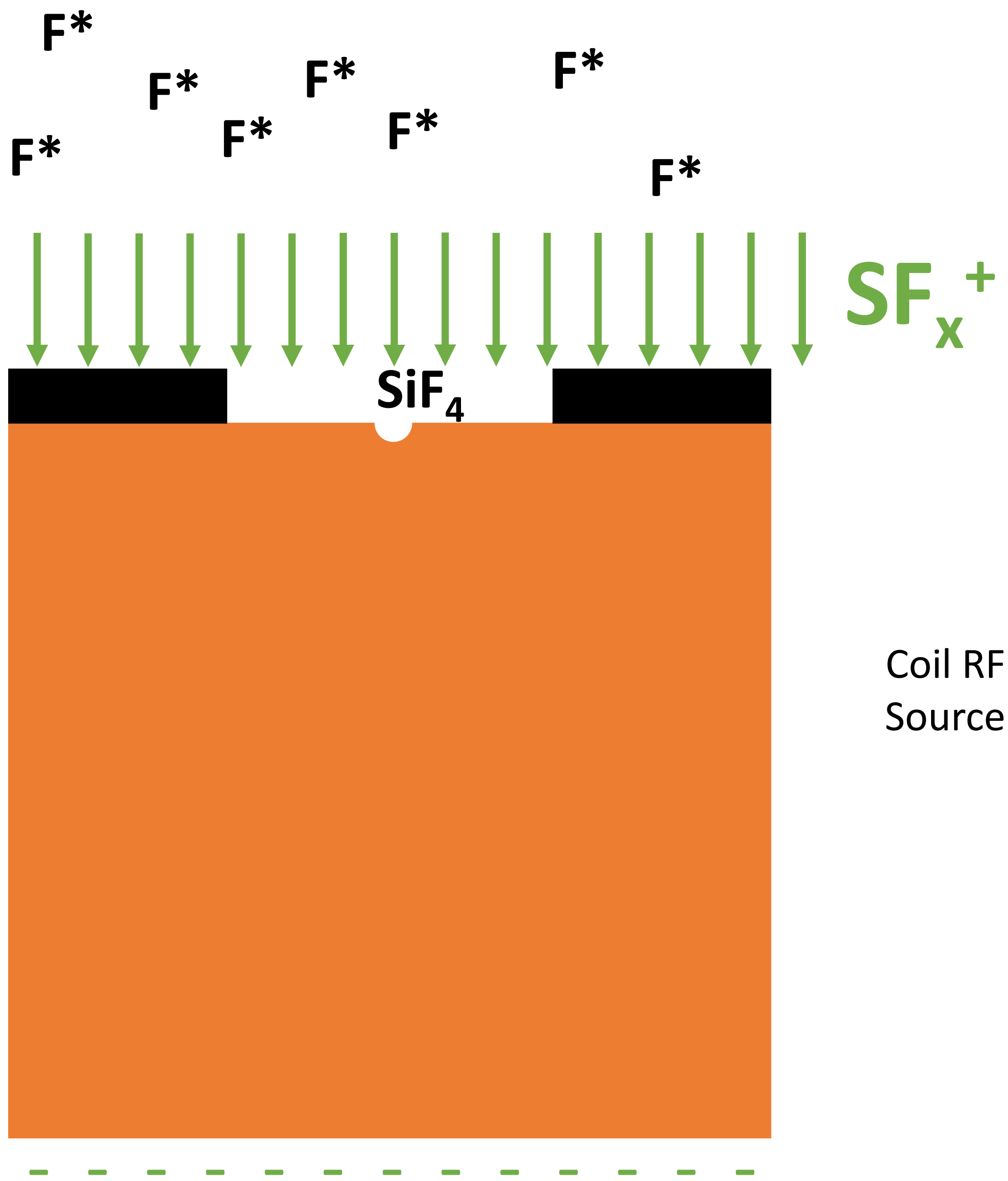

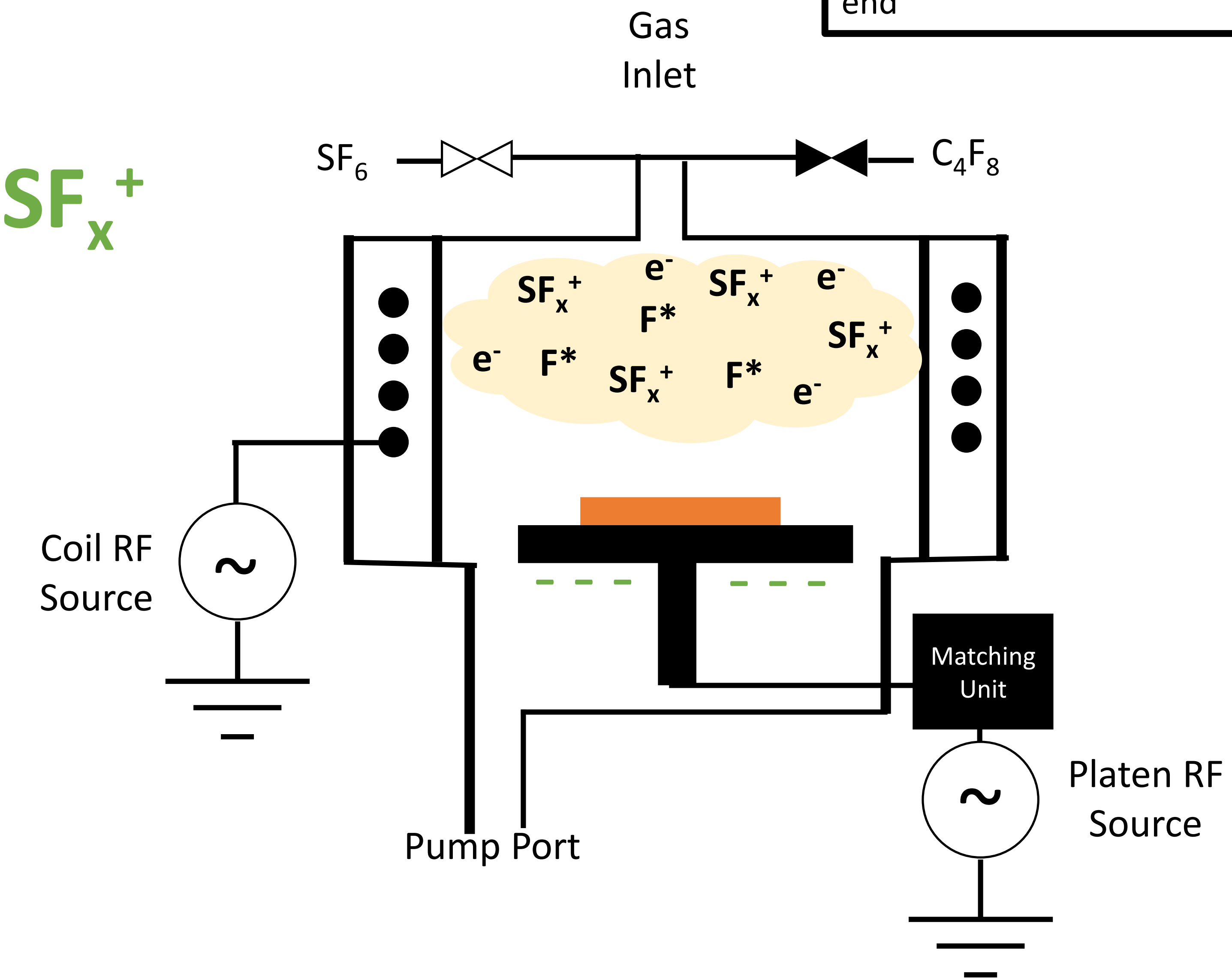

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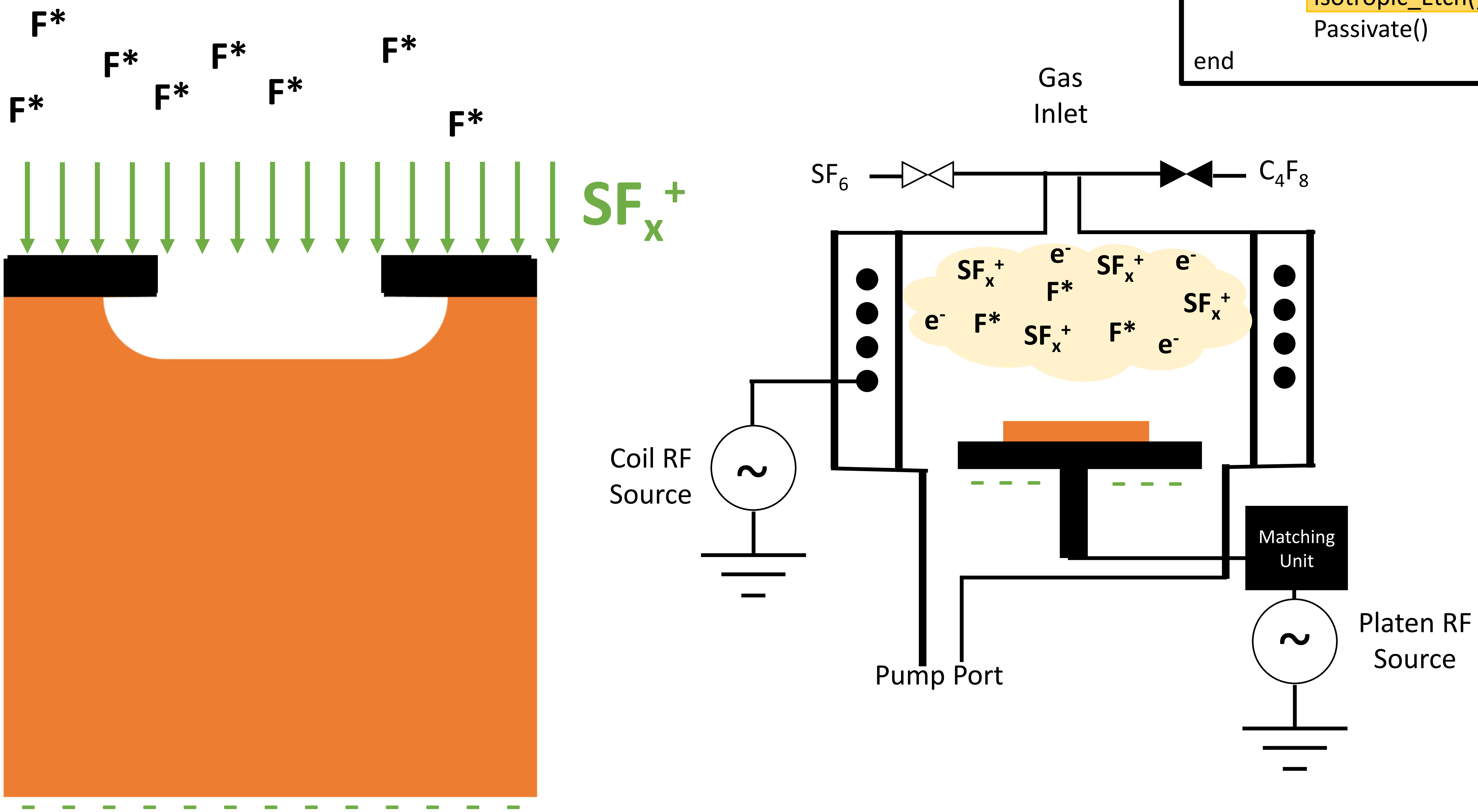

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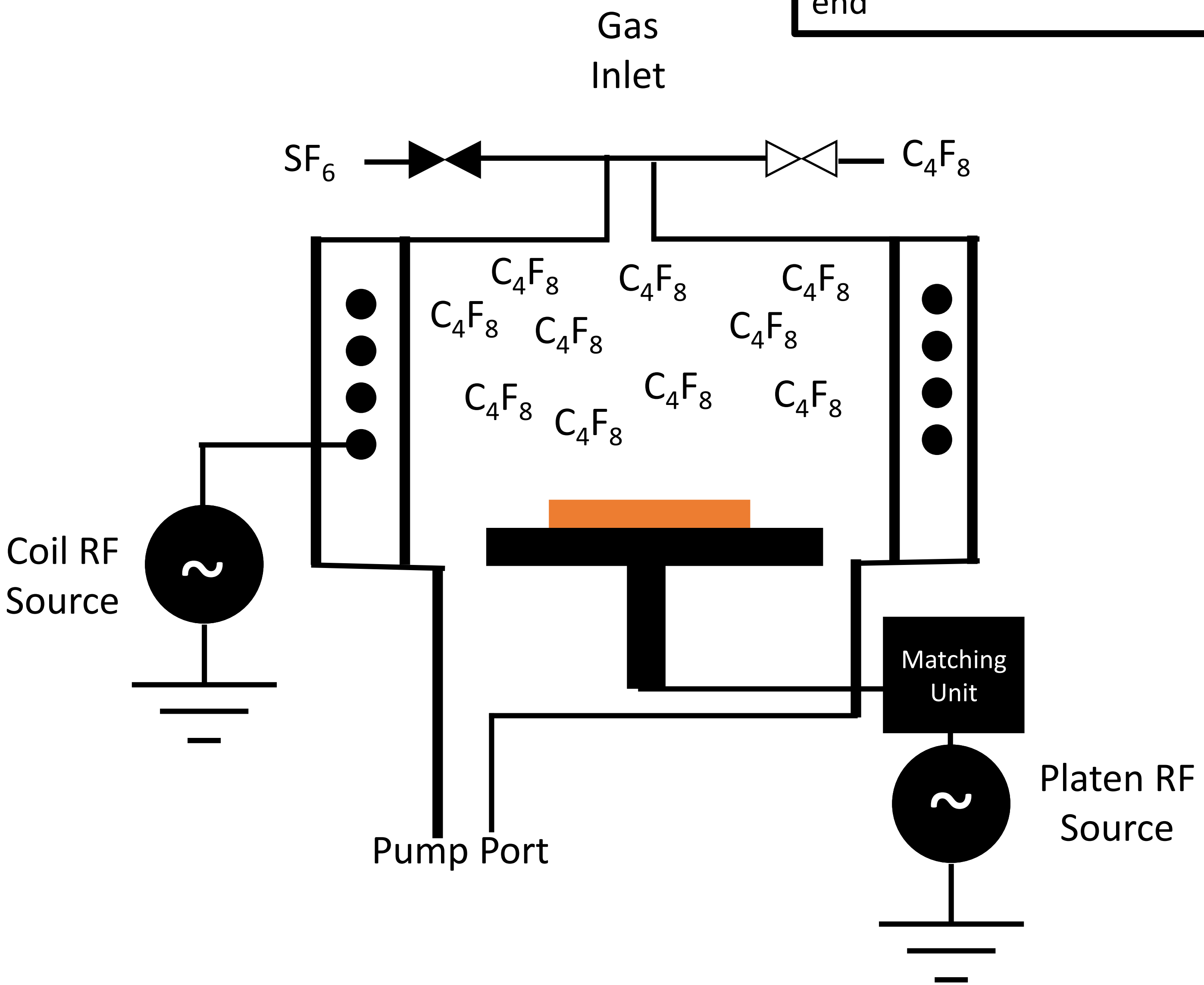

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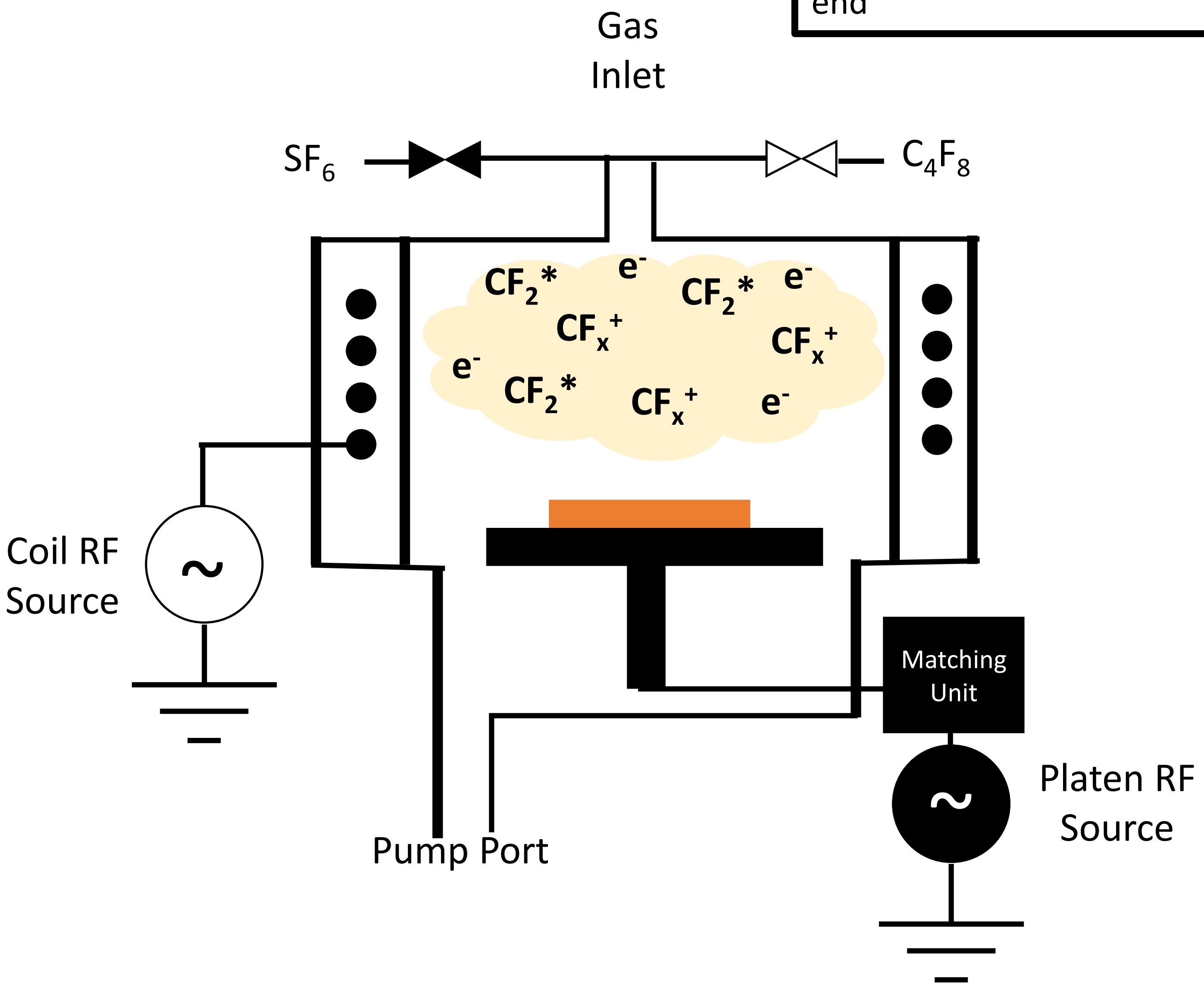

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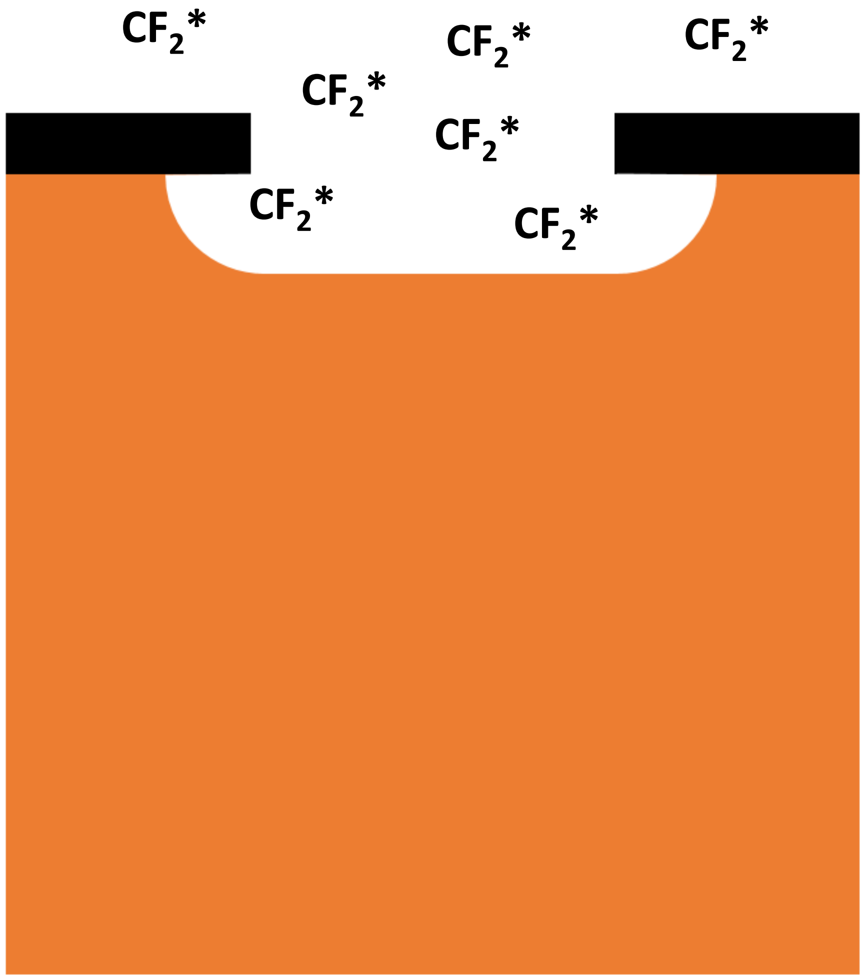

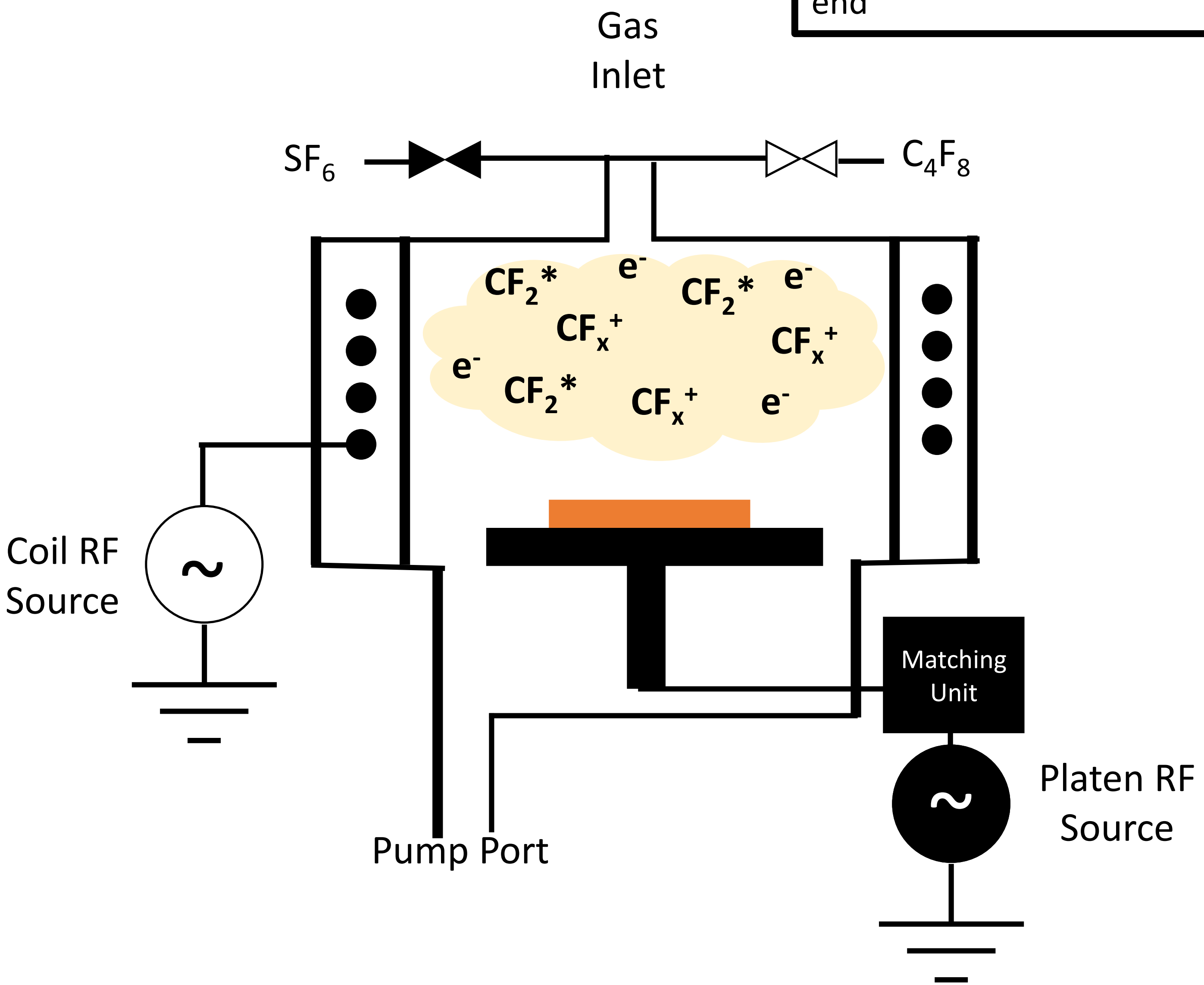

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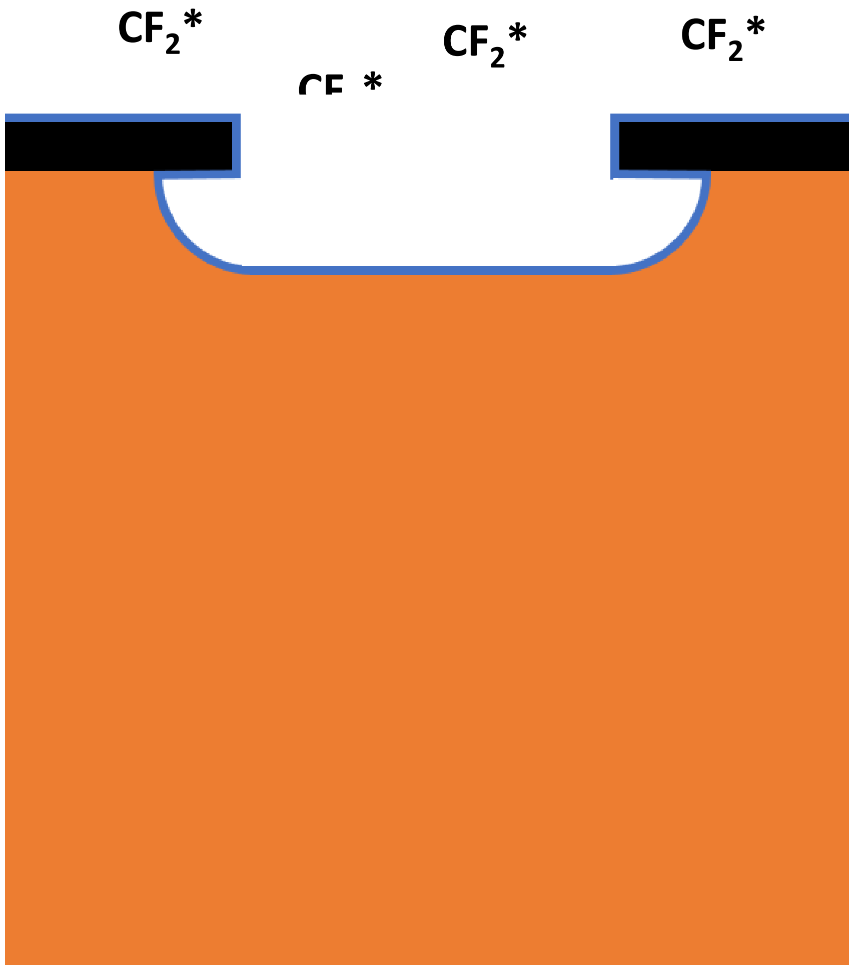

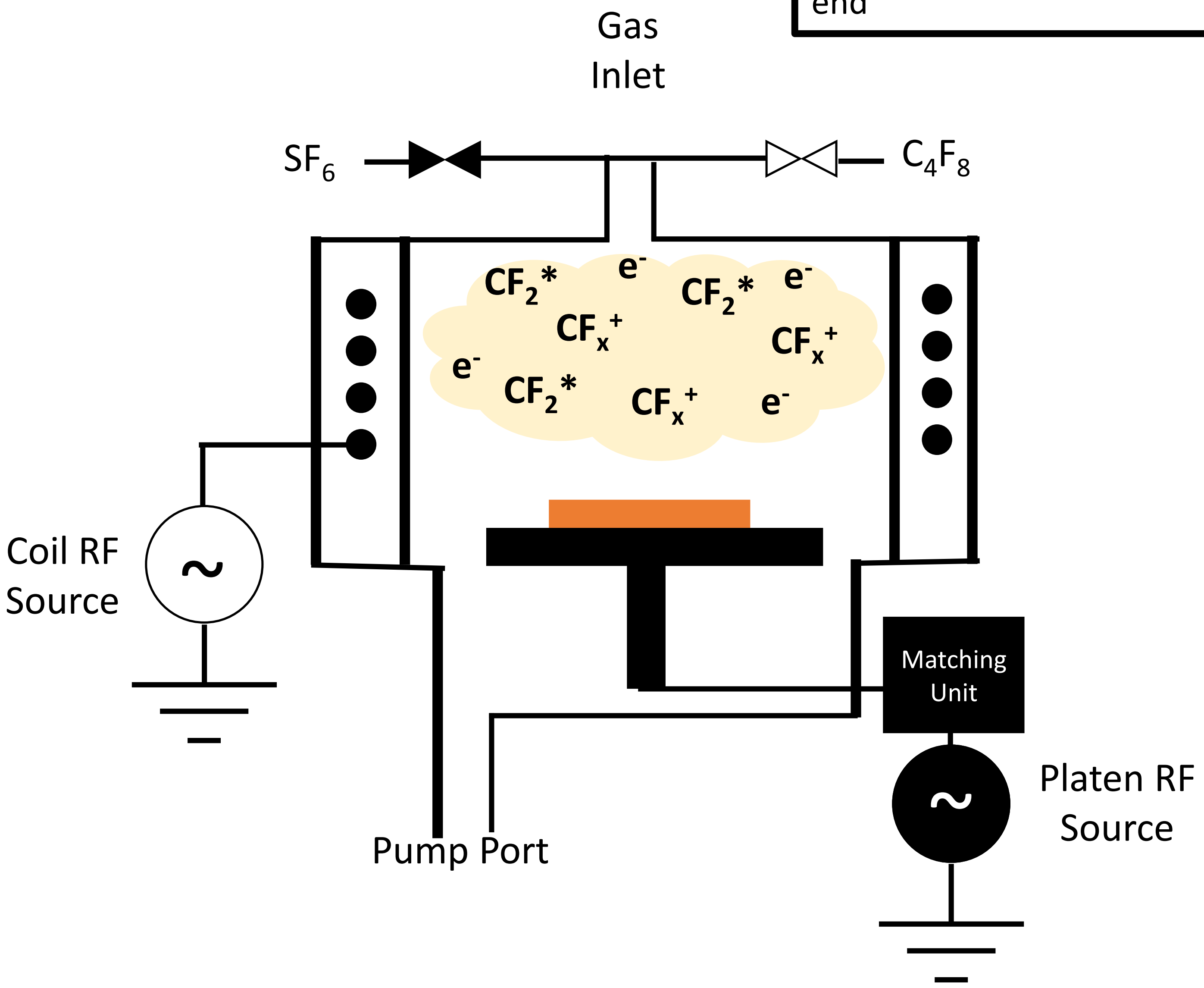

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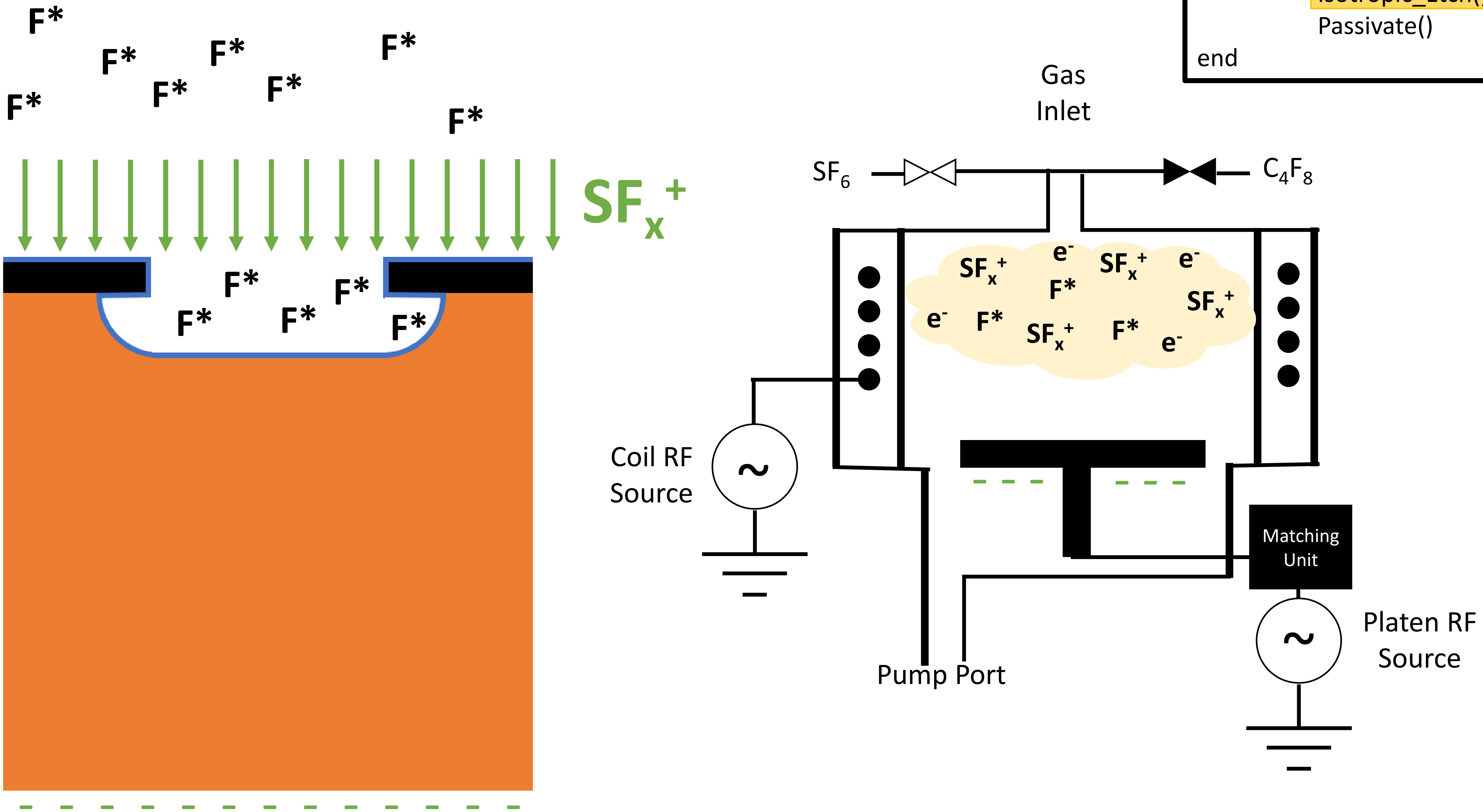

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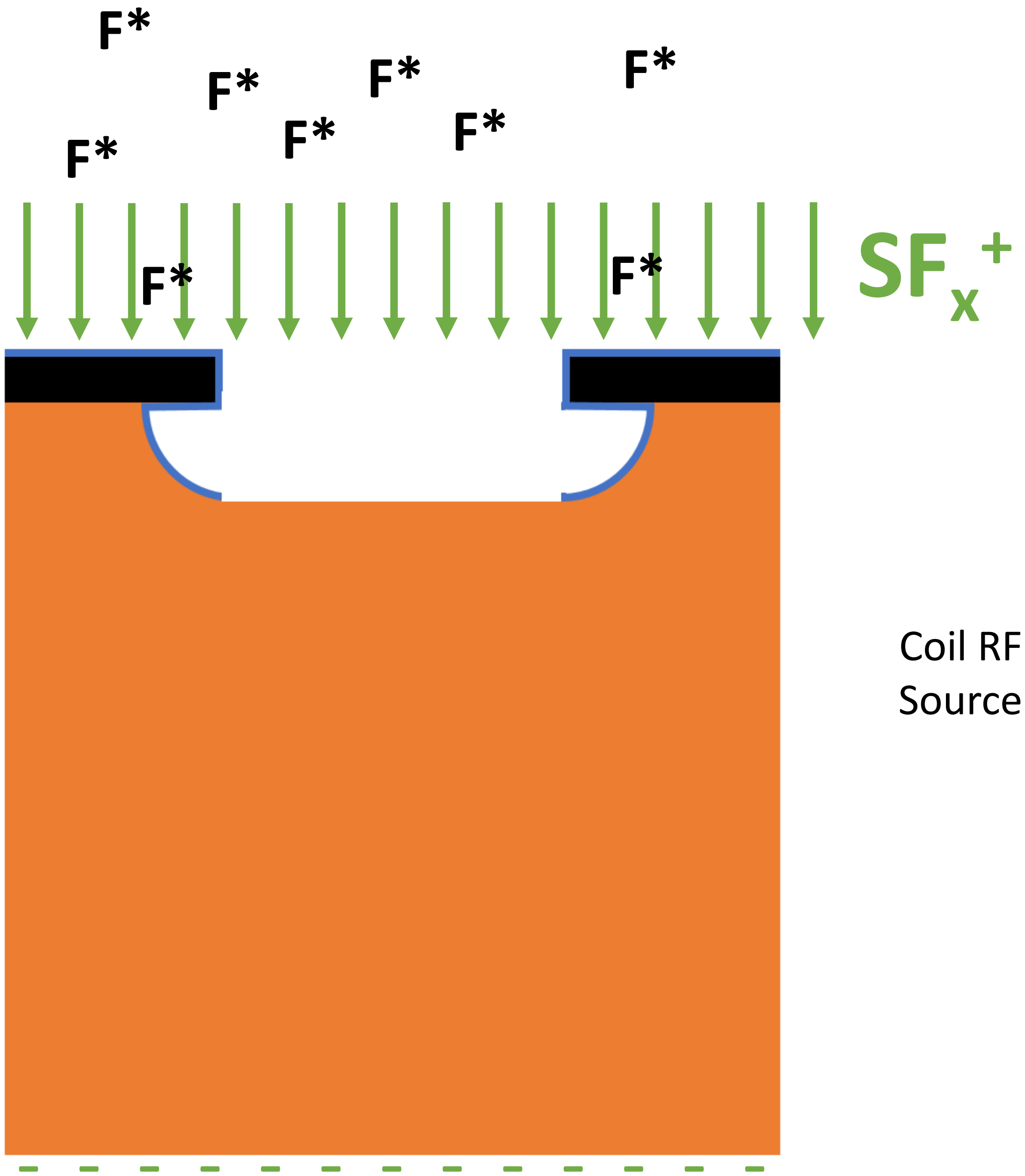

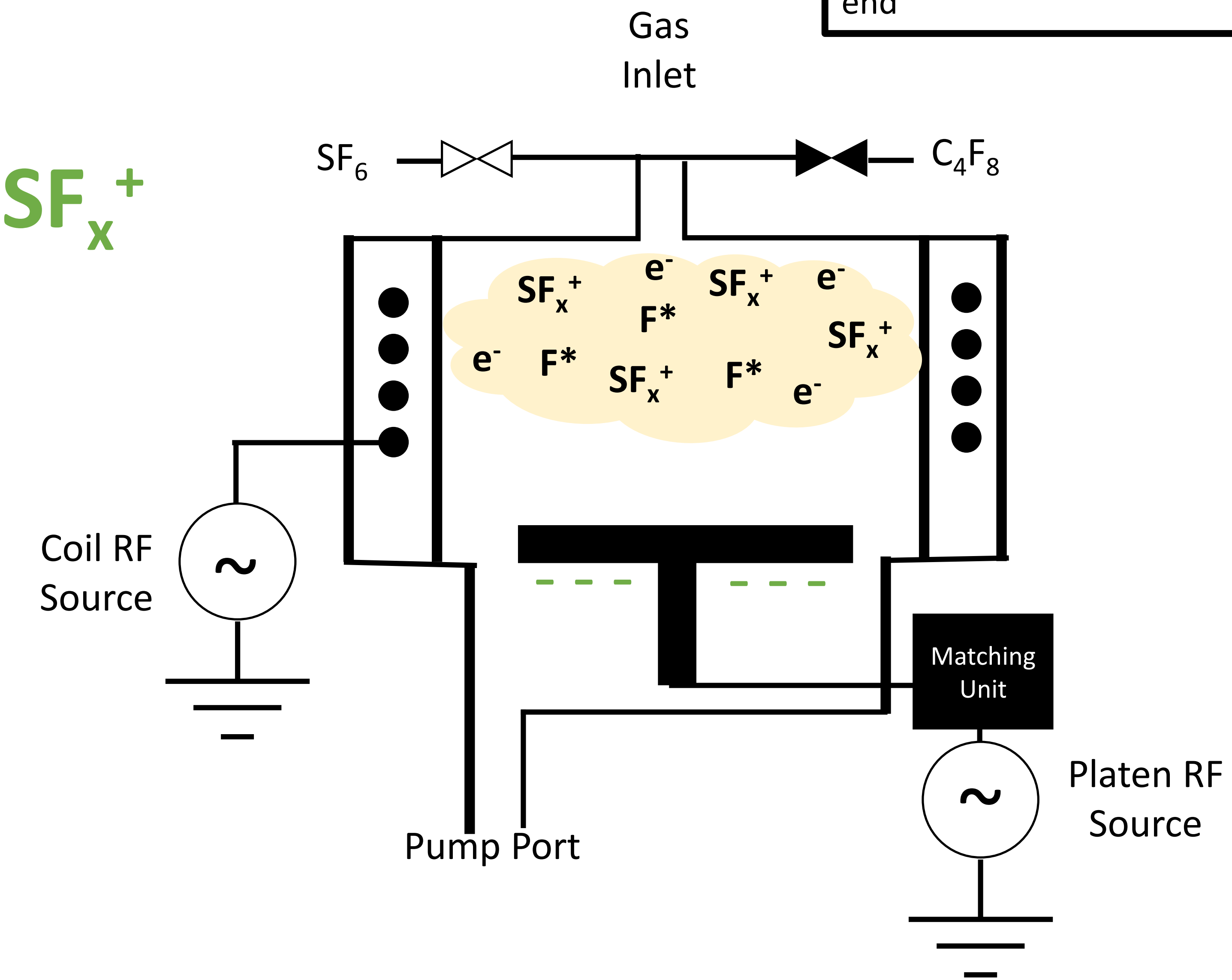

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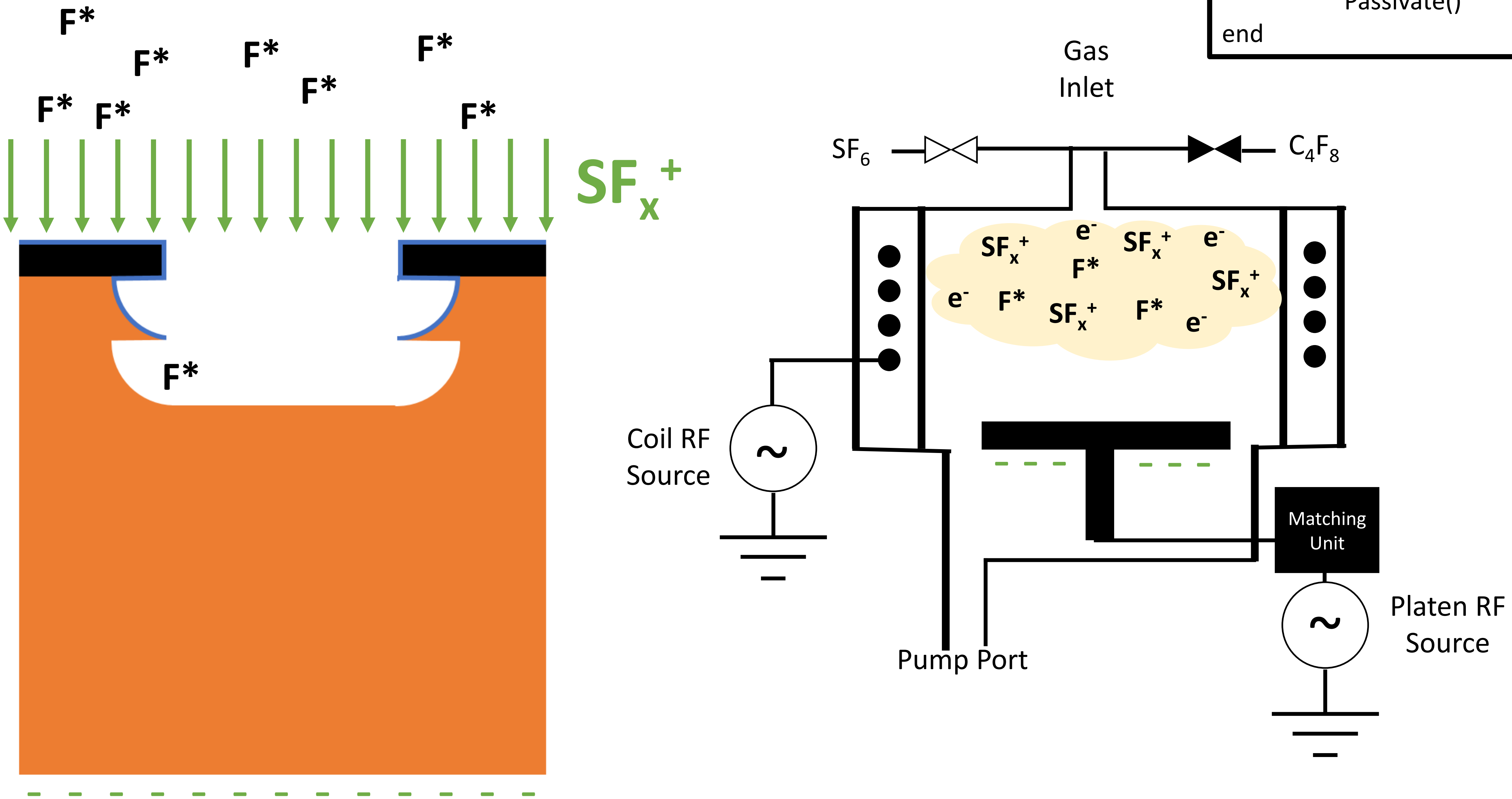

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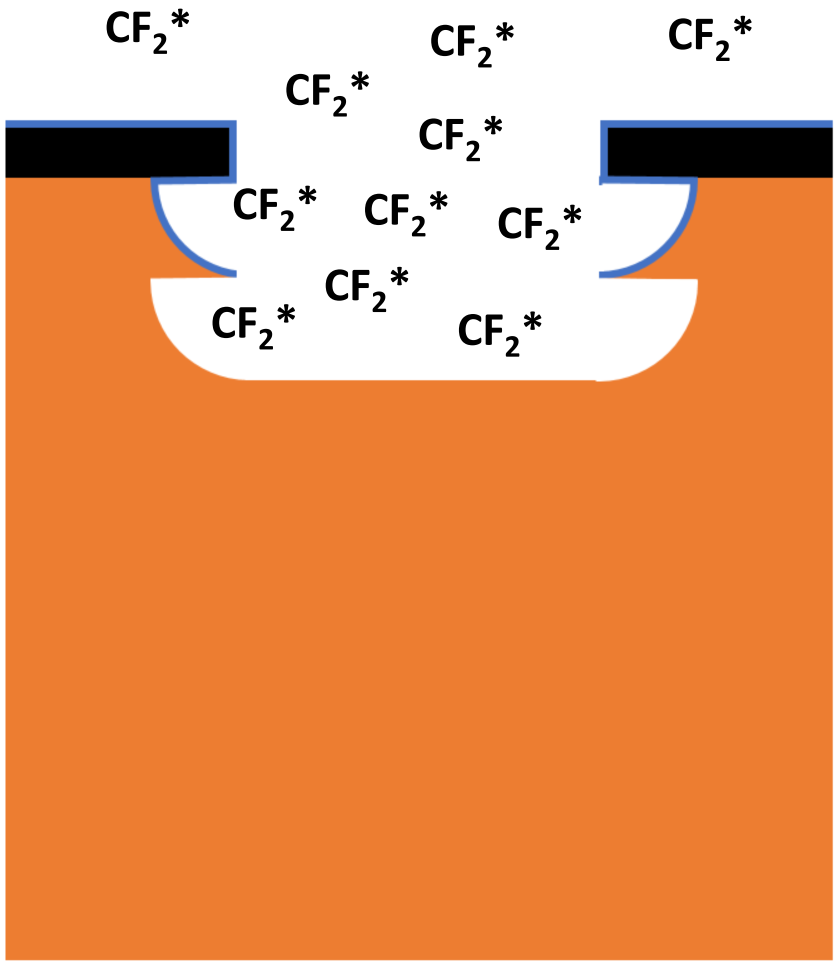

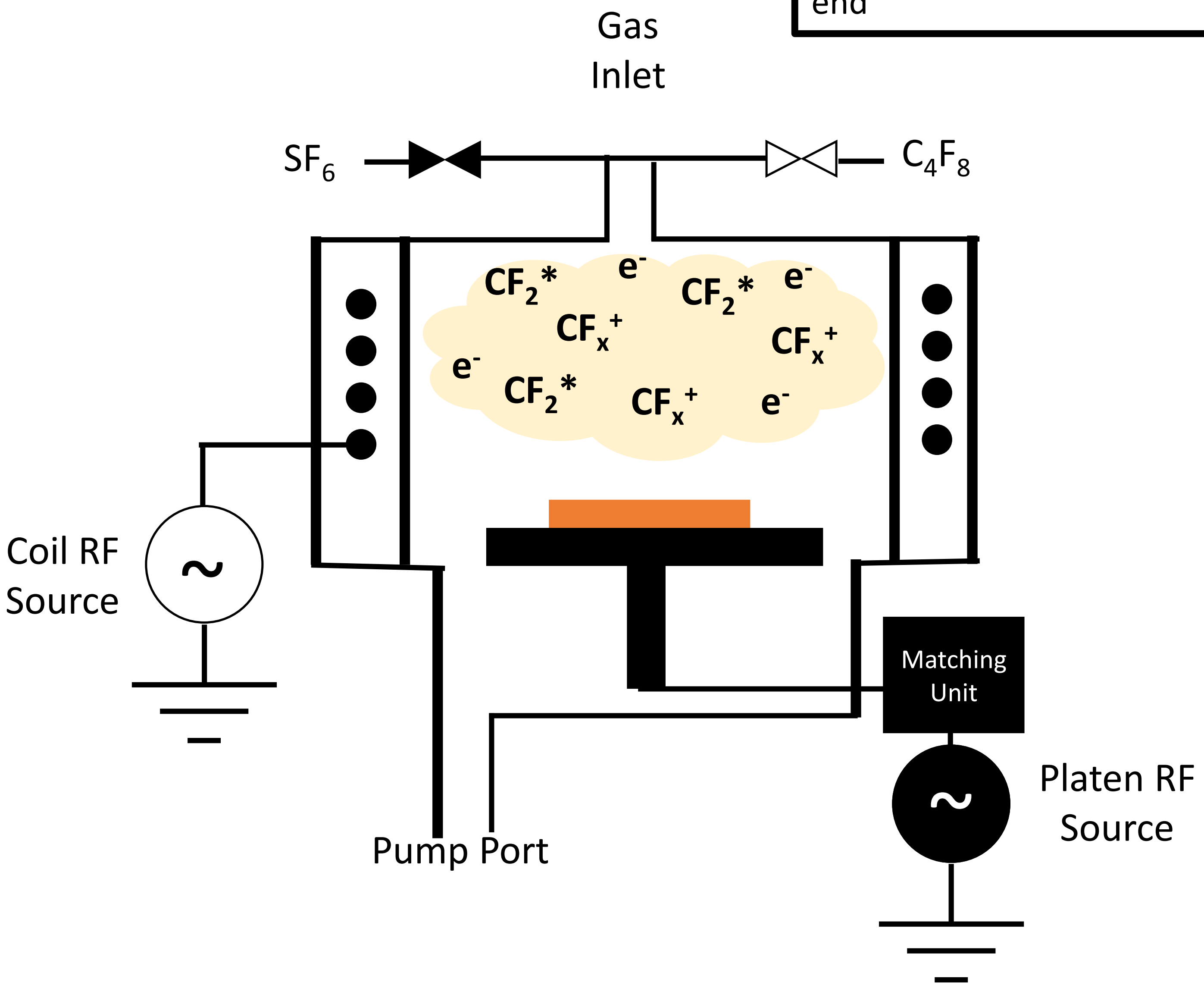

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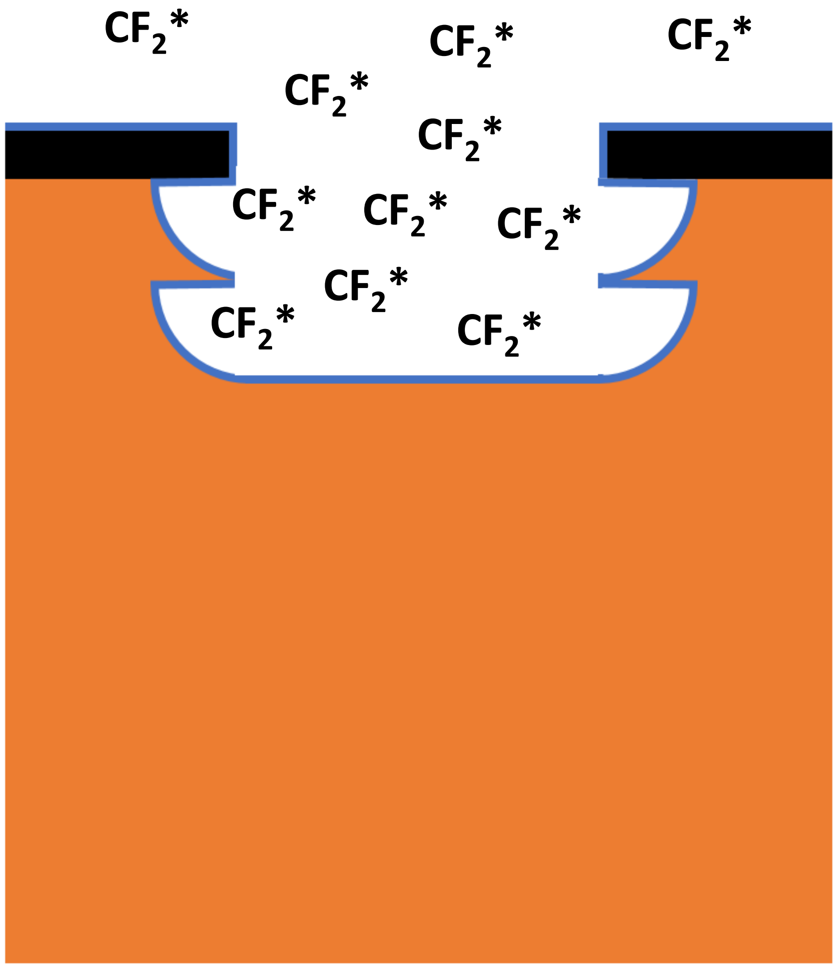
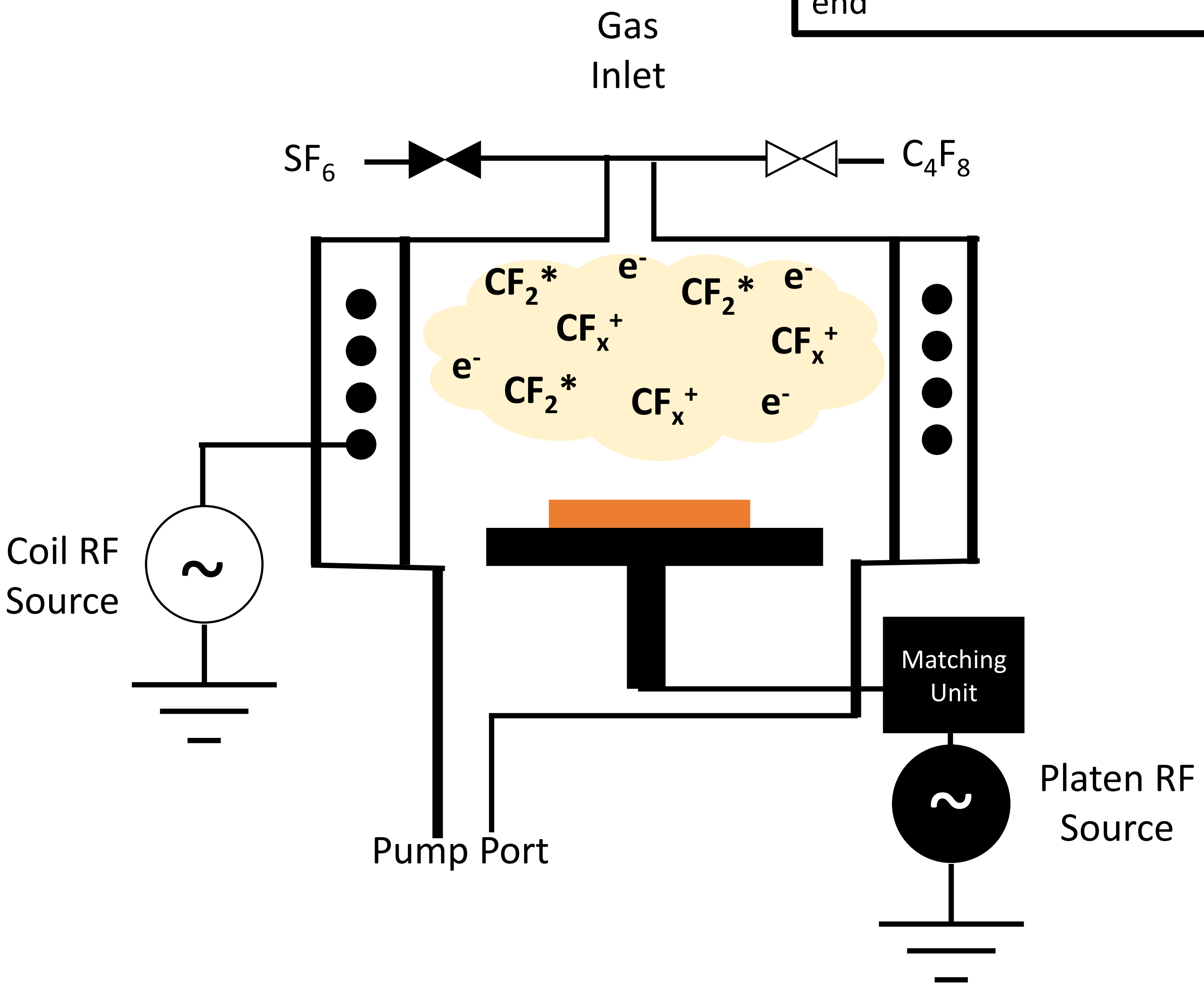
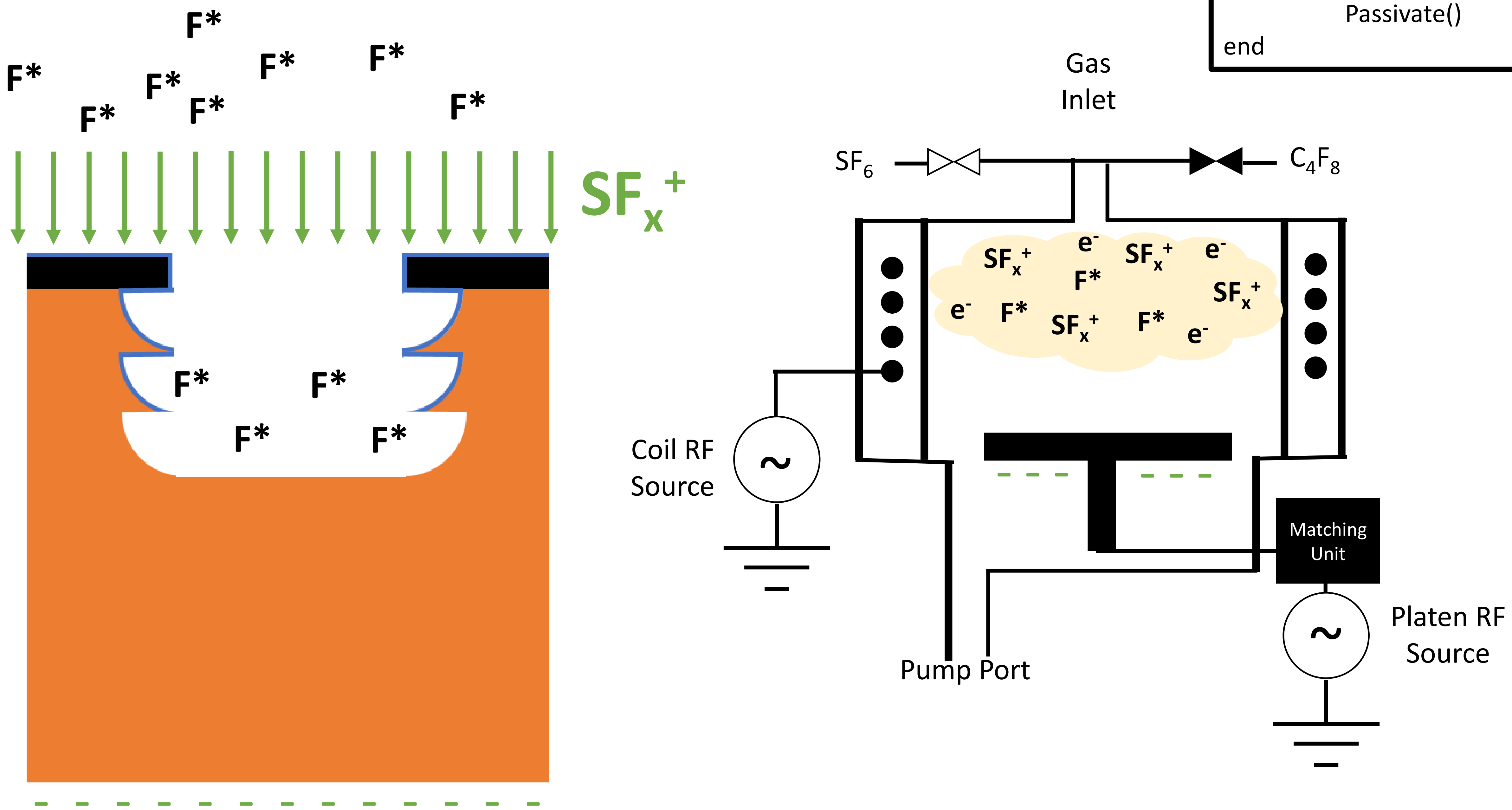




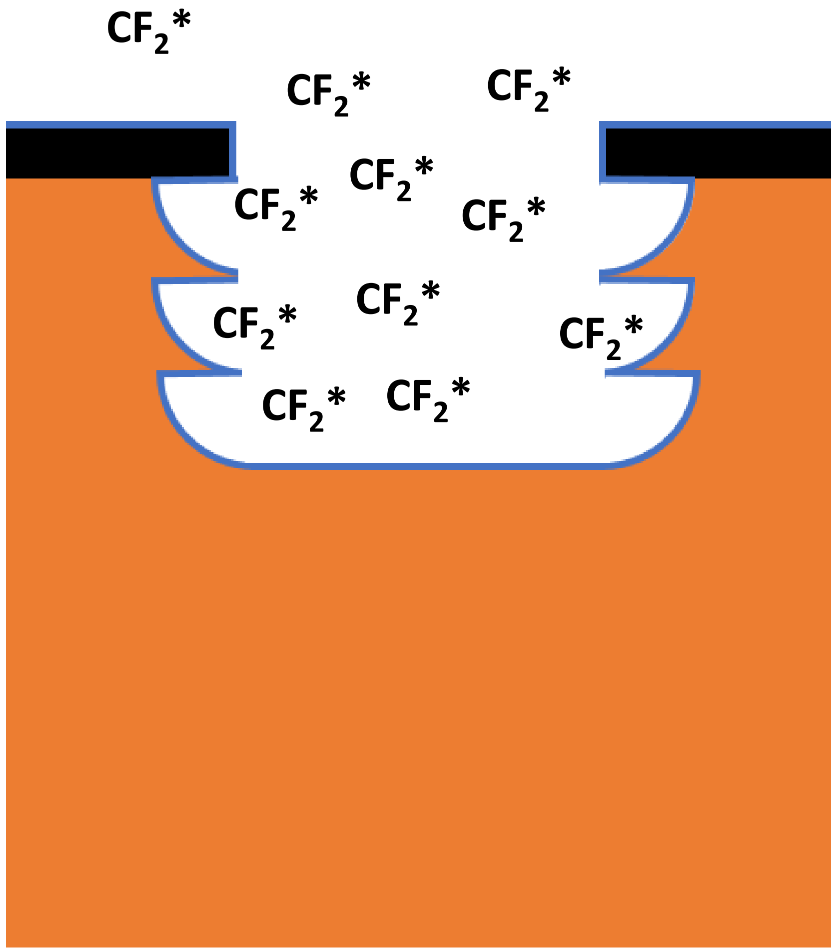
Deep Reactive Ion Etching

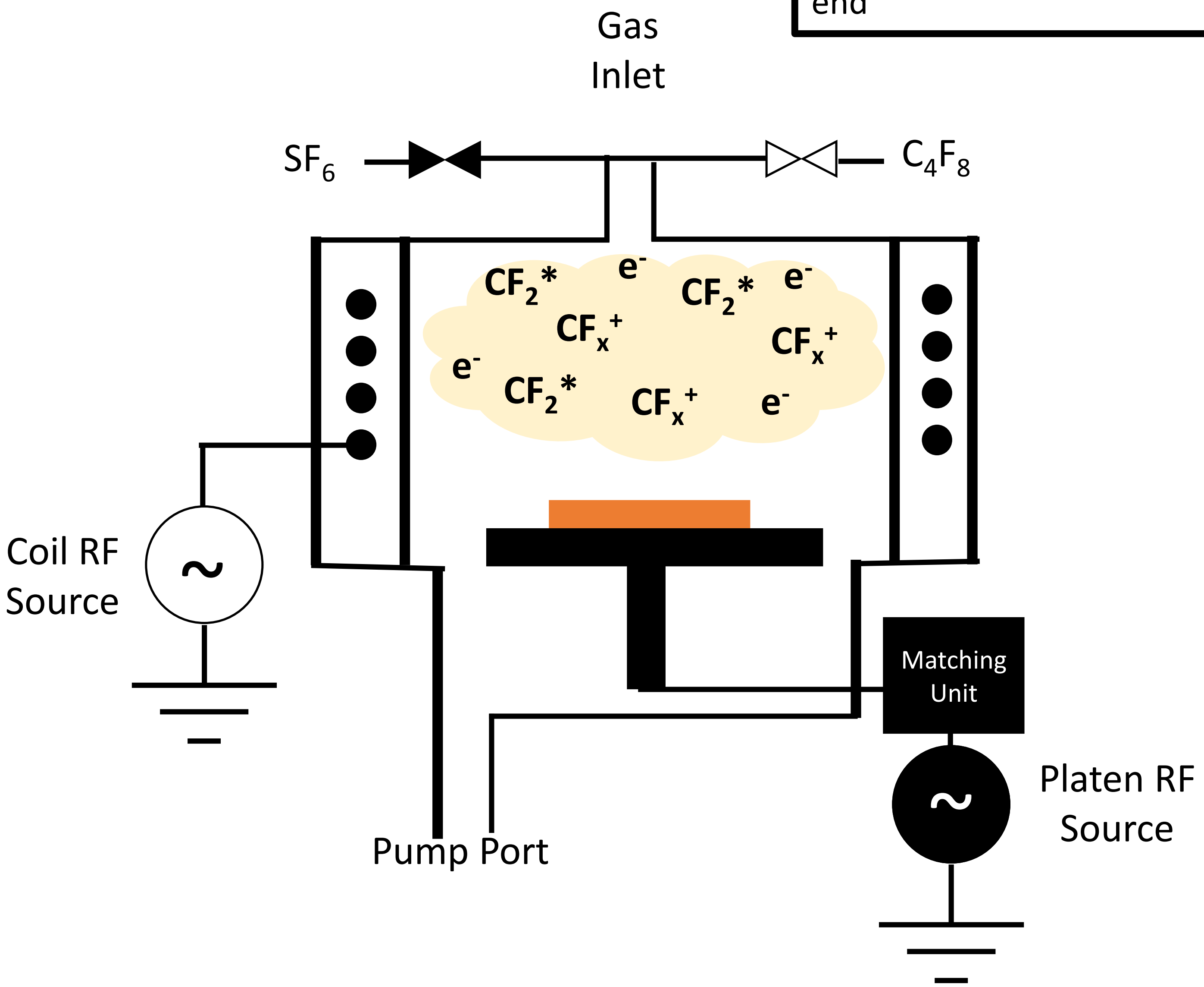
```
for i = 1:N
        Isotropic_Etch()
        Passivate()
end
```



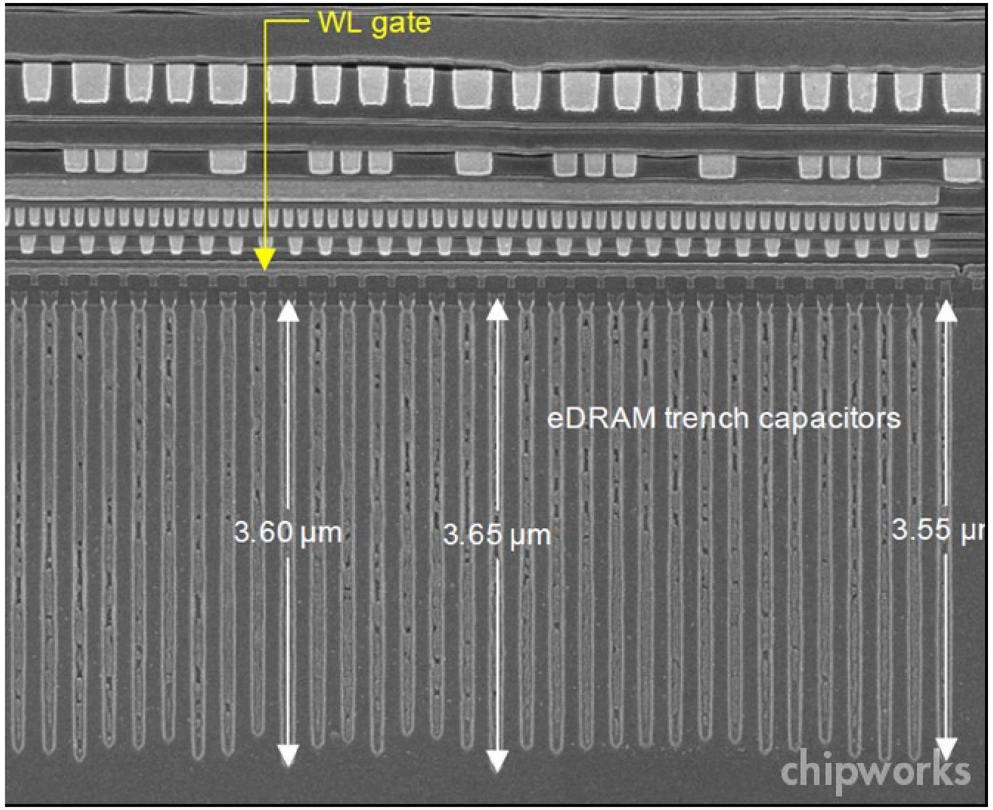
Deep Reactive Ion Etching

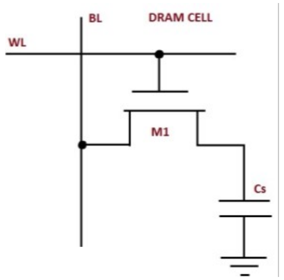
```
for i = 1:N
        Isotropic_Etch()
        Passivate()
end
```



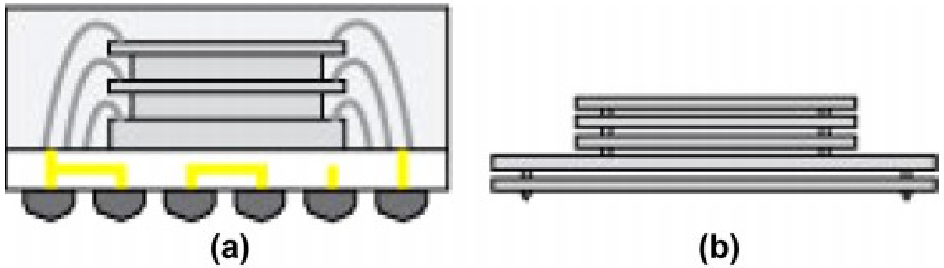


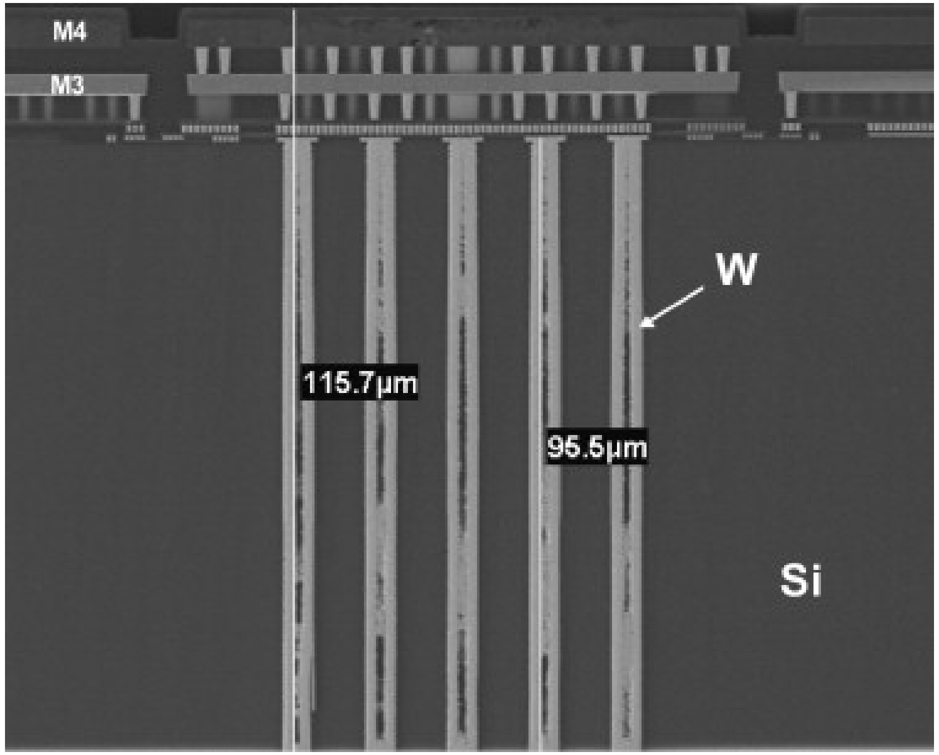
DRIE Applications in CMOS





DRAM

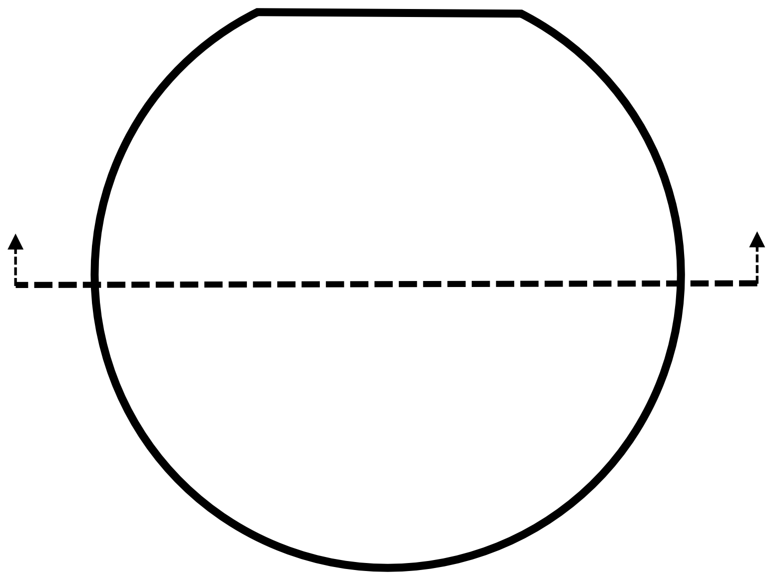


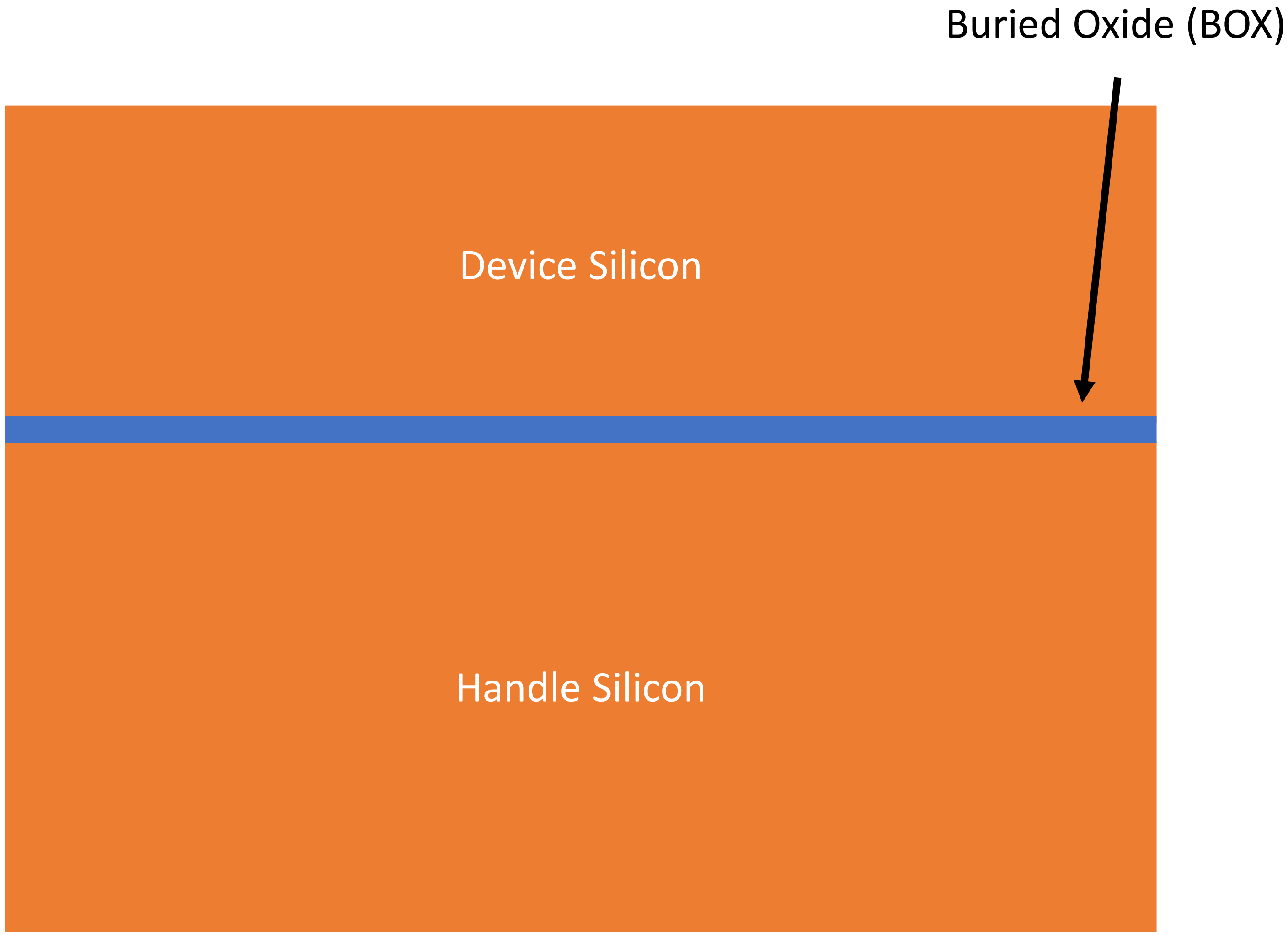


Gambino, 2015

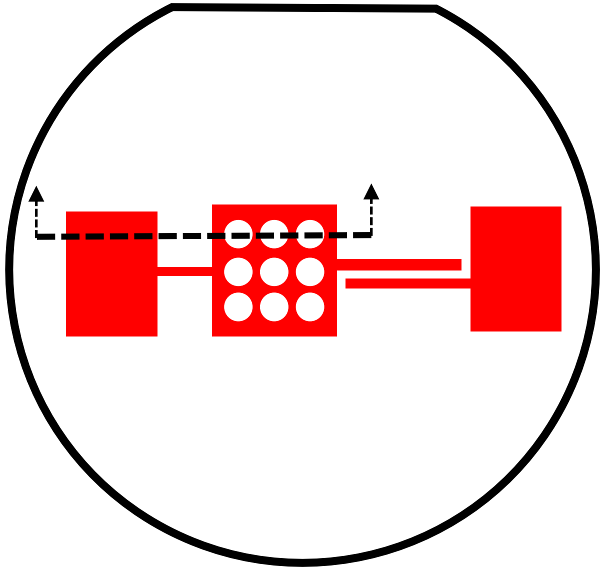
TSVs

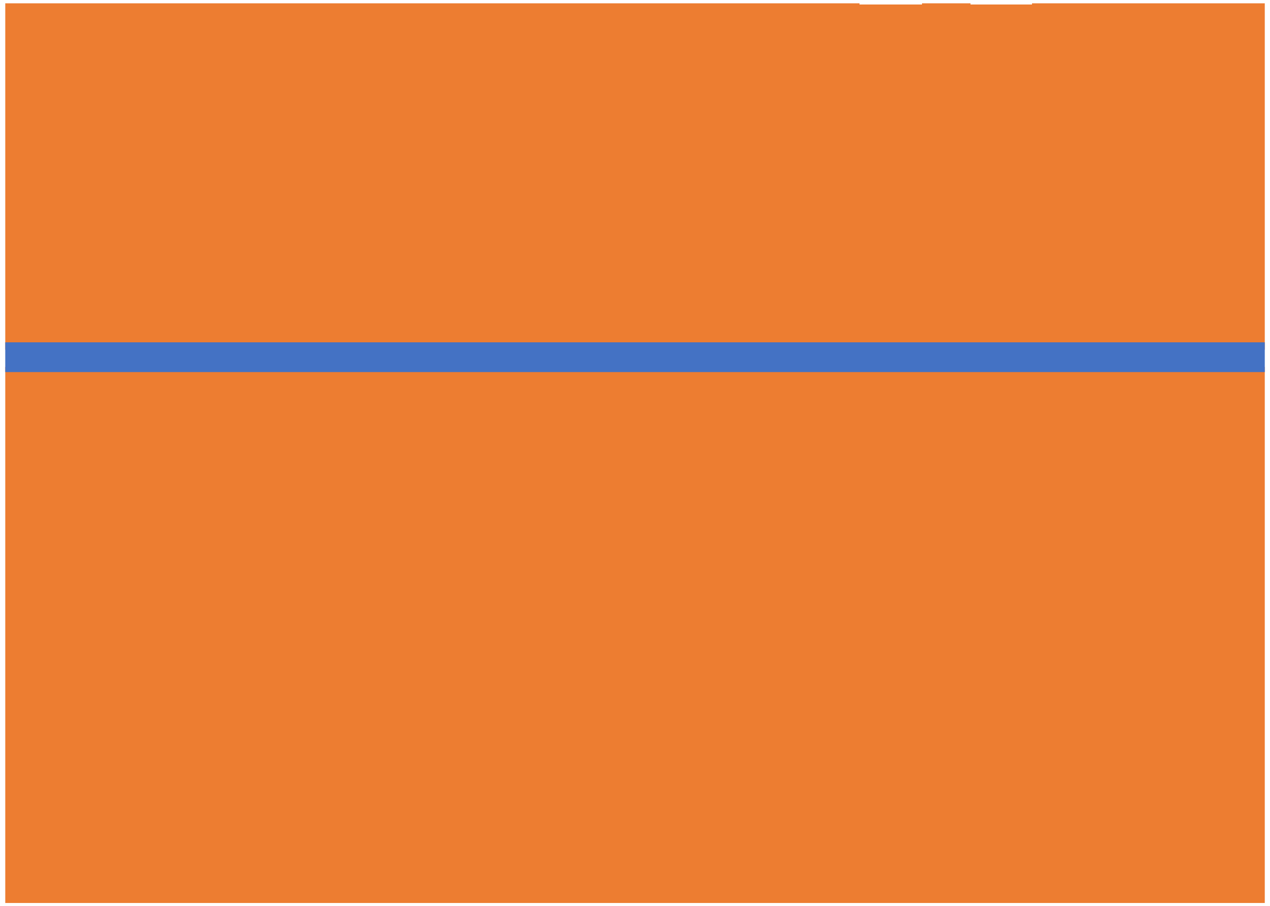
DRIE and Silicon-on-Insulator



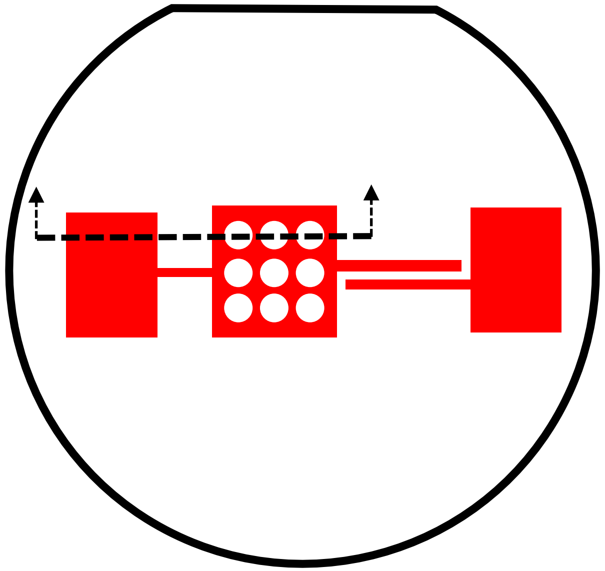


DRIE and Silicon-on-Insulator

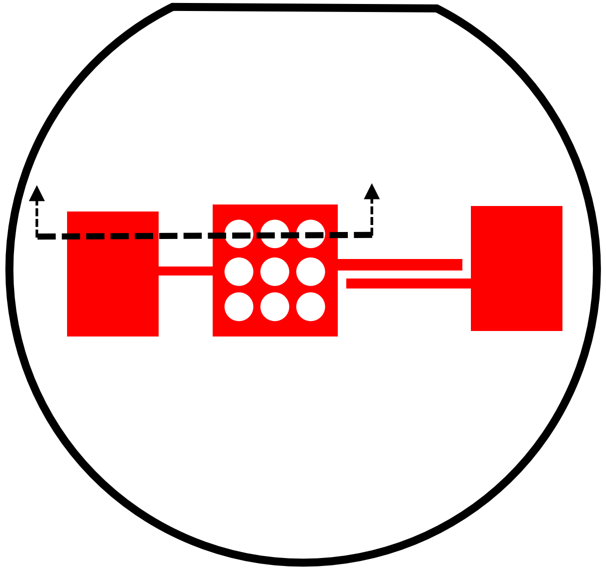


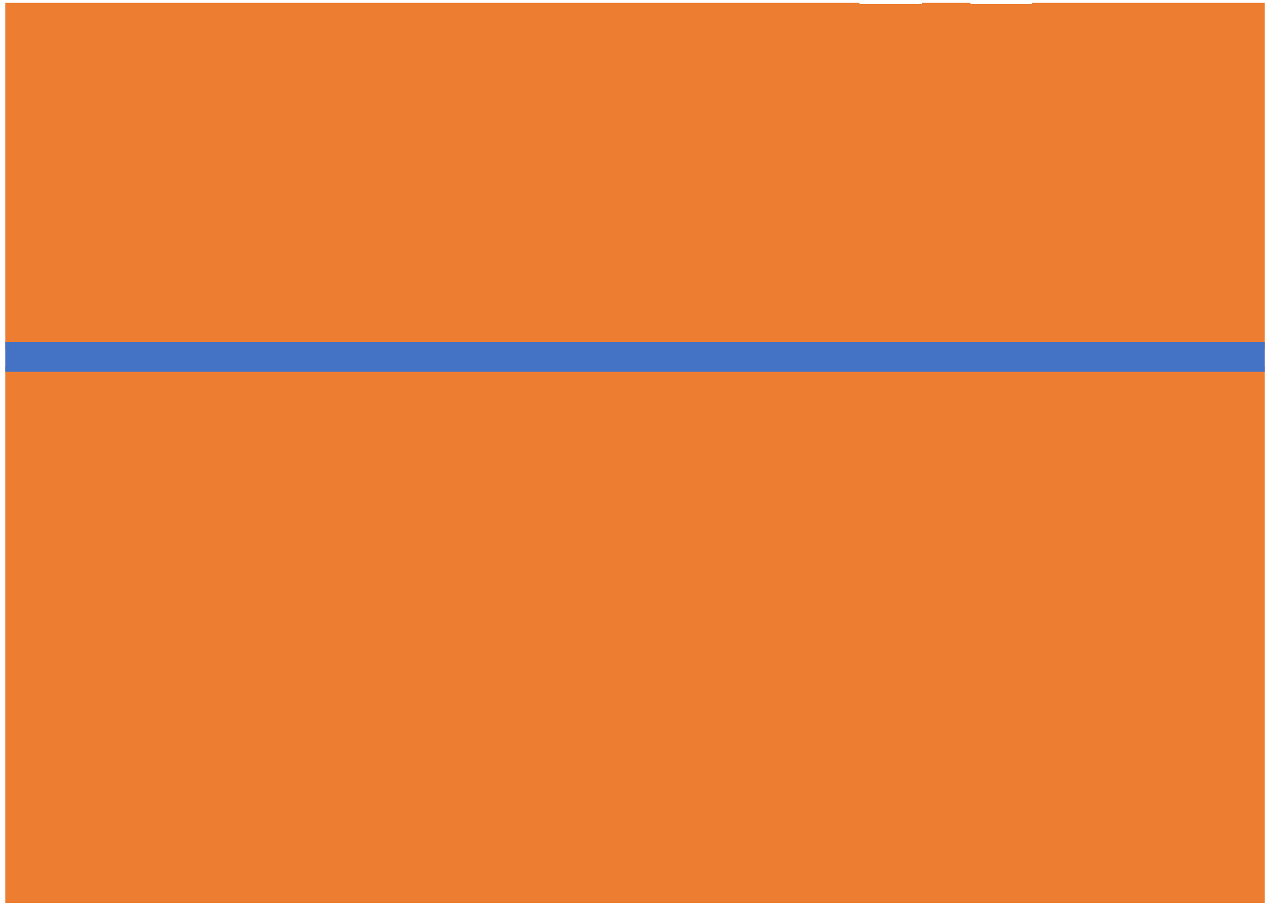


DRIE and Silicon-on-Insulator



DRIE Nonidealities - ARDE





Aspect Ratio Dependent Etch

Smaller holes/trenches etch more slowly

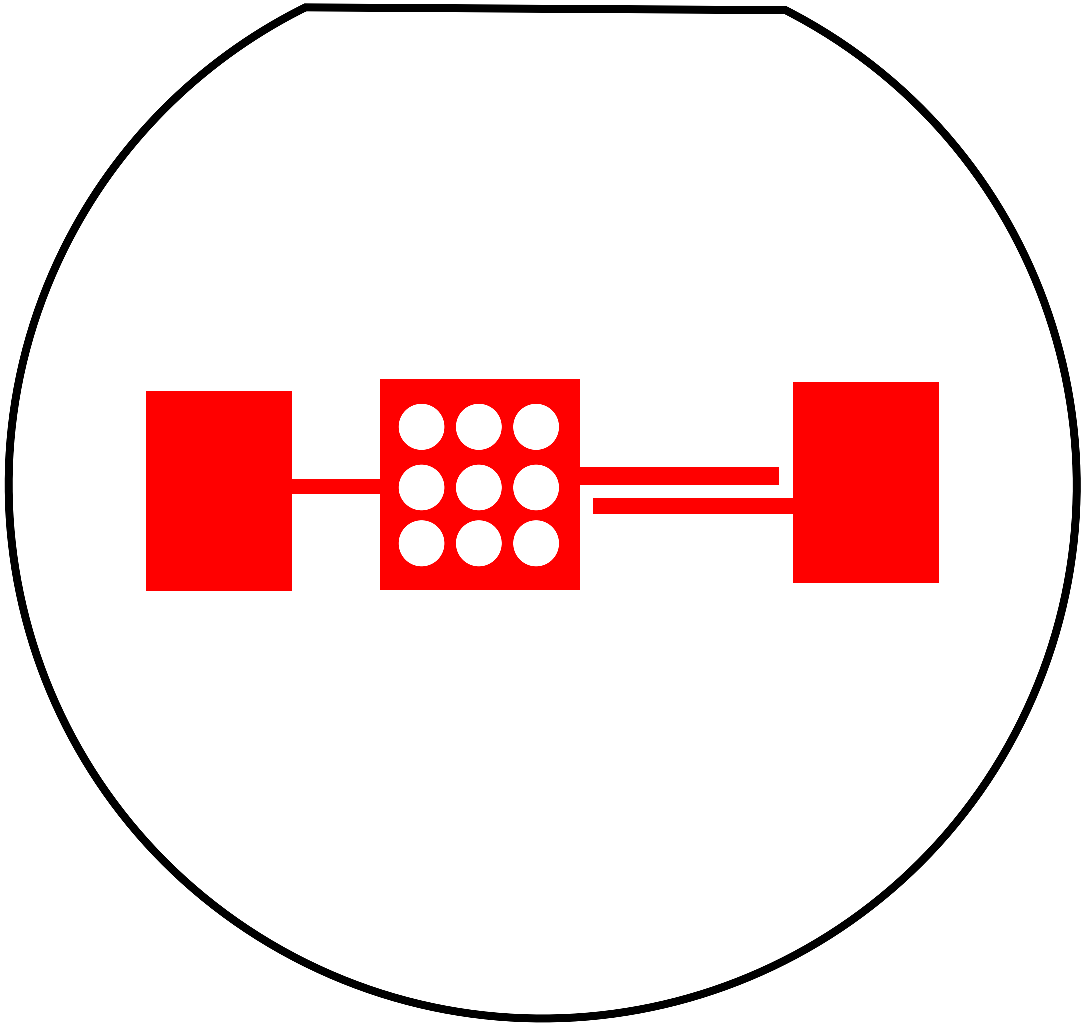
Fix

- Tune recipe
- Limit feature size variation

DRIE Nonidealities – Bullseye

Bullseye Effect

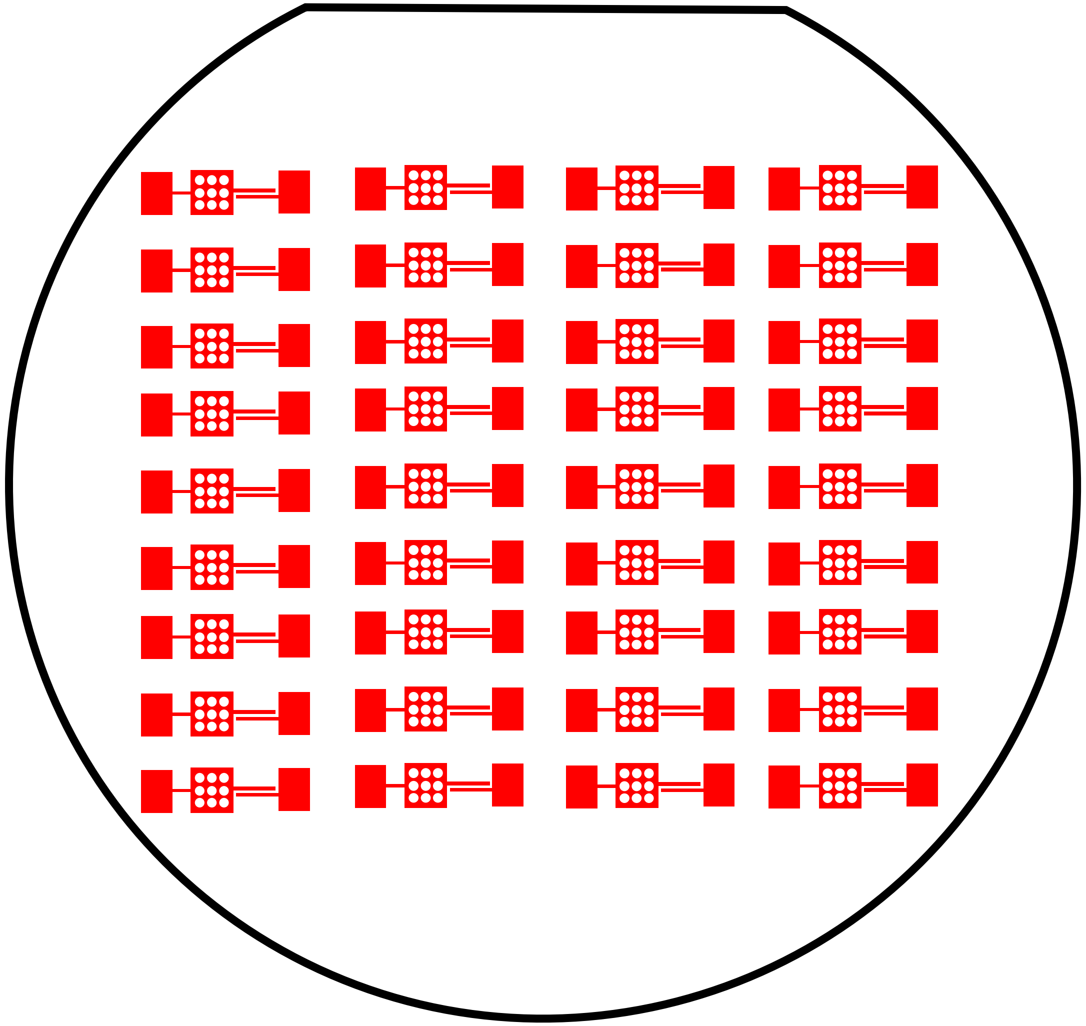
Edges of wafer etch more quickly than center



DRIE Nonidealities – Bullseye

Bullseye Effect

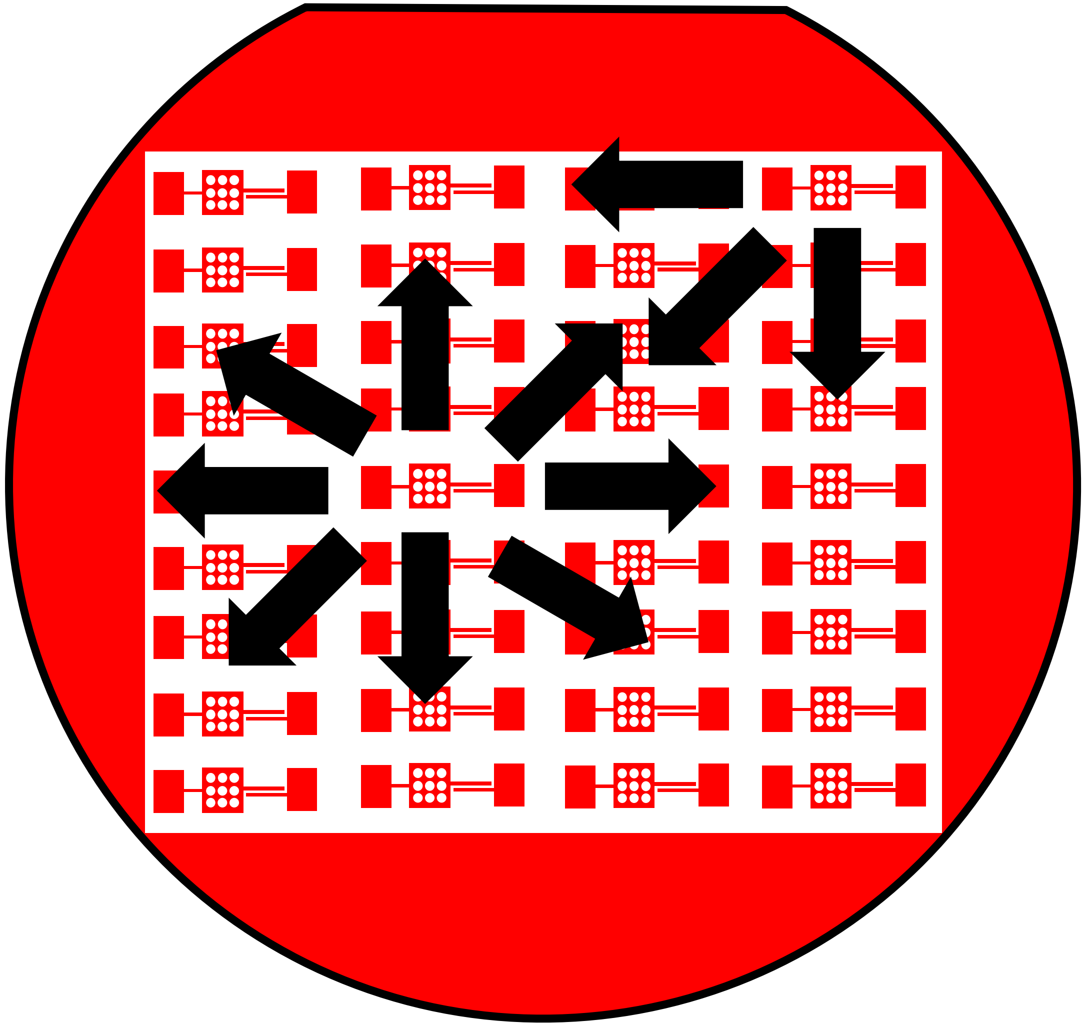
Edges of wafer etch more quickly than center



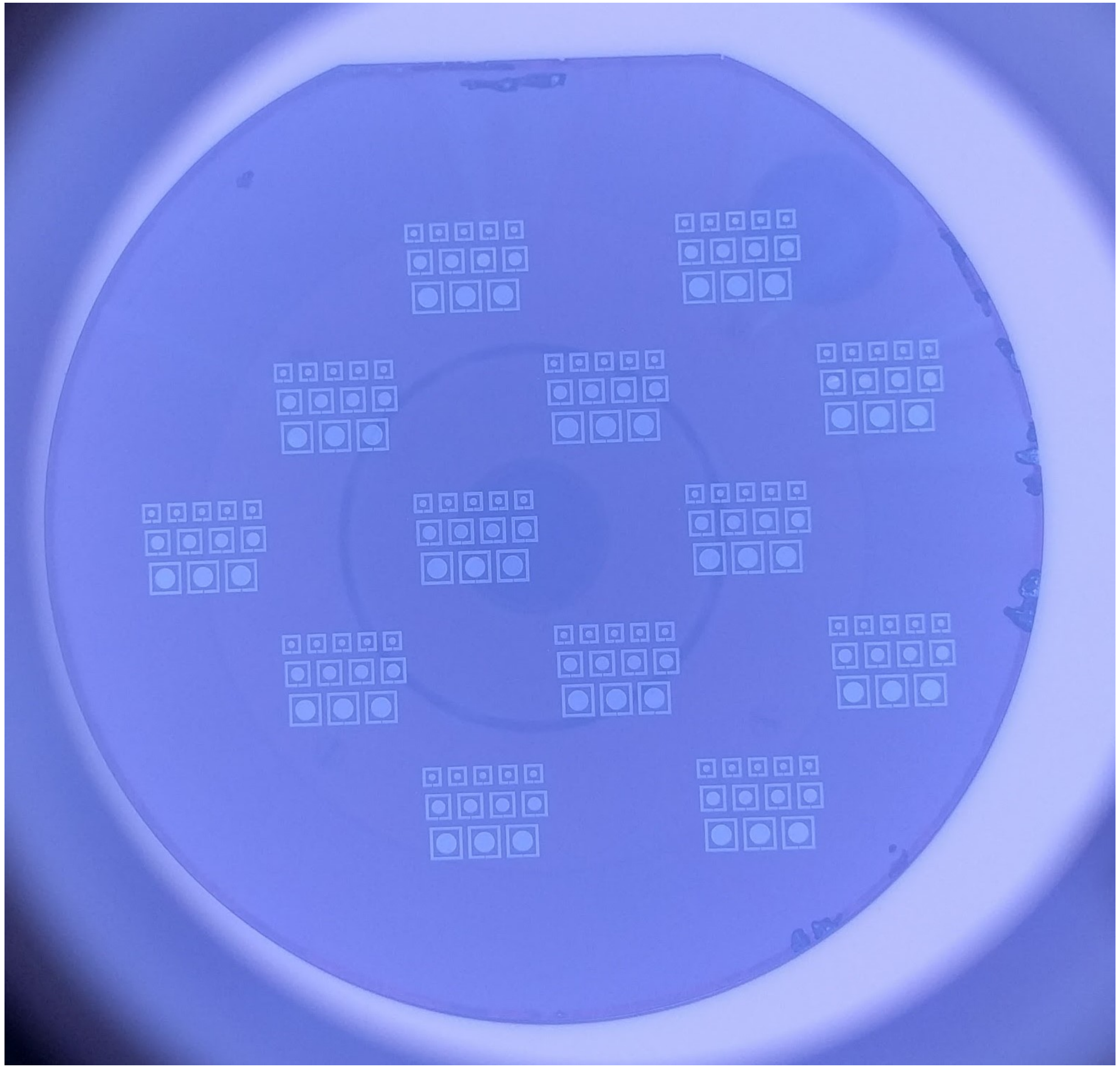
DRIE Nonidealities – Bullseye

Bullseye Effect

Edges of wafer etch more quickly than center



DRIE Nonidealities – Bullseye



Bullseye Effect

Edges of wafer etch more quickly than center

Fix

- Checkerboard

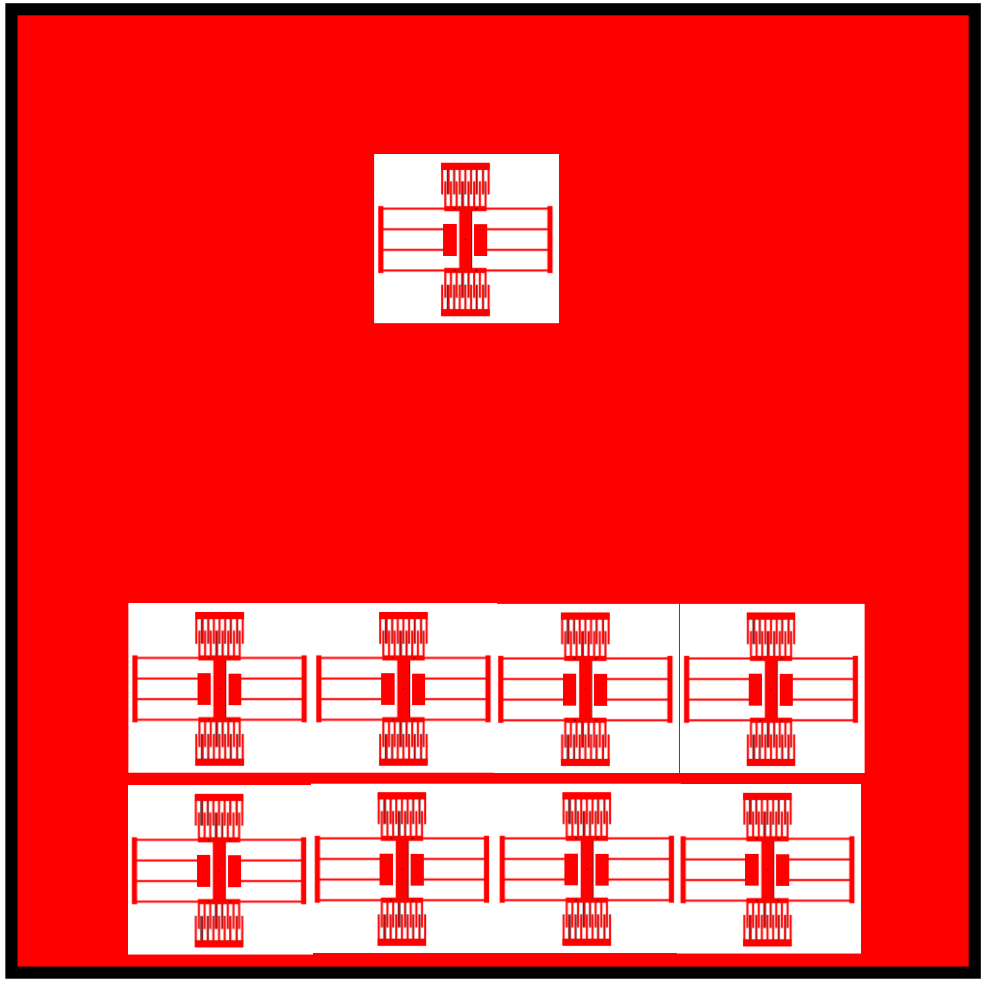
DRIE Nonidealities – Microloading

Microloading (RIE-lag)

Isolated areas etch more quickly than dense arrays

Fix

- Uniform layout
- Limit etched area



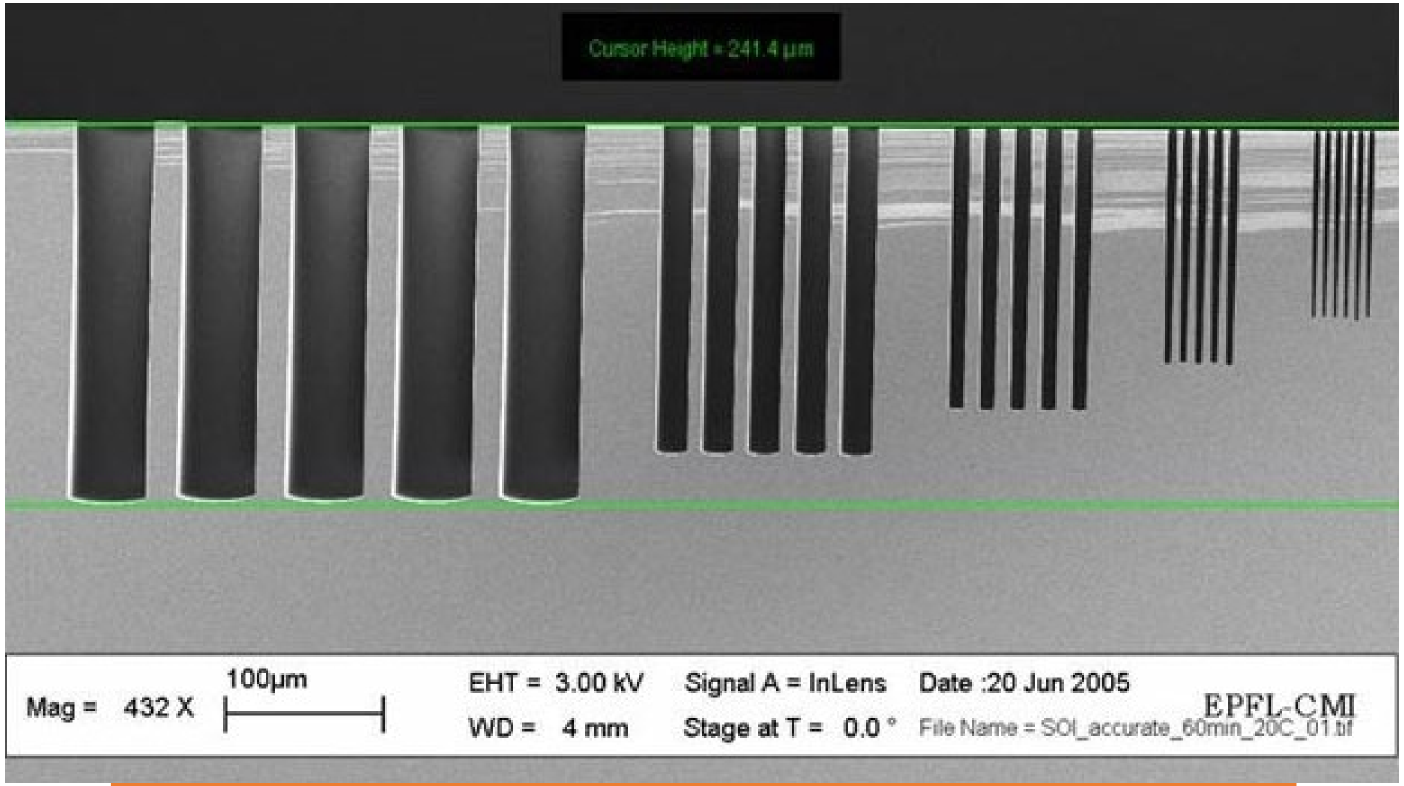
DRIE Nonidealities – Uniformity Recap

ARDE

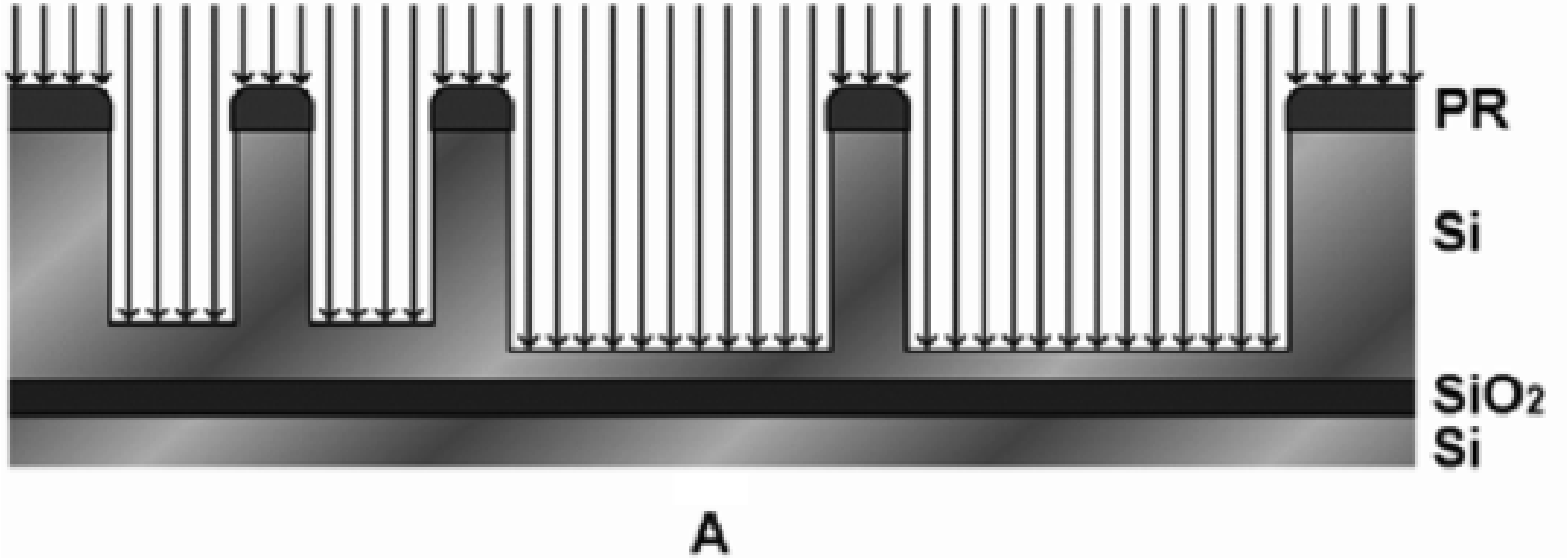
Bullseye

Microloading (RIE-lag)

Why do we care?

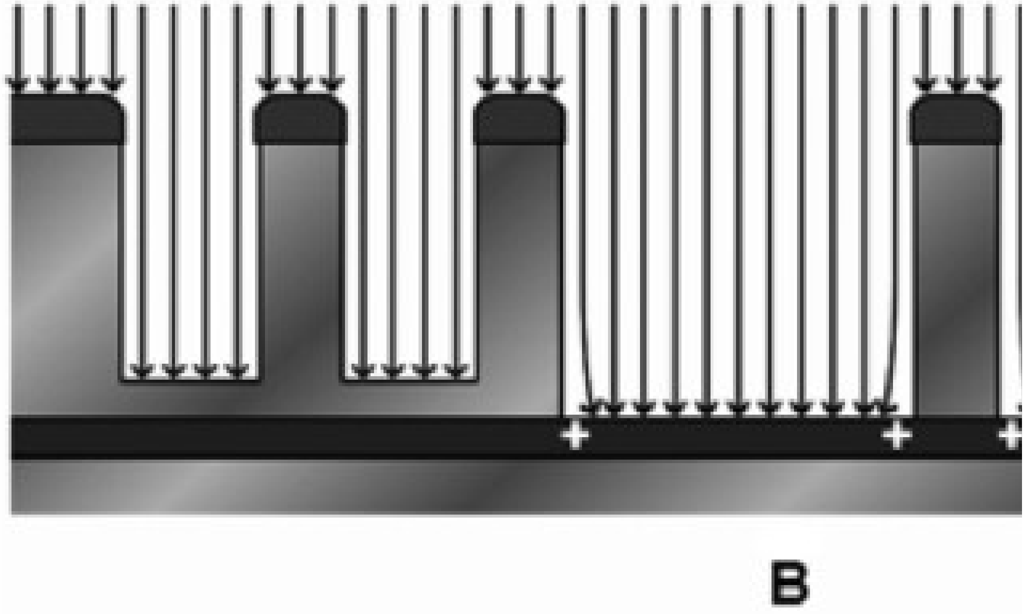


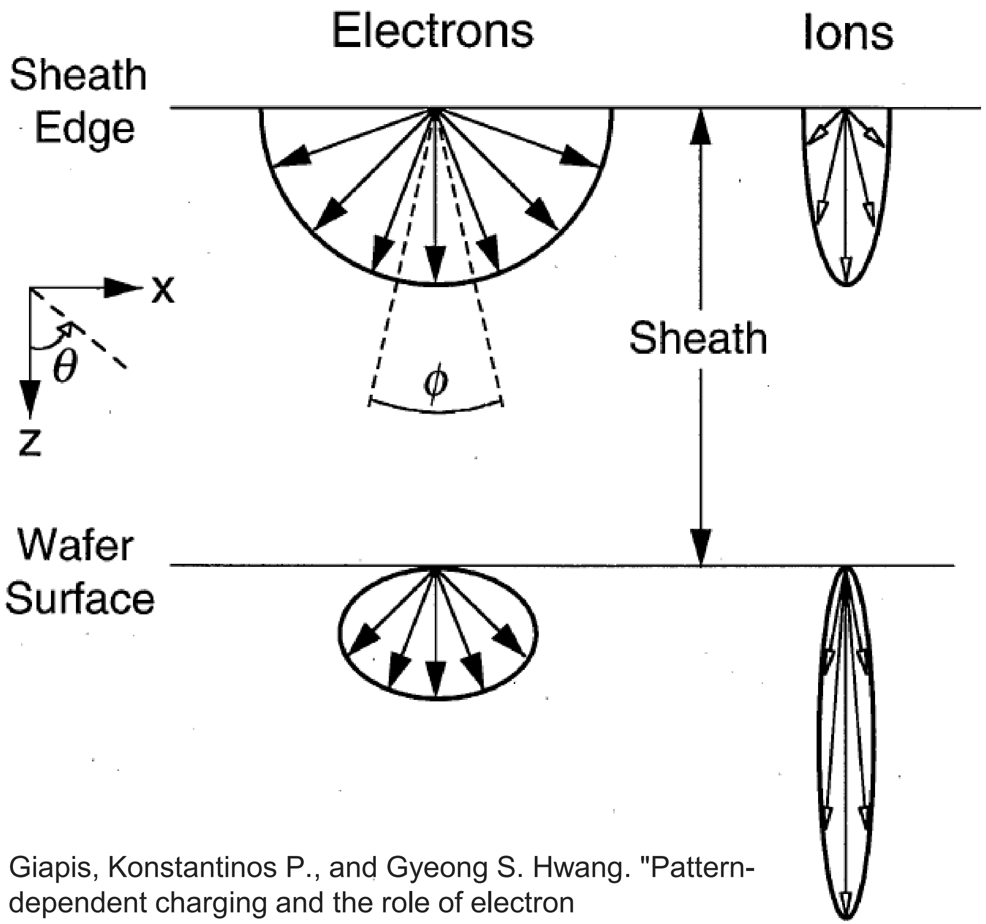
DRIE Nonidealities – Footing



Haobing, Liu, and Franck Chollet. "**Layout controlled one-step dry etch and release of MEMS using deep RIE on SOI wafer.**" *Journal of microelectromechanical systems* 15.3 (2006): 541-547.

DRIE Nonidealities – Footing

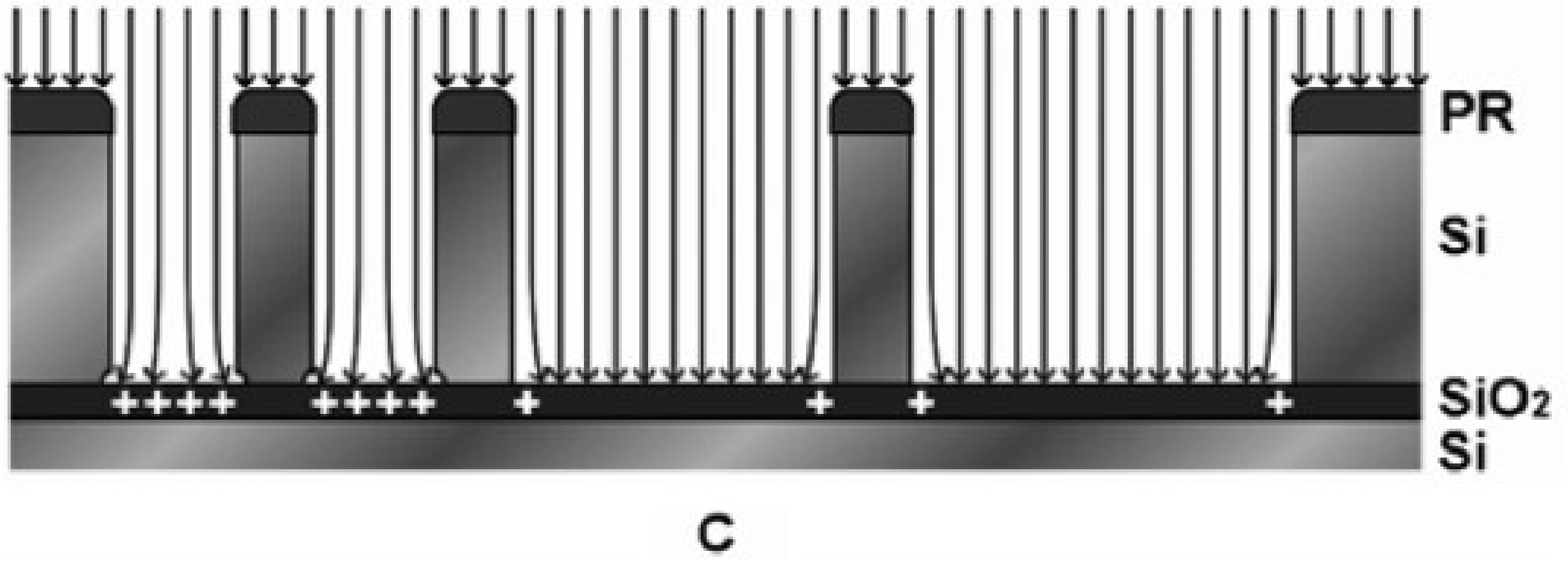




Giapis, Konstantinos P., and Gyeong S. Hwang. "Pattern-dependent charging and the role of electron tunneling." (1998)

Haobing, Liu, and Franck Chollet. "**Layout controlled one-step dry etch and release of MEMS using deep RIE on SOI wafer.**" *Journal of microelectromechanical systems* 15.3 (2006): 541-547.

DRIE Nonidealities – Footing



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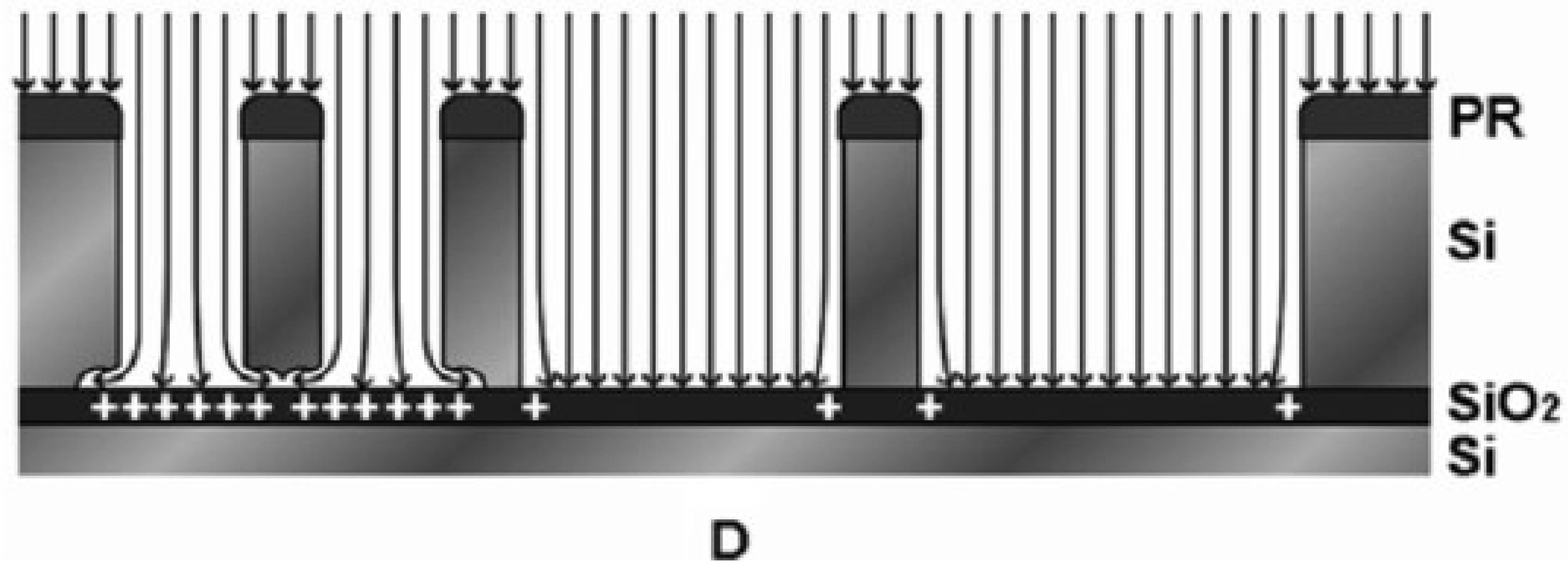
DRIE Nonidealities – Footing



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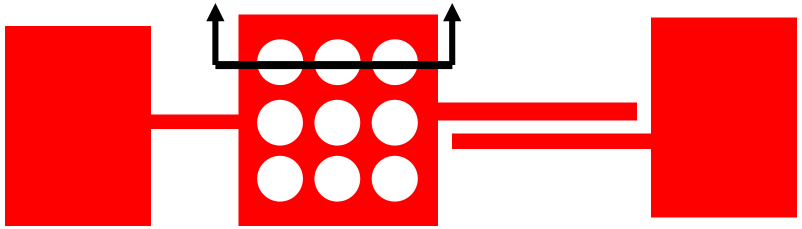
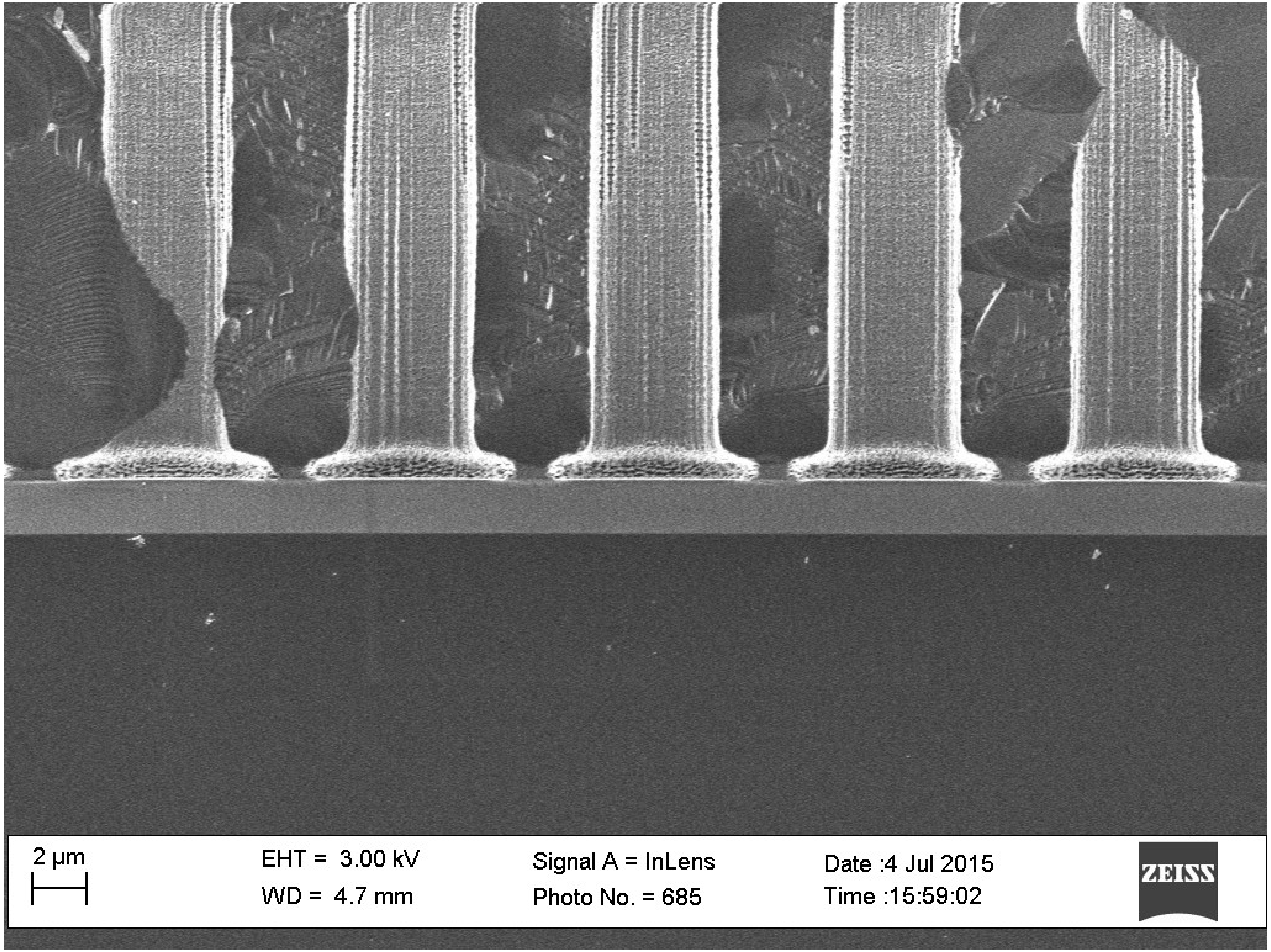
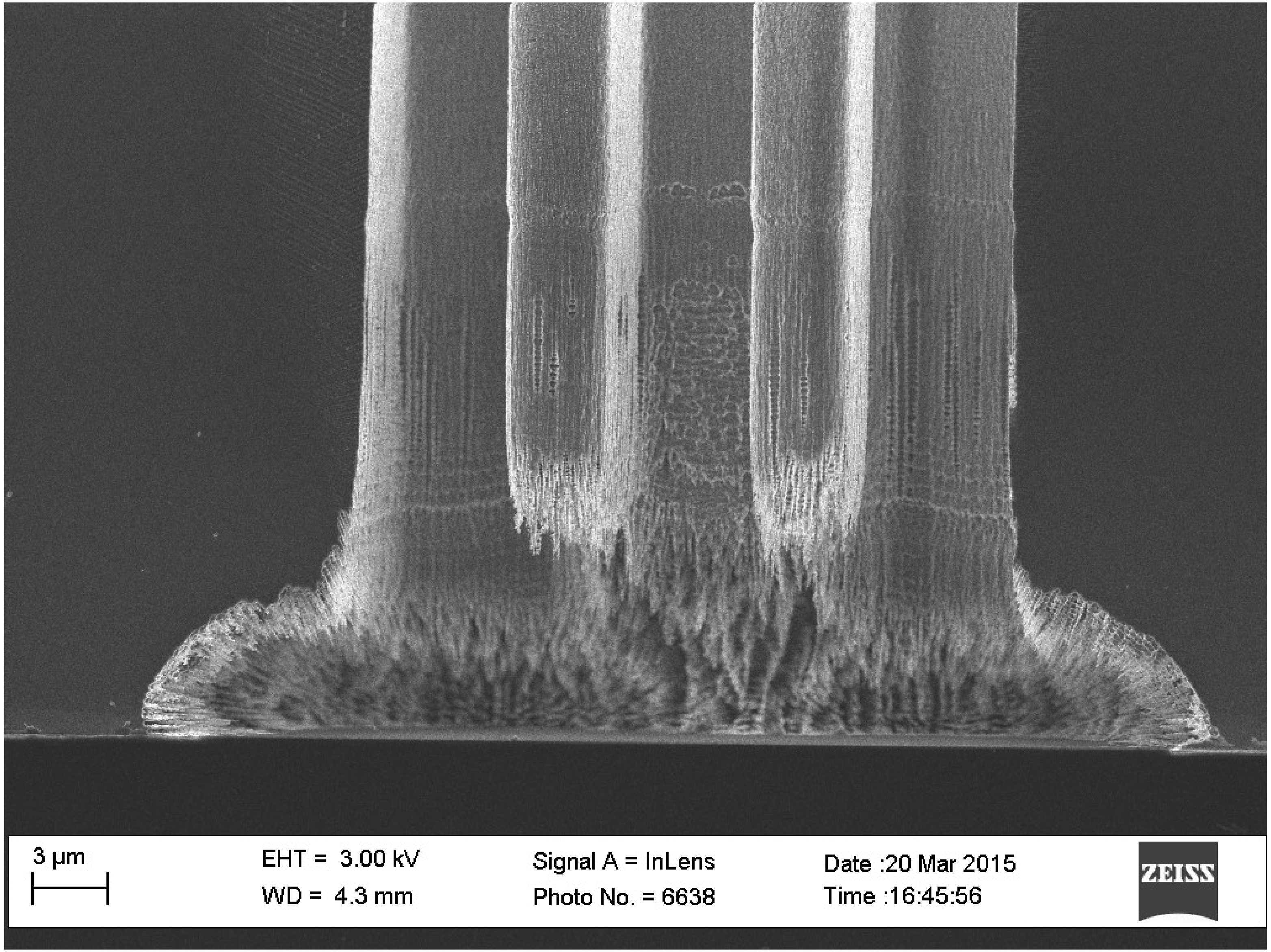
DRIE Nonidealities – Footing





DRIE Nonidealities – Footing



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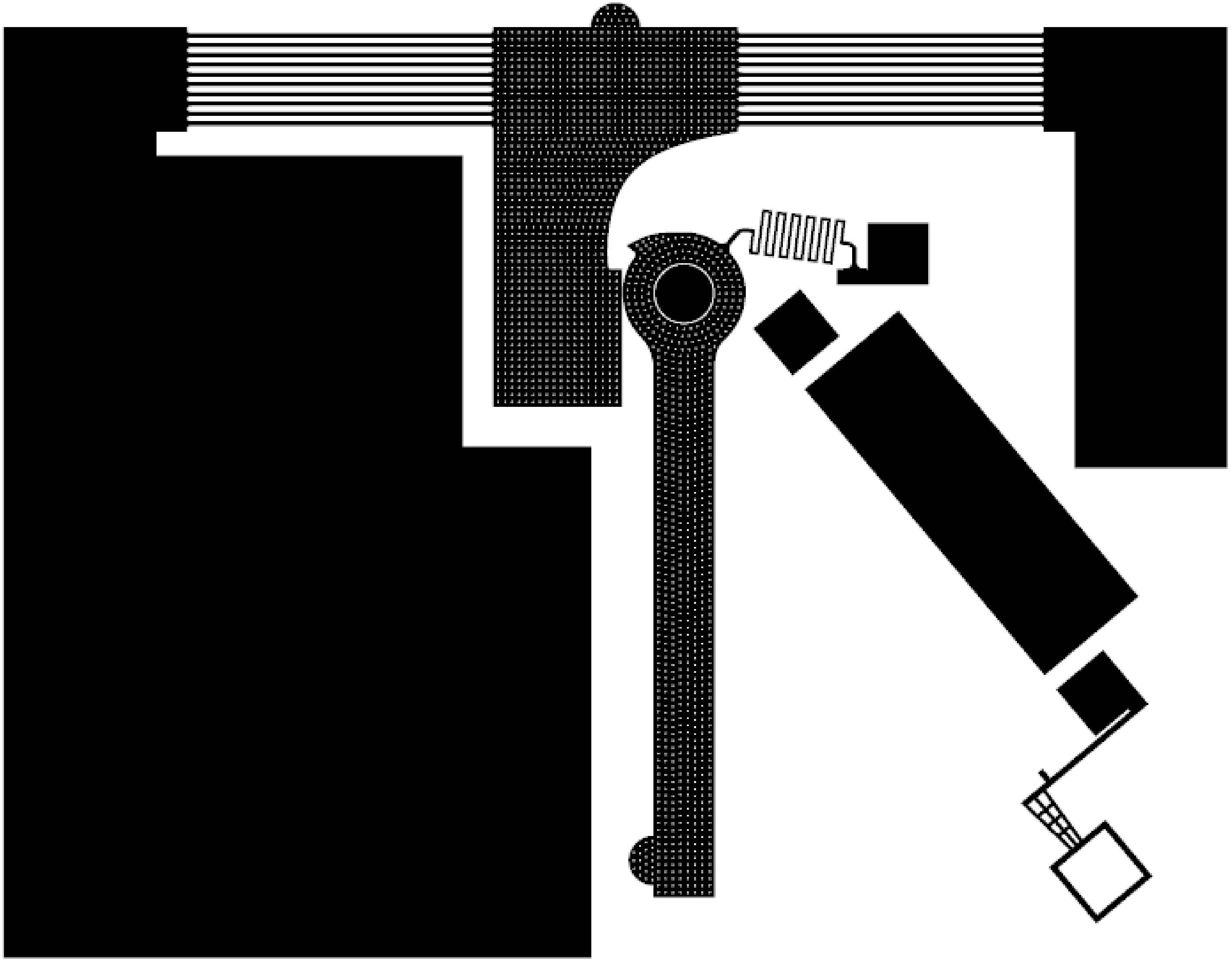

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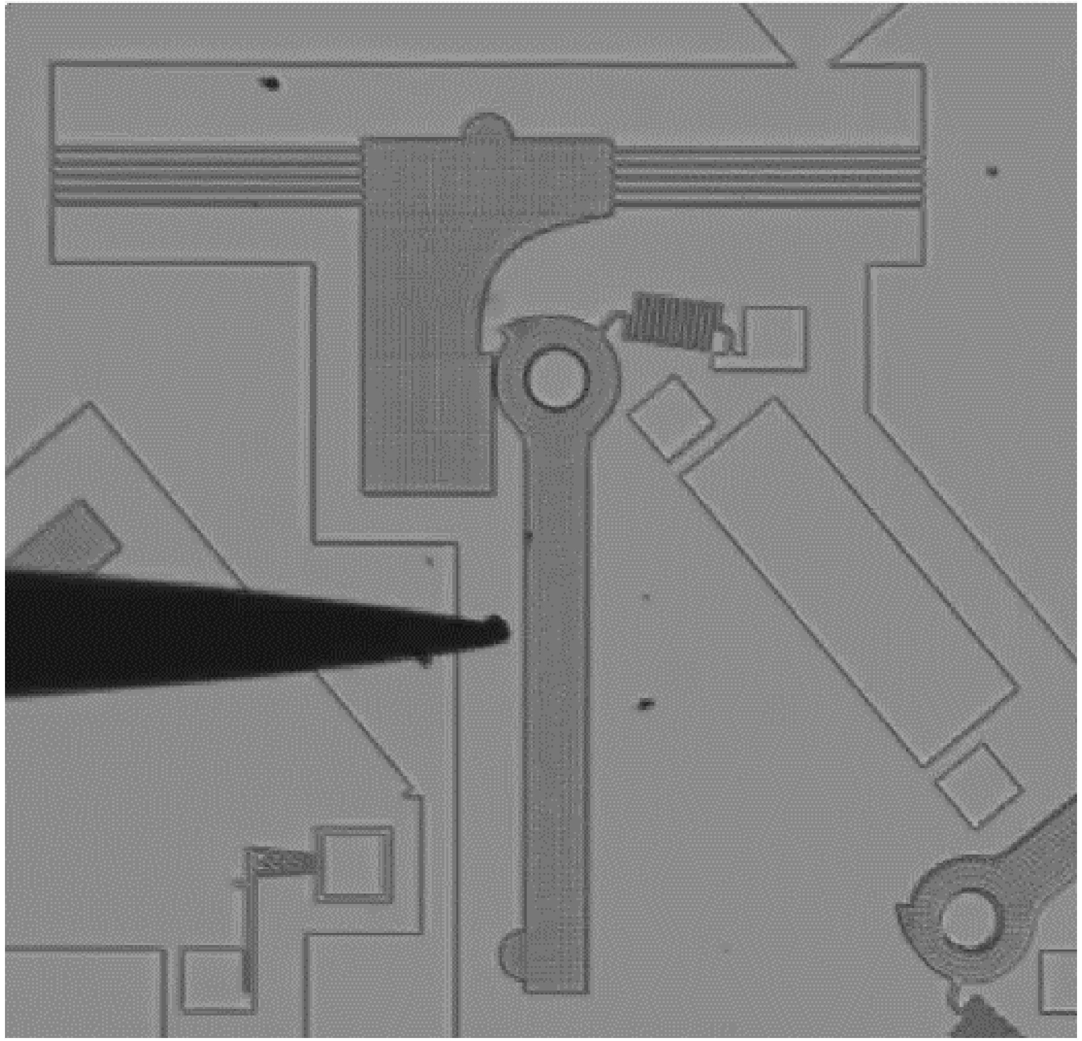

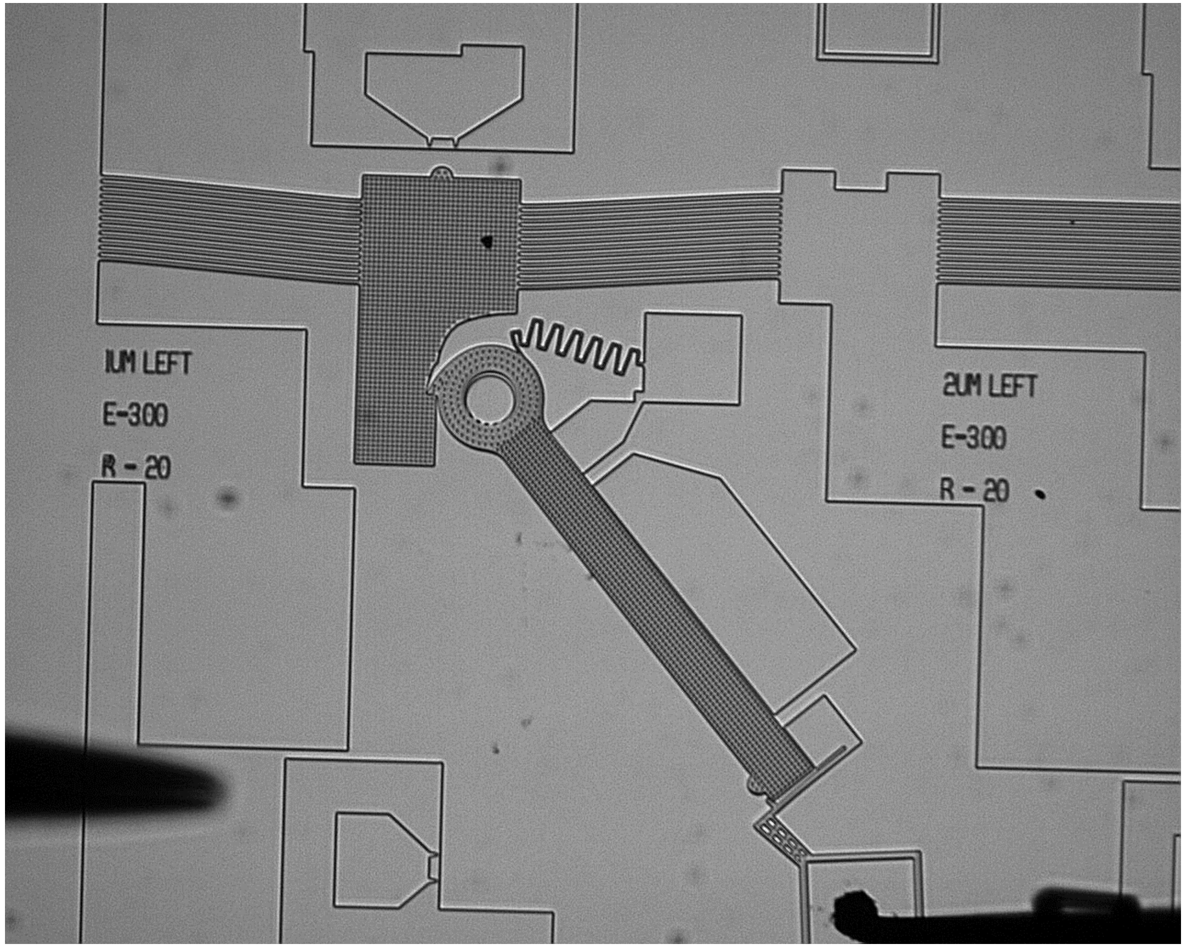

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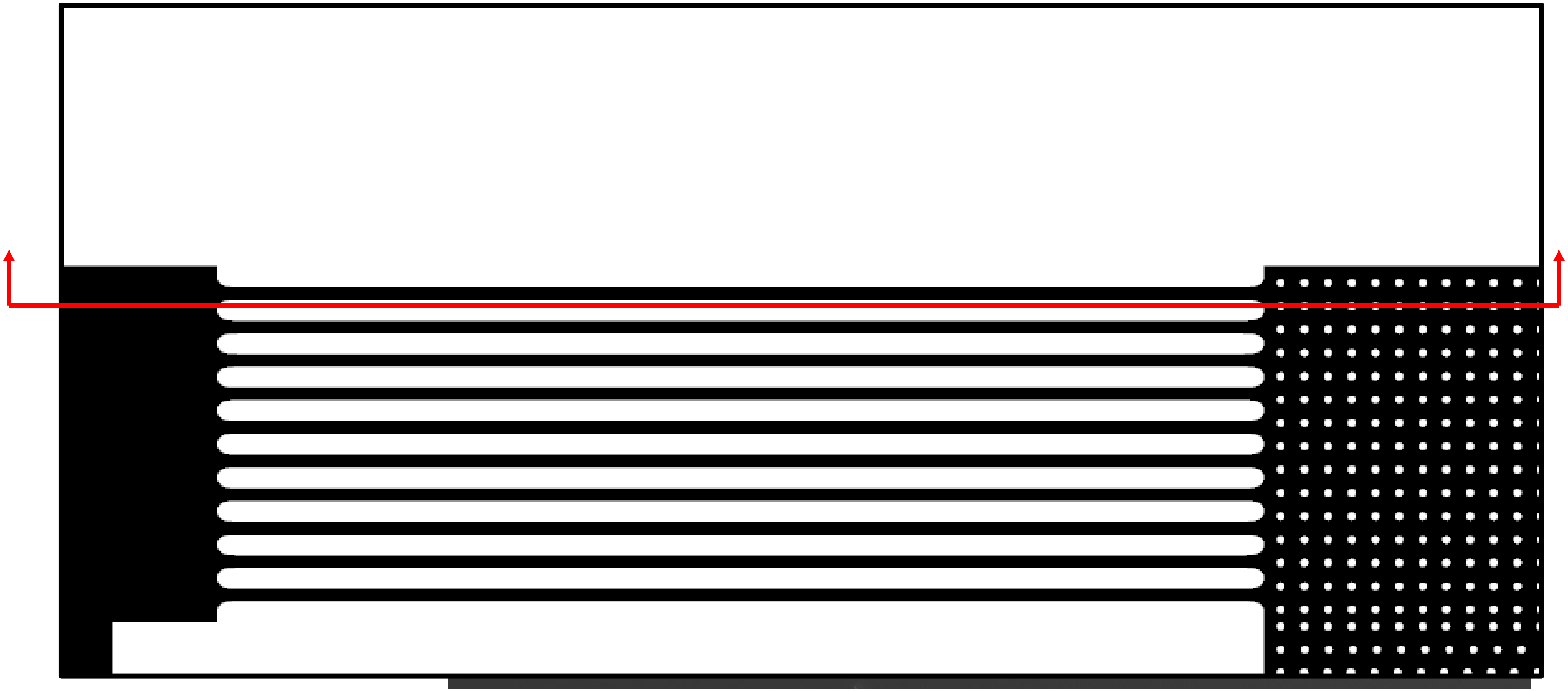

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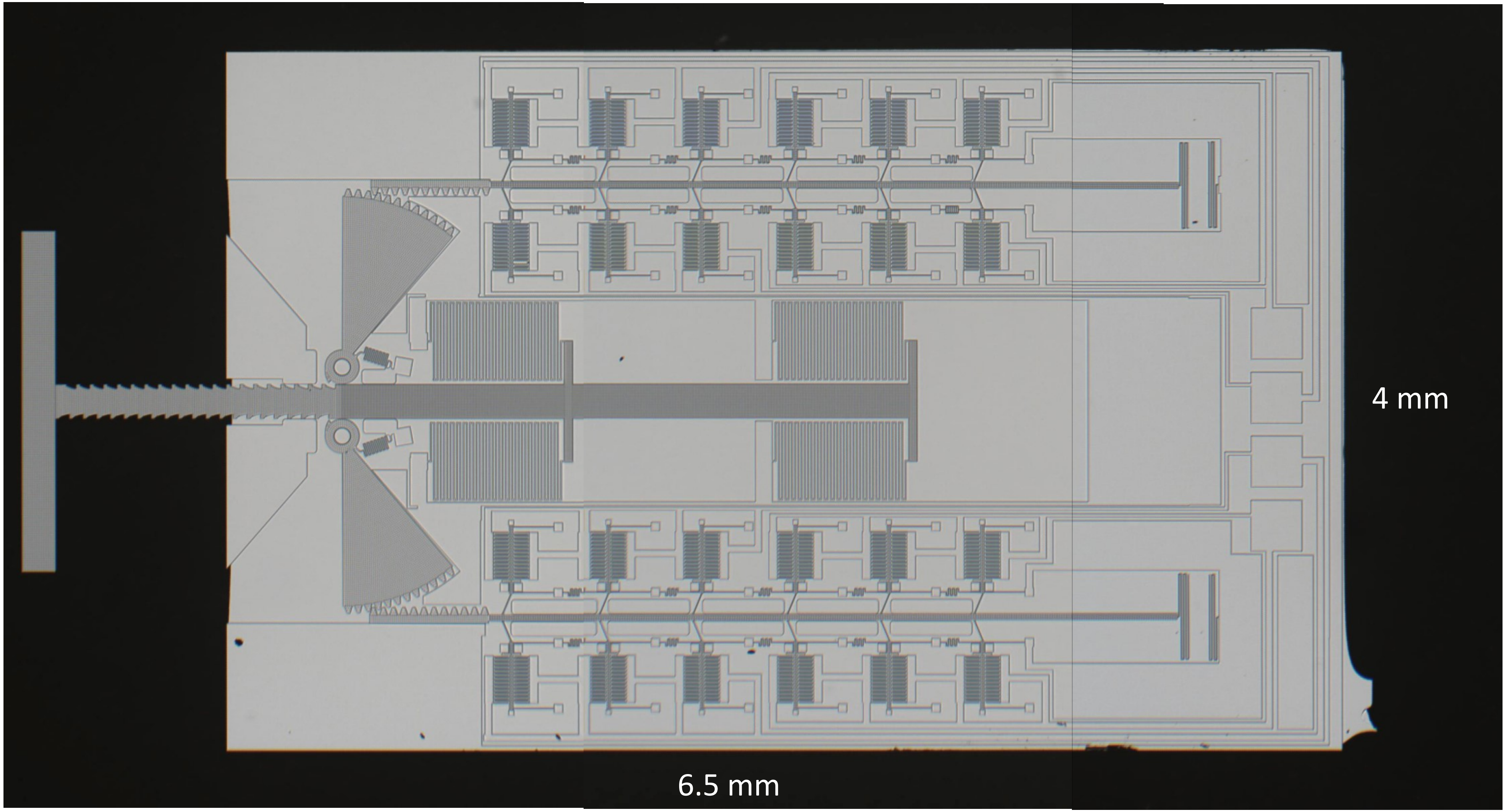
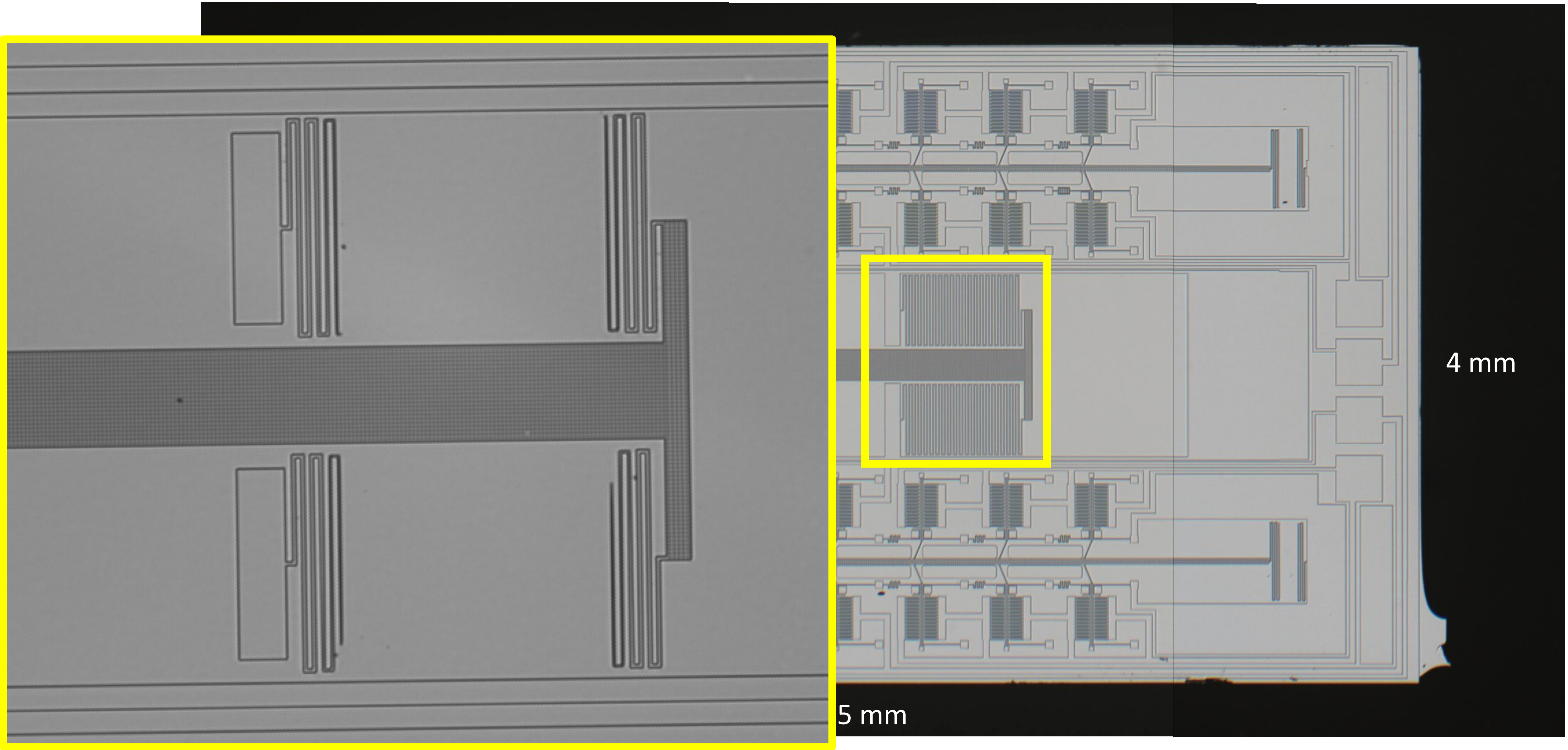
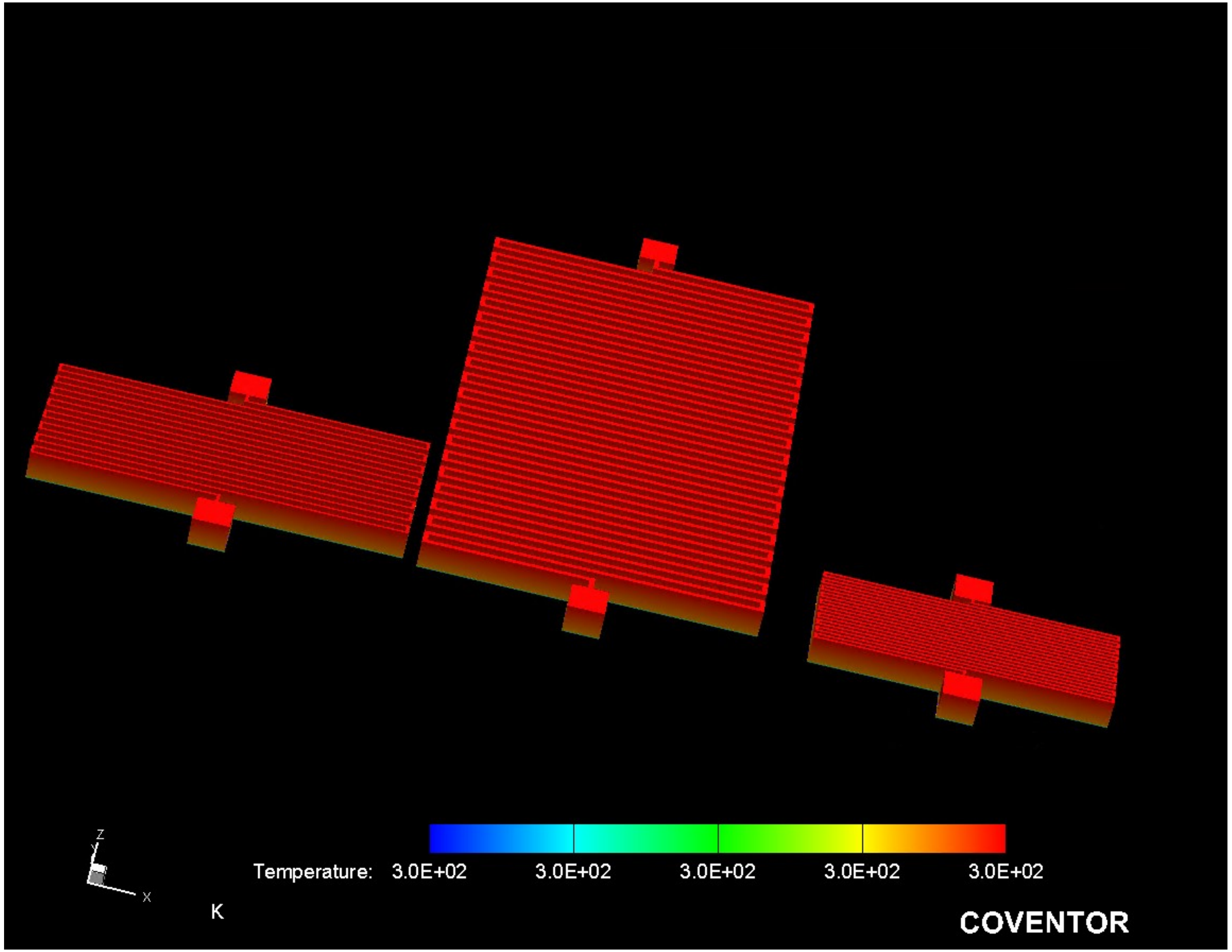
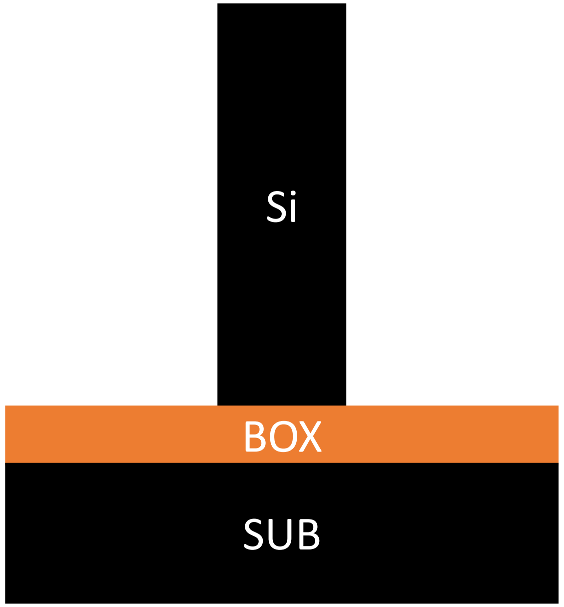


DRIE Nonidealities – Footing



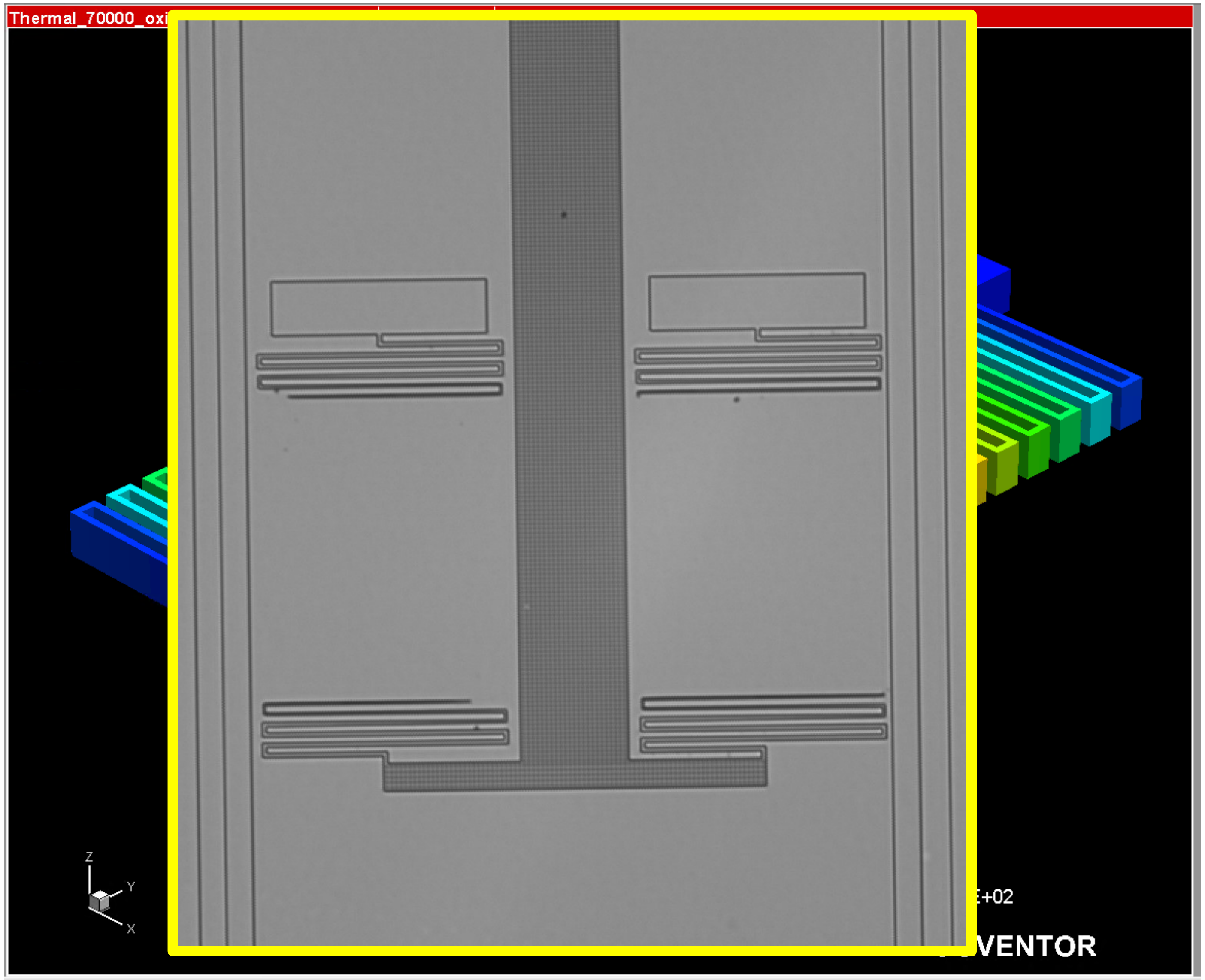
DRIE Nonidealities – Footing

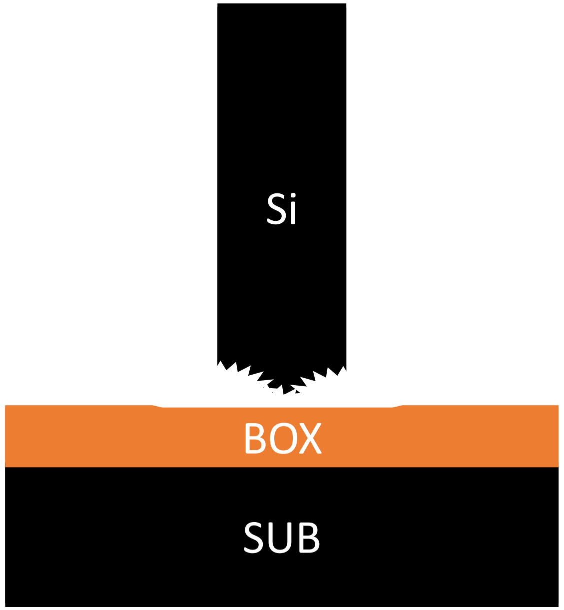




- Thermomechanical simulation
- Heat flux of 7 W/cm^2
- Beams heat up by 0.1 C

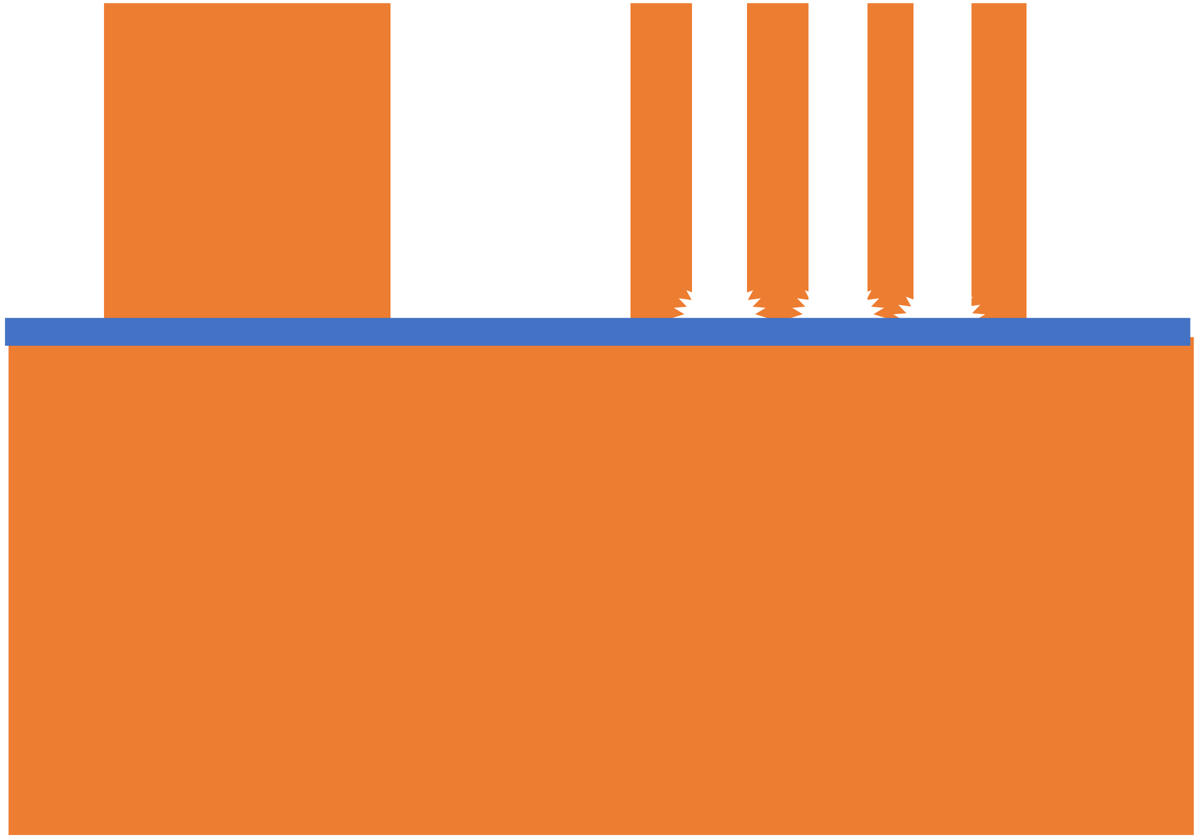
DRIE Nonidealities – Footing





- Thermomechanical simulation
- Springs fully footed
- Heat flux of 7 W/cm^2
- Beams heat up to 517 C

DRIE Nonidealities – Footing



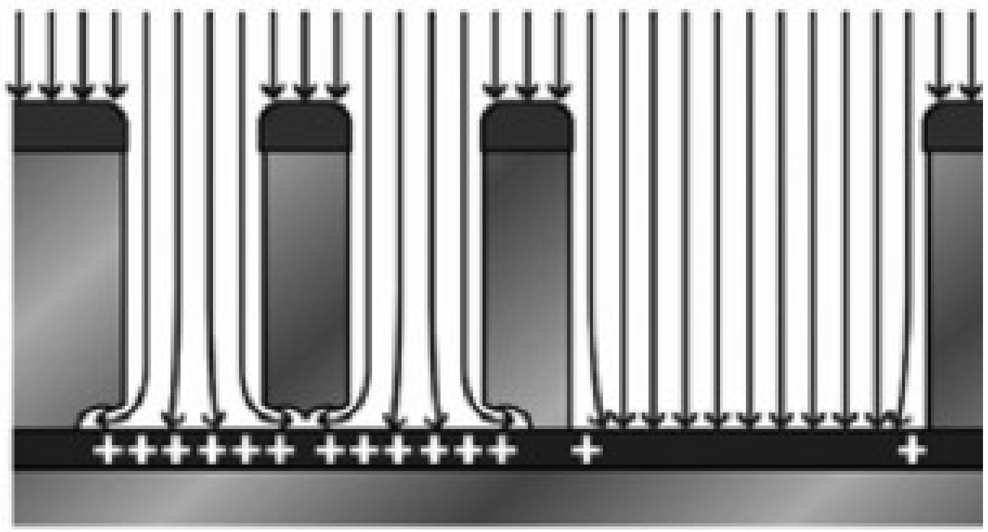
Footing/Notching

Lateral silicon etching at oxide interface

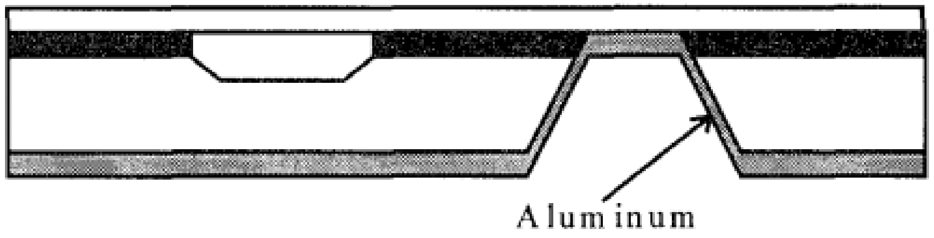
Fix

- Aluminum etch stop
- LF platen source
- LF platen duty cycle

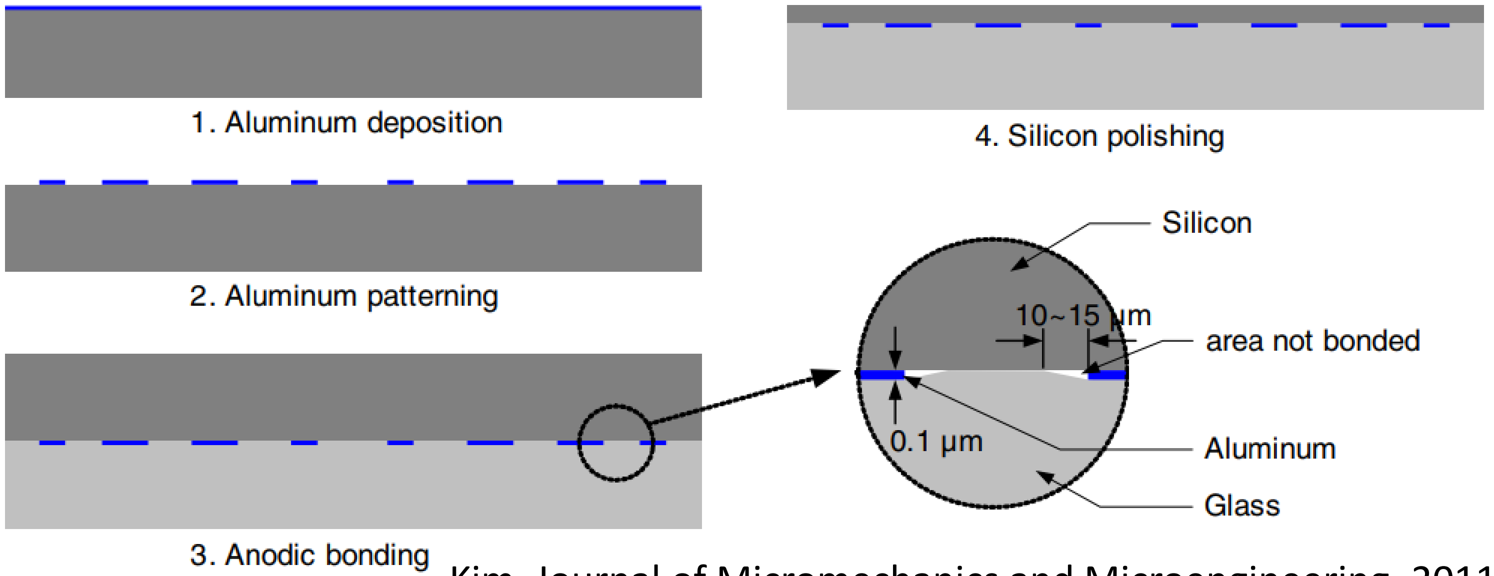
DRIE Nonidealities – Footing



Fix: Aluminum etch stop

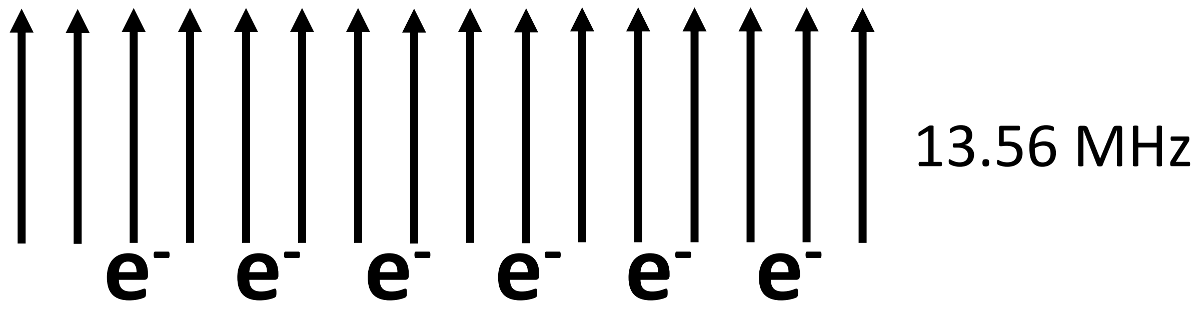


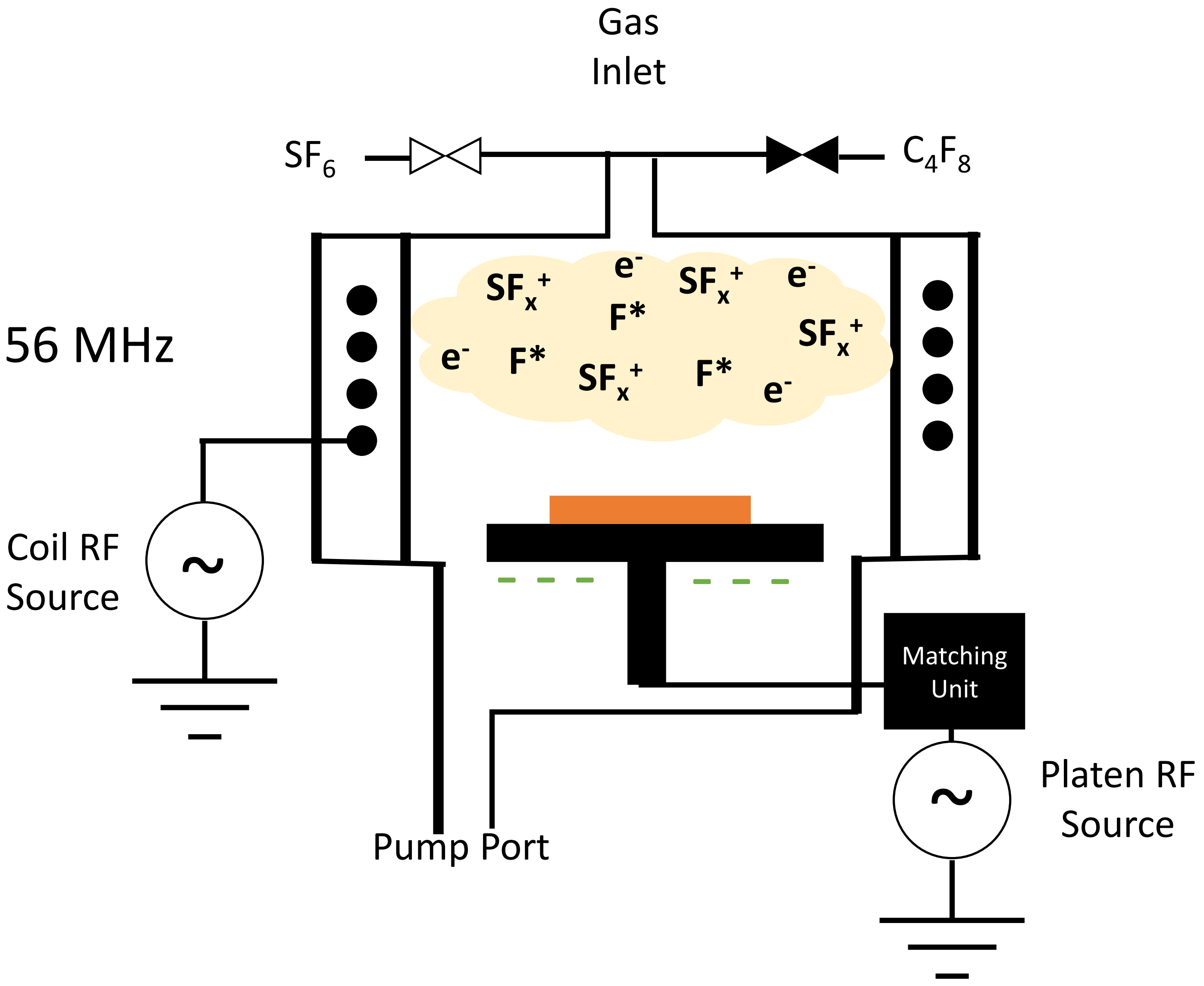
Noworolski, Solid-State Sensors and Actuators, 1995



Kim, Journal of Micromechanics and Microengineering, 2011

DRIE Nonidealities – Footing

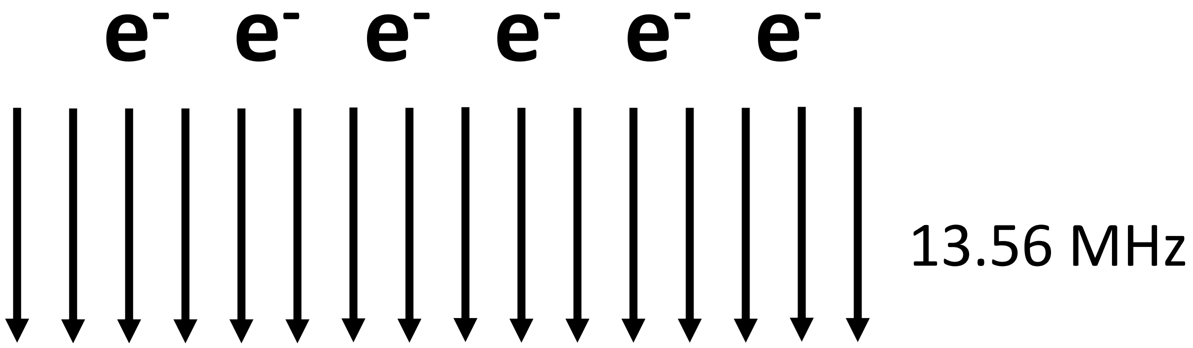


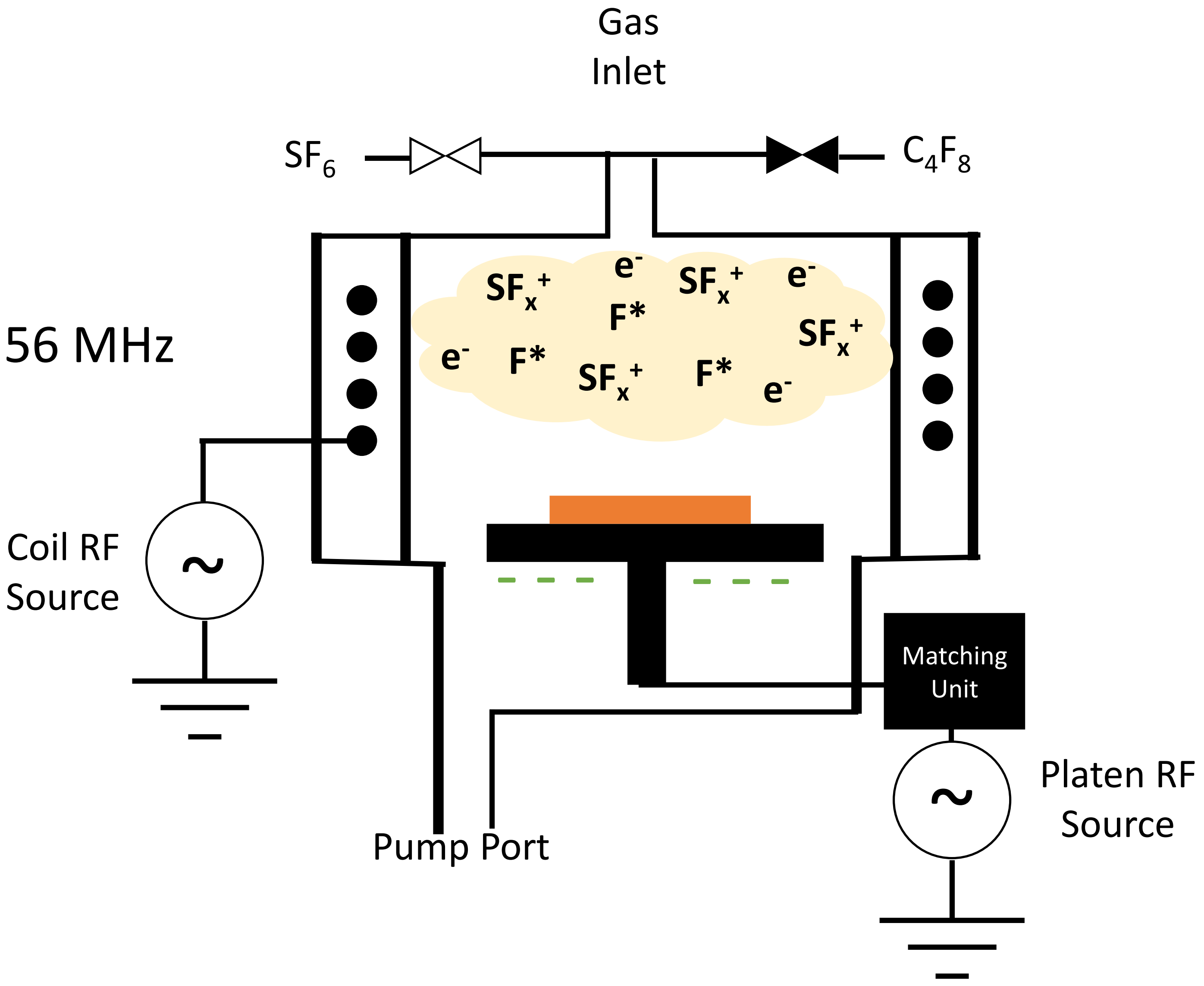


Fix:

- LF platen source
- LF platen duty cycle

DRIE Nonidealities – Footing

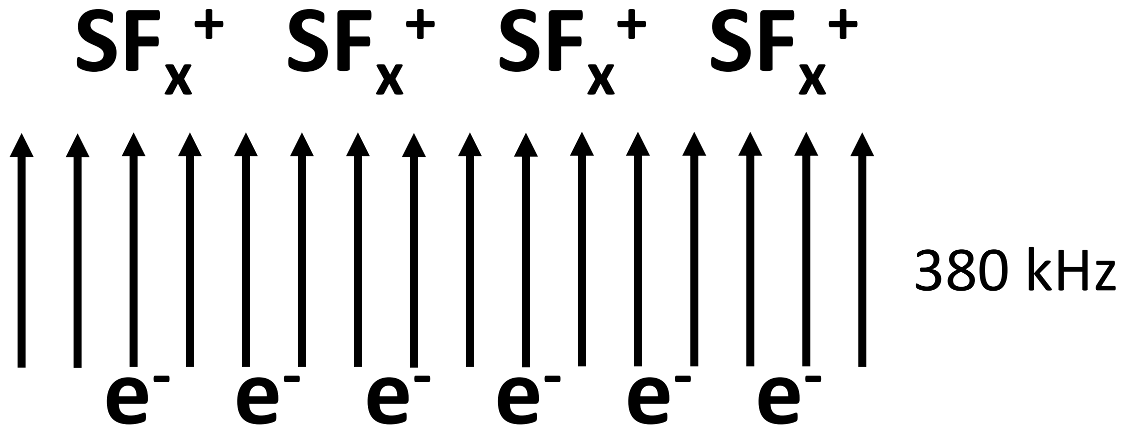


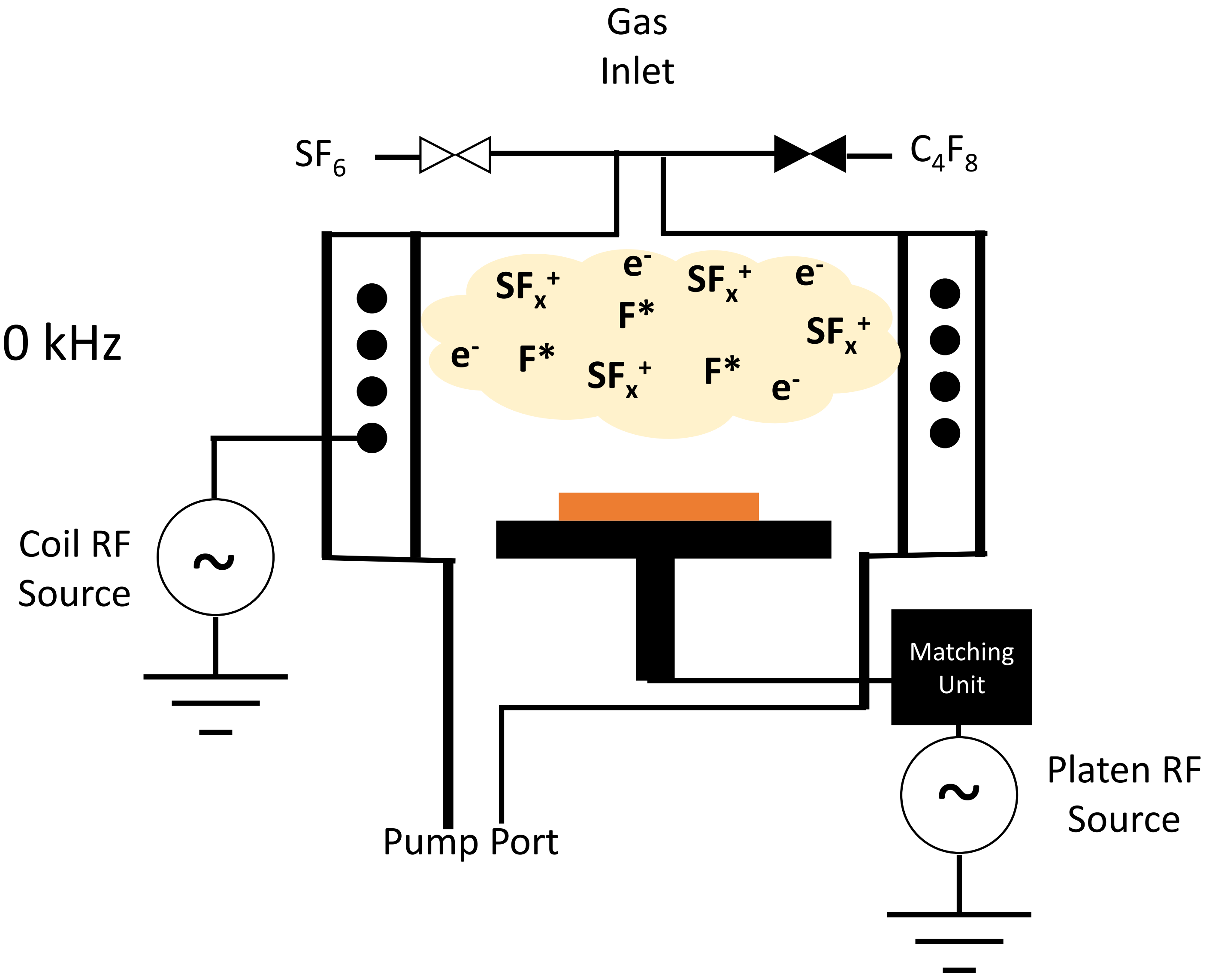


Fix

- LF platen source
- LF platen duty cycle

DRIE Nonidealities – Footing

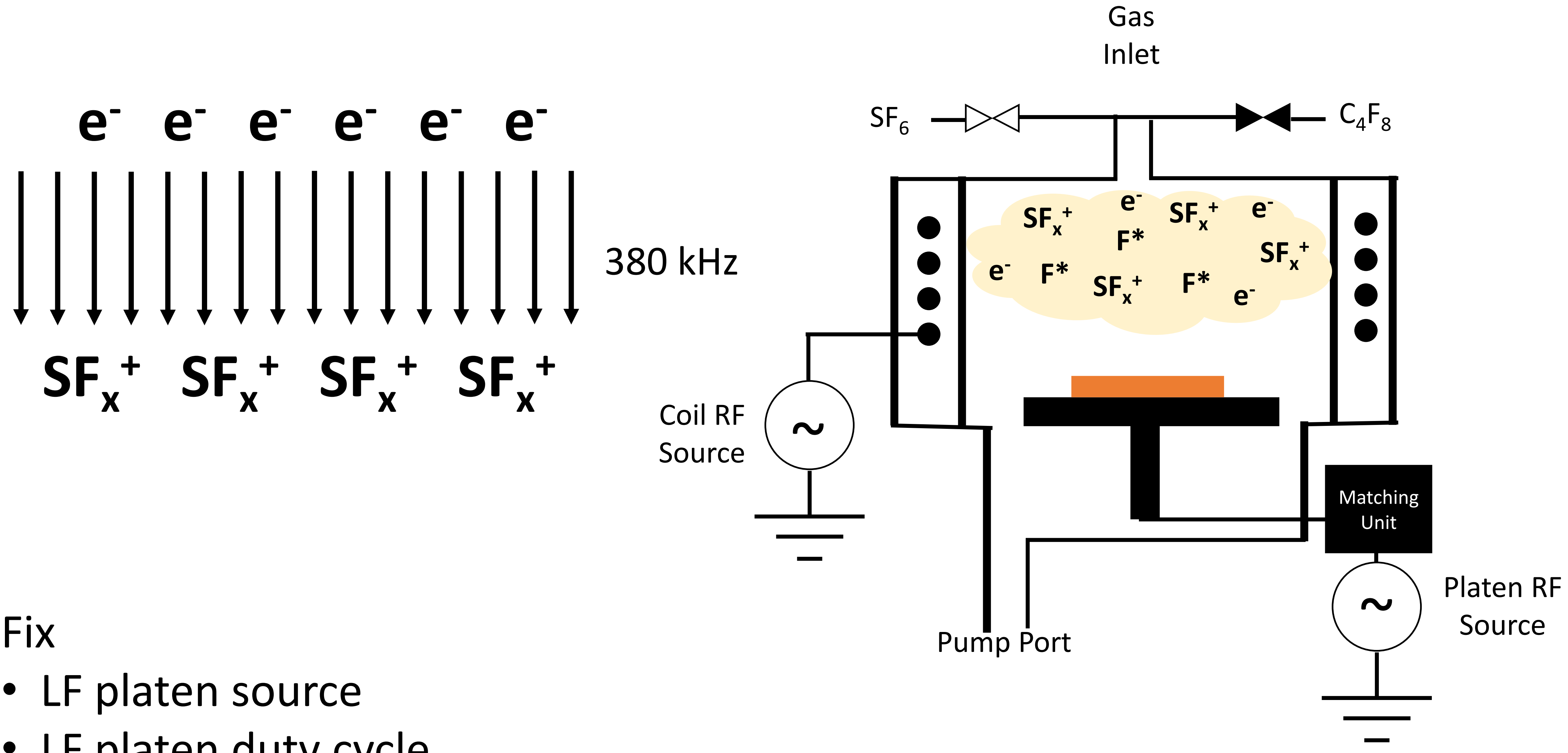




Fix

- LF platen source
- LF platen duty cycle

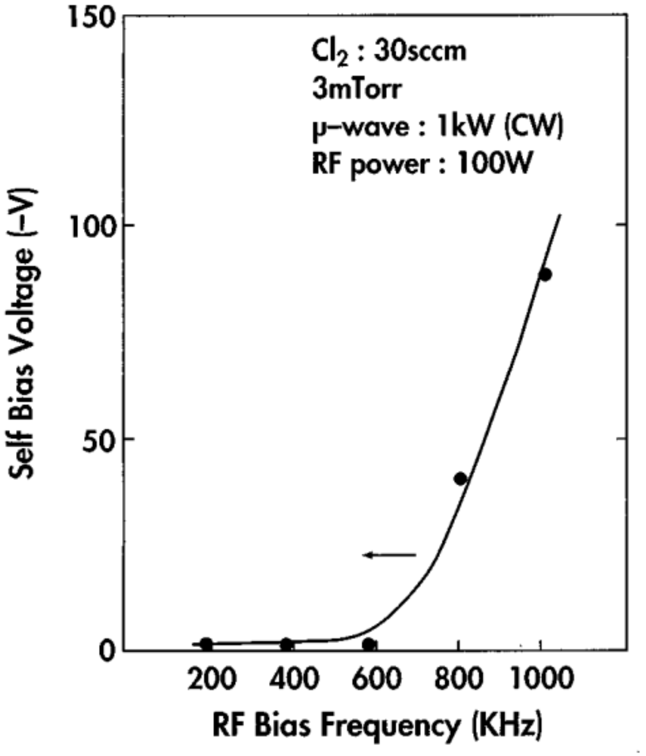
DRIE Nonidealities – Footing



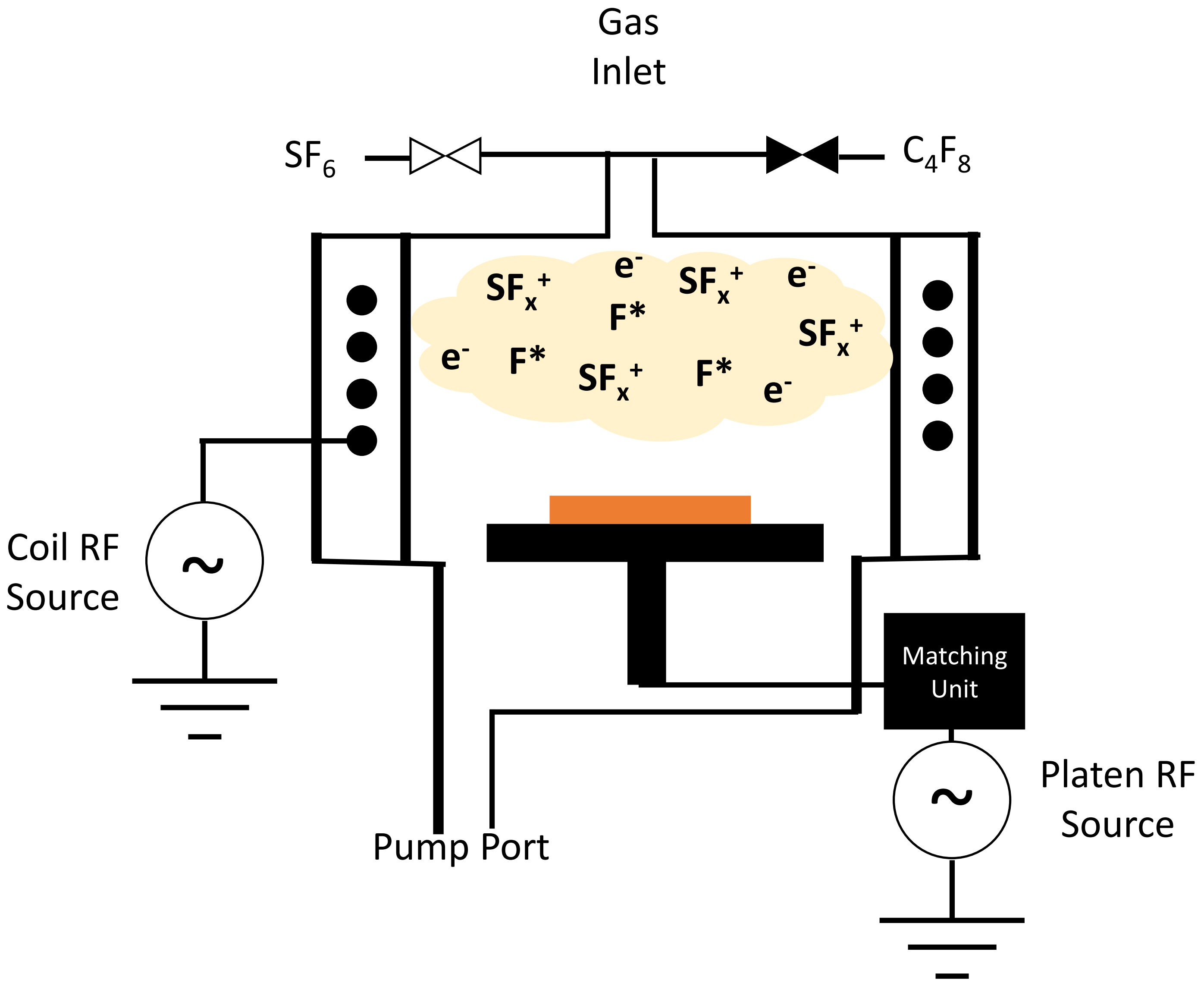
Fix

- LF platen source
- LF platen duty cycle

DRIE Nonidealities – Footing



Samukawa, Appl. Phys. Lett. 1996



Fix

- LF platen source
- LF platen duty cycle

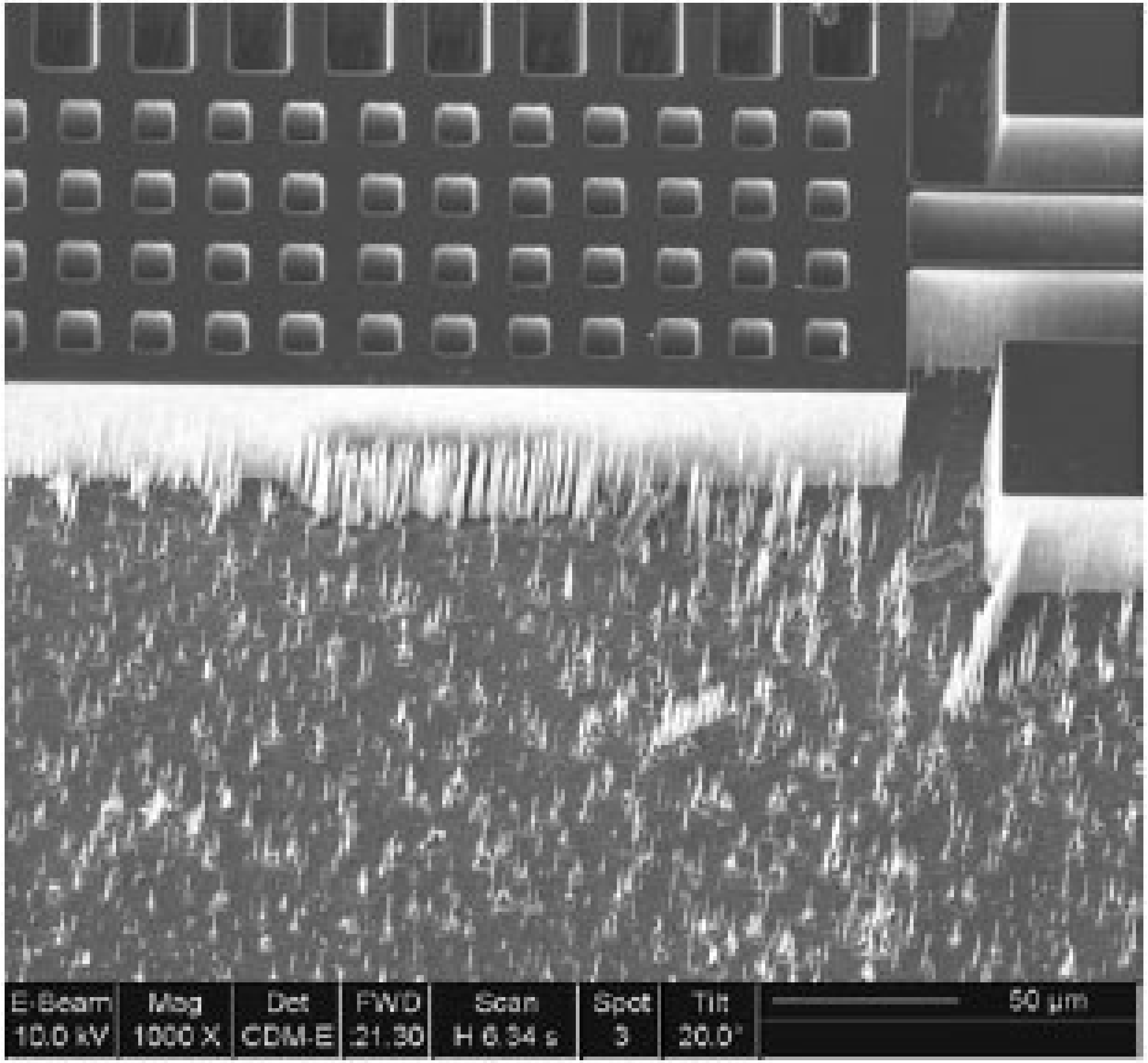
DRIE Nonidealities – Grass

Grass

Thin pillars of silicon created at bottoms of trenches

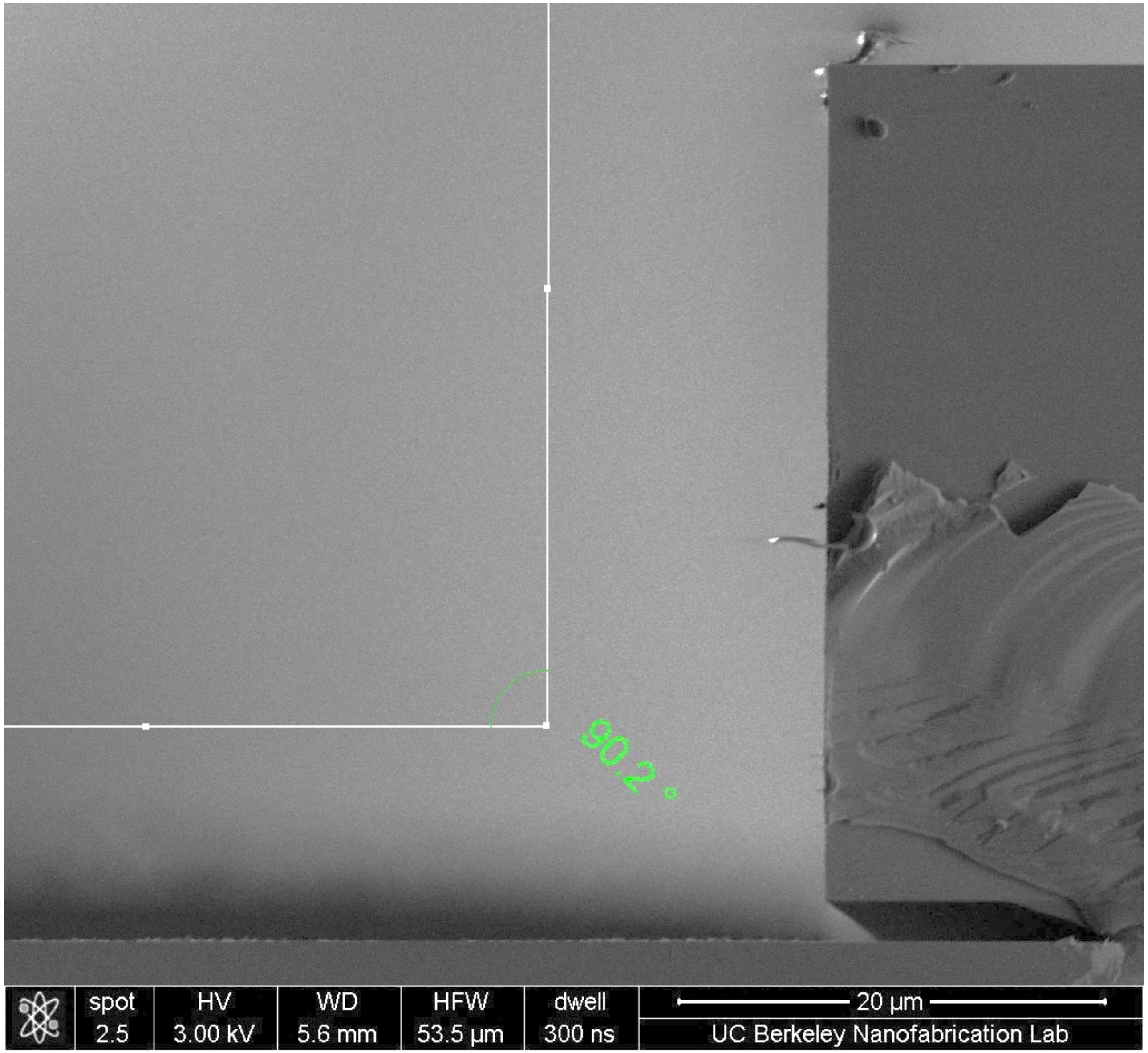
Fix

- Limit exposed area
- Recipe tune



Docker, J. Micromechanics and Microengineering, 2004

DRIE Nonidealities – Sidewall Angle



Sidewall Angle

Sidewalls are not always 90°

Fix

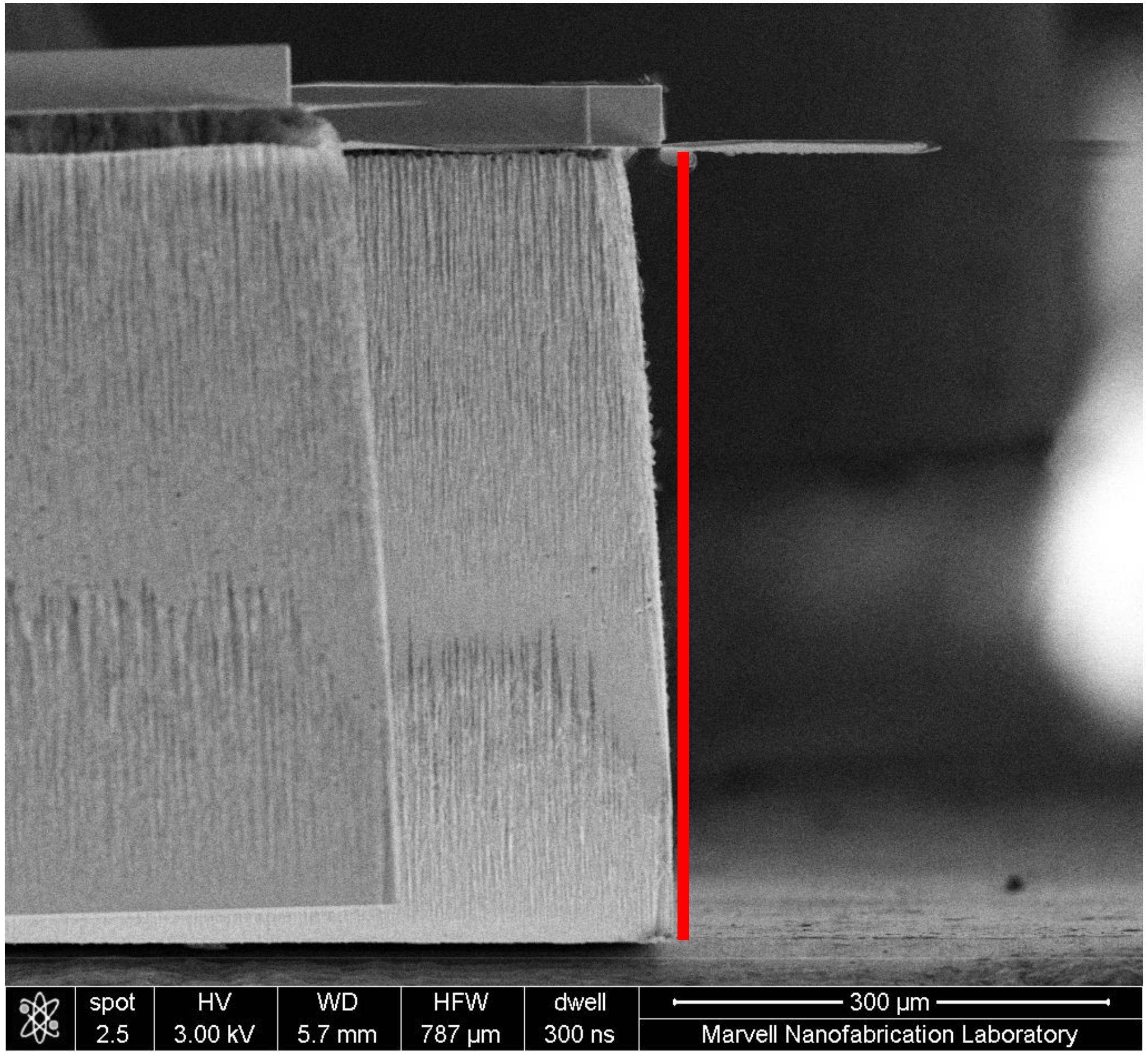
- Recipe tune

DRIE Nonidealities – Sidewall Angle

Sidewall Angle

Sidewalls are not always 90°

Fix
- Recipe tune



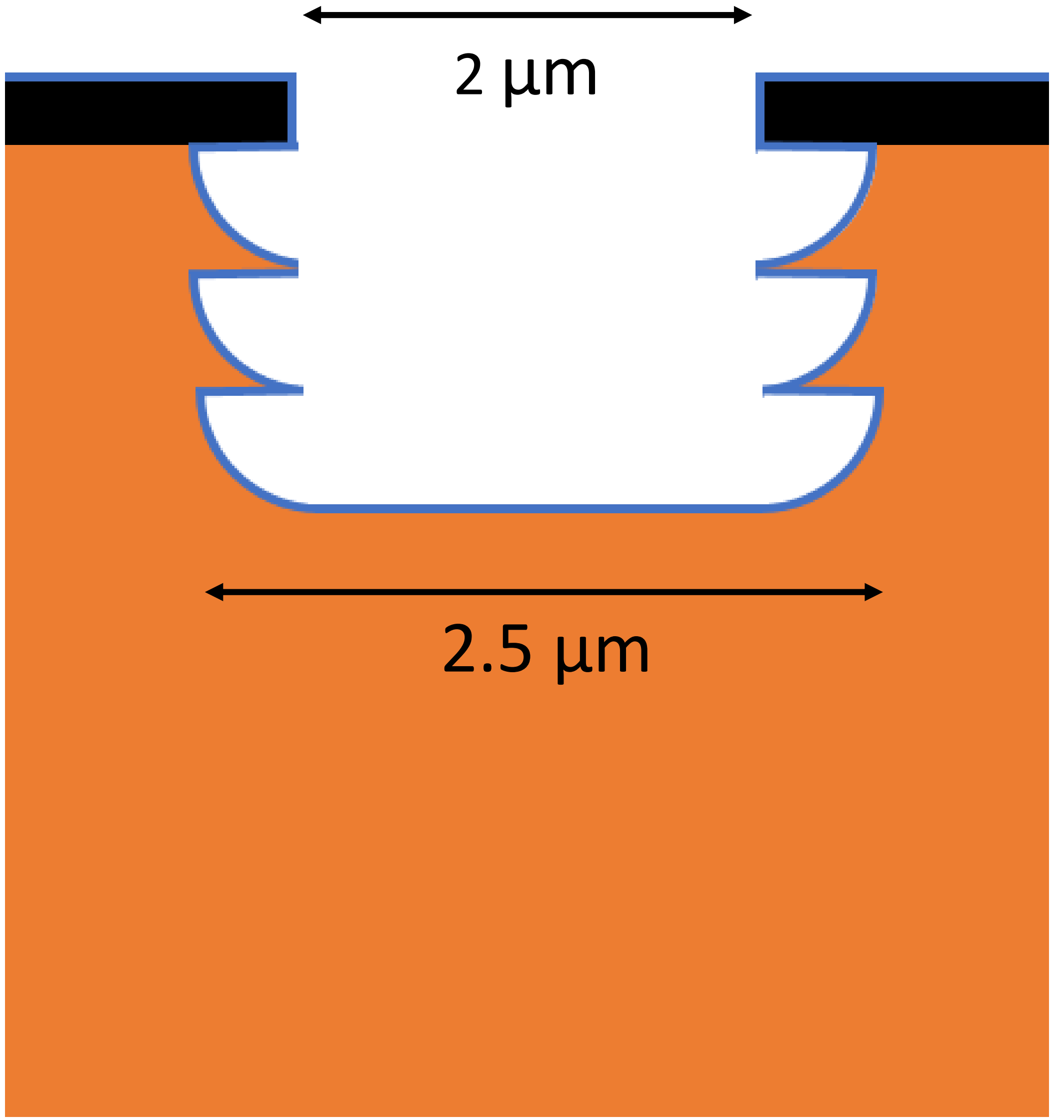
DRIE Nonidealities – Mask Undercut

Mask Undercut

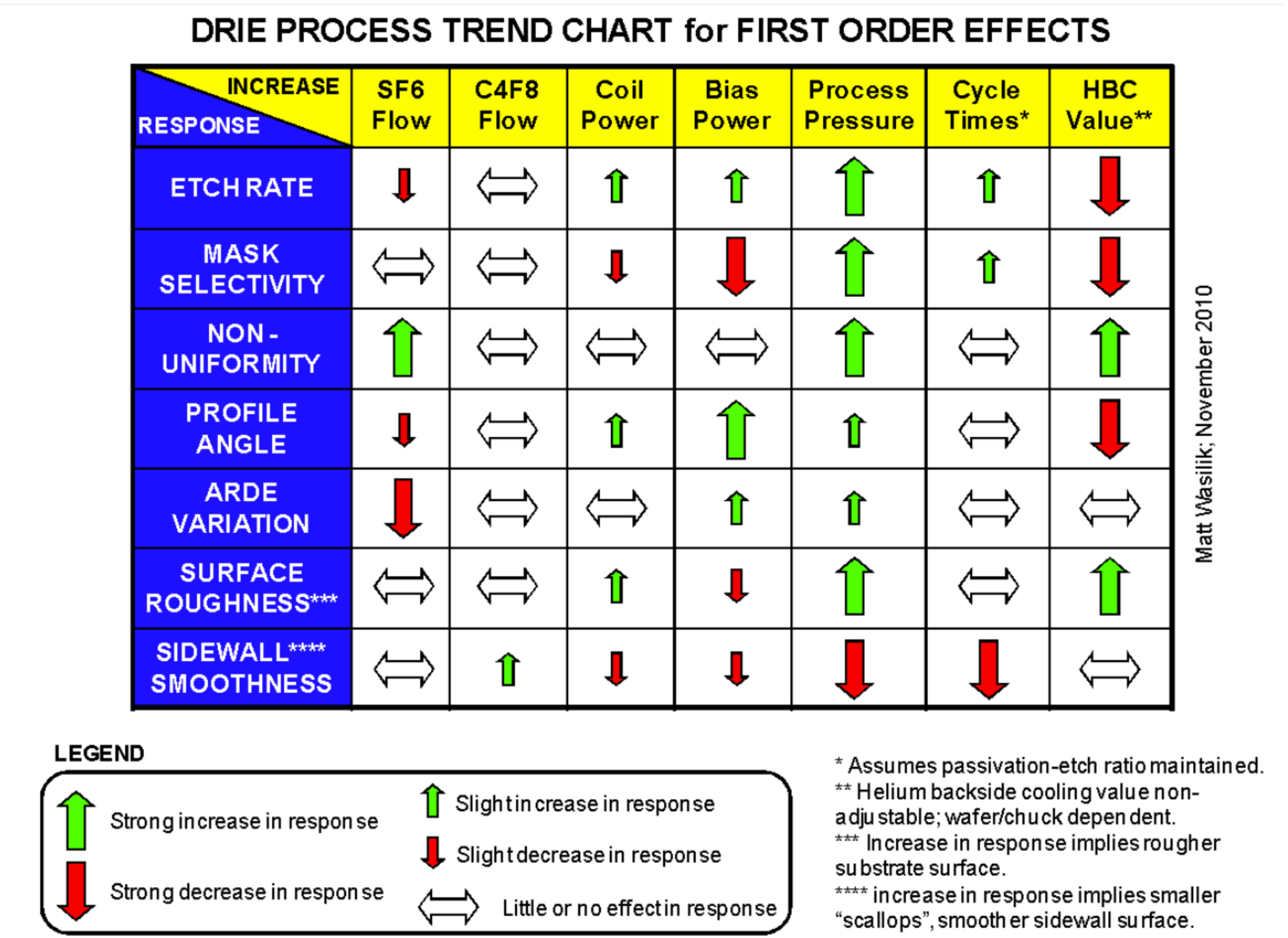
PR mask is naturally undercut by process

Fix

- Decrease etch time



Recipe Tuning



DRIE PROCESS TREND CHART for FIRST ORDER EFFECTS

INCREASE / RESPONSE	SF6 Flow	C4F8 Flow	Coil Power	Bias Power	Process Pressure	Cycle Times*	HBC Value**
ETCH RATE	↓	⇔	↑	↑	⬆	↑	⬇
MASK SELECTIVITY	⇔	⇔	↓	⬇	⬆	↑	⬇
NON-UNIFORMITY	⬆	⇔	⇔	⇔	⬆	⇔	⬆
PROFILE ANGLE	↓	⇔	↑	⬆	↑	⇔	⬇
ARDE VARIATION	⬇	⇔	⇔	↑	↑	⇔	⇔
SURFACE ROUGHNESS***	⇔	⇔	↑	↓	⬆	⇔	⬆
SIDEWALL**** SMOOTHNESS	⇔	↑	↓	↓	⬇	⬇	⇔

Matt Wasilik; November 2010

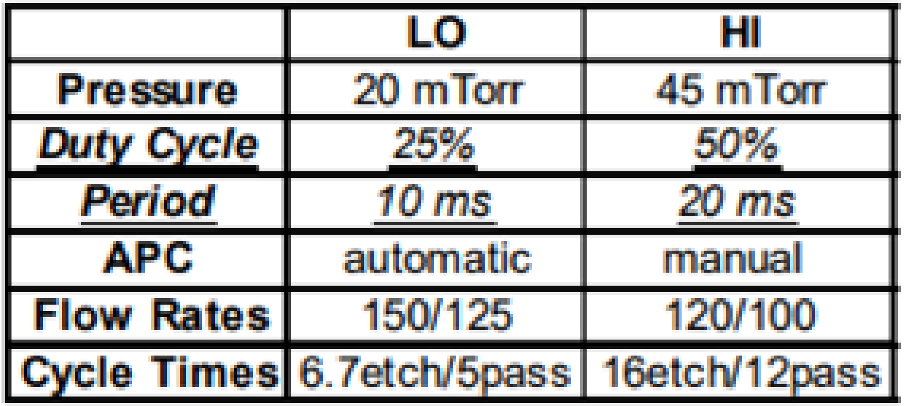
LEGEND

- ⬆ Strong increase in response
- ⬇ Strong decrease in response
- ↑ Slight increase in response
- ↓ Slight decrease in response
- ⇔ Little or no effect in response

* Assumes passivation-etch ratio maintained.
** Helium backside cooling value non-adjustable; wafer/chuck dependent.
*** Increase in response implies rougher substrate surface.
**** increase in response implies smaller "scallops", smoother sidewall surface.

Recipe Tuning – Design of Experiments

Factors



	LO	HI
Pressure	20 mTorr	45 mTorr
Duty Cycle	*25%*	*50%*
Period	*10 ms*	*20 ms*
APC	automatic	manual
Flow Rates	150/125	120/100
Cycle Times	6.7etch/5pass	16etch/12pass

TABLE 1

Response

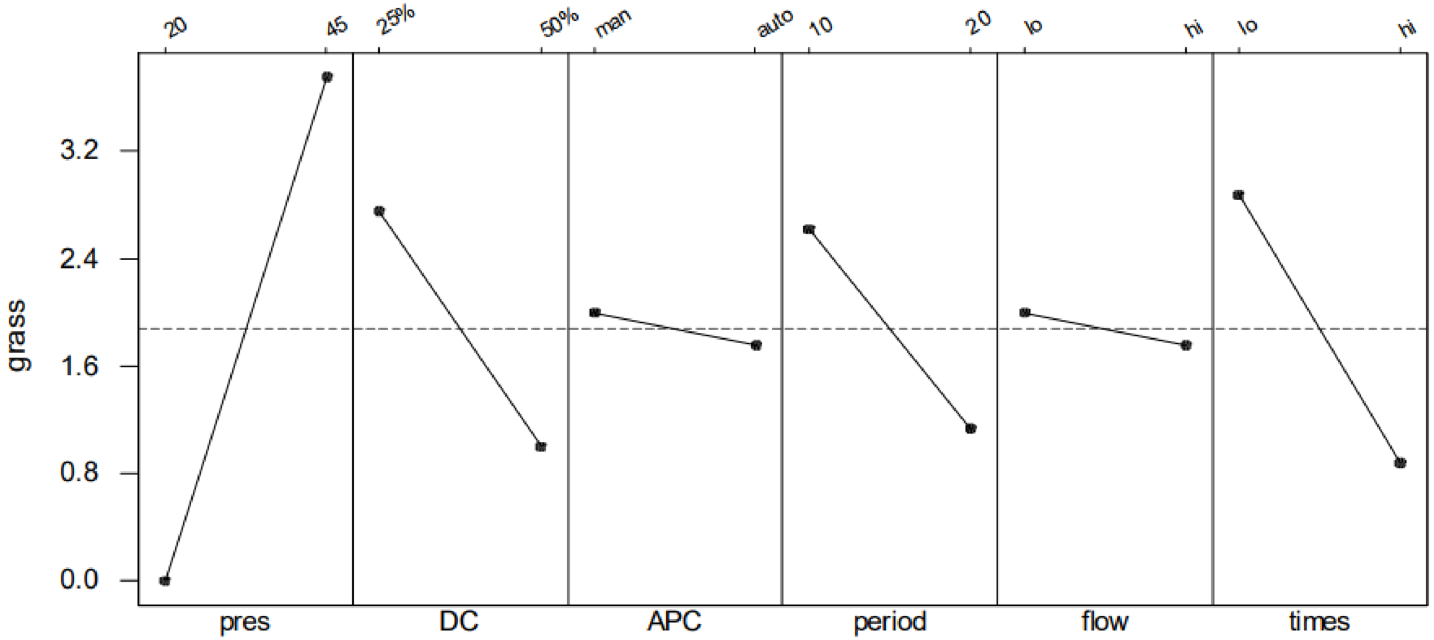
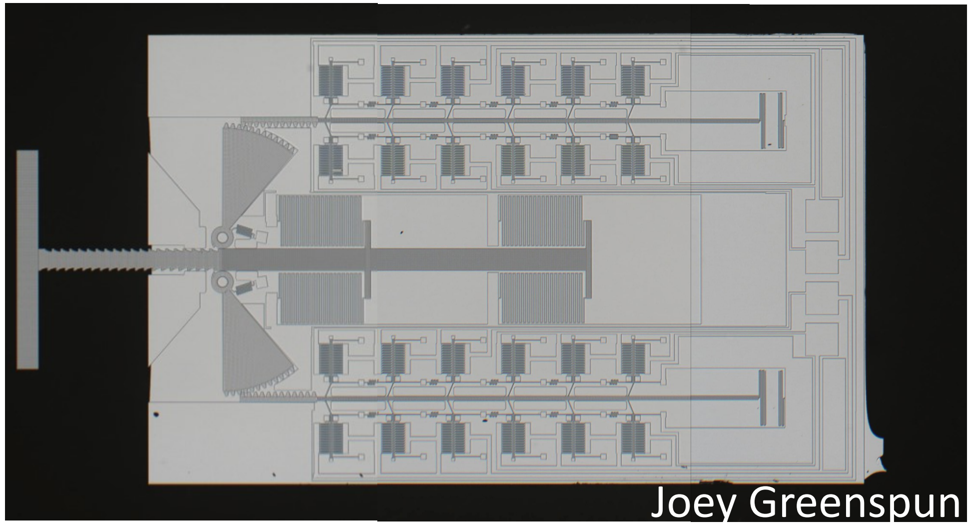


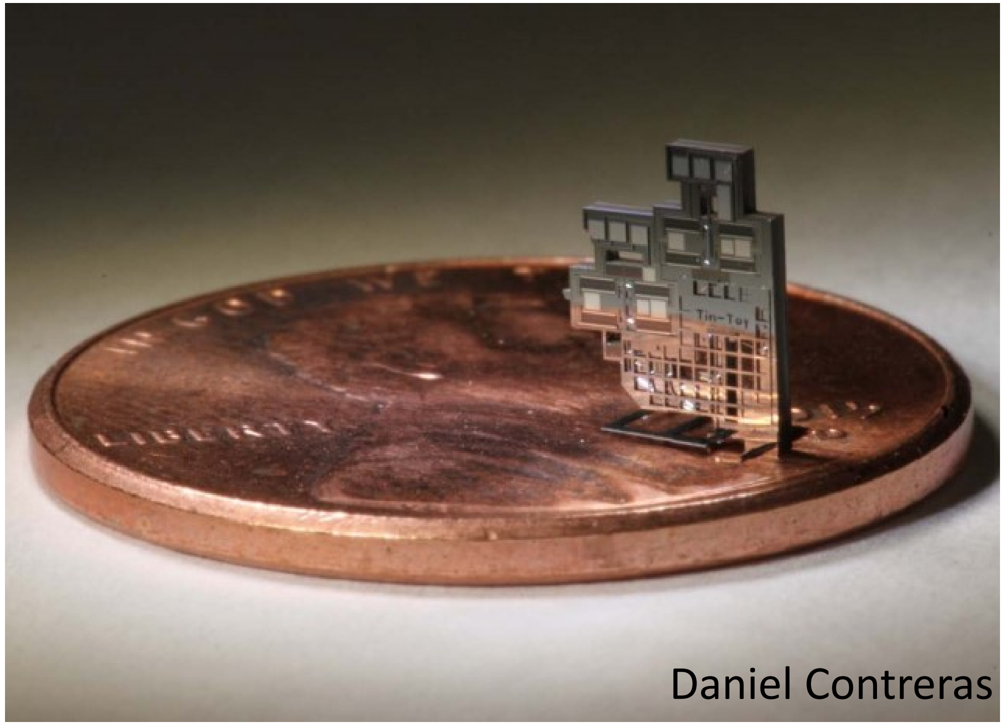
FIGURE 8
main effects plot for grass, (1-10)

Wasilik, 2001

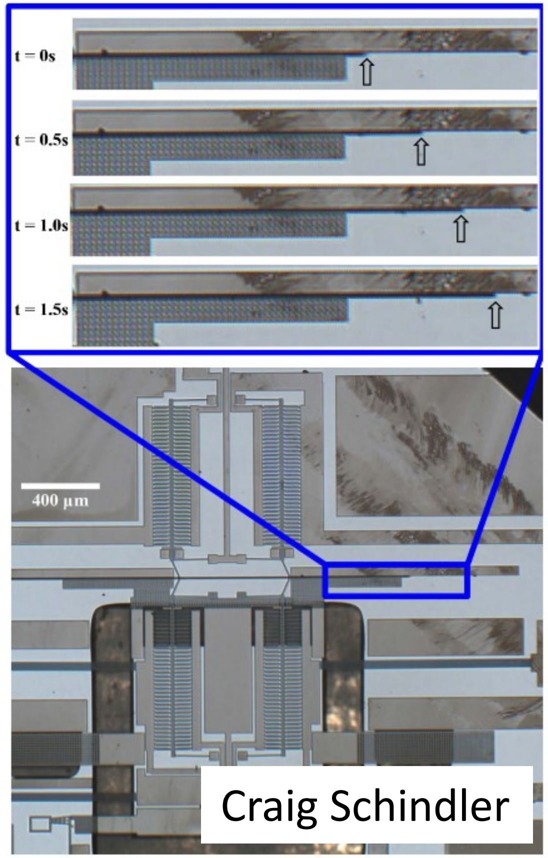
The Pister Group



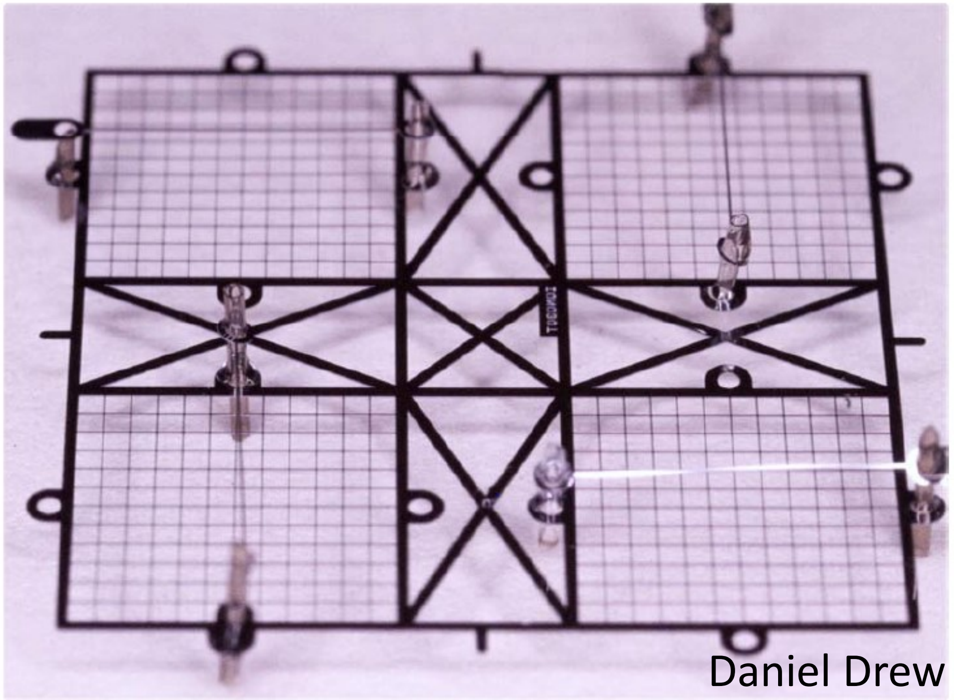
Joey Greenspun



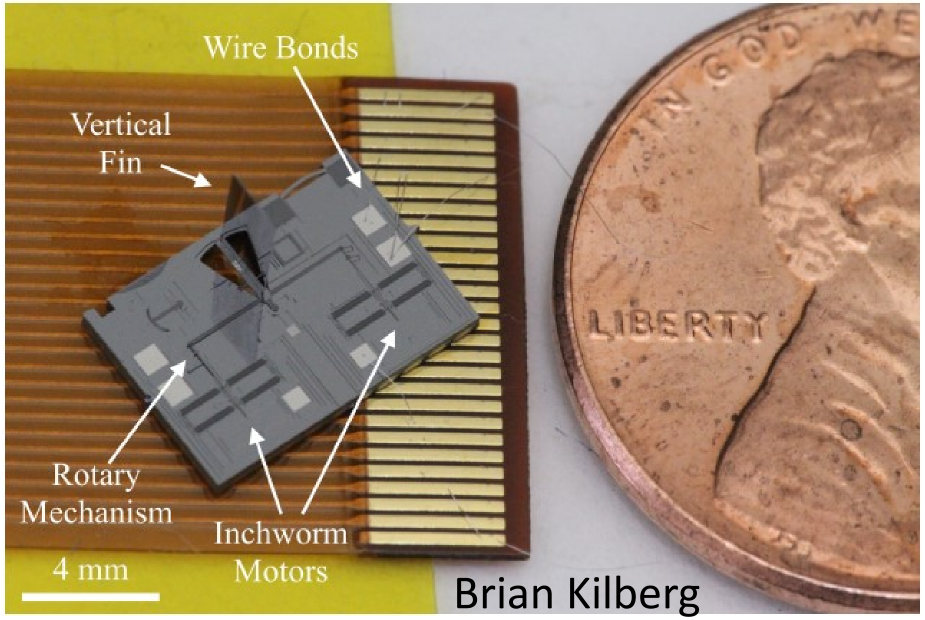
Daniel Contreras



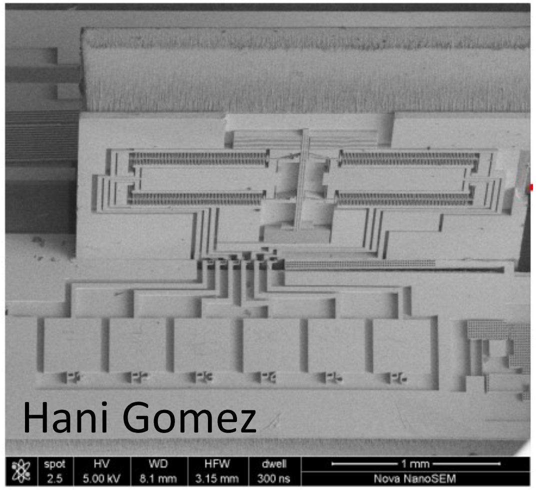
Craig Schindler



Daniel Drew



Brian Kilberg



Hani Gomez