1. 1 pt. for each part (3pts. total). For part c, an approximate answer is fine. The point is to understand that a standard MEMS run is a lot more expensive than a standard CMOS run.
   a. 5 runs per year, 2 months
   b. $4200
   c. Buying 1 standard die site with 45 die delivered at $8800 along with 4 additional die sites (15 die delivered at $3000 each) comes out to $20800 for 105 11x11mm² die. The cost per square mm will be about $1.64. CMOS is way cheaper ($0.05 per square mm)!

2. 1 pt. for each part (6 pts. total)
   a. PADMETAL must be enclosed on all sides by 3µm of SOI. The minimum feature size for PADMETAL is 3µm. This makes the pad 9µmx9µm
   b. 50µm
   c. The oxide undercut is about 1.8-2µm. A 3.6µm beam will be released. Note that the design rules state that any beam under 6µm may be released. Either of these answers is fine.
   d. On a Cartesian grid of etch holes, assume the critical diagonal undercut will be 1.8µm. The holes should be spaced \(\frac{1.8}{\sqrt{2}}\)µm = 1.27µm apart along x and y (Note that this is below the minimum feature size of any SOI feature, 2µm. If we assume that any feature under 6µm will be released by the undercut, than spacing the holes from 2µm to 4.3µm may release the plate)
   e. 33%
   f. Fillets reduce stress concentrations. Fillets are recommended to protect frontside structures during processing of the backside trench etch

3. 1 pt. for an uploaded GDSII file

4. 1 pt. for the correct structural material/sacrificial material/etchant for each reference (3pts. total for each paper, 12 pts. for the whole problem)
   Fedder, Integrated MEMS in Conventional CMOS
   Structure: metal+dielectrics;
   Sacrificial materials: dielectrics between structures, and silicon beneath structures;
   Etchants: RIE for dielectrics, fluorine plasma for silicon

   Wang et al. “A novel CMOS out-of-plane accelerometer...”
   Structure: metal+dielectrics;
   Sacrificial materials: metal between structures, dielectrics between structures, silicon beneath structures;
   Etchants: metal wet etch (H₂SO₄+H₂O₂, known as piranha), RIE for dielectrics, XeF₂ for substrate (see figures 3 and 4).

   Lin et al., “Fabrication of a Micromachined Capacitive Switch...”
Structure: aluminum
Sacrificial material: SiO2
Etchants: buffered oxide etch (HF)

Jain et al. “A single-crystal silicon micromirror...”
Structure: metal+dielectrics+silicon
Sacrificial material: dielectrics between structures, silicon between
and beneath structures
Etchants: RIE for dielectrics, RIE or DRIE for silicon

5. [ee247a] 5 pts. Yes, dammit, you could. Get to work!