1. In Figure 2 of this Analog Devices discussion on voltage regulators
   a. Assuming that SENSE is connected to VOUT, what voltage is the regulator regulating to?
   b. How would you change the circuit to regulate to a voltage less than the reference voltage? (sketch
      the circuit showing the op-amp, pass transistor, reference, and any resistors necessary)
   c. Why does the SENSE value connect to the positive input of the op-amp? Is this positive
      feedback?

2. For the circuit in figure 13.43 in Razavi (6.9 in GHLM)
   a. what ratios of C2 to C1 are needed to make a variable gain amplifier with gain equal to either 1
      and 8?
   b. Calculate the feedback factor f (be careful – f is not the reciprocal of gain) and the gain error for
      both cases above (you may assume that Cp=0)
   c. if the desired closed-loop gain accuracy is 0.4% regardless of gain setting, what is the minimum
      open-loop gain necessary for the op-amp?
   d. if the amplifier must settle to within 0.4% of the correct value within 10us, what is the minimum
      unity gain bandwidth of the op-amp?

3. In the TI document on SAR ADCs,
   a. does the comparator compare at ground or the top rail?
   b. With an input of 1V, in HOLD mode, what is the voltage on the minus input of the comparator?
   c. If the p-type body of the NMOS switch “SA” is grounded, what is likely to happen to the voltage
      on V- during the HOLD mode?

4. In a particular process, long channel (1um) devices can be very roughly modeled as quadra
   a. Carefully sketch I0 vs Vd of the transistor with Vgs=0.2V.
   b. What is the “on resistance” Ron of the MOSFET?
   c. Assuming that the gate voltage of the NMOS devices rises from 0 to 0.8V at t=0,
      i. carefully sketch the capacitor voltage vs. time, clearly showing the shape for when
         Vc>0.2V, and the time that it takes to reach 0.2V.
      ii. What is an upper bound on the time that it takes for Vc to fall from 0.2V to 1% of that
         value, 2mV (hint: think 2Ron)
      iii. The sum of these times is roughly the time required to settle to 0.4% accuracy when
         starting with a large voltage. What is that sum?

5. A PMOS-input folded cascode is biased with all devices at Vos=0.2V in unity gain feedback with the
   positive input at 0.5V. Itail = I02. At t=0, the positive input is driven from 0.5V to ground.
   a. Sketch the circuit with only the transistors which will be on just after t=0 as the amplifier slews
   b. With only a capacitive load, what is the initial rate of change of the output voltage (in terms of
      op-amp current bias values, e.g. Itail, I02, etc.)? What is the first device to drop out of saturation?
      Estimate the output voltage after the amplifier has settled.

6. You add a PMOS-input common source amplifier as a second stage to the output of the amplifier in the
   previous problem (and stabilize with a Miller capacitor!). With only a capacitive load, estimate the output
   voltage after the amplifier has settled, and the time to get within 0.1% of that value. (Hint: problem 4?)

7. An NMOS transistor is used as the φ1 switch shorting out Cg in a PGA amplifier circuit similar to your
   project. Cf=10fF, and the NMOS device has a Vtn=0.6V, and Cgd=0.5fF.
   a. As φ1 falls, what is the charge on Cgd just as the channel disappears (the switch opens, the device
      turns off, Vgs=Vtn)?
   b. After φ1 goes to 0, all of that charge ends up on V-, and cannot leave that node. During φ2, where
      does it go (which capacitor, which side)?
   c. Assuming that Vin=0 during φ1, what is the output voltage due to this charge injection?
8. To model the negative voltage spike on \( V^- \) in the PGA, assume that the op-amp is very slow and its output stays at ground while an ideal \( \phi_2 \) switch closes. Assume that \( C=100 \text{fF} \) now.
   a. If \( V_{in}=1 \text{V} \), and gain=1, what is the voltage on \( V^- \) just after \( \phi_2 \) goes high?
   b. If \( V_{in}=1/8 \text{V} \), and gain=8, what is the voltage on \( V^- \) just after \( \phi_2 \) goes high?
   c. If \( V^- = -0.5 \text{V} \), draw a cross section of the \( \phi_1 \) switch, label the voltages just after \( \phi_2 \) goes high, and show which diode is forward biased. When current flows in that diode, does the output voltage end up higher or lower than it should be (after settling)?
   d. Now assume that the \( \phi_2 \) switch has a series resistance of 10k\( \Omega \), and calculate the RC time constant of the \( \phi_2 \) switch effect on \( V^- \).
   e. If your op-amp has a unity-gain frequency of 100 Mrad/s, what series resistance should you choose for your \( \phi_2 \) switch to match the op-amp and RC time constants?